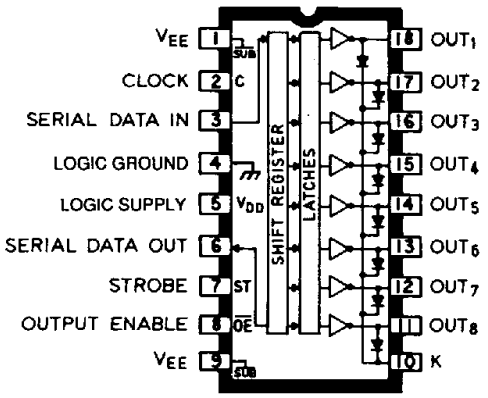
5841 THRU 5843

T-52-13-90

BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS

UCN5841A – UCN5843A



Dwg. No. A-12,659

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage, V_{CE}
- (UCN5841A/LW) . . . . . **50 V**
- (UCN5842A/LW) . . . . . **80 V**
- (UCN5843A/LW) . . . . . **100 V**

Output Voltage, $V_{CE(sus)}$
- (UCN5841A/LW) . . . . . **35 V†**
- (UCN5842A/LW) . . . . . **50 V†**
- (UCN5843A/LW) . . . . . **50 V†**

Logic Supply Voltage Range,
- V_{DD} . . . . . **4.5 V to 15 V**
- V_{DD} with Reference to V_{EE} . . . . . **25 V**

Emitter Supply Voltage, V_{EE} . . . . . **-20 V**

Input Voltage Range,
- V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**

Continuous Output Current,
- I_{OUT} . . . . . **500 mA**

Package Power Dissipation,
- P_D . . . . . **See Graph**

Operating Temperature Range,
- T_A . . . . . **-20°C to +85°C**

Storage Temperature Range,
- T_S . . . . . **-55°C to +150°C**

†For inductive load applications.

Note that the Series UCN5840A (dual in-line package) and Series UCN5840LW (small-outline IC package) are electrically identical and share a common pin number assignment.

The merging of low-power CMOS logic and bipolar output power drivers permit Series UCN5840A/LW integrated circuits to be used in a wide variety of peripheral power driver applications. The three basic devices in this series each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers. The 500 mA NPN Darlington outputs, with integral transient-suppression diodes, are suitable for use with relays, solenoids, and other inductive loads. Except for the maximum driver output voltage ratings, the UCN5841A/LW, UCN5842A/LW, and UCN5843A/LW are identical. The UCN5843A/LW offers premium performance with a minimum output-breakdown voltage rating of 100 V (50 V sustaining). All drivers can be operated with a split supply where the negative supply is up to -20 V.

BiMOS II devices have higher data-input rates than the earlier BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS and NMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, drivers can be cascaded for interface applications requiring additional drive lines.

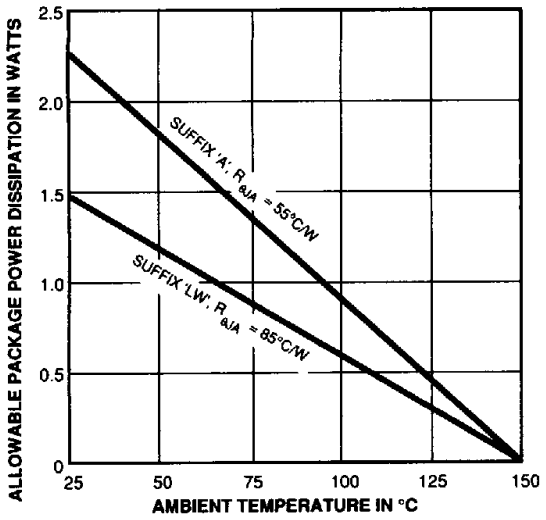
Suffix 'A' devices are furnished in a standard 18-pin plastic DIP; suffix 'LW' indicates an 18-lead wide-body SOIC.

FEATURES

- 3.3 MHz Minimum Data-Input Rate
- CMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Up/Pull-Down Resistors
- Low-Power CMOS Logic and Latches,
- High-Voltage Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- DIP, PLCC, or SOIC Packaging

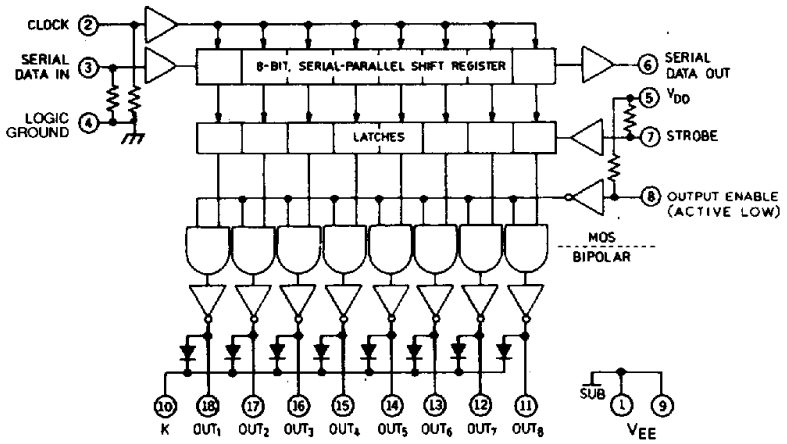
Always order by complete part number, e.g., **UCN5842LW**.

5841 THRU 5843
BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. No. GP-018A

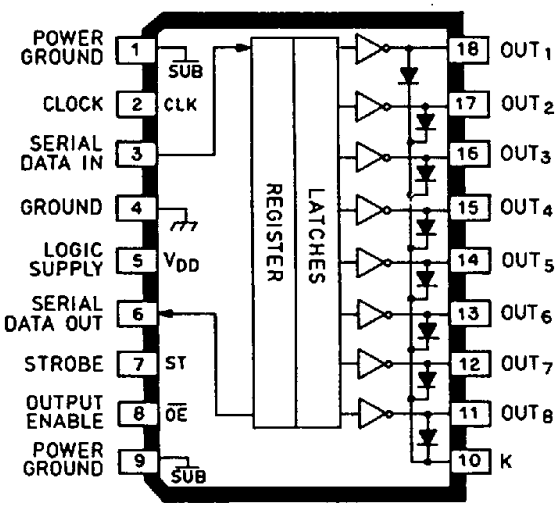
FUNCTIONAL BLOCK DIAGRAM
('A' & 'LW' Package Shown)



Dwg. No. A-12,661A

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

UCN5841LW – UCN5843LW



Dwg. No. A-14,438

Note that the Series UCN5840A (dual in-line package) and Series UCN5840LW (small-outline IC package) are electrically identical and share a common pin number assignment.

5841 THRU 5843
BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS

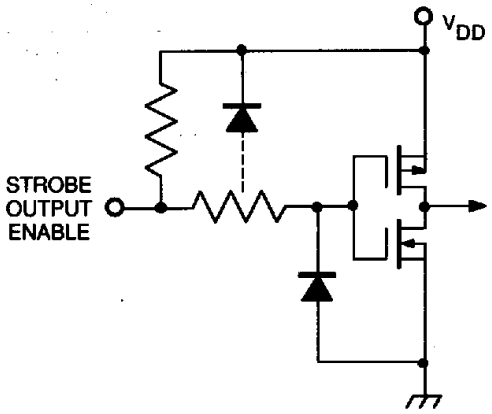
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, V_{EE} = 0 V (unless otherwise specified).

Characteristic	Symbol	Applicable Devices*	Test Conditions	Limits Min.	Limits Max.	Unit
Output Leakage Current	I_{CEX}	UCN5841	V_{OUT} = 50 V	—	50	µA
			V_{OUT} = 50 V, T_A = +70°C	—	100	µA
		UCN5842	V_{OUT} = 80 V	—	50	µA
			V_{OUT} = 80 V, T_A = +70°C	—	100	µA
		UCN5843	V_{OUT} = 100 V	—	50	µA
			V_{OUT} = 100 V, T_A = +70°C	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	I_{OUT} = 100 mA	—	1.1	V
			I_{OUT} = 200 mA	—	1.3	V
			I_{OUT} = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Collector-Emitter Sustaining Voltage	$V_{CE(sus)}$	UCN5841	I_{OUT} = 350 mA, L = 2 mH	35	—	V
		UCN5842	I_{OUT} = 350 mA, L = 2 mH	50	—	V
		UCN5843	I_{OUT} = 350 mA, L = 2 mH	50	—	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	V_{DD} = 12 V	10.5	—	V
			V_{DD} = 10 V	8.5	—	V
			V_{DD} = 5.0 V	3.5	—	V
Input Resistance	R_{IN}	ALL	V_{DD} = 12 V	50	—	kΩ
			V_{DD} = 10 V	50	—	kΩ
			V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	All Drivers ON, V_{DD} = 12 V	—	16	mA
			All Drivers ON, V_{DD} = 10 V	—	14	mA
			All Drivers ON, V_{DD} = 5.0 V	—	8.0	mA
	$I_{DD(OFF)}$	ALL	All Drivers OFF, V_{DD} = 12 V	—	2.9	mA
			All Drivers OFF, V_{DD} = 10 V	—	2.5	mA
			All Drivers OFF, V_{DD} = 5.0 V	—	1.6	mA
Clamp Diode Leakage Current	I_R	UCN5841	V_R = 50 V	—	50	µA
		UCN5842	V_R = 80 V	—	50	µA
		UCN5843	V_R = 100 V	—	50	µA
Clamp Diode Forward Voltage	V_F	ALL	I_F = 350 mA	—	2.0	V

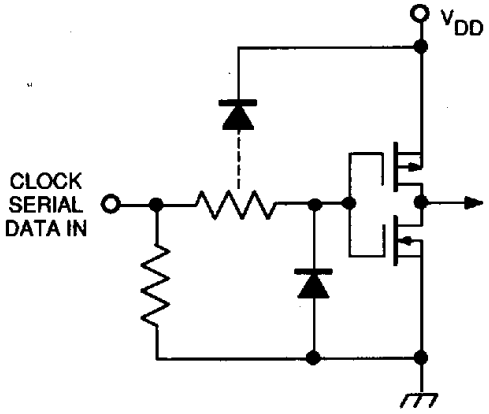
* Complete part number includes a suffix to identify package style: A = DIP, LW = SOIC.

5841 THRU 5843
BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS

TYPICAL INPUT CIRCUITS

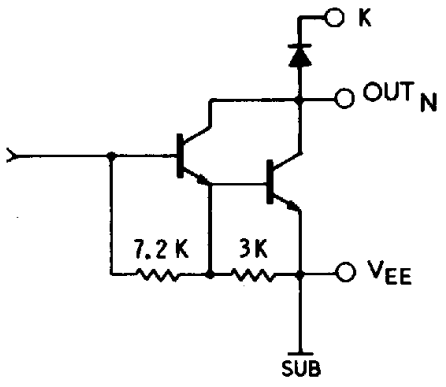


Dwg. No. EP-010-3

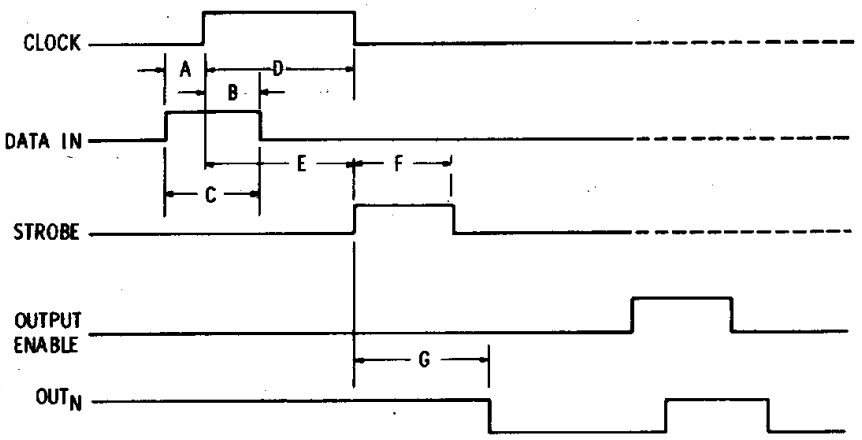


Dwg. No. EP-010-4A

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,660



Dwg. No. A-12,627

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**
C. Minimum Data Pulse Width . . . . . **150 ns**
D. Minimum Clock Pulse Width . . . . . **150 ns**
E. Minimum Time Between Clock Activation and Strobe . . . . . **300 ns**
F. Minimum Strobe Pulse Width . . . . . **100 ns**
G. Typical Time Between Strobe Activation and Output Transition . . . . . **500 ns**

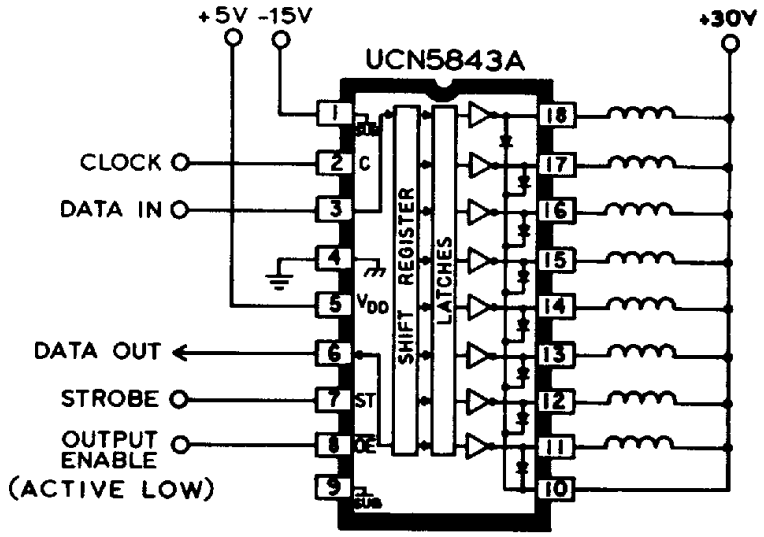
Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

5841 THRU 5843
BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS

TYPICAL APPLICATION
RELAY/SOLENOID DRIVER
Using Split Supply



Dwg. No. A-12,547

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H	⊓	H R_1 R_2 ..... R_7	R_7				
L	⊓	L R_1 R_2 ..... R_7	R_7				
X	⊔	R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State