Active Errata List

- DMA Access Request During Processor LOCK Accesses
- BUSRDY* and Waitstates on Exchange Memory Area
- Floating-point Compare Instruction Followed by OR Instruction

Errata History

Product Release	Errata List
All lot numbers	1, 2, 3

Errata Description

1. DMA Access Request During Processor LOCK Accesses

The error case appears when the DMAREQ* assertion by the DMA unit and the LOCK assertion by the processor occur in the same clock cycle. In this case, if no DMA transfer is performed during the DMA session, the processor only retrieves control on the bus after the DMA time-out has expired. The DMA time-out can be disabled by software. If DMA time-out is disabled and the error case is present, the processor will never retrieve the bus. A reset would be the only way to restart processor in normal activity.

When the error case condition is fulfilled, on the same clock rising edge, DMAGNT* assertion by the processor and internal LOCK sampling by the memory controller are executed. A DMA session is started and at the same time, the LOCK signal is decoded by the MEC. The memory controller generates an internal signal that makes the IU enter a ‘hold’ mode. The IU remains in ‘hold’ mode until internal signals are updated through DMAAS assertion or DMA time-out. The external LOCK pin is a direct representation of the IU signal whereas internal LOCK is only effective in the following rising edge of the clock.

Workarounds

Software workaround:
No inactive DMA cycle is performed. At least one DMAAS per DMA cycle.

Hardware workaround:
The DMA unit must decode the LOCK signal so that no DMA request is sent to the processor while a locked cycle is in progress. Insertion of a one-clock-cycle delay on assertion of DMAREQ* when LOCK is active is one way to avoid the above processor behavior.

2. BUSRDY* and Waitstates on Exchange Memory Area

The error appears during exchange memory accesses that use both programmed waitstates and BUSRDY*.

An exchange memory access is only terminated if on the rising edge of SYSCLK that separates the ‘waitstate cycle’ and the ‘end of cycle’ the BUSRDY* signal is low.

If BUSRDY* is high and the programmed waitstates are elapsed, the processor remains in a waiting state. It retrieves a nominal behaviour when a bus timeout occurs.

Workarounds

When ‘n’ waitstates are programmed, generate a ‘n+2’ SYSCLK cycles length BUSRDY*.

When the programmed waitstates elapse, assert a second pulse of BUSRDY*.

SPARC Processor

TSC695

Errata Sheet

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3. Floating-Point Compare Single or Double Instruction followed by specific IU Instruction followed by Floating-Point Store Double Instruction

If a floating-point compare single or double instruction (FCMPS, FCMPES, FCMPD or FCMPED) is immediately followed by one of the OR, ORcc, ORN, ORNcc, SRL, TADDccTV, Ticc, RDWIM or WRWIM instruction, and the next instruction is a floating-point store double (STDF) of any floating-point register (involved or not in the floating-point compare single or double instruction), the stored floating-point double value is corrupted.

Data corruption happens as follows: the program location of the floating-point compare single or double instruction is written into memory at the effective store address instead of the expected most significant word in the even-numbered floating-point source register.

The floating-point registers involved in the floating-point store double operation are not corrupted, nor any other floating- point register.

The error case appears when any of the four following sequences of instructions is present:

– Case 1:

```
FCMPS  %fx,%fy
IUop(1)
STD    %fz,[address]
```

– Case 2:

```
FCMPES %fx,%fy
IUop(1)
STD    %fz,[address]
```

– Case 3:

```
FCMPD  %fx,%fy
IUop(1)
STD    %fz,[address]
```

– Case 4:

```
FCMPED %fx,%fy
IUop(1)
STD    %fz,[address]
```

Note: 1. *IUop* is one of OR, ORcc, ORN, ORNcc, SRL, TADDccTV, Ticc, RDWIM or WRWIM instructions, whatever the operands are.

Workarounds

If direct control over assembly language is possible, simply insert a NOP after the floating-point compare single or double instruction:

– Case 1:

```
FCMPS  %fx,%fy
NOP
IUop(1)
STD    %fz,[address]
```

– Case 2:

```
FCMPES %fx,%fy
NOP
IUop(1)
STD    %fz,[address]
```

– Case 3:

```
FCMPD  %fx,%fy
NOP
```


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```
IUop(1)
STD     %fz,[address]
```

– Case 4:

```
FCMPED %fx,%fy
NOP
IUop(1)
STD     %fz,[address]
```

Note: 1. *IUop* is one of OR, ORcc, ORN, ORNcc, SRL, TADDccTV, Ticc, RDWIM or WRWIM instructions, whatever the operands are.

If direct control over assembly language is not possible (high-level programming language such as C), checking of the SPARC binary code against any of the four above mentioned faulty sequences of instructions shall be done using the check program provided by Atmel (*see doc7662.pdf on Atmel web site)*.

Although there is a very low likelihood of occurrence with high-level programming languages, customers facing this problem shall contact SPARC hotline (sparc-applab.hotline@nto.atmel.com).

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