

Time-Code Receiver

Description

The T4227 is a bipolar integrated straight-through receiver circuit in the frequency range of 40 kHz to 120 kHz. The device is designed for radio-controlled clock applications with very high sensitivity.

Features

- Low power consumption
- Very high sensitivity
- High selectivity by using crystal filter
- Power-down mode available
- Only a few external components necessary
- Complementary output stages
- AGC hold mode
- Wide frequency range (40 kHz to 120 kHz)
- Low battery voltage applications (1.1 V to 3.6 V)

Block Diagram

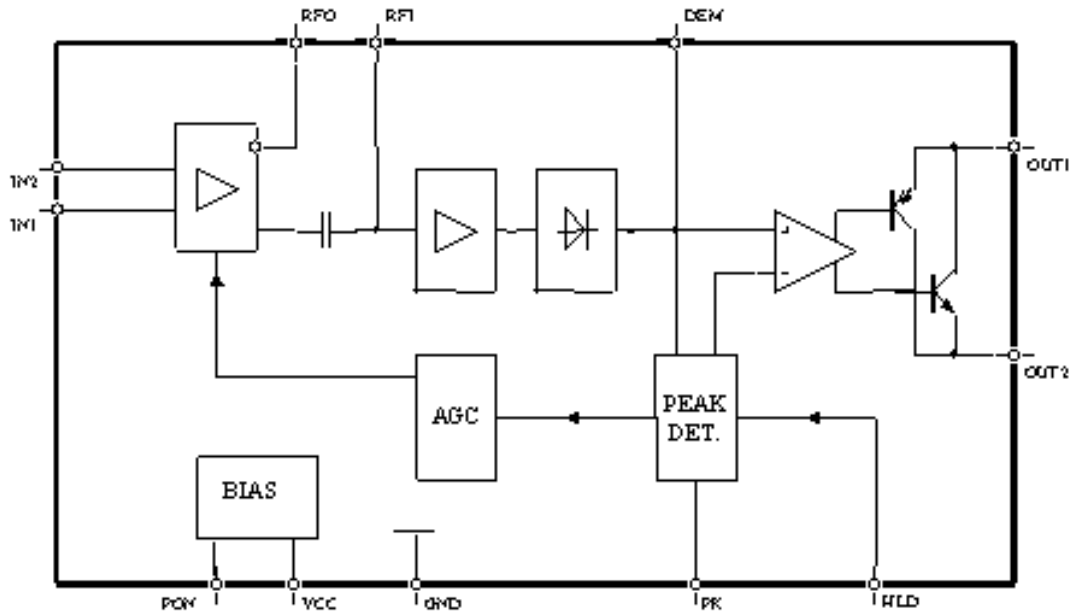


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
T4227-DDT	No	Die in trace
T4227-FB	SSO16	
T4227-FBG3	SSO16	Taped and reeled
T4227-DBQ	No	CSP Chip Scale Package

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage	V _{CC}	5.5	V
Ambient temperature range	T _{amb}	-40 to +85	°C
Storage temperature range	R _{stg}	-55 to +150	°C
Junction temperature	T _j	125	°C
Electrostatic handling (MIL Standard 883 D HBM)	± V _{ESD}	2000	V

PAD Coordinates

The T4227 is available as die for “chip-on-board” mounting and in SSO16 package.

DIE size: 1.65 x 1.44 mm

PAD size: 100 x 100 μm (contact window 88 x 88 μm)

Thickness: 300 μm ± 10 μm

Symbol	Function	x-axis (μm)	y-axis (μm)	Pad # (dice)	Pin # (SSO16*)
RFI	RF-input (from crystal)	130	1141	1	2
GND	Ground	130	934	2	3
RFO	RF-output (to crystal)	130	727	3	4
Vcc	Supply voltage	130	520	4	5
IN2	Antenna input 2	130	313	5	6
IN1	Antenna input 1	130	106	6	7
OUT2	Negative signal output	1430	106	7	10
OUT1	Positive signal output	1430	313	8	11
PON	Power on input	1430	520	9	12
PK	Peak detector output	1430	727	10	13
HLD	AGC hold	1430	934	11	14
DEM	Demodulator output	1430	1141	12	15

* Pin 1, 8, 9 and 16 not connected

PAD Layout

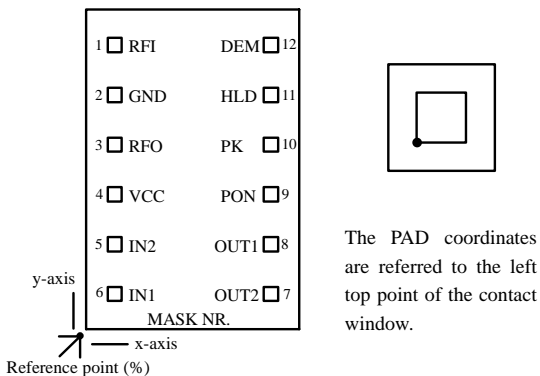


Figure 2. Pad layout

Pin Layout SSO16

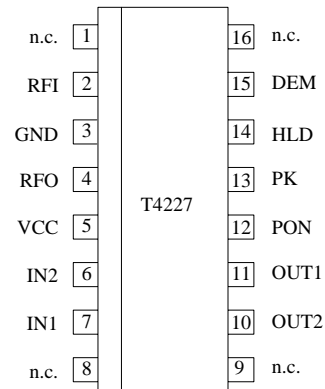


Figure 3. Pin layout SSO16

IN1, IN2

A ferrite antenna is connected between IN1 and IN2. For high sensitivity, the Q factor of the antenna circuit should be as high as possible. Please note that a high Q factor requires temperature compensation of the resonant frequency in most cases. We recommend a Q factor between 40 and 150. Depending on the application. An optimal signal-to-noise ratio will be achieved by a resonant resistance of 50 kΩ to 200 kΩ.

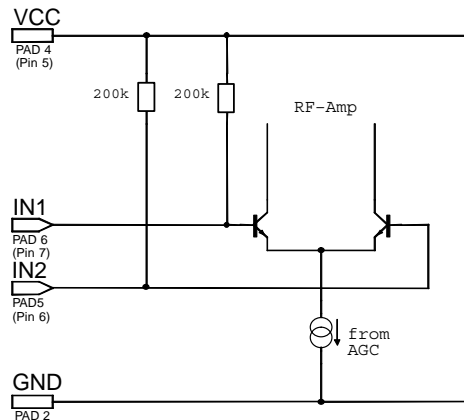


Figure 4.

RFO

In order to achieve a high selectivity, a crystal is connected between the Pins RFO and RFI. It is used with the serial resonant frequency according to the time-code transmitter (e.g., 60 kHz WWVB, 77.5 kHz DCF or 40 kHz Japan) and acts as a serial resonator. The given parallel capacitor of the filter crystal (about 0.8 pF) is internally compensated so that the bandwidth of the filter is about 10 Hz. The impedance of RFI is high. Parasitic loads have to be avoided.

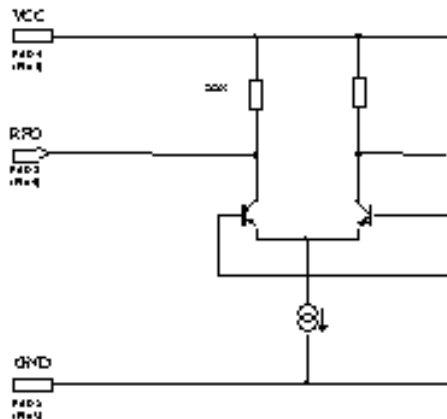


Figure 5.

RFI

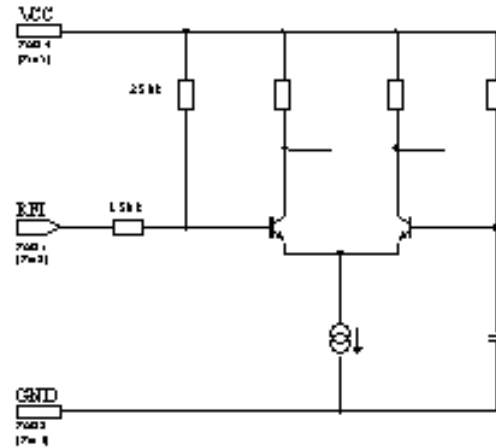


Figure 6.

DEM

Demodulator output. To ensure the function, a external capacitor has to be connected at this output.

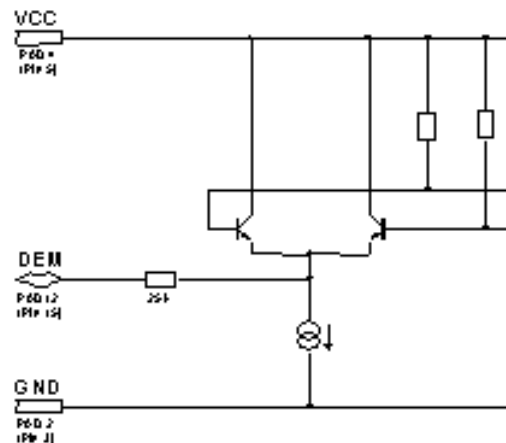


Figure 7.

HLD

AGC hold mode: HLD high ($V_{HDL} = V_{CC}$) sets normal function, SL low ($V_{HDL} = 0$) holds for a short time the AGC voltage. This can be used to prevent the AGC from peak voltages, created by e.g. a stepper motor.

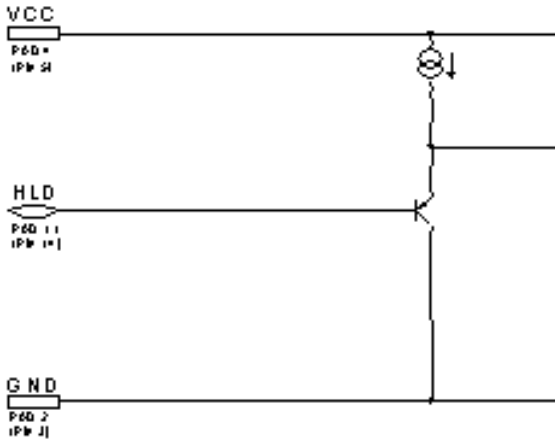


Figure 8.

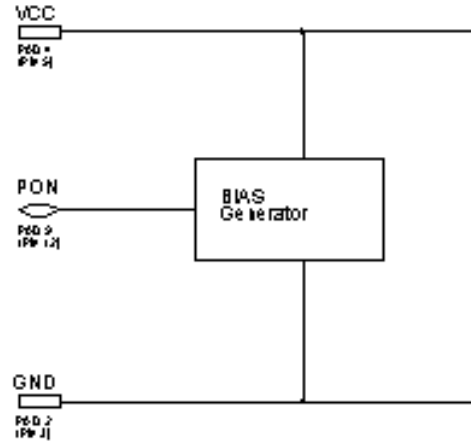


Figure 10.

PK

Peak detector output: An external capacitor has to be connected to ensure the function of the peak detector. The value of the capacitance influences the AGC regulation time.

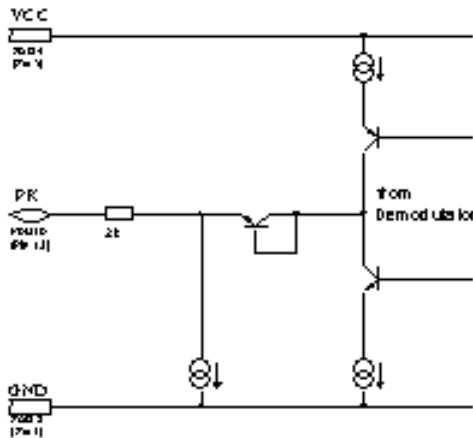


Figure 9.

VCC, GND

VCC and GND are the supply voltage inputs. To power down the circuitry it is recommended to use the PDN input and not to switch the power supply. Switching the power supply effects in a long power up waiting time.

PON

If PON is connected to GND, the receiver will be activated. The set-up time is typically 0.5 s after applying GND at this pin. If PON is connected to VCC, the receiver will switch to power-down mode.

OUT1, OUT2

The serial signal of the time-code transmitter can be directly decoded by a microcomputer. Details about the time-code format of several transmitters are described separately.

The output consists of a combination of a NPN / PNP open collector stage. The function depends on the external circuitry:

- A load resistor is connected from OUT1 to Vcc, OUT2 is connected to GND. This performs the functionality of a NPN open collector stage.
- A load resistor is connected from OUT2 to GND, OUT1 is connected to VCC. This performs the functionality of a PNP open collector stage.

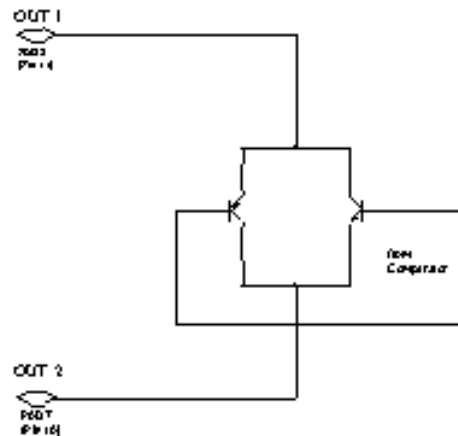


Figure 11.

Design Hints for the Ferrite Antenna

The bar antenna is a very critical device of the complete clock receiver. Observing some basic RF design rules helps to avoid possible problems. The IC requires a resonant resistance of 50 kΩ to 200 kΩ. This can be achieved by a variation of the L/C-relation in the antenna circuit. It is not easy to measure such high resistances in the RF region. A more convenient way is to distinguish between the different bandwidths of the antenna circuit and to calculate the resonant resistance afterwards.

Thus, the first step in designing the antenna circuit is to measure the bandwidth. Figure 12 shows an example for the test circuit. The RF signal is coupled into the bar antenna by inductive means, e.g., a wire loop. It can be measured by a simple oscilloscope using the 10:1 probe. The input capacitance of the probe, typically about 10 pF, should be taken into consideration. By varying the frequency of the signal generator, the resonant frequency can be determined.

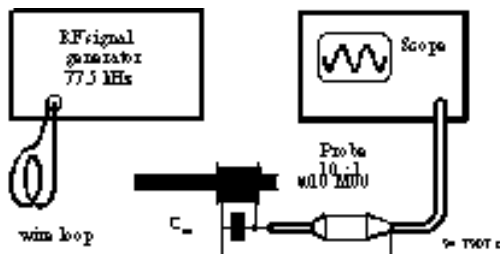


Figure 12.

At the point where the voltage of the RF signal at the probe drops by 3 dB, the two frequencies can then be measured. The difference between these two frequencies is called the bandwidth BW_A of the antenna circuit. As the value of the capacitor C_{res} in the antenna circuit is known, it is easy to compute the resonant resistance according to the following formula:

$$R_{res} = \frac{1}{2 \times \pi \times BW_A \times C_{res}}$$

where

R_{res} is the resonant resistance,

BW_A is the measured bandwidth (in Hz)

C_{res} is the value of the capacitor in the antenna circuit (in Farad).

If high inductance values and low capacitor values are used, the additional parasitic capacitance of the coil must be considered. The Q value of the capacitor should be no problem if a high Q type is used. The Q value of the coil differs more or less from the DC resistance of the wire. Skin effects can be observed but do not dominate.

Therefore, it should not be a problem to achieve the recommended values of the resonant resistance. The use of thicker wire increases the Q value and accordingly reduces bandwidth. This is advantageous in order to improve reception in noisy areas. On the other hand, temperature compensation of the resonant frequency might become a problem if the bandwidth of the antenna circuit is low compared to the temperature variation of the resonant frequency. Of course, the Q value can also be reduced by a parallel resistor.

Temperature compensation of the resonant frequency is a must if the clock is used at different temperatures. Please ask your supplier of bar antenna material and of capacitors for specified values of the temperature coefficient.

Furthermore, some critical parasitics have to be considered. These are shortened loops (e.g., in the ground line of the PCB board) close to the antenna and undesired loops in the antenna circuit. Shortened loops decrease the Q value of the circuit. They have the same effect like conducting plates close to the antenna. To avoid undesired loops in the antenna circuit, it is recommended to mount the capacitor C_{res} as close as possible to the antenna coil or to use a twisted wire for the antenna-coil connection. This twisted line is also necessary to reduce feedback of noise from the microprocessor to the IC input. Long connection lines must be shielded.

A final adjustment of the time-code receiver can be carried out by pushing the coil along the bar antenna.

Electrical Characteristics

$V_{CC} = 3\text{ V}$, reference point Pin 3, input signal frequency $77.5\text{ kHz} \pm 5\text{ Hz}$; carrier voltage 100% reduction to 25% for $t_{MOD} = 200\text{ms}$; $T_{amb} = 25^\circ\text{C}$, unless otherwise specified.

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pad/Pin V_{CC}	V_{CC}	1.1		5.5	V
Supply current	Pad/Pin V_{CC}	I_{CC}		200	250	μA
Set-up time after V_{CC} ON	$V_{CC} = 3\text{ V}$	t		1.5		s
Reception frequency range		f_{in}	40		120	kHz
Minimum input voltage	Pad/Pin IN1, IN2	V_{in}		0.3	0.6	μV
Maximum input voltage	Pad/Pin IN1, IN2	V_{in}	30	50		mV
Input amplifier max. gain ($V_{PK} = 0.1\text{ V}$)		V_{U1}		53		dB
Input amplifier min. gain ($V_{PK} = 0.8\text{ V}$)		V_{U2}		-40		dB
Output voltage (OUT1, low) external circuitry like npn open collector stage	$V_1 = 100\text{ }\mu\text{V}$; $I_{OUT1\ L} = 30\text{ }\mu\text{A}$	$V_{Out1\ L}$			0.3	V
Output voltage (OUT2, high) external circuitry like pnp open collector stage	$V_1 = 100\text{ }\mu\text{V}$; $I_{OUT2\ H} = 30\text{ }\mu\text{A}$	$V_{Out2\ H}$	$V_{DD}-0.5$	$V_{DD}-0.3$		V
Output current (OUT 1 high) external circuitry like npn open collector stage	$V_1 = 100\text{ }\mu\text{V}$; 100% amplitude	$I_{OUT1\ H}$			1	μA
Output current (OUT 1 low) external circuitry like npn open collector stage	$V_1 = 100\text{ }\mu\text{V}$; 25% amplitude	$I_{OUT1\ L}$	30		500	μA
Output current (OUT 2 high) external circuitry like pnp open collector stage	$V_1 = 100\text{ }\mu\text{V}$; 25% amplitude	$-I_{OUT2\ H}$	30		500	μA
Output current (OUT 2 low) external circuitry like npn open collector stage	$V_1 = 100\text{ }\mu\text{V}$; 100% amplitude	$-I_{OUT2\ L}$			1	μA
Power-down control; PON Pad/Pin PON						
Switch current receiver ON	$V_{PDN} = 0\text{ V}$, Pad PON	$-I_{PDN}$		14	20	μA
Quiescent current receiver OFF	$V_{PDN} = V_{CC}$, Pad/Pin V_{CC}	I_{CC0}			0.5	μA
Set-up time after PON		t		0.5	2	s
AGC hold mode; HLD Pad/Pin HLD						
Switch voltage receiver normal mode	$V_{HLD} = V_{CC}$	V_{HLD}	$V_{CC}-0.2$			V
Input current AGC in hold mode	$V_{HLD} = 0\text{ V}$	$-I_{HLD}$			2	μA
AC characteristics						
Output pulse with for OUT1 and OUT2	Modulation according DCF77, 200 ms pulse	t_{WO200}	170	195	230	ms
Output pulse with for OUT1 and OUT2	Modulation according DCF77, 100 ms pulse	t_{WO100}	70	95	130	ms

Test Circuitry with Pull-up Resistor (77.5 kHz)

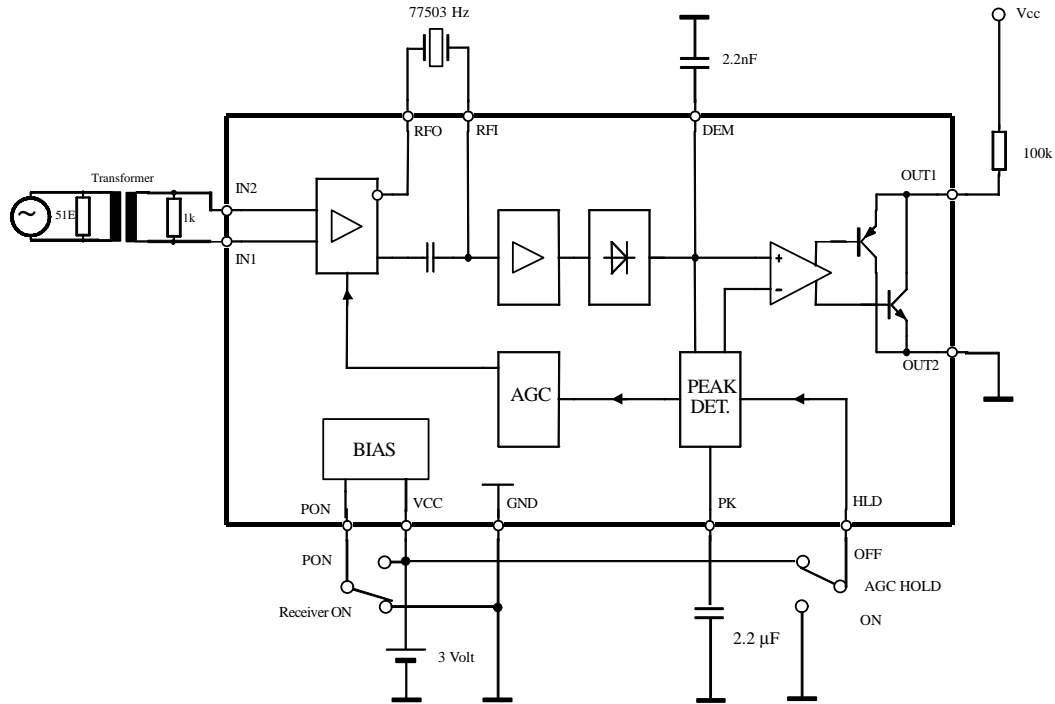


Figure 13. Test circuit

Test Circuitry with Pull-down Resistor (77.5 kHz)

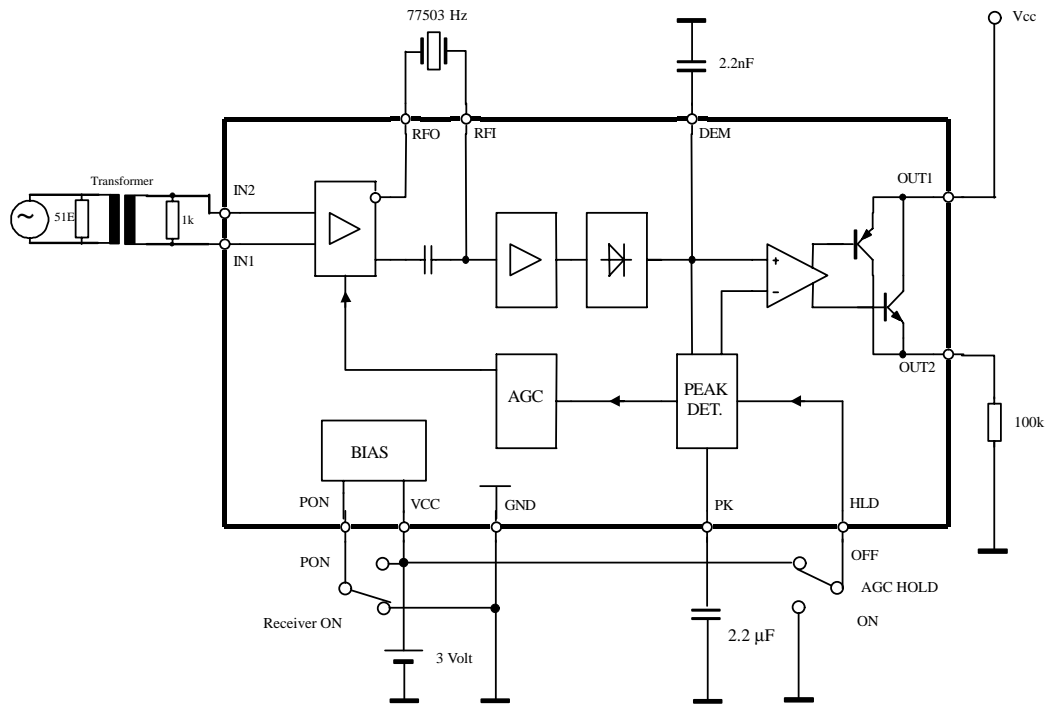


Figure 14. Test circuit

Information on the German Transmitter (Customer is responsible to verify the information!)

Station: DCF 77,
Frequency 77.5 kHz,
Transmitting power 50 kW

Location: Mainflingen/Germany,
Geographical coordinates: 50° 0.1'N, 09° 00'E
Time of transmission: permanent

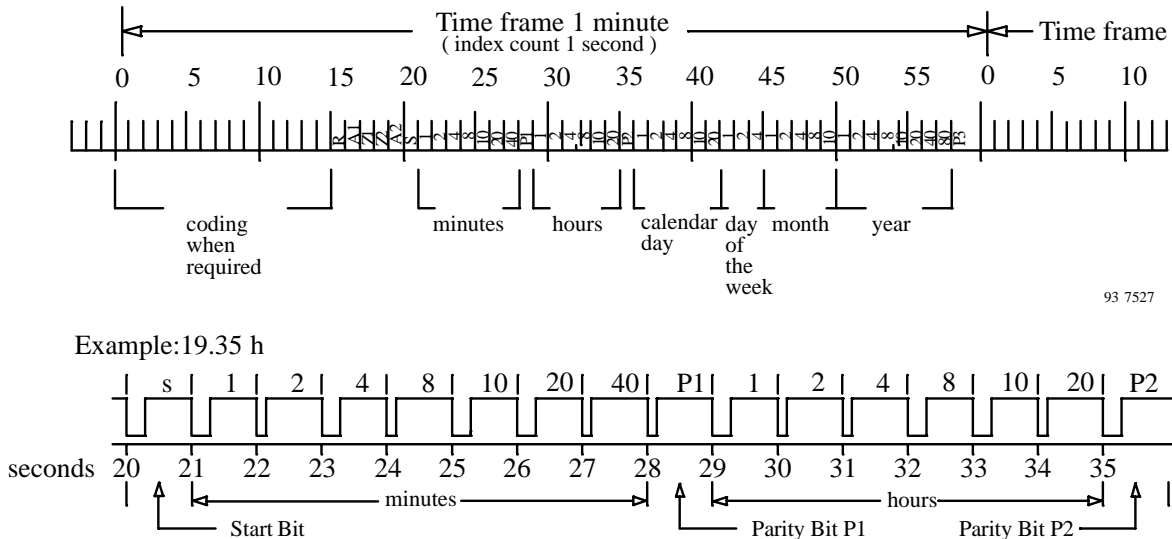


Figure 15.

Modulation

The carrier amplitude is reduced to 25% at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one), except the 59th second.

Time-Code Format (based on Information of Deutsche Bundespost)

The time-code format consists of 1-minute time frames. There is no modulation at the beginning of the 59th

second to indicate the switch over to the next 1-minute time frame. A time frame contains BCD-coded information of minutes, hours, calendar day, day of the week, month and year between the 20th second and 58th second of the time frame, including the start bit S (200 ms) and parity bits P1, P2 and P3. Furthermore, there are 5 additional bits R (transmission by reserve antenna), A1 (announcement of change-over to summer time), Z1 (during summer time 200 ms, otherwise 100 ms), Z2 (during standard time 200 ms, otherwise 100 ms) and A2 (announcement of leap second) transmitted between the 15th second and 19th second of the time frame.

**Information on the British Transmitter
(Customer is responsible to verify the information!)**

Station: MSF
 Frequency 60 kHz
 Transmitting power 50 kW
 Location: Teddington, Middlesex

Geographical coordinates: 52° 22'N, 01° 11'W
 Time of transmission: permanent, except the first Tuesday of each month from 10.00 h to 14.00 h.

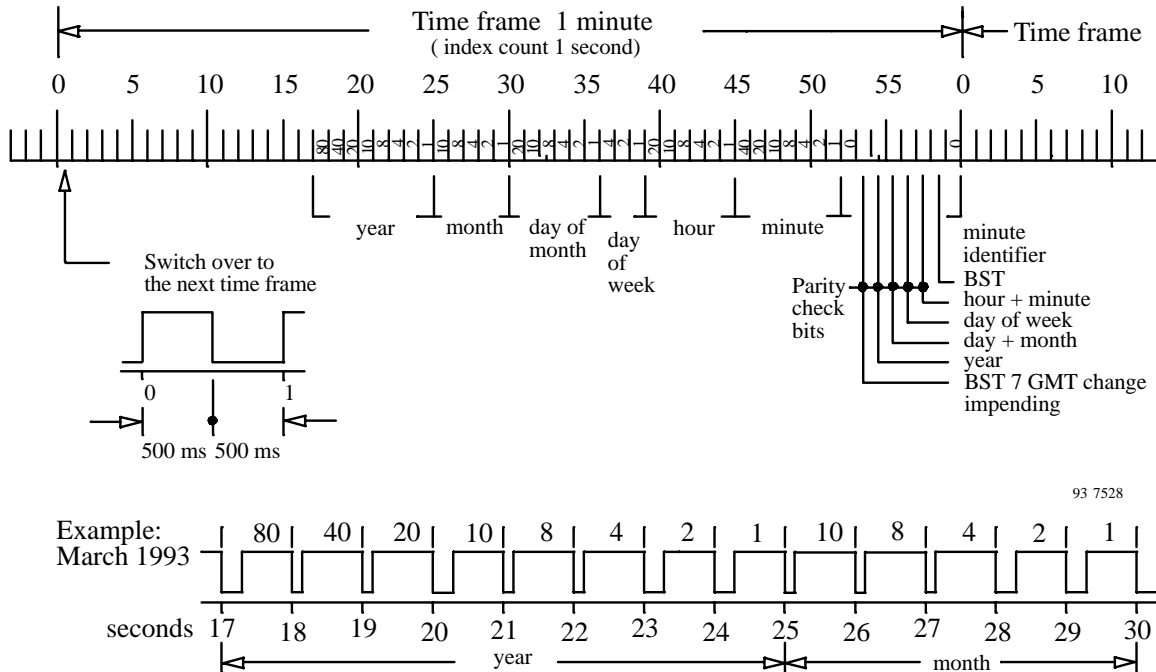


Figure 16.

Modulation

The carrier amplitude is switched off at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one).

Time-Code Format

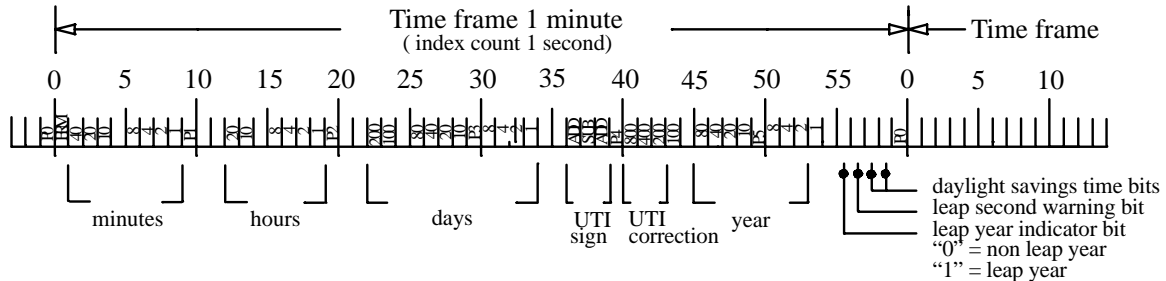
The time-code format consists of 1-minute time frames. A time frame contains BCD-coded information of year, month, calendar day, day of the week, hours and minutes. At the switch-over to the next time frame, the carrier amplitude is reduced for a period of 500 ms.

The presence of the fast code during the first 500 ms at the beginning of the minute is not guaranteed. The transmission rate is 100 bits/s and the code contains information of hour, minute, day and month.

Information on the US Transmitter (Customer is responsible to verify the information!)

Station: WWVB
 Frequency 60 kHz
 Transmitting power 10 kW

Location: Fort Collins
 Geographical coordinates: 40° 40'N, 105° 03'W
 Time of transmission: permanent



93 7529 e

Example: UTC 18.42 h

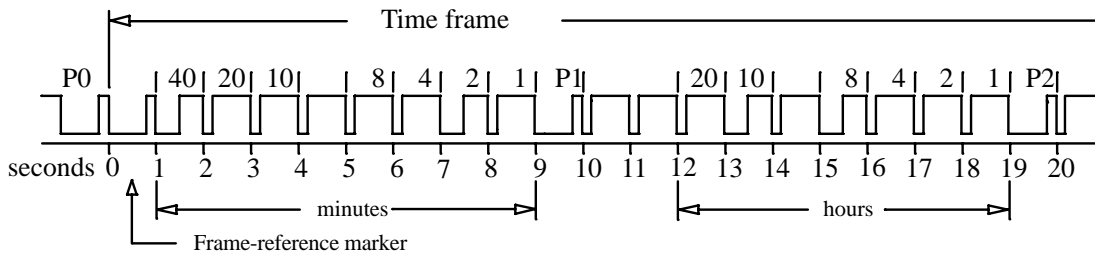


Figure 17.

Modulation

The carrier amplitude is reduced by 10 dB at the beginning of each second and is restored within 500 ms (binary one) or within 200 ms (binary zero).

Time-Code Format

The time-code format consists of 1-minute time frames. A time frame contains BCD1-coded information of minutes, hours, days and year. In addition, there are 6 position-identifier markers (P0 thru P5) and 1 frame-reference marker with reduced carrier amplitude of 800 ms duration.

Information on the Japanese Transmitter (preliminary)
(Customer is responsible to verify the information!)

Station: JJY
Frequency 40 kHz
Transmitting power 50 kW

Location: Sanwa, Ibaraki
Geographical coordinates: 36°11' N, 139°51' E
Time of transmission: permanent

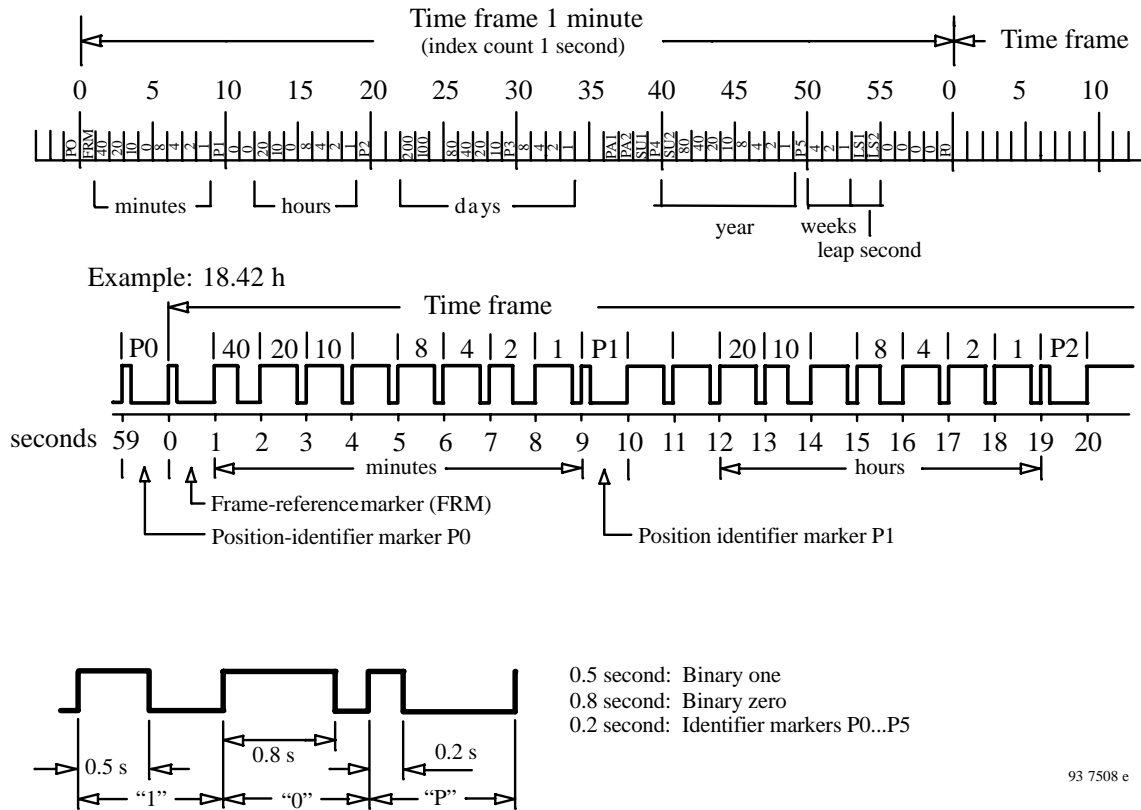


Figure 18.

Modulation

The carrier amplitude is 100% at the beginning of each second and is switched to 10% after 500 ms (binary one) or after 800 ms (binary zero) and to 200 ms for identifier marker P0 ... P5.

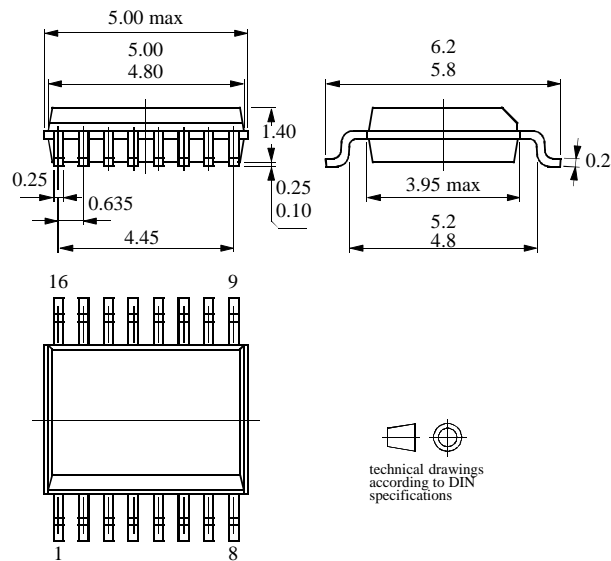
Time-Code Format

The time-code format consists of 1-minute time frames. A time frame contains BCD-coded information of minutes, hours, days, weeks and year. In addition, there are 6 position-identifier markers (P0 thru P5) with reduced carrier amplitude of 500 ms duration.

Package Information

Package SSO16

Dimensions in mm



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It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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Data sheets can also be retrieved from the Internet: <http://www.temic-semi.com>

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