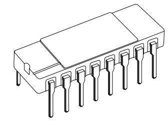
M54HC4538

RAD HARD DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

- HIGH SPEED:
  t_{PD} = 25 ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  STAND BY STATE:
  I_{CC}=4µA (MAX.) at T_A=25°C
  ACTIVE STATE:
  I_{CC}=200µA (TYP.) at V_{CC} = 6V
- HIGH NOISE IMMUNITY:
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}|$ = I_{OL} = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- WIDE OUTPUT PULSE WIDTH RANGE:
  t_{WOUT} = 120 ns ~ 60 s OVER AT V_{CC} = 4.5 V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 4538
- DEVICE FULLY COMPLIANT WITH SCC-9207-008



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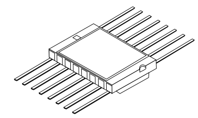

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ORDER CODES

PACKAGE	FM	EM
DILC	M54HC4538D	M54HC4538D1
FPC	M54HC4538K	M54HC4538K1

DESCRIPTION

The M54HC4538 is an high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology.

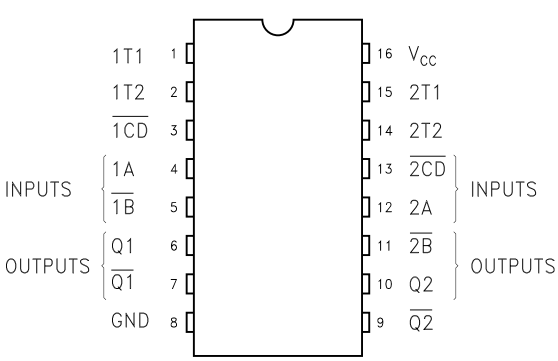
Each multivibrator features both a negative A, and a positive B, edge triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The monostable multivibrator are retriggerable. That is, they may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended. Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques.

The output pulse equation is simply:

PW = 0.7 (R)(C) where PW is in seconds, R in Ohms and C is in Farads.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION



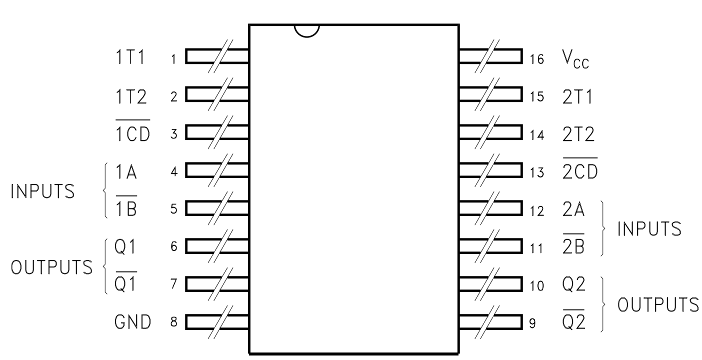


Figure 1: IEC Logic Symbols

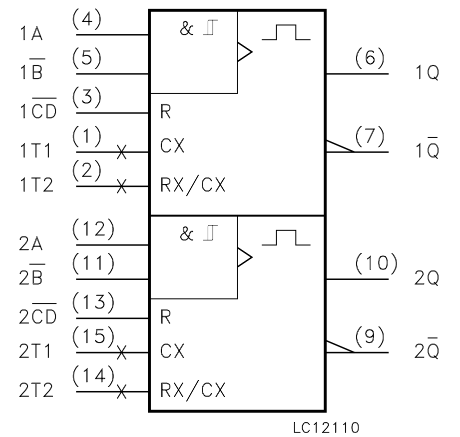


Figure 2: Input And Output Equivalent Circuit

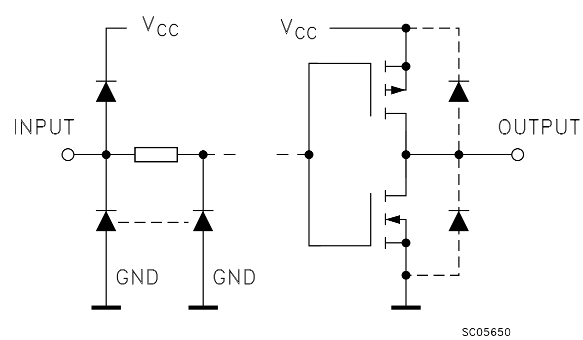


Table 1: Pin Description

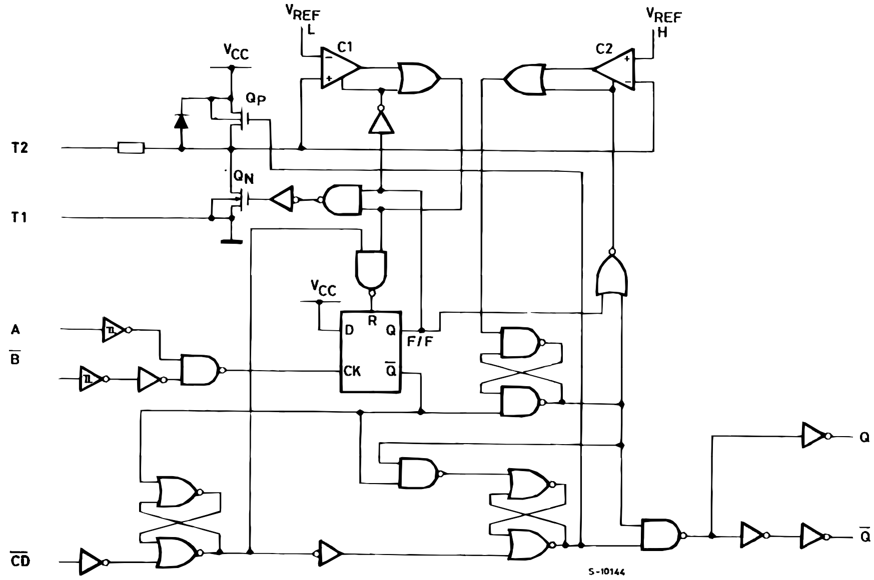
PIN N°	SYMBOL	NAME AND FUNCTION
1, 15	1T1, 2T1	External Capacitor Connections
2, 14	1T2, 2T2	External Resistor/ Capacitor Connections
3, 13	$\overline{1CD}$, $\overline{2CD}$	Direct Reset Inputs (Active Low)
4, 12	1A, 2A	Trigger Inputs (LOW to HIGH, Edge-Triggered)
5, 11	1$\overline{B}$, 2$\overline{B}$	Trigger Inputs (HIGH to LOW, Edge Triggered)
6, 10	Q1, Q2	Pulse Outputs
7, 9	$\overline{Q}$1, $\overline{Q}$2	Complementary Pulse Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

Table 2: TRUTH TABLE

INPUTS			OUTPUTS		NOTE
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$	
↑	H	H	⊓	⊔	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↓	H	⊓	⊔	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X : Don't Care

Figure 3: System Diagram



This logic diagram has not be used to estimate propagation delays

Figure 4: Timing Chart

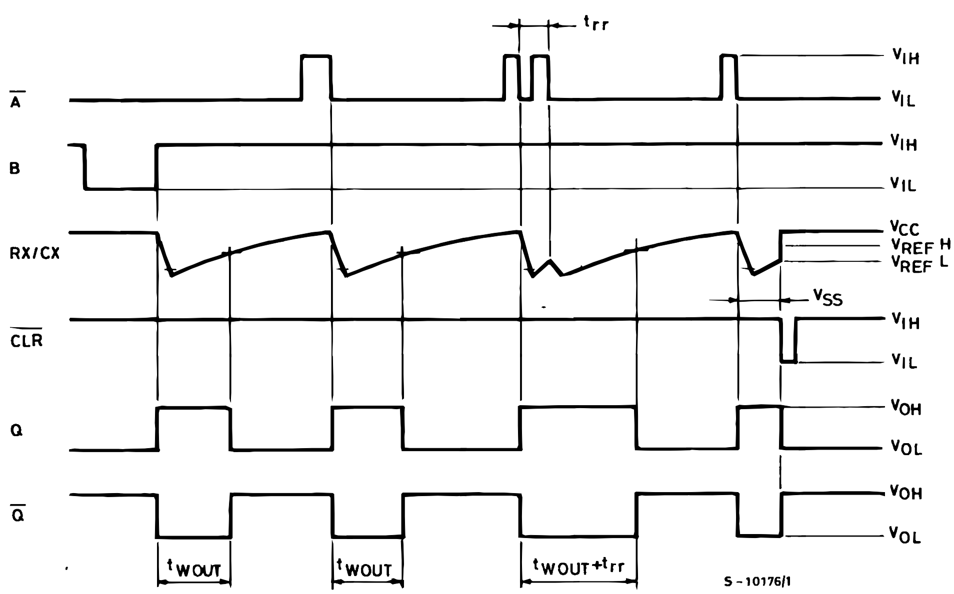
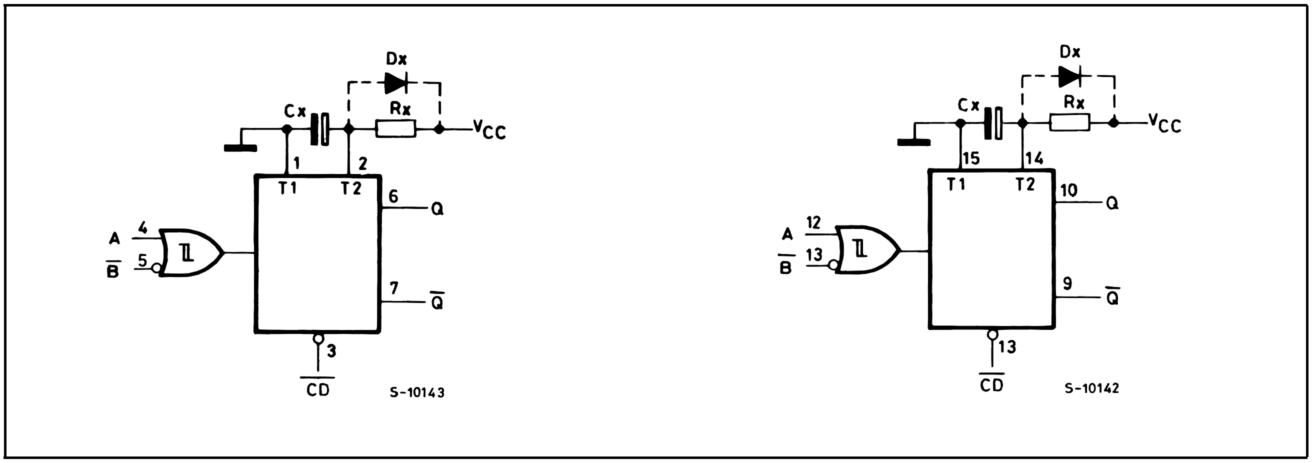


Figure 5: Block Diagram



(1) Cx, Rx, Dx are external components.
(2) Dx is a clamping diode.
The external capacitor is charged to V_{CC} in the stand-by-state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly trough an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidly, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage to the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows:
$t_f \geq (V_{CC} - 0.7) \times Cx/20mA$
In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

STAND-BY STATE

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned-off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

TRIGGER OPERATION

Triggering occurs when:
1 st) A is "LOW" and $\overline{B}$ has a falling edge;
2 nd) $\overline{B}$ is "HIGH" and A has a rising edge;
After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node Rx/Cx external falls.
When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn reset the flip-flop and Qn is turned off.
At this point C1 stops functioning but C2 continues to operate.
The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.
Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}. At this point C2 output goes low and G goes low. C2 stop operating. That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx · Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse t_W (out) is as follows:

$$t_{W(OUT)} = 0.72\ Cx \cdot Rx$$

RE - TRIGGERED OPERATION

When a second trigger pulse follows the first its effect will depend on the state of the multivibrator. If the capacitor Cx is being charged the voltage level of Rx/Cx external falls to V_{REFL} again and Q remains High i.e. the retrigger pulse arrives in a time shorter than the period Rx · Cx seconds, the capacitor charging time constant. If the second trigger pulse is very close to the initial trigger pulse it is ineffective; i.e. the second trigger must arrive in the capacitor discharge cycle to be ineffective; Hence the minimum time for a second trigger to be effective, t_{rr} (MIN.) depends on V_{CC} and Cx

RESET OPERATION

$\overline{CD}$ is normally high. If $\overline{CD}$ is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

Also transistor Op is turned on and Cx is charged quickly to V_{CC}. This means if $\overline{CD}$ input goes low the IC becomes waiting state both in operating and non operating state.

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	300	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4: Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time ($\overline{CD}$ only)	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns
Cx	External Capacitor		NO LIMITATION	pF
Rx	External Resistor	V_{CC} < 3V	5K to 1M	Ω
		$V_{CC} \geq$ 3V	1K to 1M	

The Maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of device and leakage due to the board layout and surface resistance. Susceptibility to externally induced noise may occur for Rx > 1MΩ

Table 5: DC Specifications

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND			± 0.1		± 1		± 1	µA
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND Rext/Cext			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND			4		40		80	µA
I_{CC}	Quiescent Supply Current	2.0	$V_I = V_{CC}$ or GND Pin 2 or 14 $V_{IN} = V_{CC}/2$		40	120		160		200	µA
		4.5			0.2	0.3		0.4		0.6	mA
		6.0			0.3	0.6		0.8		1.0	mA

Table 6: AC Electrical Characteristics (C_L = 50 pF, Input t_r = t_f = 6ns)

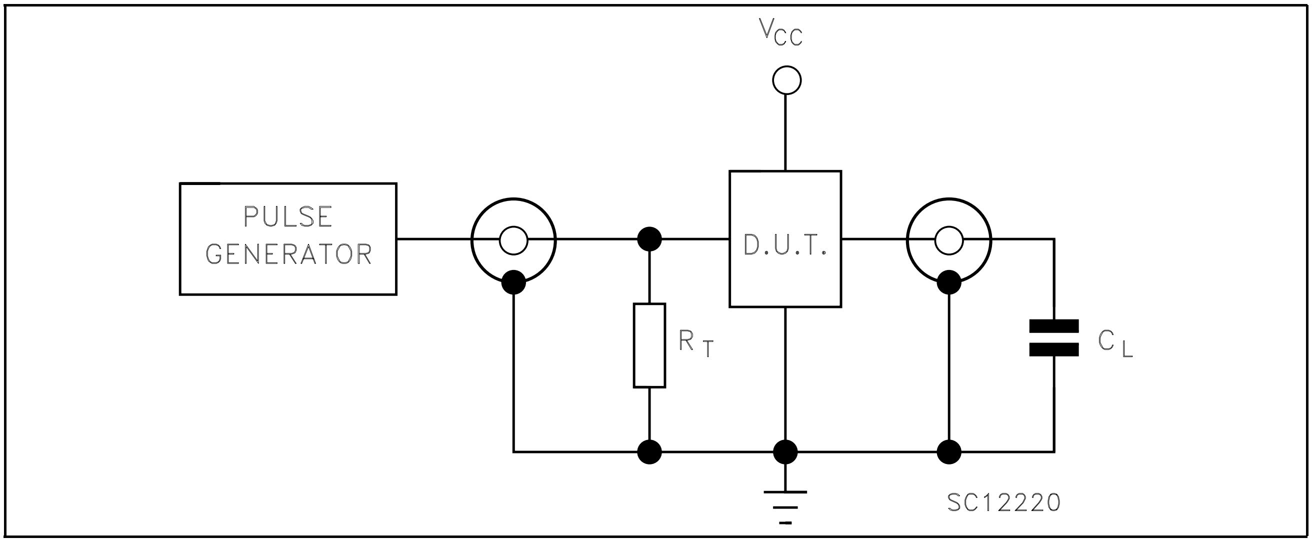
Symbol	Parameter	V_{CC} (V)	Test Condition	T_A = 25°C			-40 to 85°C		-55 to 125°C		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, $\overline{B}$ - Q, $\overline{Q}$)	2.0			120	250		315		375	ns
		4.5			30	50		63		75	
		6.0			25	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CD}$ - Q, $\overline{Q}$)	2.0			100	195		245		295	ns
		4.5			25	39		49		59	
		6.0			20	33		42		50	
t_{WOUT}	Output Pulse Width	2.0	Cx=0, Rx = 5KΩ		540	1200		1500		1800	ns
		4.5	Cx=0, Rx = 1KΩ		180	250		320		375	
		6.0	Cx=0, Rx= 1KΩ		150	200		260		320	
		2.0	Cx = 0.01µF Rx = 10KΩ	70	83	96	70	96	70	96	µs
		4.5		69	77	85	69	85	69	85	
		6.0		69	77	85	69	85	69	85	
		2.0	Cx = 0.1µF Rx = 10KΩ	0.67	0.75	0.83	0.67	0.83	0.67	0.9	ms
		4.5		0.67	0.73	0.77	0.67	0.77	0.67	0.8	
		6.0		0.67	0.73	0.77	0.67	0.77	0.67	0.8	
Δt_{WOUT}	Output Pulse Width Error Between Circuits in Same Package				±1						%
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (A,$\overline{B}$)	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CD}$)	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{REM}	Minimum Clear Removal Time	2.0			0	15		15		20	ns
		4.5			0	5		5		7	
		6.0			0	5		5			
t_{rr}	Minimum Retrigger Time	2.0	Cx = 0.1 µF Rx = 1KΩ		380						ns
		4.5			92						
		6.0			72						
		2.0	Cx = 0.01µF Rx = 1KΩ		6						µs
		4.5			1.4						
		6.0			1.2						

Table 7: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			70						pF

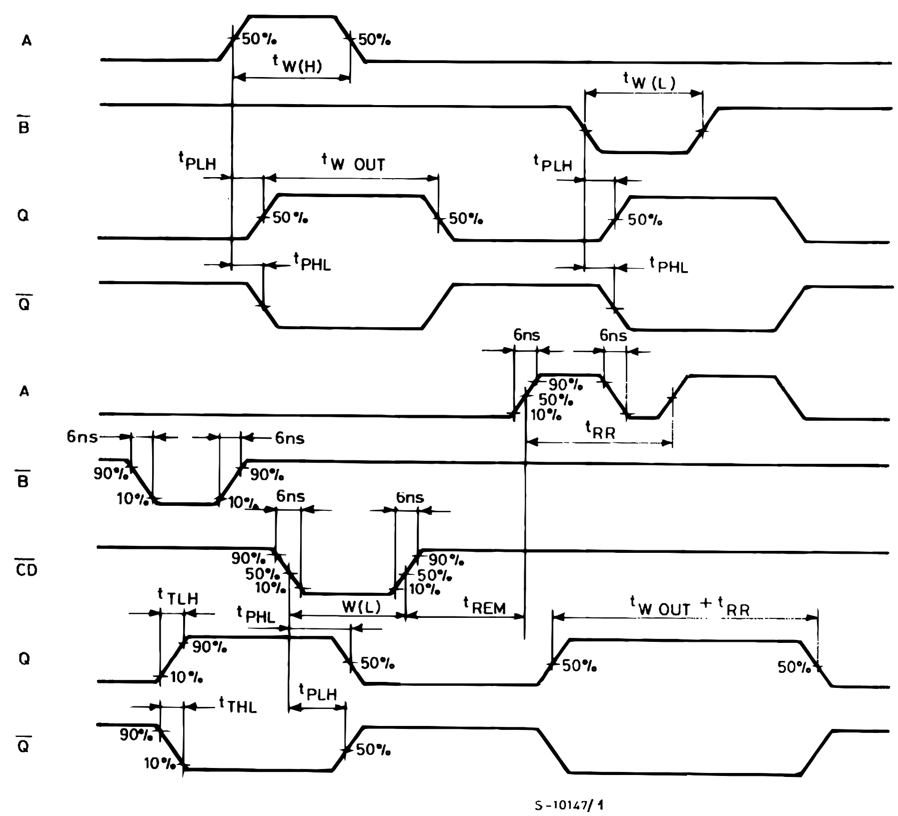
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$' Duty/100 + $I_{C/2}$(per monostable) (I_{cc}': Active Supply current) (Duty:%)

Figure 6: Test Circuit



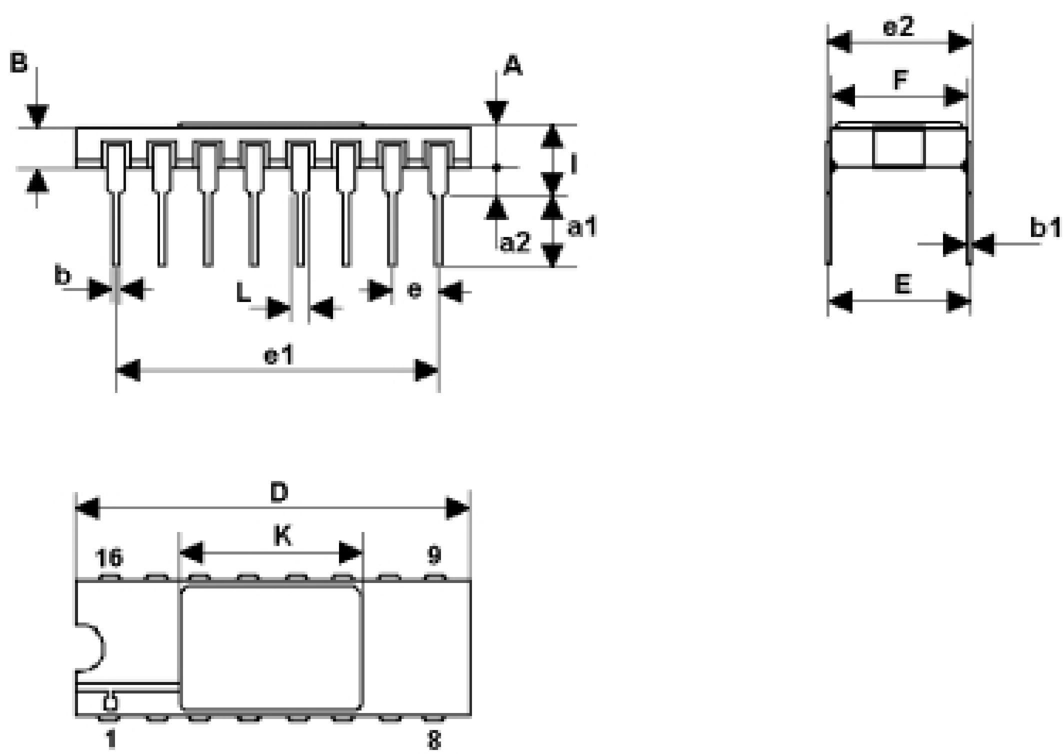
C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 7: Switching Characteristics Test Waveform (f=1MHz; 50% duty cycle)



DILC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82		2.39	0.072		0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	20.06	20.32	20.58	0.790	0.800	0.810
E	7.36	7.62	7.87	0.290	0.300	0.310
e		2.54			0.100	
e1	17.65	17.78	17.90	0.695	0.700	0.705
e2	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.83			0.151
K	10.90		12.1	0.429		0.476
L	1.14		1.5	0.045		0.059



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FPC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	6.75	6.91	7.06	0.266	0.272	0.278
B	9.76	9.94	10.14	0.384	0.392	0.399
C	1.49		1.95	0.059		0.077
D	0.102	0.127	0.152	0.004	0.005	0.006
E	8.76	8.89	9.01	0.345	0.350	0.355
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H	6.0			0.237		
L	18.75		22.0	0.738		0.867
M	0.33	0.38	0.43	0.013	0.015	0.017
N		4.31			0.170	

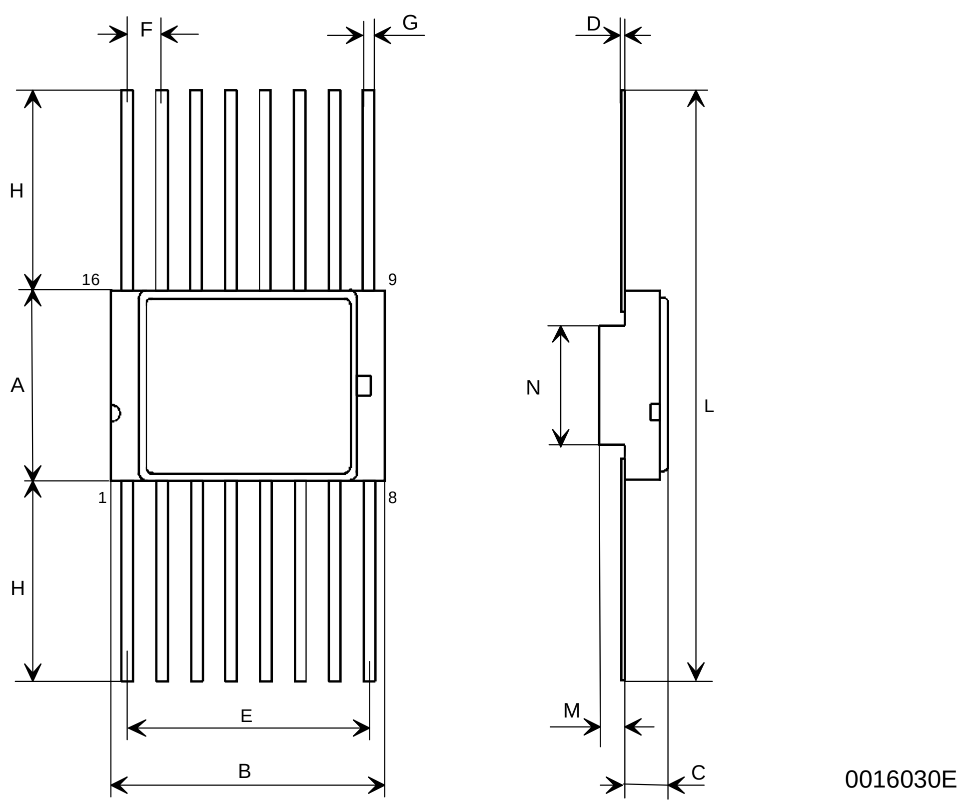

Table 8: Revision History

Date	Revision	Description of Changes
16-Jun-2004	1	First Release