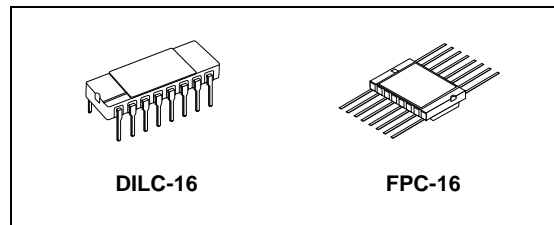


RAD-HARD HEX D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED:
 $f_{MAX} = 66\text{MHz}$ (TYP.) at $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH
 54 SERIES 174
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON
 REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS
 IRRADIATION
- DEVICE FULLY COMPLIANT WITH
 SCC-9306-052

DESCRIPTION

The M54HC174 is an high speed CMOS HEX D-TYPE FLIP FLOP WITH CLEAR fabricated with silicon gate C²MOS technology.



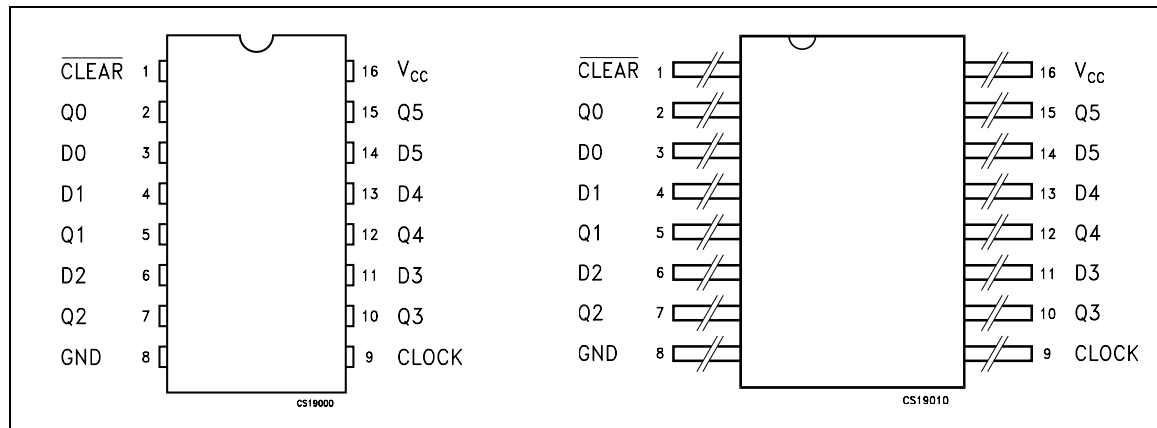
ORDER CODES

PACKAGE	FM	EM
DILC	M54HC174D	M54HC174D1
FPC	M54HC174K	M54HC174K1

Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse. When the CLEAR input is held low, the Q outputs are held low independently of the other inputs.

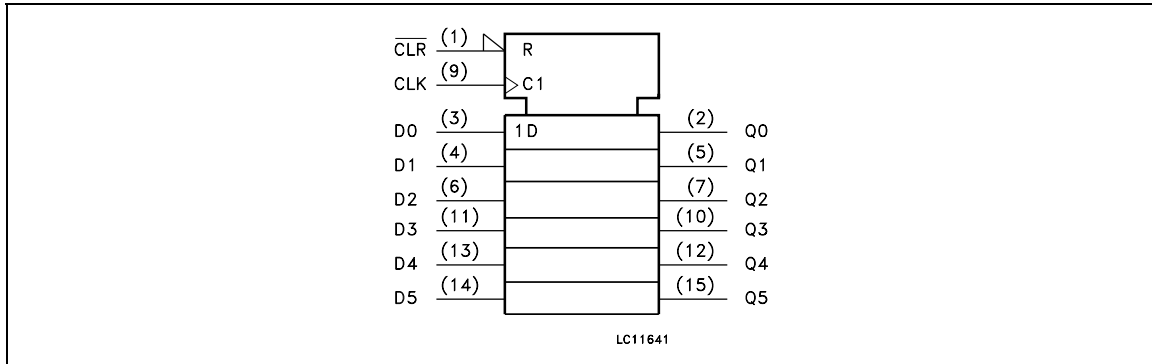
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION

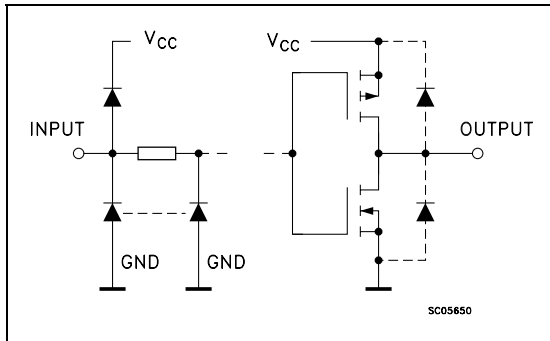


M54HC174

IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

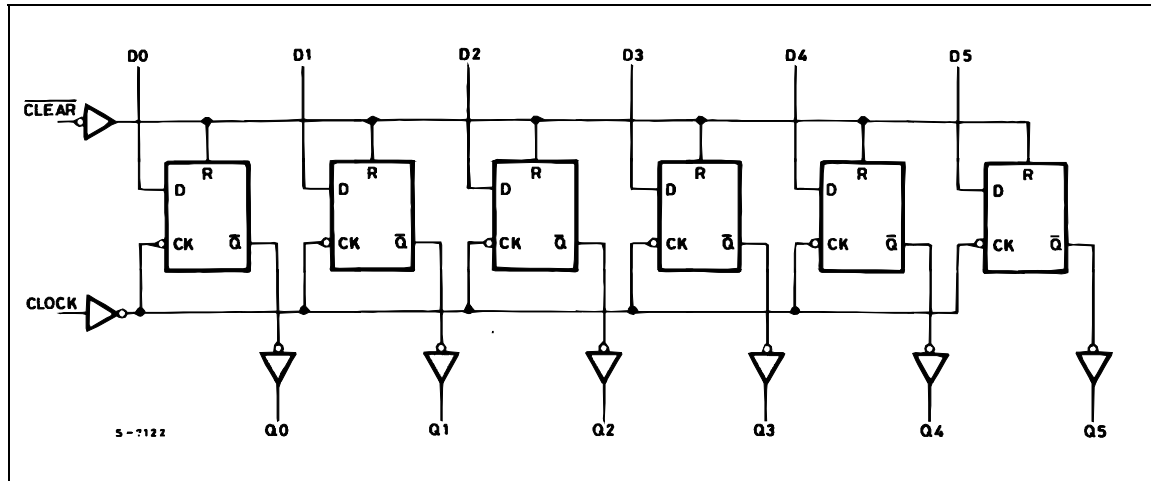
PIN N°	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Asynchronous Master Reset (Active Low)
2, 5, 7, 10, 12, 15	Q0 to Q5	Flip-Flop Outputs
3, 4, 6, 11, 13, 14	D0 to D5	Data Inputs
9	CLOCK	Clock Input (LOW to HIGH, edge triggered)
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
$\overline{\text{CLEAR}}$	D	CK	Q	
L	X	X	L	CLEAR
H	L		L	
H	H		H	
H	X		Q _n	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not to be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	300	mW
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (10 sec)	265	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	Input Voltage	0 to V_{CC}	V	
V_O	Output Voltage	0 to V_{CC}	V	
T_{op}	Operating Temperature	-55 to 125	$^{\circ}C$	
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V _{OH}	High Level Output Voltage	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I _O =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I _O =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I _O =-5.2 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I _O =20 μA		0.0	0.1		0.1		0.1	
		6.0	I _O =20 μA		0.0	0.1		0.1		0.1	
		4.5	I _O =4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I _O =5.2 mA		0.18	0.26		0.33		0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			4		40		80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	Test Condition		Value						Unit		
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns	
		4.5			8	15		19		22		
		6.0			7	13		16		19		
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			68	135		170		205	ns	
		4.5			17	27		34		41		
		6.0			14	23		29		35		
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Q)	2.0			72	145		180		220	ns	
		4.5			18	29		36		44		
		6.0			15	25		31		37		
f_{MAX}	Maximum Clock Frequency	2.0			7.2	14		5.8		4.8	MHz	
		4.5			36	56		29		24		
		6.0			42	66		34		28		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0				24	75		95		110	ns
		4.5				6	15		19		22	
		6.0				5	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0				24	75		95		110	ns
		4.5				6	15		19		22	
		6.0				5	13		16		19	
t_s	Minimum Set-up Time	2.0				28	75		95		110	ns
		4.5				7	15		19		22	
		6.0				6	13		16		19	
t_h	Minimum Hold Time	2.0					0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t_{REM}	Minimum Removal Time	2.0				5	5		5		5	ns
		4.5				5	5		5		5	
		6.0				5	5		5		5	

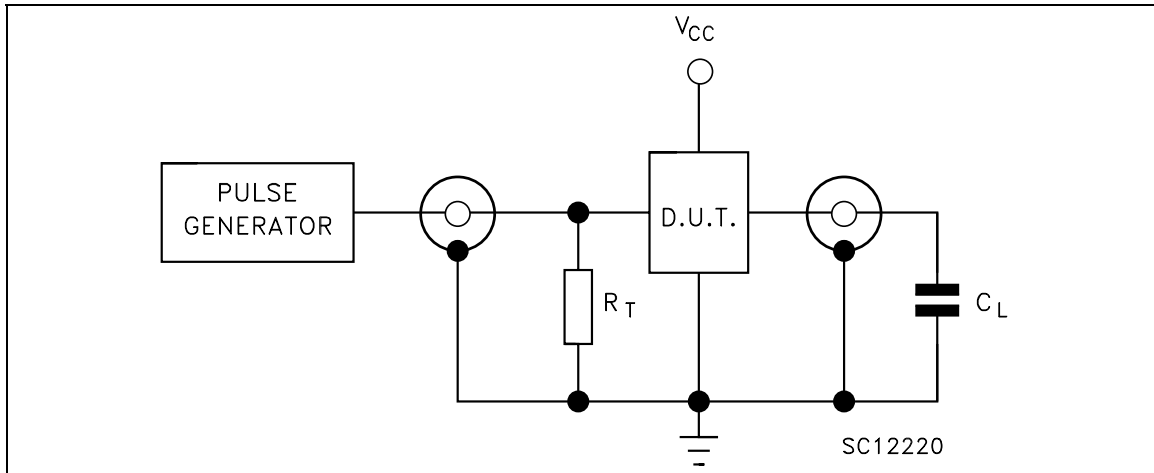
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit		
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
C_{IN}	Input Capacitance	5.0				5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0				40						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/6$ (per FLIP/FLOP)

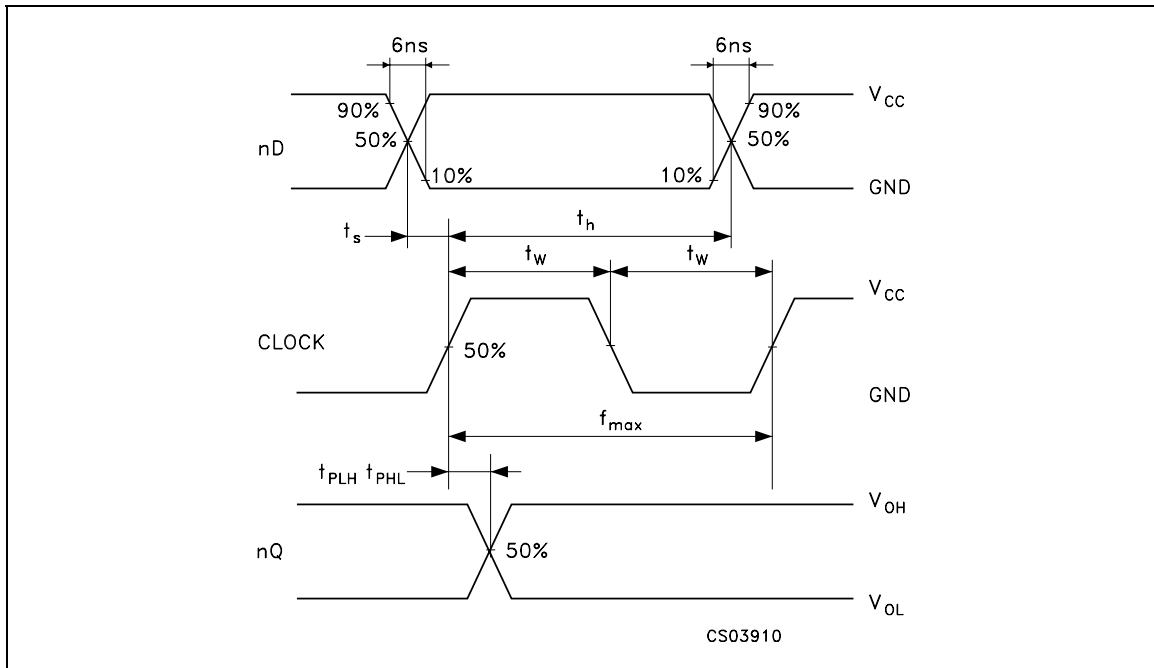
And the total CPD when N pcs of FLIP-FLOP operate can be gained by the following equation: $CPD(\text{total}) = 38 + 15 \times n$

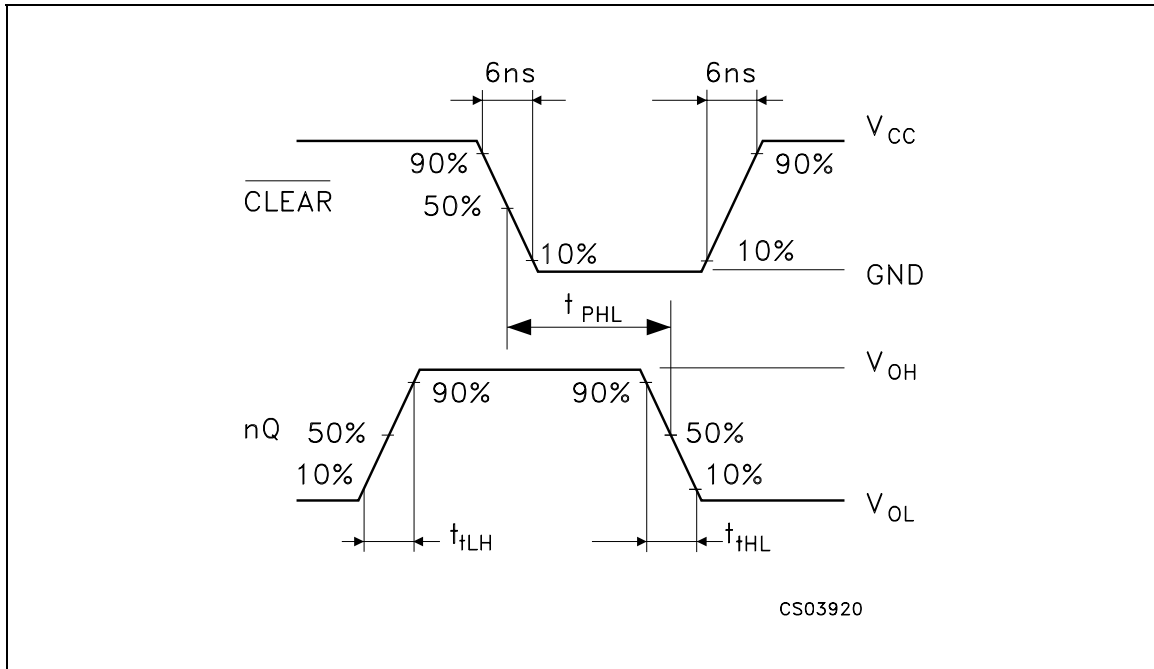
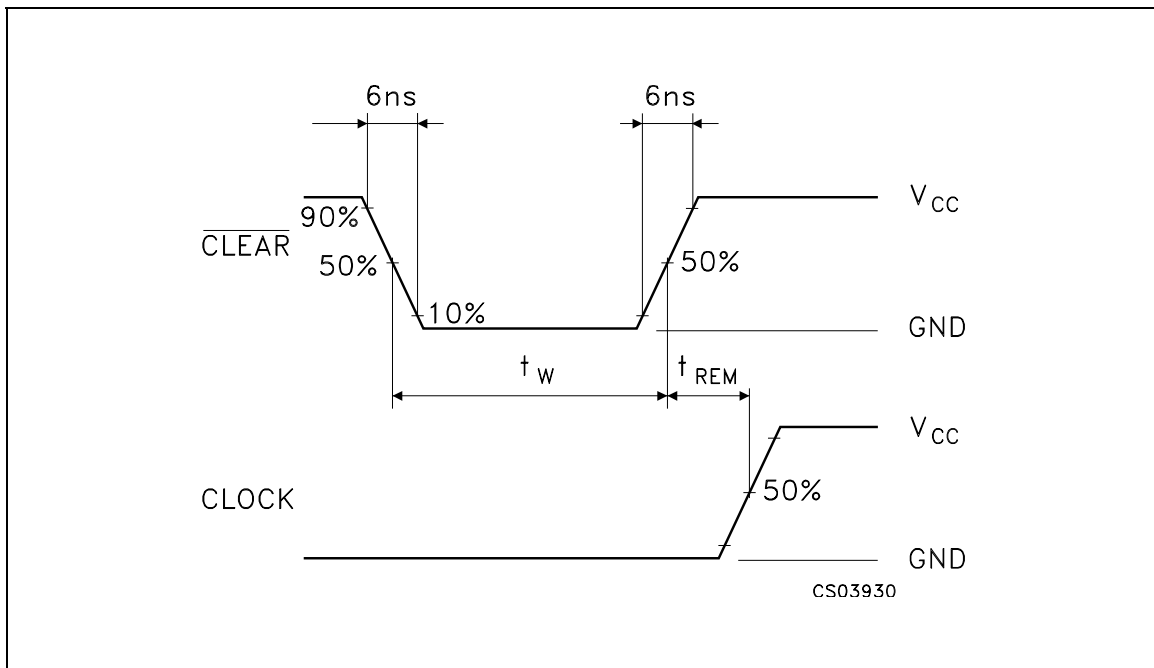
TEST CIRCUIT



$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

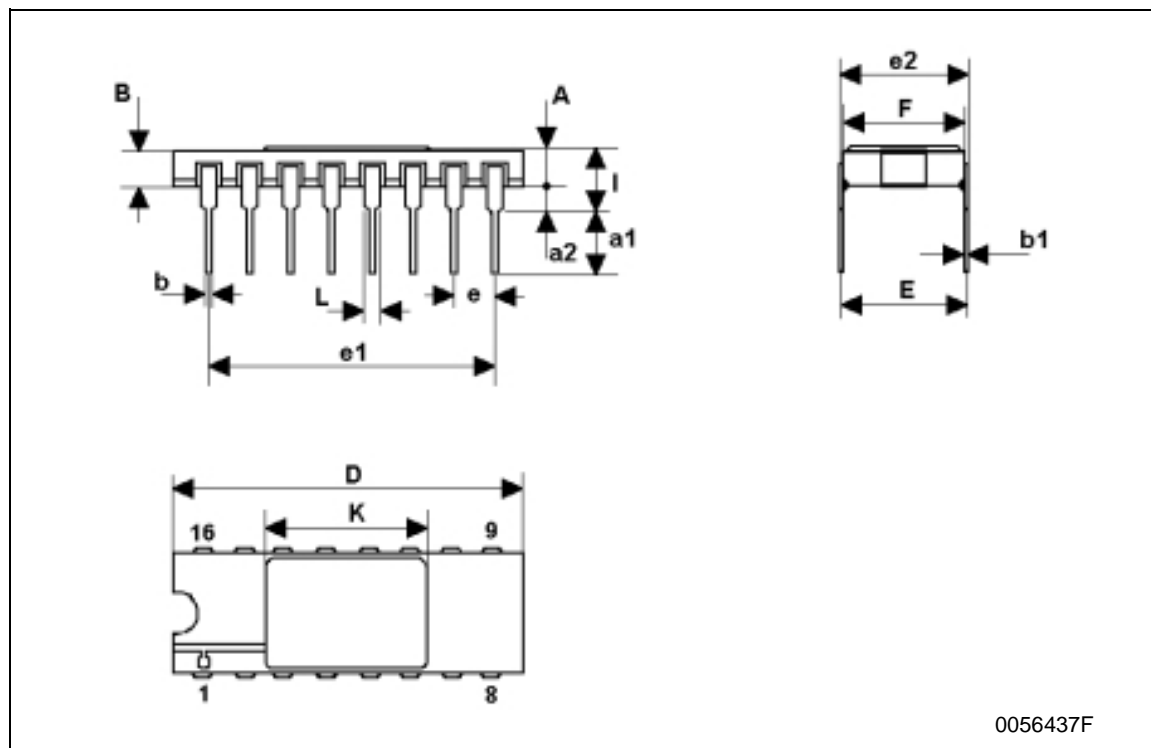
WAVEFORM 1: PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH (CLOCK), SETUP AND HOLD TIME (nD TO CLOCK), CLOCK MAXIMUM FREQUENCY ($f=1\text{MHz}$; 50% duty cycle)



WAVEFORM 2: PROPAGATION DELAY TIME (nQ TO $\overline{\text{CLEAR}}$) ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 3: MINIMUM PULSE WIDTH ($\overline{\text{CLEAR}}$), MINIMUM REMOVAL TIME ($\overline{\text{CLEAR}}$ TO CLOCK)** ($f=1\text{MHz}$; 50% duty cycle)

DILC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82		2.39	0.072		0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	20.06	20.32	20.58	0.790	0.800	0.810
e	7.36	7.62	7.87	0.290	0.300	0.310
e1		2.54			0.100	
e2	17.65	17.78	17.90	0.695	0.700	0.705
e3	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.83			0.151
K	10.90		12.1	0.429		0.476
L	1.14		1.5	0.045		0.059



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