

54ABT16245

16-Bit Transceiver with TRI-STATE® Outputs

General Description

The 'ABT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The T/R inputs determine the direction of data flow through the device. The OE inputs disable both the A and B ports by placing them in a high impedance state.

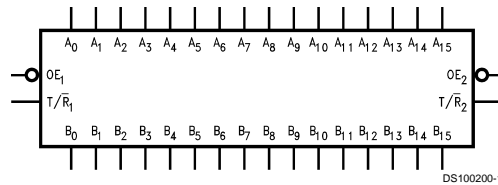
- Separate control logic for each byte
- 16-bit version of the 'ABT245
- A and B output sink capability of 48 mA, source capability of 24 mA
- Guaranteed latching protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9317501

Features

- Bidirectional non-inverting buffers

Military	Package Number	Package Description
54ABT16245W-QML	WA48A	48-Lead Cerpack

Logic Symbol



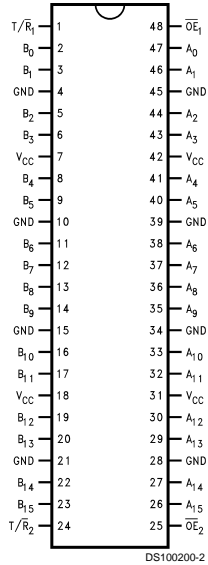
Pin Description

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active Low)
T/R _n	Transmit/Receive Input
A ₀ -A ₁₅	Side A Inputs/Outputs
B ₀ -B ₁₅	Side B Inputs/Outputs

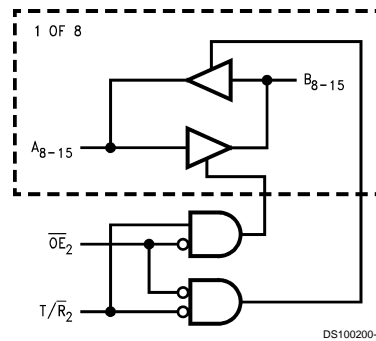
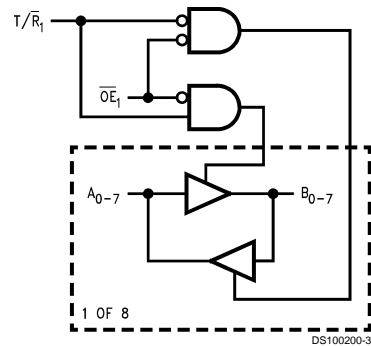
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Connection Diagram

Pin Assignment for Cerpack



Logic Diagrams



Functional Description

The 'ABT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Table

Inputs		Outputs
\overline{OE}_1	T/\overline{R}_1	
L	L	Bus B ₀ -B ₇ Data to Bus A ₀ -A ₇
L	H	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇
H	X	HIGH-Z State on A ₀ -A ₇ , B ₀ -B ₇

Inputs		Outputs
\overline{OE}_2	T/\overline{R}_2	
L	L	Bus B ₈ -B ₁₅ Data to Bus A ₈ -A ₁₅
L	H	Bus A ₈ -A ₁₅ Data to Bus B ₈ -B ₁₅
H	X	HIGH-Z State on A ₈ -A ₁₅ , B ₈ -B ₁₅

H = High Voltage Level
 L = Low Voltage Level
 X = Immaterial
 Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V _{CC} Pin Potential to	
Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V _{CC}

Current Applied to Output	
in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT16245			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA ($\overline{OE}_n, T/\overline{R}_n$)
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{OH} = -3 mA (A _n , B _n)
		54ABT	2.0		V	Min	I _{OH} = -24 mA (A _n , B _n)
V _{OL}	Output LOW Voltage	54ABT	0.55		V	Min	I _{OL} = 48 mA (A _n , B _n)
I _{IH}	Input HIGH Current		5		μA	Max	V _{IN} = 2.7V ($\overline{OE}_n, T/\overline{R}_n$) (Note 3)
			5		μA	Max	V _{IN} = V _{CC} ($\overline{OE}_n, T/\overline{R}_n$)
I _{BVI}	Input HIGH Current Breakdown Test		7		μA	Max	V _{IN} = 7.0V ($\overline{OE}_n, T/\overline{R}_n$)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)		100		μA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current		-5		μA	Max	V _{IN} = 0.5V ($\overline{OE}_n, T/\overline{R}_n$) (Note 3)
			-5		μA	Max	V _{IN} = 0.0V ($\overline{OE}_n, T/\overline{R}_n$)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA ($\overline{OE}_n, T/\overline{R}_n$) All Other Pins Grounded
I _{IH} + I _{OZH}	Output Leakage Current		50		μA	0 - 5.5V	V _{OUT} = 2.7V (A _n , B _n); $\overline{OE} = 2.0V$
I _{IL} + I _{OZL}	Output Leakage Current		-50		μA	0 - 5.5V	V _{OUT} = 0.5V (A _n , B _n); $\overline{OE} = 2.0V$
I _{OS}	Output Short-Circuit Current	-100	-275		mA	Max	V _{OUT} = 0.0V (A _n , B _n)
I _{CEX}	Output High Leakage Current		50		μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test		100		μA	0.0	V _{OUT} = 5.50V (A _n , B _n); All Others GND
I _{CCH}	Power Supply Current		100		μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current		60		mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current		100		μA	Max	$\overline{OE}_n = V_{CC}, T/\overline{R}_n = GND$ or V _{CC} All others at V _{CC} or GND
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled	2.5		mA		V _I = V _{CC} - 2.1V
		Outputs TRI-STATE	2.5		mA	Max	$\overline{OE}_n, T/\overline{R}_n, V_I = V_{CC} - 2.1V$
		Outputs TRI-STATE	50		μA		Data Input V _I = V _{CC} - 2.1V All others at V _{CC} or GND

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT16245			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{CCD}	Dynamic I _{CC} No Load			0.1	mA/ MHz	Max	Outputs Open $\overline{OE}_n = \text{GND}$, $T/\overline{R}_n = \text{GND}$ or V_{CC} One Bit Taggling, 50% Duty Cycle

Note 3: Guaranteed, but not tested.

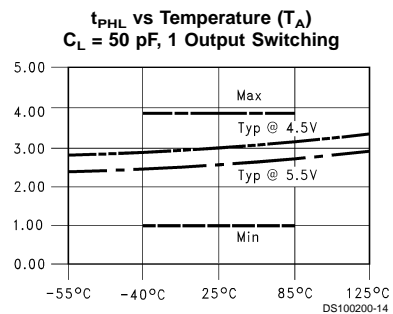
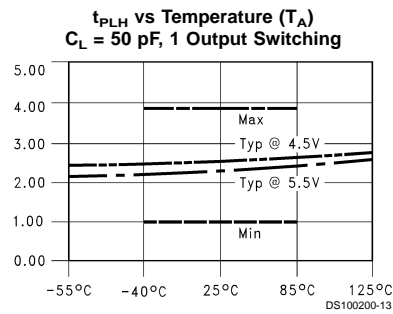
AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V-5.5V C _L = 50 pF			
		Min	Max		
t _{PLH}	Propagation	0.5	4.5	ns	Figure 5
t _{PHL}	Delay Data to Outputs	0.5	5.2		
t _{PZH}	Output Enable Time	0.8	6.4	ns	Figure 4
t _{PZL}	Output Disable Time	0.9	6.9	ns	Figure 4
t _{PHZ}	Output Disable Time	1.3	6.9	ns	Figure 4
t _{PLZ}	Output Disable Time	1.0	6.9	ns	Figure 4

Capacitance

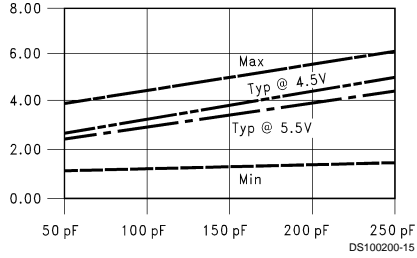
Symbol	Parameter	Typ	Units	Conditions, T _A = 25°C
C _{IN}	Input Capacitance	5	pF	V _{CC} = 0.0V (\overline{OE}_n , T/\overline{R}_n)
C _{I/O} (Note 4)	Output Capacitance	11	pF	V _{CC} = 5.0V (A _n , B _n)

Note 4: C_{I/O} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

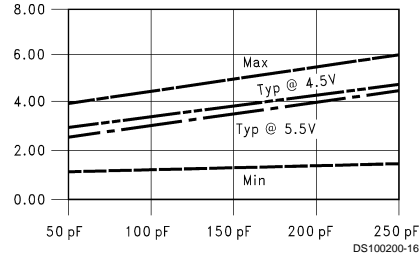


Capacitance (Continued)

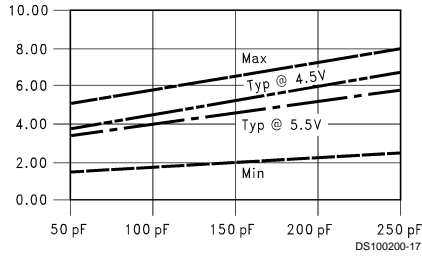
t_{PLH} vs Load Capacitance
1 Output Switching, $T_A = 25^\circ\text{C}$



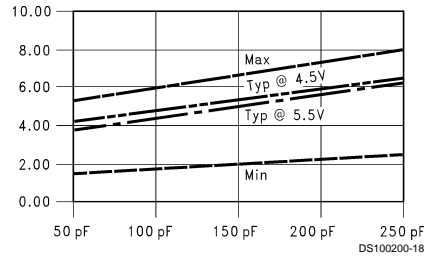
t_{PHL} vs Load Capacitance
1 Output Switching, $T_A = 25^\circ\text{C}$



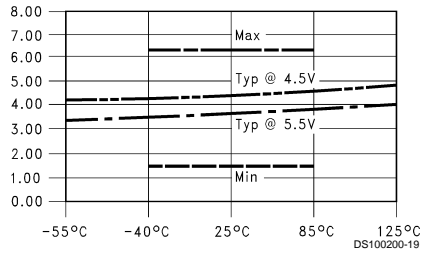
t_{PLH} vs Load Capacitance
16 Outputs Switching, $T_A = 25^\circ\text{C}$



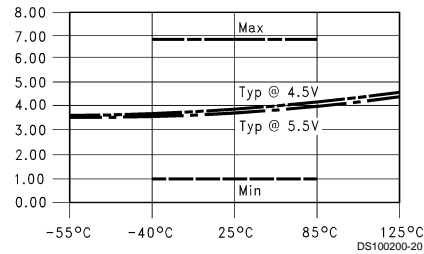
t_{PHL} vs Load Capacitance
16 Outputs Switching, $T_A = 25^\circ\text{C}$



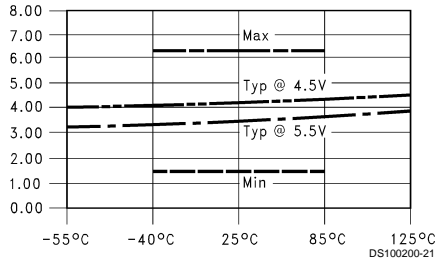
t_{PZL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



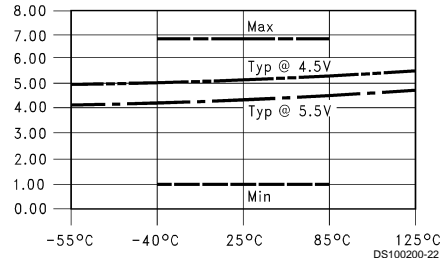
t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



t_{PZH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching

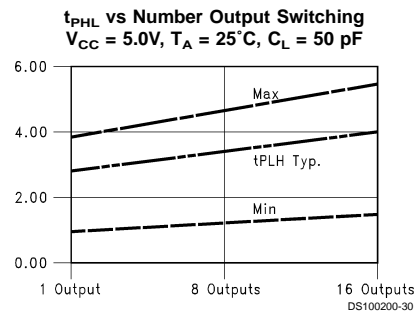
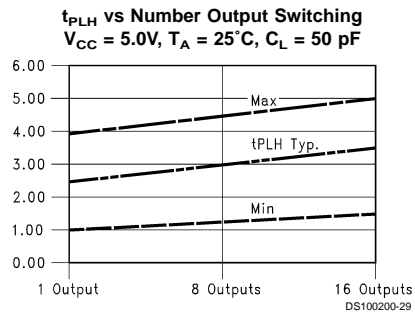
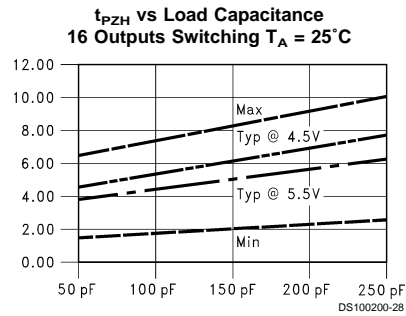
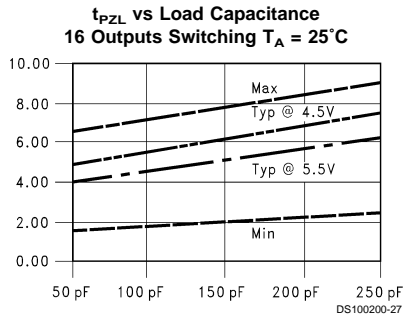
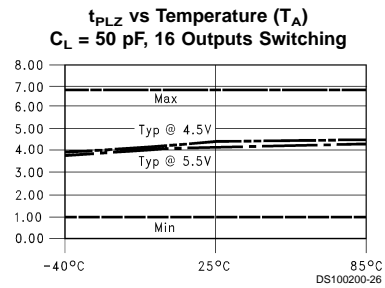
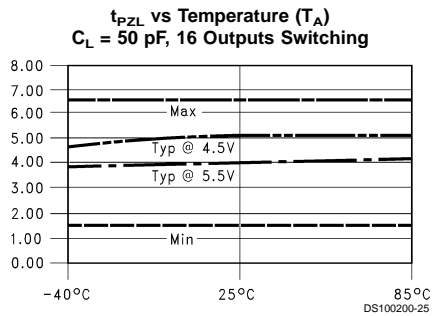
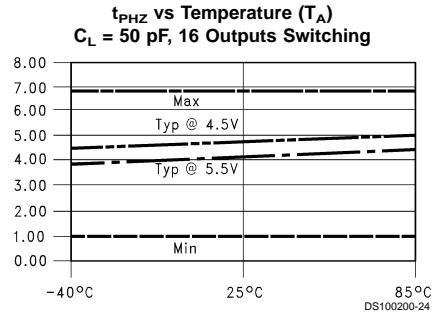
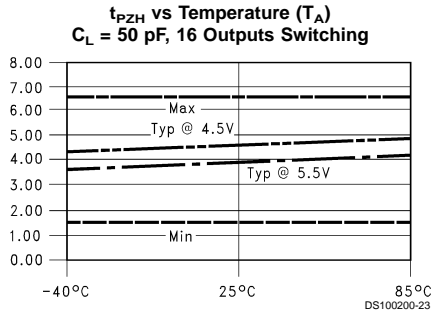


t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

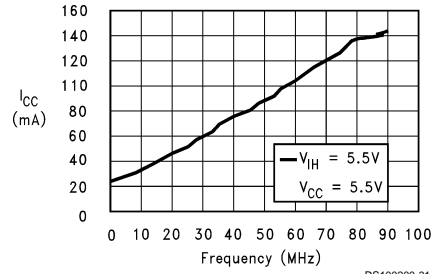
Capacitance (Continued)



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

Capacitance (Continued)

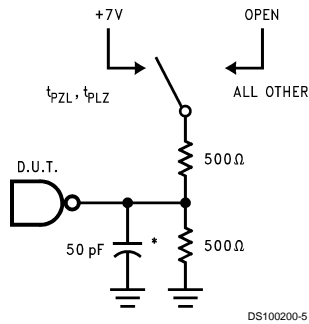
I_{CC} vs Frequency
Average, $T_A = 25^\circ\text{C}$, $V_{CC} = 5.5\text{V}$
All Outputs Unloaded/Unterminated;
16 Outputs Switching In-Phase at 50
Duty Cycle



DS100200-31

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

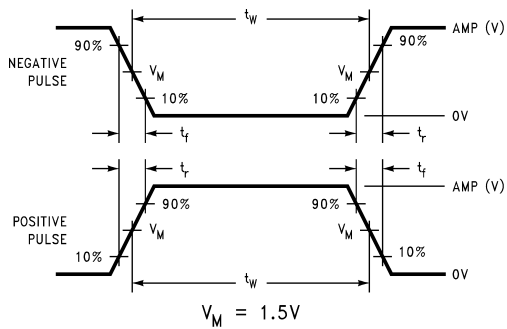


FIGURE 2. Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

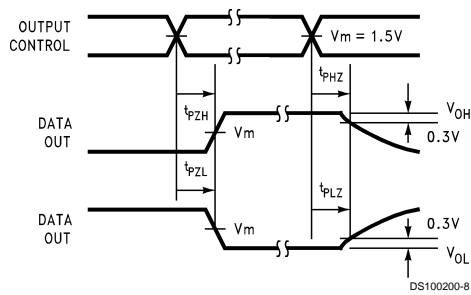


FIGURE 4. TRI-STATE Output HIGH and LOW Enable and Disable Times

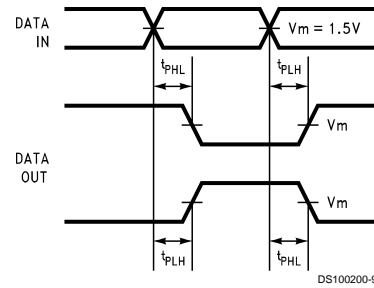
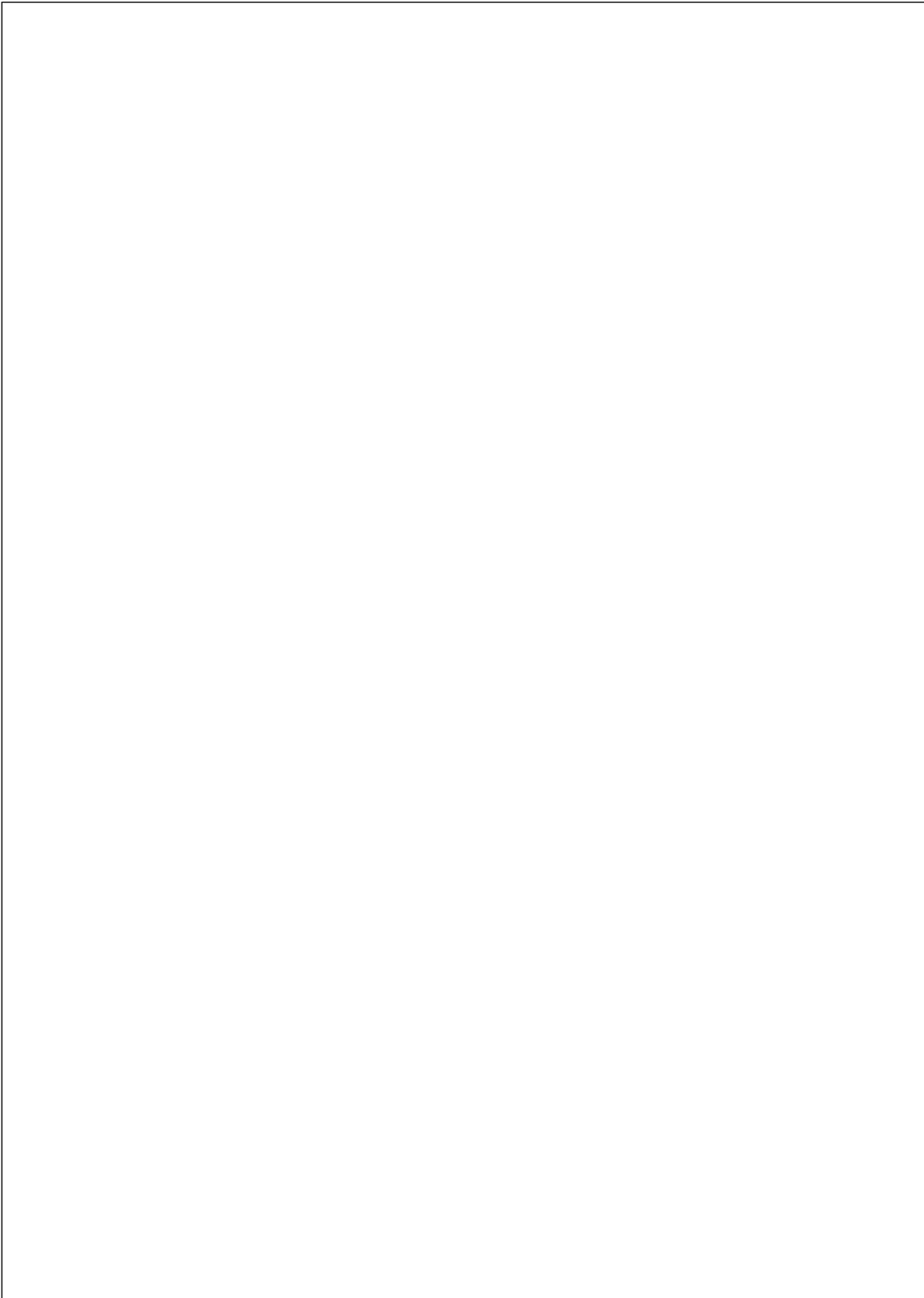
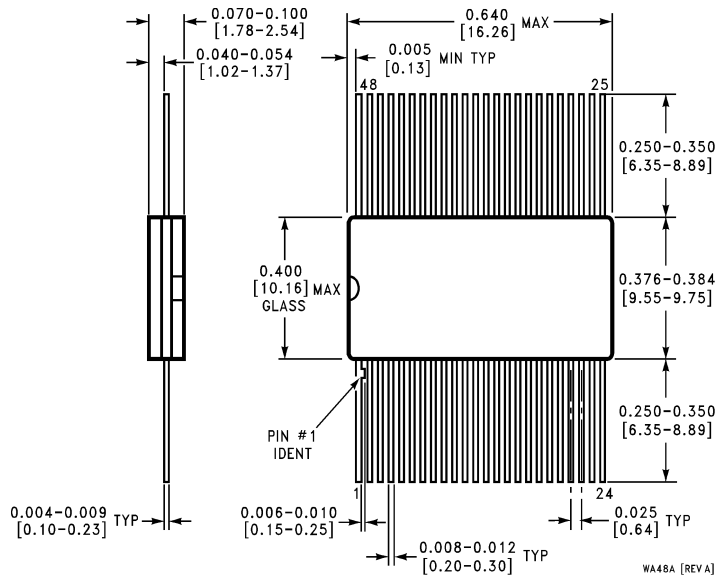


FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

Book
Extract
End



Physical Dimensions inches (millimeters) unless otherwise noted



**48-Lead Cerpack
NS Package Number WA48A**

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