National Semiconductor

July 1998

54ABT574
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'ABT574 is an octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The device is functionally identical to the 'ABT374 except for the pinouts.

Features

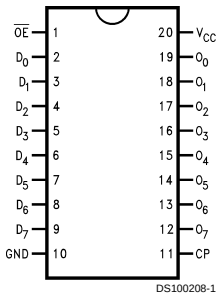
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ABT374
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 48 mA, source capability of 24 mA
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9322001

Ordering Code

Military	Package Number	Package Description
54ABT574J/883	J20A	20-Lead Ceramic Dual-In-Line
54ABT574W/883	W20A	20-Lead Cerpack
54ABT574E/883	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagrams

Pin Assignment for DIP and Flatpak



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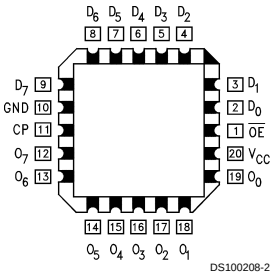
Pin Assignment for LCC



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Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Outputs

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Functional Description

The 'ABT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

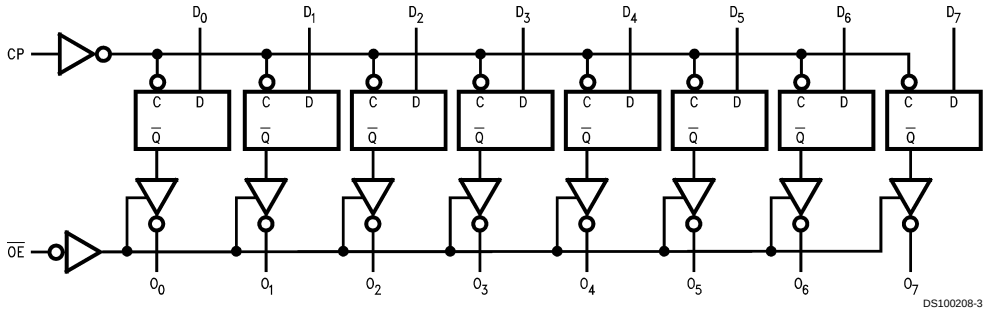
Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H or L	L	NC	Z	Hold

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H or L	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H or L	L	NC	NC	No Change in Data
L	H or L	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in	
the Disabled or Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		ABT574 Min	ABT574 Typ	ABT574 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −24 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (Note 4)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (Note 4)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA
								All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Other GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}$ = V_{CC}
								All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA		V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA	Max	Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V
								All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}	No Load				mA/	Max	Outputs Open, $\overline{OE}$ = GND,
	(Note 4)				0.30	MHz		One Bit Toggling (Note 3),
								50% Duty Cycle

Note 3: For 8-bit toggling, I_{CCD} < 0.8 mA/MHz.

Note 4: Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT $T_A = -55^\circ C$ to $+125^\circ C$, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units
		Min	Max	
f_{max}	Max Clock Frequency	150		MHz
t_{PLH}	Propagation Delay	1.5	7.0	ns
t_{PHL}	CP to O_n	1.5	7.4	
t_{PZH}	Output Enable Time	1.0	6.5	ns
t_{PZL}		1.0	7.2	
t_{PHZ}	Output Disable Time	1.0	7.2	ns
t_{PLZ}		1.0	6.7	

AC Operating Requirements

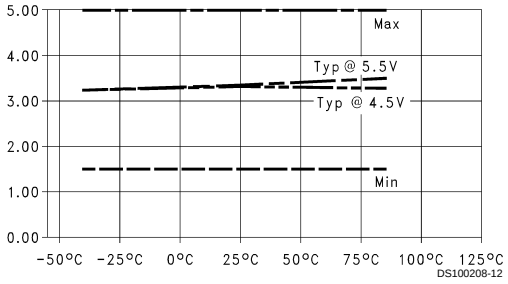
Symbol	Parameter	54ABT $T_A = -55^\circ C$ to $+125^\circ C$, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units
		Min	Max	
$t_s(H)$	Setup Time, HIGH	1.5		ns
$t_s(L)$	or LOW D_n to CP	2.0		
$t_h(H)$	Hold Time, HIGH	2.0		ns
$t_h(L)$	or LOW D_n to CP	2.0		
$t_w(H)$	Pulse Width, CP,	3.3		ns
$t_w(L)$	HIGH or LOW	3.3		

Capacitance

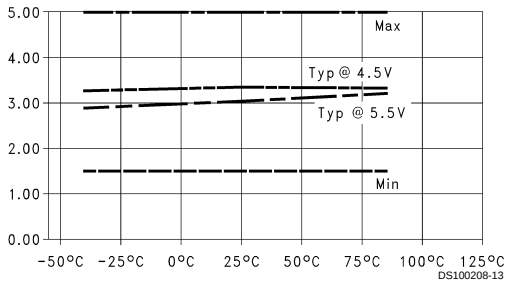
Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ C$
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 0V
C_{OUT} (Note 5)	Output Capacitance	9.0	pF	V_{CC} = 5.0V

Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

T_{PHL} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching, Clock to Output

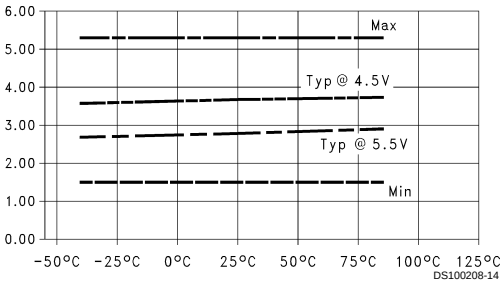


T_{PLH} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching, Clock to Output

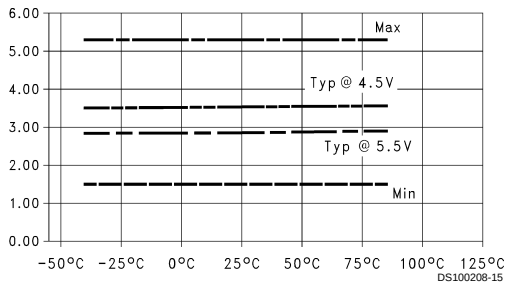


Capacitance (Continued)

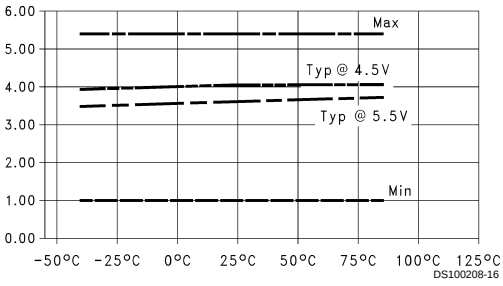
T_{PZH} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching, OE to Output



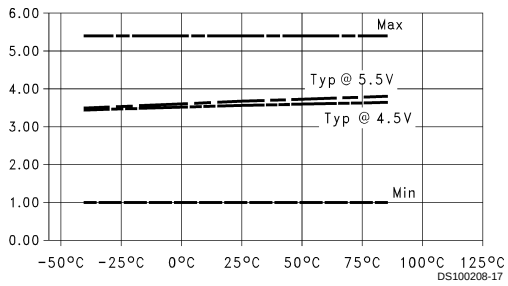
T_{PZL} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching, OE to Output



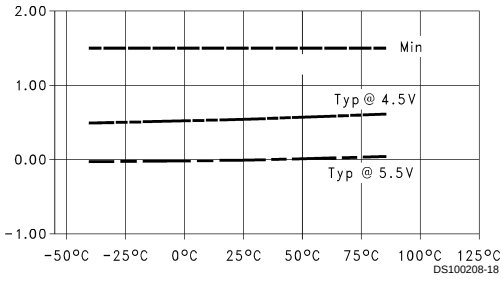
T_{PHZ} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching, OE to Output



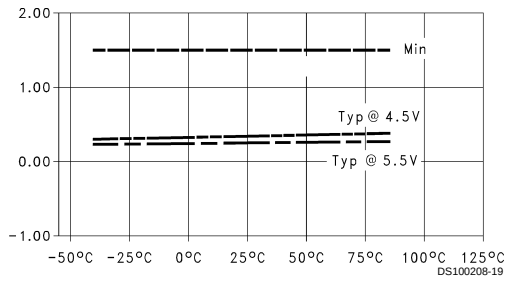
T_{PLZ} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching, OE to Output



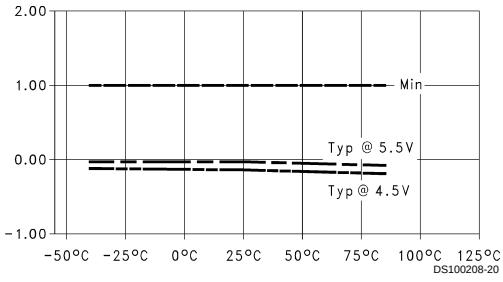
T_{SET} LOW vs Temperature (T_A) C_L = 50 pF, 1 Output Switching, Data to Clock



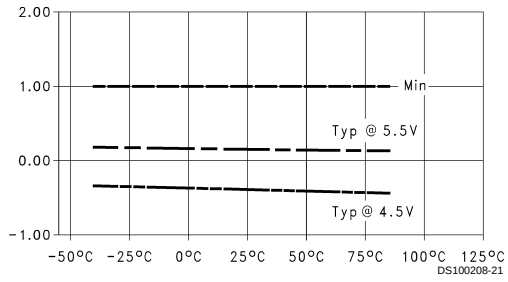
T_{SET} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching, Data to Clock



T_{HOLD} HIGH vs Temperature (T_A) C_L = 50 pF, 1 Output Switching, Data to Clock

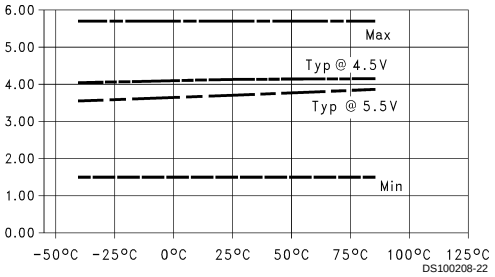


T_{HOLD} LOW vs Temperature (T_A) C_L = 50 pF, 1 Output Switching, Data to Clock

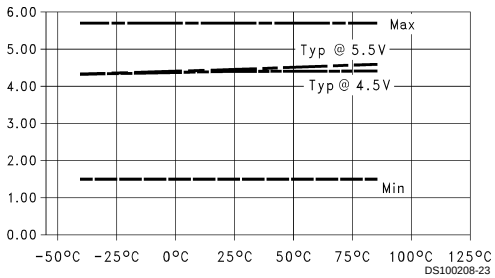


Capacitance (Continued)

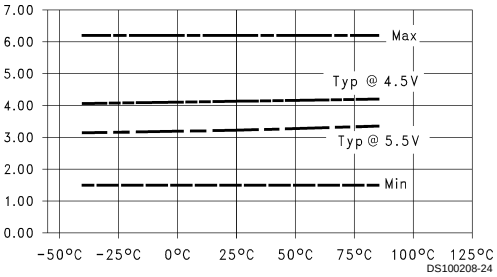
T_{PLH} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching, Clock to Output



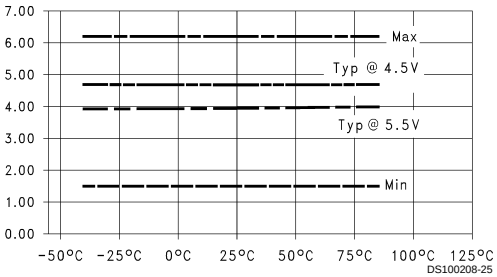
T_{PHL} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching, Clock to Output



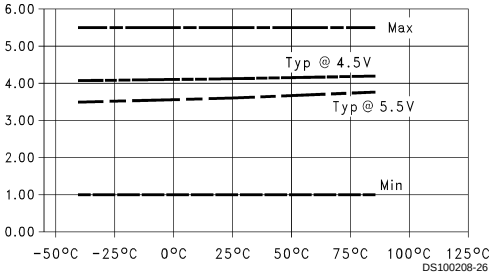
T_{PZH} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching, OE to Output



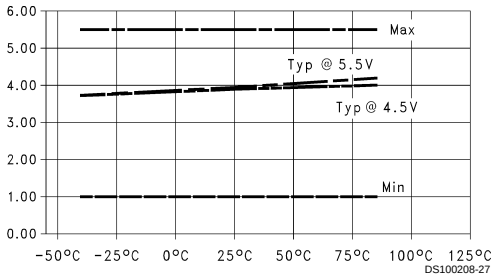
T_{PZL} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching, OE to Output



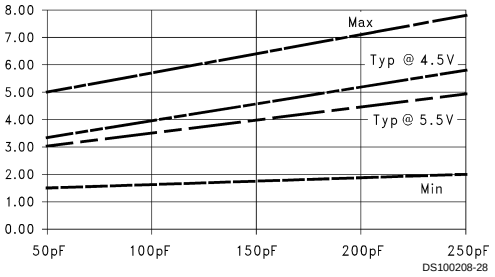
T_{PHZ} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching, OE to Output



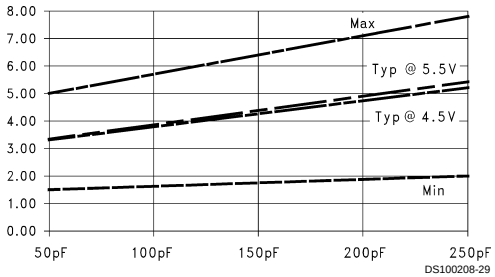
T_{PLZ} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching, OE to Output



T_{PLH} vs Load Capacitance T_A = 25°C, 1 Output Switching, Clock to Output

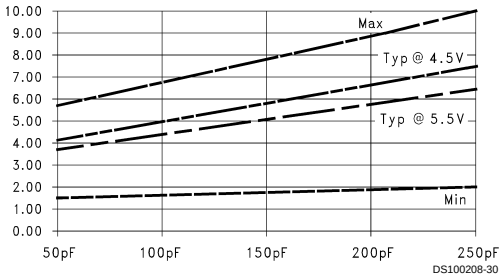


T_{PHL} vs Load Capacitance T_A = 25°C, 1 Output Switching, Clock to Output



Capacitance (Continued)

T_{PLH} vs Load Capacitance T_A = 25˚C, 8 Outputs Switching, Clock to Output



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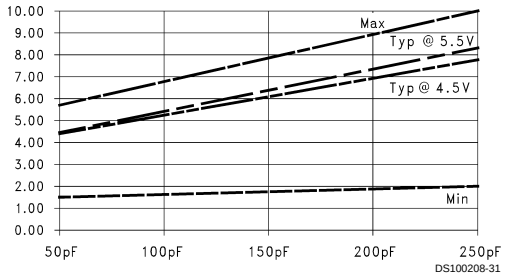
T_{PHL} vs Load Capacitance T_A = 25˚C, 8 Outputs Switching, Clock to Output



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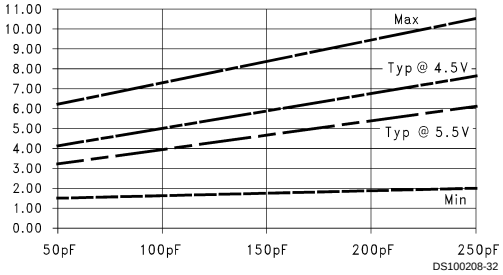
T_{PZH} vs Load Capacitance T_A = 25˚C, 8 Outputs Switching, $\overline{OE}$ to Output



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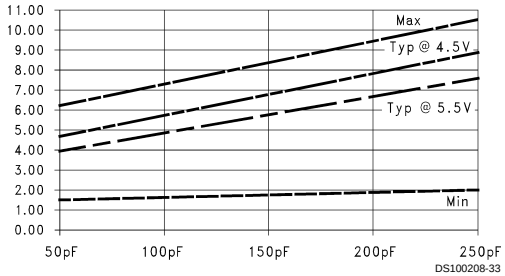
T_{PZL} vs Load Capacitance T_A = 25˚C, 8 Outputs Switching, $\overline{OE}$ to Output



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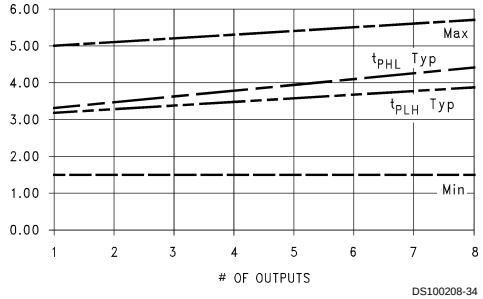
T_{PLH} and T_{PHL} vs Number Outputs Switching C_L = 50 pF, T_A = 25˚C, V_{CC} = 5.0V, Outputs In Phase, Clock to Output



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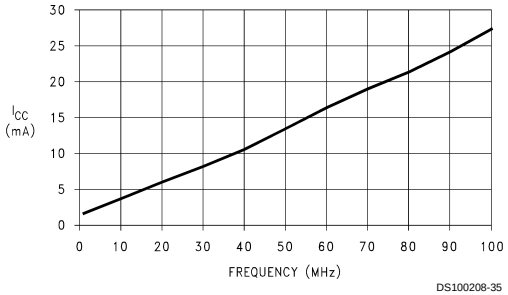
Typical I_{CC} vs Output Switching Frequency C_L = 0 pF, V_{CC} = V_{IH} = 5.5V, 1 Output Switching at 50% Duty Cycle



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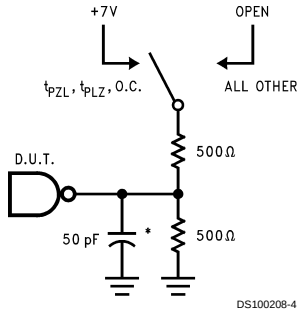
AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

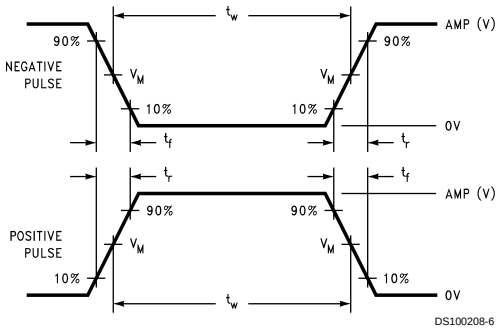


FIGURE 2. V_M = 1.5V

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

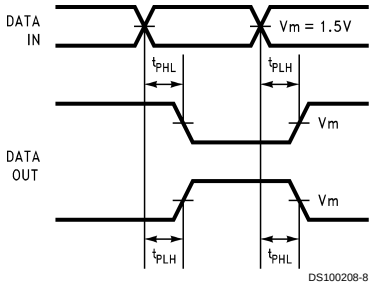


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

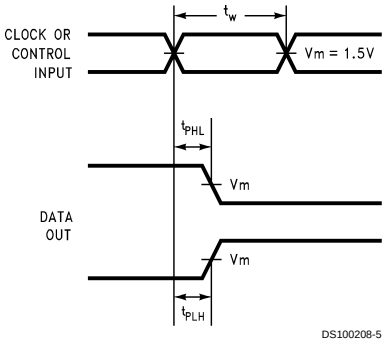


FIGURE 5. Propagation Delay, Pulse Width Waveforms

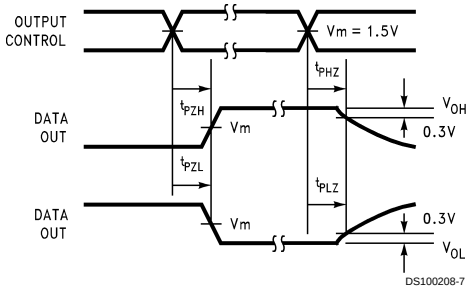


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

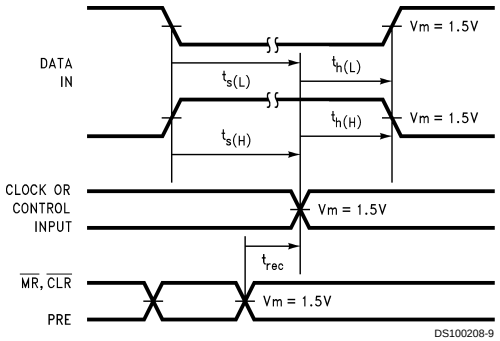
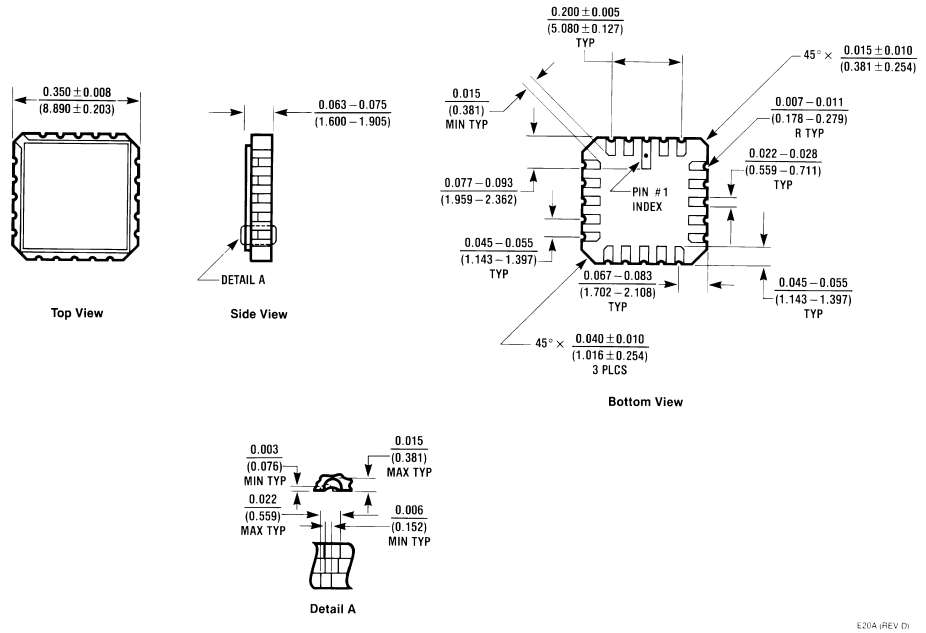
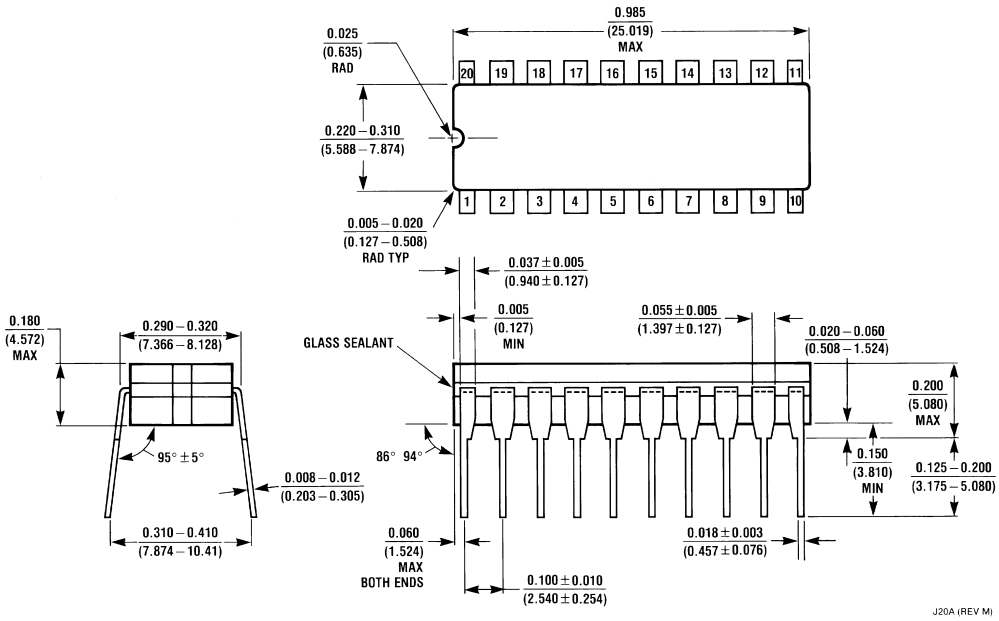


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

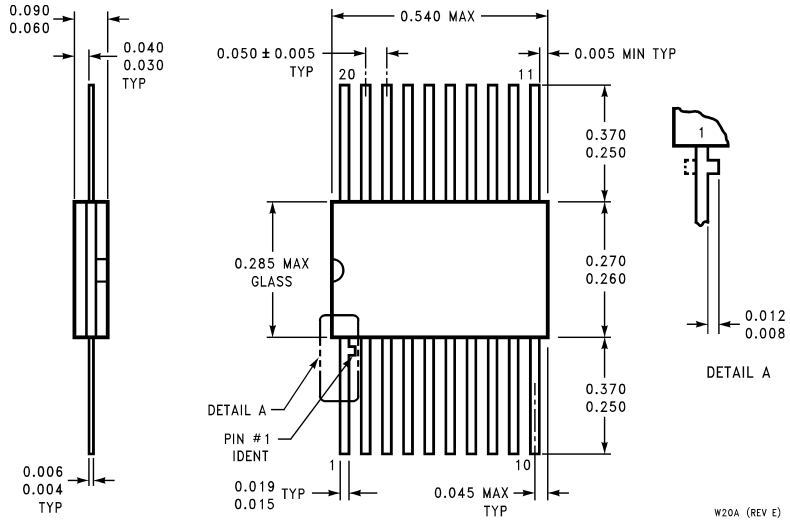


20-Terminal Ceramic Chip Carrier (L)
NS Package Number E20A



20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

LIFE SUPPORT POLICY

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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