AMCC NPe405L
PowerNP
Data Sheet

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PowerNP NPe405L Data Sheet

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PowerNP NPe405L Embedded Processor Data Sheet

Features

- PowerNP™ technology using an IBM PowerPC® 405 32-bit RISC processor core operating up to 266 MHz
- PC-133 synchronous DRAM (SDRAM) interface
  - 32-bit interface for non-ECC applications
  - 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
- External bus for peripheral devices
  - Flash and ROM interface
  - Direct support for 8-, or 16-bit SRAM and external peripherals
  - Up to 4 devices
- DMA support for external peripherals, internal UARTs and memory
  - Scatter-gather chaining supported
  - Four channels
- Two 10/100 Ethernet MACs supporting up to two external PHYs via MII, RMII, or SMII interfaces
- HDLC interface with 32 channels through two ports at up to 4.096 Mbps each or 8.192 Mbps for a single port
- Programmable interrupt controller
  - Seven external and 29 internal
  - Edge triggered or level-sensitive
  - Positive or negative active
  - Non-critical or critical interrupt to processor core
  - Programmable critical interrupt priority ordering
  - Programmable critical interrupt vector
- Programmable timers
- Two serial ports (16550 compatible UART)
- One IIC interface
- General Purpose I/O (GPIO) available
- Supports JTAG for board level testing
- Internal processor local bus (PLB) runs at SDRAM interface frequency

Description

Designed specifically to address embedded applications, the NPe405L provides a high-performance, low-power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and lower power dissipation requirements.

This chip contains a high-performance RISC processor core, SDRAM controller, Ethernet EMACs, HDLC controller, external bus controller for ROM, Flash, and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

Technology: IBM CMOS SA-12E 0.25 µm (0.18 µm L_{eff})
Package: 23mm, 324-ball enhanced plastic ball grid array (E-PBGA)
Power (typical): 1.3W at 133MHz, 1.7W at 200MHz, 1.8W at 266MHz

Contents

Tables

Figures

Ordering, PVR, and JTAG Information

Product Name	Order Part Number[1]	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
NPe405L	IBM25NPe405L-3FA133C	133MHz	23mm, 324 E-PBGA	A	0x416100C0	0x04247409
NPe405L	IBM25NPe405L-3FA133CZ	133MHz	23mm, 324 E-PBGA	A	0x416100C0	0x04247409
NPe405L	IBM25NPe405L-3FA200C	200MHz	23mm, 324 E-PBGA	A	0x416100C0	0x04247409
NPe405L	IBM25NPe405L-3FA200CZ	200MHz	23mm, 324 E-PBGA	A	0x416100C0	0x04247409
NPe405L	IBM25NPe405L-3FA266C	266MHz	23mm, 324 E-PBGA	A	0x416100C0	0x04247409
NPe405L	IBM25NPe405L-3FA266CZ	266MHz	23mm, 324 E-PBGA	A	0x416100C0	0x04247409

Note 1: Z at the end of the Order Part Number indicates a tape and reel shipping package. Otherwise, the chips are shipped in a tray.

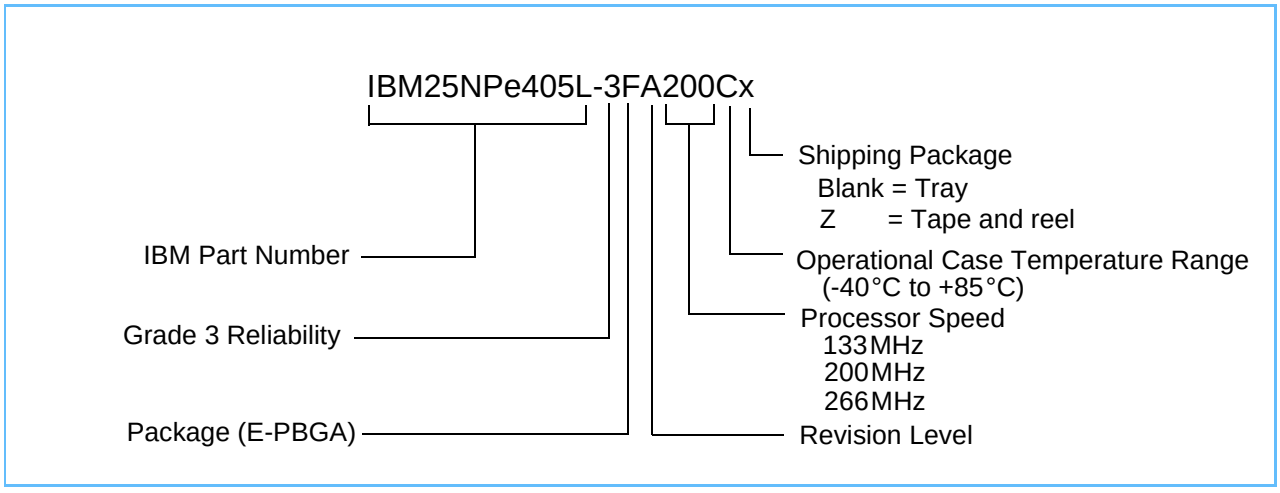
This section provides the part numbering nomenclature for the NPe405L. For availability, contact your local IBM sales office.

The part number contains a part modifier. This modifier provides for identification of future enhancements (for example, higher performance).

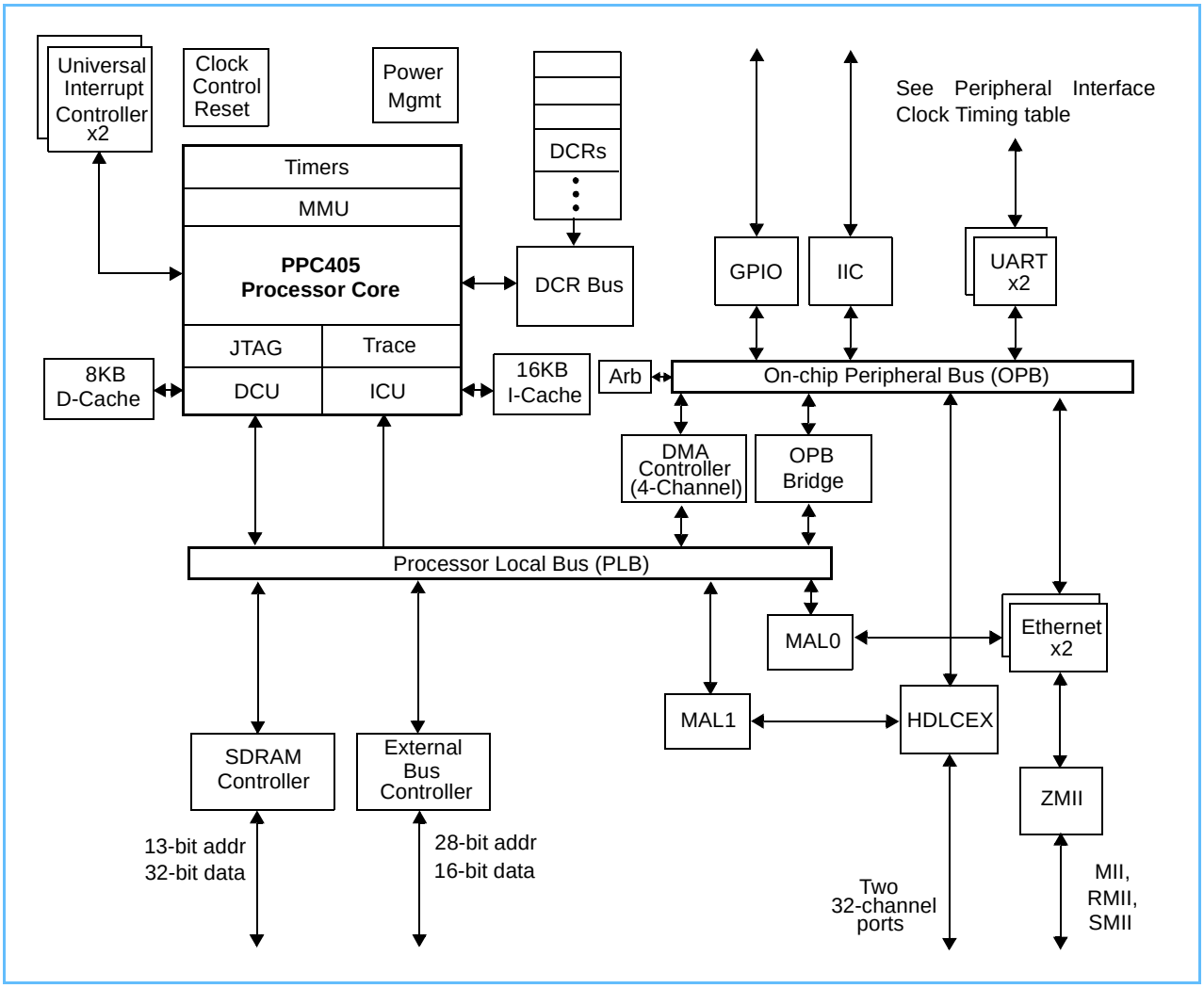
Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

The PVR (Processor Version Register) is software accessible and contains additional information about the revision level of the part. Refer to the NPe405L User's Manual for details on the register content.

IBM Part Number Key



NPe405L Embedded Controller Functional Block Diagram



The NPe405L is designed using the IBM Microelectronics Blue Logic™ methodology in which major functional blocks are integrated to create an application-specific ASIC product. This approach provides a consistent way to generate complex ASICs using IBM CoreConnect™ Bus Architecture.

Address Map Support

The NPe405L incorporates two separate address maps. The first is a fixed processor address map that serves the PowerPC family of processors. This address map defines the possible contents of various address regions which the processor can access. The second address map is for Device Configuration Registers (DCRs). The DCRs are accessed by software running on the NPe405L processor through the use of **mtdcr** and **mfdcr** commands.

System Address Map 4GB Total System Memory

Function	Subfunction	Start Address	End Address	Size
General use	SDRAM, External peripherals **Note:** Any of the address ranges listed at right may be use for any of the above functions.	0x00000000	0xE7FFFFFF	3712MB
		0xE8010000	0xE87FFFFF	8MB
		0xEC000000	0xEEBFFFFF	44MB
		0xEEE00000	0xEF3FFFFF	6MB
		0xEF500000	0xEF5FFFFF	1MB
		0xEF900000	0xFFFFFFFF	263MB
Boot-up	External peripheral bus boot [1]	0xFFE00000	0xFFFFFFFF	2MB
Internal peripherals	UART0	0xEF600300	0xEF600307	8B
	UART1	0xEF600400	0xEF600407	8B
	IIC0	0xEF600500	0xEF60051F	32B
	OPB Arbiter	0xEF600600	0xEF60063F	64B
	GPIO0 controller registers	0xEF600700	0xEF60077F	128B
	GPIO1 controller registers	0xEF600780	0xEF6007FF	128B
	Ethernet MAC 0 registers	0xEF600800	0xEF6008FF	256B
	Ethernet MAC 1 registers	0xEF600900	0xEF6009FF	256B
	ZMII control registers	0xEF600C10	0xEF600C1F	16B
	HDLCEX	0xEF610000	0xEF61FFFF	64KB

Notes:

1. When external peripheral bus boot is selected, peripheral bank 0 is automatically configured at reset to the address range listed above.
2. After the boot process, software may reassign the boot memory regions for other uses.
3. All address ranges not listed above are reserved.

DCR Address Map 4KB Device Configuration Register

Function	Start	End	Size
DCR address space[1]	0x000	0x3FF	1KW (4KB)[1]
Reserved	0x000	0x00F	16W
Memory controller registers	0x010	0x011	2W
External bus controller registers	0x012	0x013	2W
Reserved	0x014	0x07F	108W
PLB registers	0x080	0x08F	16W
Reserved	0x090	0x09F	16W
OPB bridge-out registers	0x0A0	0x0A7	8W
Reserved	0x0A8	0x0AF	8W
Clock, control and reset	0x0B0	0x0B7	8W
Power management	0x0B8	0x0BF	8W
Interrupt controller 0	0x0C0	0x0CF	16W
Interrupt controller 1	0x0D0	0x0DF	16W
Reserved	0x0E0	0x0EF	16W
Miscellaneous	0x0F0	0x0FF	16W
DMA controller registers	0x100	0x13F	64W
Reserved	0x140	0x17F	64W
MAL0 registers (Ethernet)	0x180	0x1FF	128W
MAL1 registers (HDLCEX)	0x200	0x27F	128W
Reserved	0x280	0x3FF	384W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

SDRAM Memory Controller

The NPe405L Memory Controller provides a low latency access path to SDRAM memory. The memory controller supports four logical banks. Up to 256 MB per bank are supported, for a maximum of 1 GB total. Memory access and refresh timing, address and bank sizes, and memory addressing modes are programmable.

Features include:

- 11x8 to 13x11 row-column address modes (2- and 4-bank devices supported)
- Memory bus operates at same frequency as PLB
- 32-bit memory interface support
- Programmable address range for each bank of memory
  - 4 GB address space
- Industry standard 168-pin DIMMS are supported (some configurations)
- 200 MHz NPe405H supports up to 100 MHz memory with PC100 support
- 266 MHz NPe405H supports up to 133 MHz memory with PC133 support
- 4 MB to 256 MB per bank
- Programmable timing
- Auto refresh
- Page Mode Accesses with up to 4 open pages
- Power Management (self-refresh)
- Error Checking and Correction (ECC) support
  - Standard single error correct, double error detect coverage
  - Aligned nibble error detect
  - Address error logging

External Bus Controller (EBC)

- Supports four ROM, EPROM, SRAM, Flash, and Slave Peripheral I/O banks supported
- Up to 66.66 MHz operation
- Burst and non-burst devices
- 8-, 16-bit byte-addressable data bus width support
- Latch data on Ready, Synchronous or Asynchronous
- Programmable 2K clock-cycle time-out counter with disable for Ready

- Programmable access timing per device
  - 0–255 wait states for non-bursting devices
  - 0 –31 Burst Wait States for first access and up to 7 Wait States for subsequent accesses
  - Programmable chip select assertion/negation relative to driving address bus
  - Programmable output and write-enable assertion/negation relative to assertion of chip select
- Programmable address mapping
- Peripheral device wait via “Ready”

DMA Controller

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external bus attached)
- 32-bit addressing
- Address increment or decrement
- Internal 32-byte data buffering capability
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

Serial Interface

- Two 8-pin UART interfaces provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with NS16550 register set
- Complete status reporting capability
- Transmitter and receiver are each buffered with 16-byte FIFOs when in FIFO mode
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

IIC Bus Interface

- Compliant with Phillips® Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocol
- Programmable error recovery

HDLCEX Interface

- 32-channel HDLC controller
- Two full-duplex Pulse Code Modulation (PCM) Highway ports at speeds up to 4.096 Mbps per port or 8.192 Mbps when using a single port
- Supports HDLC protocol as well as a Transparent mode
- For a single channel per port, autonomous management of I-Frames and S-Frames of the Normal Response mode (NRM) protocol on one channel per port. U-frames are handled by software.
- Supports software emulation of NRM on all channels

General Purpose IO (GPIO) Controller

- Most GPIOs are pin-shared with other functions. Configuration registers are provided to determine whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose. The GPIO function has 32 I/Os.
- Each GPIO output is separately programmable to emulate an open-drain driver (drives to zero, three-stated if output bit is 1)

Universal Interrupt Controller (UIC)

Two cascaded Universal Interrupt Controllers (UICs) provide the control, status, and communications necessary for the interrupt sources and the PowerPC processor.

Features include:

- Seven external and 29 internal interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Selectable non-critical or critical interrupt requests to the PPC405 processor core
- Programmable critical interrupt priority ordering
- Programmable critical interrupt vector generation for reduced latency interrupt handling

10/100 Mbps Ethernet MAC

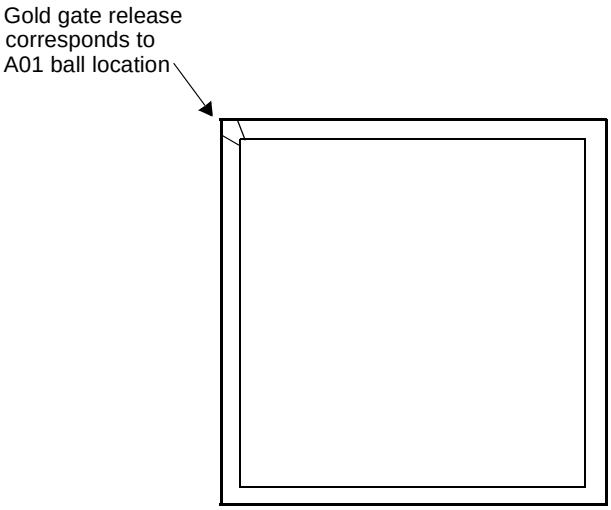
- Two units capable of full- and half-duplex, 10 Mbps or 100 Mbps operation
- Integrated ZMII Bridge supports use of MII, SMII or RMII connections to external PHYs (PHYs not included on chip)
  - Reduced Media Independent Interface (RMII) or Serial Media Independent Interface (SMII) for one to two PHY applications
  - Media Independent Interface (MII) for single or dual PHY applications
- Dedicated media access layer (MAL) provides DMA support

JTAG

- IEEE 1149.1 Test Access Port
- Debugger support
- JTAG boundary scan support (BSDL file available)

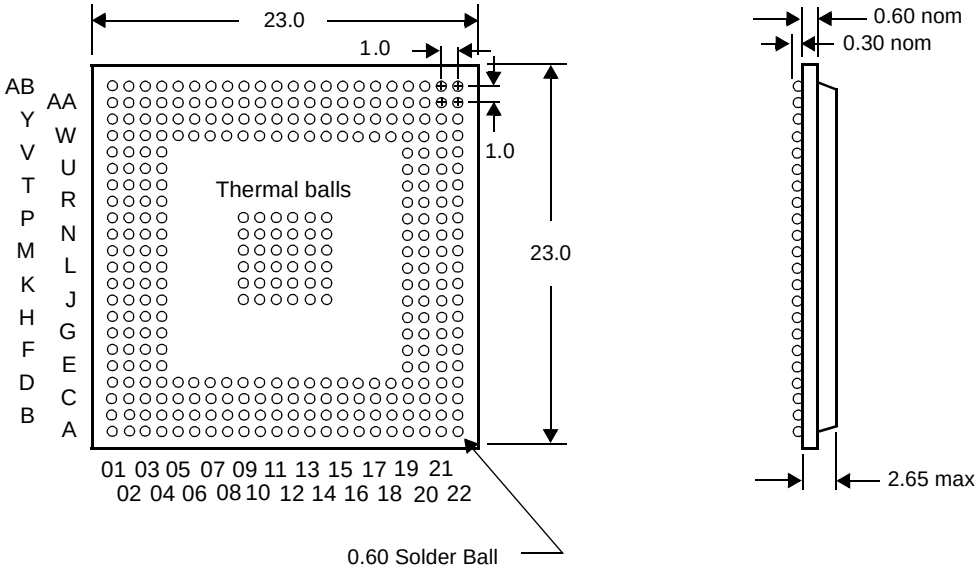
23mm, 324-Ball E-PBGA Package

Top View



Note: All dimensions are in mm.

Bottom View



Signal Lists

The following table lists all the external signals in alphabetical order and shows the ball number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal or signals in brackets. Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in "Signal Functional Description" on page 32 where the signals in the indicated interface group begin.

Signals Listed Alphabetically (Part 1 of 11)

Signal Name	Ball	Interface Group	Page
AV_{DD}	H21	Power	37
BA0	AB15	SDRAM	33
BA1	Y14		
$\overline{\text{BankSel0}}$	AA07	SDRAM	33
$\overline{\text{BankSel1}}$	Y08		
$\overline{\text{BankSel2}}$	AB06		
$\overline{\text{BankSel3}}$	AA06		
$\overline{\text{CAS}}$	AA12	SDRAM	33
ClkEn0	Y13	SDRAM	33
ClkEn1	AA13		
[$\overline{\text{DMAAck0}}$]GPIO13	U22	External Peripheral Bus	34
[$\overline{\text{DMAAck1}}$]GPIO14	U21		
[$\overline{\text{DMAAck2}}$]GPIO15	T20		
[$\overline{\text{DMAAck3}}$]GPIO16	D17		
[$\overline{\text{DMAReq0}}$]GPIO09	P19	External Peripheral Bus	34
[$\overline{\text{DMAReq1}}$]GPIO10	T22		
[[$\overline{\text{DMAReq2}}$]GPIO11	T21		
[$\overline{\text{DMAReq3}}$]GPIO12	R20		
DQM0	U03	SDRAM	33
DQM1	U01		
DQM2	R02		
DQM3	L01		
DQMCB	AA04	SDRAM	33
ECC0	AA05	SDRAM	33
ECC1	Y06		
ECC2	AB04		
ECC3	AA03		
ECC4	Y05		
ECC5	AB03		
ECC6	Y04		
ECC7	W06		
EMC0MDClk	AB16	Ethernet	32
EMC0MDIO	AA16	Ethernet	32
[EMC0Sync]EMC0TxEn[EMC0Tx0En]	AB21	Ethernet	32

Signals Listed Alphabetically (Part 2 of 11)

Signal Name	Ball	Interface Group	Page
EMC0TxD0[EMC0Tx0D0][EMC0Tx0D]	AA22	Ethernet	32
EMC0TxD1[EMC0Tx0D1][EMC0Tx1D]	U19		
EMC0TxD2[EMC0Tx1D0]	W20		
EMC0TxD3[EMC0Tx1D1]	Y22		
EMC0TxEn[EMC0Tx0En][EMC0Sync]	AB21	Ethernet	32
EMC0TxErr[EMC0Tx1En]	AB20	Ethernet	32
[EMC0Tx0En]EMC0TxEn[EMC0Sync]	AB21	Ethernet	32
[EMC0Tx1En]EMC0TxErr	AB20		
[$\overline{\text{EOT0}}$/$\overline{\text{TC0}}$]GPIO24	B19	External Peripheral Bus	34
[$\overline{\text{EOT1}}$/$\overline{\text{TC1}}$]GPIO25	B18		
[$\overline{\text{EOT2}}$/$\overline{\text{TC2}}$]GPIO26	C16		
[$\overline{\text{EOT3}}$/$\overline{\text{TC3}}$]GPIO27	B17		
GND	A01	Power **Note:** J09-J14, K09-K14, L09-L14, M09-M14, N09-N14, and P09-P14 are also thermal balls.	37
GND	A05		
GND	A09		
GND	A14		
GND	A18		
GND	A22		
GND	B02		
GND	B21		
GND	C03		
GND	C20		
GND	D04		
GND	D08		
GND	D11		
GND	D12		
GND	D15		
GND	D19		
GND	E01		
GND	E22		
GND	H04		
GND	H19		
GND	J01		
GND	J09-J14		
GND	J22		
GND	K09-K14		
GND	L04		
GND	L09-L14		
GND	L19		

Signals Listed Alphabetically (Part 3 of 11)

Signal Name	Ball	Interface Group	Page
GND	M04	Power **Note:** J09-J14, K09-K14, L09-L14, M09-M14, N09-N14, and P09-P14 are also thermal balls.	37
GND	M09-M14		
GND	M19		
GND	N09-N14		
GND	P01		
GND	P09-P14		
GND	P22		
GND	R04		
GND	R19		
GND	V01		
GND	V22		
GND	W04		
GND	W08		
GND	W11		
GND	W12		
GND	W15		
GND	W19		
GND	Y03		
GND	Y20		
GND	AA02		
GND	AA21		
GND	AB01		
GND	AB05		
GND	AB09		
GND	AB14		
GND	AB18		
GND	AB22		

Signals Listed Alphabetically (Part 4 of 11)

Signal Name	Ball	Interface Group	Page
GPIO00[TrcClk]	B20	System	37
GPIO01[TS1E]GPIO08[TS6]	C18		
GPIO02[TS2E]	A20		
GPIO03[TS1O]	N20		
GPIO04[TS2O]	N22		
GPIO05[TS3]	P21		
GPIO06[TS4]	P20		
GPIO07[TS5]	R22		
GPIO08[TS6]	R21		
GPIO09[$\overline{\text{DMAReq0}}$]	P19		
GPIO10[$\overline{\text{DMAReq1}}$]	T22		
GPIO11[$\overline{\text{DMAReq2}}$]	T21		
GPIO12[$\overline{\text{DMAReq3}}$]	R20		
GPIO13[$\overline{\text{DMAAck0}}$]	U22		
GPIO14[$\overline{\text{DMAAck1}}$]	U21		
GPIO15[$\overline{\text{DMAAck2}}$]	T20		
GPIO16[$\overline{\text{DMAAck3}}$]	D17		
GPIO17[IRQ0]	F20		
GPIO18[IRQ1]	J20		
GPIO19[IRQ2]	L21		
GPIO20[IRQ3]	M21		
GPIO21[IRQ4]	AA17		
GPIO22[IRQ5]	AB17		
GPIO23[IRQ6]	W14		
GPIO24[$\overline{\text{EOT0}}$/$\overline{\text{TC0}}$]	B19		
GPIO25[$\overline{\text{EOT1}}$/$\overline{\text{TC1}}$]	B18		
GPIO26[$\overline{\text{EOT2}}$/$\overline{\text{TC2}}$]	C16		
GPIO27[$\overline{\text{EOT3}}$/$\overline{\text{TC3}}$]	B17		
GPIO28[$\overline{\text{UART1\_DCD}}$][HDLCEXTxEnA]	AA15		
GPIO29[$\overline{\text{UART1\_RI}}$][HDLCEXTxEnB]	T01		
GPIO30	T03		
GPIO31[$\overline{\text{PerWE}}$]	A13		
$\overline{\text{Halt}}$	F22	System	37
HDLCEXRxClk	L20	HDLC 32-Channel	32
HDLCEXRxDataA	M22	HDLC 32-Channel	32
HDLCEXRxDataB	N21		
HDLCEXRxFS	M20	HDLC 32-Channel	32
HDLCEXTxClk	K20	HDLC 32-Channel	32
HDLCEXTxDataA	K21	HDLC 32-Channel	32
HDLCEXTxDataB	L22		
[HDLCEXTxEnA]GPIO28[$\overline{\text{UART1\_DCD}}$]	AA15	HDLC 32-Channel	32
[HDLCEXTxEnB]GPIO29[$\overline{\text{UART1\_RI}}$]	T01		
HDLCEXTxFS	K22	HDLC 32-Channel	32

Signals Listed Alphabetically (Part 5 of 11)

Signal Name	Ball	Interface Group	Page
IICSCL[IECSCL]	C17	Internal Peripheral	35
IICSDA[IECSDA]	A19		
[IRQ0]GPIO17	F20	Interrupts	36
[IRQ1]GPIO18	J20		
[IRQ2]GPIO19	L21		
[IRQ3[GPIO20	M21		
[IRQ4[GPIO21	AA17		
[IRQ5]GPIO22	AB17		
[IRQ6[GPIO23	W14		
MemAddr00	Y12	SDRAM **Note:** During a $\overline{CAS}$ cycle MemAddr00 is the least significant bit (lsb) on this bus.	33
MemAddr01	Y11		
MemAddr02	AB11		
MemAddr03	AA11		
MemAddr04	AA10		
MemAddr05	Y10		
MemAddr06	AB10		
MemAddr07	AA09		
MemAddr08	Y09		
MemAddr09	AB08		
MemAddr10	AA08		
MemAddr11	W09		
MemAddr12	AB07		
MemClkOut0	AA14	SDRAM	33
MemClkOut1	AB13		

Signals Listed Alphabetically (Part 6 of 11)

Signal Name	Ball	Interface Group	Page
MemData00	AB02	SDRAM **Notes:** 1. MemData00 is the most significant bit (msb). 2. MemData31 is the least significant bit (lsb)	33
MemData01	AA01		
MemData02	U04		
MemData03	W03		
MemData04	Y01		
MemData05	V03		
MemData06	Y02		
MemDatar07	W01		
MemData08	W02		
MemData09	V02		
MemData10	U02		
MemData11	R03		
MemData12	T02		
MemData13	P04		
MemData14	R01		
MemData15	P03		
MemData16	P02		
MemData17	N01		
MemData18	N03		
MemData19	N02		
MemData20	M02		
MemData21	M01		
MemData22	M03		
MemData23	L03		
MemData24	L02		
MemData25	K02		
MemData26	K03		
MemData27	K01		
MemData28	J02		
MemData29	J03		
MemData30	H01		
MemData31	H02		

Signals Listed Alphabetically (Part 7 of 11)

Signal Name	Ball	Interface Group	Page
OV_{DD}	D05	Power	37
OV_{DD}	D07		
OV_{DD}	D16		
OV_{DD}	D18		
OV_{DD}	E04		
OV_{DD}	E19		
OV_{DD}	G04		
OV_{DD}	G19		
OV_{DD}	T19		
OV_{DD}	T04		
OV_{DD}	V04		
OV_{DD}	V19		
OV_{DD}	W05		
OV_{DD}	W07		
OV_{DD}	W16		
OV_{DD}	W18		

Signals Listed Alphabetically (Part 8 of 11)

Signal Name	Ball	Interface Group	Page
PerAddr04	D06	External Peripheral Bus	34
PerAddr05	C04		
PerAddr06	A03		
PerAddr07	C05		
PerAddr08	B03		
PerAddr09	A04		
PerAddr10	C06		
PerAddr11	B04		
PerAddr12	B05		
PerAddr13	C07		
PerAddr14	B06		
PerAddr15	C08		
PerAddr16	B07		
PerAddr17	A07		
PerAddr18	D09		
PerAddr19	B08		
PerAddr20	A08		
PerAddr21	C09		
PerAddr22	B09		
PerAddr23	A10		
PerAddr24	C10		
PerAddr25	B10		
PerAddr26	B11		
PerAddr27	A11		
PerAddr28	C11		
PerAddr29	C12		
PerAddr30	A12		
PerAddr31	B12		
$\overline{\text{PerBLast}}$	C15	External Peripheral Bus	34
PerClk	A17	External Peripheral Bus	34
$\overline{\text{PerCS0}}$	B14	External Peripheral Bus	34
$\overline{\text{PerCS1}}$	C14		
$\overline{\text{PerCS2}}$	A15		
$\overline{\text{PerCS3}}$	B15		

Signals Listed Alphabetically (Part 9 of 11)

Signal Name	Ball	Interface Group	Page
PerData00	J04	External Peripheral Bus **Note:** PerData00 is the most significant bit (msb) on this bus.	34
PerData01	G01		
PerData02	G02		
PerData03	H03		
PerData04	F01		
PerData05	F02		
PerData06	G03		
PerData07	E02		
PerData08	D02		
PerData09	F03		
PerData10	D01		
PerData11	C02		
PerData12	E03		
PerData13	C01		
PerData14	D03		
PerData15	F04		
PerErr	J21	External Peripheral Bus	34
$\overline{\text{PerOE}}$	D14	External Peripheral Bus	34
PerPar0	B01	External Peripheral Bus	34
PerPar1	A02		
PerR/$\overline{\text{W}}$	A16	External Peripheral Bus	34
PerReady	B16	External Peripheral Bus	34
$\overline{\text{PerWBE0}}$	B13	External Peripheral Bus	34
$\overline{\text{PerWBE1}}$	C13		
[$\overline{\text{PerWE}}$]GPIO31	A13	External Peripheral Bus	34
PHY0Col[PHY0Rx1Er]	W17	Ethernet	32
PHY0CrS[PHY0CrS0DV]	Y18	Ethernet	32
[PHY0CrS1DV]PHY0RxDV	Y17	Ethernet	32
PHY0RxClk	AB19	Ethernet	32
[PHY0RefClk]PHY0TxClk	Y19	Ethernet	32
PHY0RxD0[PHY0Rx0D0][PHY0Rx0D]	Y15	Ethernet	32
PHY0RxD1[PHY0Rx0D1][PHY0Rx1D]	Y16		
PHY0RxD2[PHY0Rx1D0]	AA18		
PHY0RxD3[PHY0Rx1D1]	AA19		
PHY0RxDV[PHY0CrS1DV]	Y17	Ethernet	32
PHY0RxErr[PHY0Rx0Er]	AA20	Ethernet	32
[PHY0Rx0Er]PHY0RxErr	AA20	Ethernet	32
PHY0TxClk[PHY0RefClk]	Y19	Ethernet	32
$\overline{\text{RAS}}$	AB12	SDRAM	33
SysClk	G22	System	37
SysErr	C21	System	37
$\overline{\text{SysReset}}$	A21	System	37
TCK	J19	JTAG	36

Signals Listed Alphabetically (Part 10 of 11)

Signal Name	Ball	Interface Group	Page
[TC0/EOT0]GPIO24	B19	External Peripheral Bus	34
[TC1/EOT1]GPIO25	B18		
[[TC2/EOT2]GPIO26	C16		
[TC3/EOT3]GPIO27	B17		
TDI	G21	JTAG	36
TDO	F21	JTAG	36
TestEn	H20	System	37
TmrClk	D20	System	37
TMS	E21	JTAG	36
[TrcClk]GPIO00	B20	Trace	37
TRST	H22	JTAG	36
[TS1E]GPIO01	C18	Trace	37
[TS2E]GPIO02	A20		
[TS1O]GPIO03	N20	Trace	37
[TS2O]GPIO04	N22		
[TS3]GPIO05	P21	Trace	37
[TS4]GPIO06	P20		
[TS5]GPIO07	R22		
[TS6]GPIO08	R21		
UART0_CTS	B22	Internal Peripheral	35
UART0_DCD	C19		
UART0_DSR	A06		
UART0_DTR	G20		
UART0_RI	D22		
UART0_RTS	D21		
UART0_Rx	C22		
UART0_Tx	F19		
UART1_CTS	W22	Internal Peripheral	35
[UART1_DCD]GPIO28[HDLCEXTxEnA]	AA15		
UART1_DSR	W21		
UART1_DTR	U20		
[UART1_RI]GPIO29[HDLCEXTxEnB]	T01		
UART1_RTS	V21		
UART1_Rx	V20		
UART1_Tx	Y21		
UARTSerClk	E20		

Signals Listed Alphabetically (Part 11 of 11)

Signal Name	Ball	Interface Group	Page
V_{DD}	D10	Power	37
V_{DD}	D13		
V_{DD}	K19		
V_{DD}	K04		
V_{DD}	N19		
V_{DD}	N04		
V_{DD}	W10		
V_{DD}	W13		
$\overline{WE}$	Y07	SDRAM	33

Signals Listed by Ball Assignment (Part 1 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	GND	B01	PerPar0	C01	PerData13	D01	PerData10
A02	PerPar1	B02	GND	C02	PerData11	D02	PerData08
A03	PerAddr06	B03	PerAddr08	C03	GND	D03	PerData14
A04	PerAddr09	B04	PerAddr11	C04	PerAddr05	D04	GND
A05	GND	B05	PerAddr12	C05	PerAdd7	D05	OV_{DD}
A06	$\overline{\text{UART0\_DSR}}$	B06	PerAddr14	C06	PerAddr10	D06	PerAddr04
A07	PerAddr17	B07	PerAddr16	C07	PerAddr13	D07	OV_{DD}
A08	PerAddr20	B08	PerAddr19	C08	PerAddr15	D08	GND
A09	GND	B09	PerAddr22	C09	PerAddr21	D09	PerAddr18
A10	PerAddr23	B10	PerAddr25	C10	PerAddr24	D10	V_{DD}
A11	PerAddr27	B11	PerAddr26	C11	PerAddr28	D11	GND
A12	PerAddr30	B12	PerAddr31	C12	PerAddr29	D12	GND
A13	GPIO31[$\overline{\text{PerWE}}$]	B13	$\overline{\text{PerWBE0}}$	C13	$\overline{\text{PerWBE1}}$	D13	V_{DD}
A14	GND	B14	$\overline{\text{PerCS0}}$	C14	$\overline{\text{PerCS1}}$	D14	$\overline{\text{PerOE}}$
A15	$\overline{\text{PerCS2}}$	B15	$\overline{\text{PerCS3}}$	C15	$\overline{\text{PerBLast}}$	D15	GND
A16	PerR/$\overline{\text{W}}$	B16	PerReady	C16	GPIO26[$\overline{\text{EOT2}}$/$\overline{\text{TC2}}$]	D16	OV_{DD}
A17	PerClk	B17	GPIO27[$\overline{\text{EOT3}}$/$\overline{\text{TC3}}$]	C17	IICSCL[IECSCL]	D17	GPIO16[$\overline{\text{DMAAck3}}$]
A18	GND	B18	GPIO25[$\overline{\text{EOT1}}$/$\overline{\text{TC1}}$]	C18	GPIO01[TS1E]	D18	OV_{DD}
A19	IICSDA[IECSDA]	B19	GPIO24[$\overline{\text{EOT0}}$/$\overline{\text{TC0}}$]	C19	$\overline{\text{UART0\_DCD}}$	D19	GND
A20	GPIO02[TS2E]	B20	GPIO00[TrcClk]	C20	GND	D20	TmrClk
A21	$\overline{\text{SysReset}}$	B21	GND	C21	SysErr	D21	$\overline{\text{UART0\_RTS}}$
A22	GND	B22	$\overline{\text{UART0\_CTS}}$	C22	UART0_Rx	D22	$\overline{\text{UART0\_RI}}$

Signals Listed by Ball Assignment (Part 2 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	GND	F01	PerData04	G01	PerData01	H01	MemData30
E02	PerData07	F02	PerData05	G02	PerData02	H02	MemData31
E03	PerData12	F03	PerData09	G03	PerData06	H03	PerData03
E04	OV_{DD}	F04	PerData15	G04	OV_{DD}	H04	GND
E05	No ball	F05	No ball	G05	No ball	H05	No ball
E06	No ball	F06	No ball	G06	No ball	H06	No ball
E07	No ball	F07	No ball	G07	No ball	H07	No ball
E08	No ball	F08	No ball	G08	No ball	H08	No ball
E09	No ball	F09	No ball	G09	No ball	H09	No ball
E10	No ball	F10	No ball	G10	No ball	H10	No ball
E11	No ball	F11	No ball	G11	No ball	H11	No ball
E12	No ball	F12	No ball	G12	No ball	H12	No ball
E13	No ball	F13	No ball	G13	No ball	H13	No ball
E14	No ball	F14	No ball	G14	No ball	H14	No ball
E15	No ball	F15	No ball	G15	No ball	H15	No ball
E16	No ball	F16	No ball	G16	No ball	H16	No ball
E17	No ball	F17	No ball	G17	No ball	H17	No ball
E18	No ball	F18	No ball	G18	No ball	H18	No ball
E19	OV_{DD}	F19	UART0_Tx	G19	OV_{DD}	H19	GND
E20	UARTSerClk	F20	GPIO17[IRQ0]	G20	$\overline{\text{UART0\_DTR}}$	H20	TestEn
E21	TMS	F21	TDO	G21	TDI	H21	AV_{DD}
E22	GND	F22	$\overline{\text{Halt}}$	G22	SysClk	H22	$\overline{\text{TRST}}$

Signals Listed by Ball Assignment (Part 3 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	GND	K01	MemData27	L01	DQM3	M01	MemData21
J02	MemData28	K02	MemData25	L02	MemData24	M02	MemData20
J03	MemData29	K03	MemData26	L03	MemData23	M03	MemData22
J04	PerData00	K04	V_{DD}	L04	GND	M04	GND
J05	No ball	K05	No ball	L05	No ball	M05	No ball
J06	No ball	K06	No ball	L06	No ball	M06	No ball
J07	No ball	K07	No ball	L07	No ball	M07	No ball
J08	No ball	K08	No ball	L08	No ball	M08	No ball
J09	GND	K09	GND	L09	GND	M09	GND
J10	GND	K10	GND	L10	GND	M10	GND
J11	GND	K11	GND	L11	GND	M11	GND
J12	GND	K12	GND	L12	GND	M12	GND
J13	GND	K13	GND	L13	GND	M13	GND
J14	GND	K14	GND	L14	GND	M14	GND
J15	No ball	K15	No ball	L15	No ball	M15	No ball
J16	No ball	K16	No ball	L16	No ball	M16	No ball
J17	No ball	K17	No ball	L17	No ball	M17	No ball
J18	No ball	K18	No ball	L18	No ball	M18	No ball
J19	TCK	K19	V_{DD}	L19	GND	M19	GND
J20	GPIO18[IRQ1]	K20	HDLCEXTxClk	L20	HDLCEXRxClk	M20	HDLCEXRxFS
J21	PerErr	K21	HDLCEXTxDataA	L21	GPIO19[IRQ2]	M21	GPIO20[IRQ3]
J22	GND	K22	HDLCEXTxFS	L22	HDLCEXTxDataB	M22	HDLCEXRxDataA

Signals Listed by Ball Assignment (Part 4 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	MemData17	P01	GND	R01	MemData14	T01	GPIO29[$\overline{\text{UART1\_RI}}$] [HDLCEXTxEnB]
N02	MemData19	P02	MemData16	R02	DQM2	T02	MemData12
N03	MemData18	P03	MemData15	R03	MemData11	T03	GPIO30
N04	V_{DD}	P04	MemData13	R04	GND	T04	OV_{DD}
N05	No ball	P05	No ball	R05	No ball	T05	No ball
N06	No ball	P06	No ball	R06	No ball	T06	No ball
N07	No ball	P07	No ball	R07	No ball	T07	No ball
N08	No ball	P08	No ball	R08	No ball	T08	No ball
N09	GND	P09	GND	R09	No ball	T09	No ball
N10	GND	P10	GND	R10	No ball	T10	No ball
N11	GND	P11	GND	R11	No ball	T11	No ball
N12	GND	P12	GND	R12	No ball	T12	No ball
N13	GND	P13	GND	R13	No ball	T13	No ball
N14	GND	P14	GND	R14	No ball	T14	No ball
N15	No ball	P15	No ball	R15	No ball	T15	No ball
N16	No ball	P16	No ball	R16	No ball	T16	No ball
N17	No ball	P17	No ball	R17	No ball	T17	No ball
N18	No ball	P18	No ball	R18	No ball	T18	No ball
N19	V_{DD}	P19	GPIO09[$\overline{\text{DMAReq0}}$]	R19	GND	T19	OV_{DD}
N20	GPIO3[TS1O]	P20	GPIO06[TS4]	R20	GPIO12[$\overline{\text{DMAReq3}}$]	T20	GPIO15[$\overline{\text{DMAAck2}}$]
N21	HDLCEXRxDataB	P21	GPIO05[TS3]	R21	GPIO08[TS6]	T21	GPIO11[$\overline{\text{DMAReq2}}$]
N22	GPIO4[TS2O]	P22	GND	R22	GPIO07[TS5]	T22	GPIO10[$\overline{\text{DMAReq1}}$]

Signals Listed by Ball Assignment (Part 5 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	DQM1	V01	GND	W01	MemData07	Y01	MemData04
U02	MemData10	V02	MemData09	W02	MemData08	Y02	MemData06
U03	DQM0	V03	MemData05	W03	MemData03	Y03	GND
U04	MemData02	V04	OV_{DD}	W04	GND	Y04	ECC6
U05	No ball	V05	No ball	W05	OV_{DD}	Y05	ECC4
U06	No ball	V06	No ball	W06	ECC7	Y06	ECC1
U07	No ball	V07	No ball	W07	OV_{DD}	Y07	$\overline{WE}$
U08	No ball	V08	No ball	W08	GND	Y08	$\overline{BankSel1}$
U09	No ball	V09	No ball	W09	MemAddr11	Y09	MemAddr08
U10	No ball	V10	No ball	W10	V_{DD}	Y10	MemAddr05
U11	No ball	V11	No ball	W11	GND	Y11	MemAddr01
U12	No ball	V12	No ball	W12	GND	Y12	MemAddr00
U13	No ball	V13	No ball	W13	V_{DD}	Y13	ClkEn0
U14	No ball	V14	No ball	W14	GPIO23[IRQ6]	Y14	BA1
U15	No ball	V15	No ball	W15	GND	Y15	PHY0RxD0 [PHY0Rx0D0] [PHY0Rx0D]
U16	No ball	V16	No ball	W16	OV_{DD}	Y16	PHYRxD1 [PHY0Rx0D1] [PHY0Rx1D]
U17	No ball	V17	No ball	W17	PHY0Col[PHY0Rx1Er]	Y17	PHY0RxDV [PHY0CrS1DV]
U18	No ball	V18	No ball	W18	OV_{DD}	Y18	PHY0CrS [PHY0CrS0DV]
U19	EMC0TxD1 [EMC0Tx0D1] [EMC0Tx1D]	V19	OV_{DD}	W19	GND	Y19	PHY0TxClk [PHY0RefClk]
U20	$\overline{UART1\_DTR}$	V20	UART1_Rx	W20	EMC0TxD2 [EMC0Tx1D0]	Y20	GND
U21	GPIO14[$\overline{DMAAck1}$]	V21	$\overline{UART1\_RTS}$	W21	$\overline{UART1\_DSR}$	Y21	UART1_Tx
U22	GPIO13[$\overline{DMAAck0}$]	V22	GND	W22	$\overline{UART1\_CTS}$	Y22	EMC0TxD3 [EMC0Tx1D1]

Signals Listed by Ball Assignment (Part 6 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	MemData01	AB01	GND				
AA02	GND	AB02	MemData00				
AA03	ECC3	AB03	ECC5				
AA04	DQMCB	AB04	ECC2				
AA05	ECC0	AB05	GND				
AA06	$\overline{\text{BankSel3}}$	AB06	$\overline{\text{BankSel2}}$				
AA07	$\overline{\text{BankSel0}}$	AB07	MemAddr12				
AA08	MemAddr10	AB08	MemAddr09				
AA09	MemAddr07	AB09	GND				
AA10	MemAddr04	AB10	MemAddr06				
AA11	MemAddr03	AB11	MemAddr02				
AA12	$\overline{\text{CAS}}$	AB12	$\overline{\text{RAS}}$				
AA13	ClkEn1	AB13	MemClkOut1				
AA14	MemClkOut0	AB14	GND				
AA15	GPIO28[$\overline{\text{UART1\_DCD}}$] [HDLCEXTxEnA]	AB15	BA0				
AA16	EMC0MDIO	AB16	EMC0MDClk				
AA17	GPIO21[IRQ4]	AB17	GPIO22[IRQ5]				
AA18	PHY0RxD2 [PHY0Rx1D0]	AB18	GND				
AA19	PHY0RxD3 [PHY0Rx1D1]	AB19	PHY0RxClk				
AA20	PHY0RxErr [PHY0Rx0Er]	AB20	EMC0TxErr [EMC0Tx1En]				
AA21	GND	AB21	EMC0TxEn [EMC0Tx0En] [EMC0Sync]				
AA22	EMC0TxD0 [EMC0Tx0D0] [EMC0Tx0D]	AB22	GND				

Signal Description

The following table provides a summary of the number of package pins (balls) associated with each functional interface group.

Pin Summary

Group	No. of Pins
Nonmultiplexed Signals	167
Multiplexed Signals	48
Total Signal Pins	**215**
AV_{DD}	1
OV_{DD}	16
V_{DD}	8
Gnd	48
Gnd (and thermal)	36
Reserved	0
Total Pins	**324**

Multiplexed pins

In the table “Signal Functional Description” on page 32, each external signal is listed along with a short description of the signal function. The signals are grouped together according to their function. Some signals are multiplexed on the same package pin (ball) so that the pin can be used for different functions. In most cases, the signal name is shown in this table unaccompanied by multiplexed signal names that may be associated with it. In cases where multiplexed signals are in the same functional group, the names appear as a default signal followed by secondary signals in square brackets (for example, EMC0TxErr[EMC0Tx1En]). Active-low signals (for example, $\overline{\text{RAS}}$) are marked with an overline. Any signal that is not the primary (default) signal on a multiplexed pin is shown in square brackets.

The active signal on a multiplexed pin is controlled by programming. It is expected that in any single application, a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

Initialization Strapping

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Initialization” on page 51). Note that the use of these pins for strapping is not considered multiplexing since the strapping function is not programmable.

Pull-up and Pull-down Resistors

Pull-up and pull-down resistors are used for strapping during reset and to retain unused or undriven inputs in an appropriate state. The recommended pull-up value of 3kΩ to +3.3V (10kΩ to +5V can be used on 5V tolerant I/Os) and pull-down value of 1kΩ to GND, applies only to individually terminated signals. To prevent possible damage to the device, I/Os capable of becoming outputs *must never* be tied together and terminated through a common resistor.

If your system-level test methodology permits, input-only signals can be connected together and terminated through either a common resistor or directly to +3.3V or GND. When a resistor is used, its value must ensure

that the grouped I/Os reach a valid logic zero or logic one state when accounting for the total input current into the NPe405L.

Unused I/Os

Strapping of some pins may be necessary when they are unused. Although the NPe405L requires only the pull-up and pull-down terminations as specified in the “Signal Functional Description” on page 32, good design practice is to terminate all unused inputs or to configure I/Os such that they always drive. If unused, the peripheral and SDRAM bus should be configured and terminated as follows:

- Peripheral interface—PerAddr00:31, PerData00:31, and all of the control signals are driven by default. Terminate PerReady high and PerError low.
- SDRAM—Program SDRAM0_CFG[EMDULR]=1 and SDRAM0_CFG[DCE]=1. This causes the NPe405L to actively drive all of the SDRAM address, data, and control signals.

External Peripheral Bus Control Signals

All external peripheral bus control signals ($\overline{\text{PerCS0:3}}$, PerR/$\overline{\text{W}}$, $\overline{\text{PerWBE0:1}}$, $\overline{\text{PerOE}}$, $\overline{\text{PerWE}}$, $\overline{\text{PerBLast}}$) are set to the high-impedance state when $\overline{\text{ExtReset}}$=0. In addition, as detailed in the *PowerNP NPe405L Embedded Processor User’s Manual*, the peripheral bus controller can be programmed via EBC0_CFG to float some of these control signals between transactions. As a result, a pull-up resistor should be added to those control signals where an undriven state may affect any devices receiving that particular signal.

The following table lists all of the I/O signals provided by the NPe405L. Please see “Signals Listed Alphabetically” on page 13 for the pin number to which each signal is assigned. In cases where a multiplexed signal (indicated by the square brackets) is shown without the other signals that are assigned to that pin, you can see what the other signals are by referring to the same table.

Signal Functional Description (Part 1 of 6)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 31.

Signal Name	Description	I/O	Type	Notes
HDLCEX Interface				
HDLCEXTxClk	Transmit Clock	I	3.3V LVTTL	
HDLCEXTxFS	Transmit Frame Synchronization	I	3.3V LVTTL	
HDLCEXTxDataA	Transmit Data port A	O	3.3V LVTTL	
HDLCEXTxDataB	Transmit Data port B	O	3.3V LVTTL	
HDLCEXRxClk	Receive Clock	I	3.3V LVTTL	
HDLCEXRxFS	Receive Frame Synchronization	I	3.3V LVTTL	
HDLCEXRxDataA	Receive Data port A	I	3.3V LVTTL	
HDLCEXRxDataB	Receive Data port B	I	3.3V LVTTL	
[HDLCEXTxEnA]	Transmit Enable port A	O	5V tolerant 3.3V LVTTL	
[HDLCEXTxEnB]	Transmit Enable port B	O	5V tolerant 3.3V LVTTL	
Ethernet Interface				
EMC0MDClk	Management Data Clock. The MDClk is sourced to the PHY. Management information is transferred synchronously with respect to this clock (MII, RMII, and SMII).	O	3.3V LVTTL	
EMC0MDIO	Management Data Input/Output is a bidirectional signal between the Ethernet controller and the PHY. It is used to transfer control and status information (MII, RMII, and SMII).	I/O	5V tolerant 3.3V LVTTL	1, 4
EMC0TxD0[EMC0Tx0D0][EMC0Tx0D] EMC0TxD1[EMC0Tx0D1][EMC0Tx1D] EMC0TxD2[EMC0Tx1D0] EMC0TxD3[EMC0Tx1D1]	Transmit Data. A nibble wide data bus towards the net. The data is synchronous with PHY0TxClk (MII 0[RMII 0, 1][SMII 0, 1]).	O	3.3V LVTTL	
EMC0TxEn[EMC0Tx0En][EMC0Sync]	Transmit Enable. This signal is driven by EMAC2 to the PHY. Data is valid during the active state of this signal. Deassertion of this signal indicates end of frame transmission. This signal is synchronous with PHYTxClk (MII 0[RMII 0]). or SMII Sync.	O	3.3V LVTTL	
EMC0TxErr[EMC0Tx1En]	Transmit Error. This signal is generated by the Ethernet controller, is connected to the PHY and is synchronous with the PHY0TxClk. It informs the PHY that an error was detected (MII 0). or Transmit Enable [RMII 1].	O	3.3V LVTTL	

Signal Functional Description (Part 2 of 6)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 31.

Signal Name	Description	I/O	Type	Notes
PHY0Col[PHY0Rx1Er]l	Collision [receive error] signal from the PHY. This is an asynchronous signal (MII 0). or Receive Error ([RMII 1]).	I	5V tolerant 3.3V LVTTL	
PHY0CrS[PHY0CrS0DV]	Carrier Sense signal from the PHY. This is an asynchronous signal (MII 0). or Carrier sense data valid ([RMII 0]).	I	5V tolerant 3.3V LVTTL	1, 5
PHY0RxClk	Receiver medium clock. This signal is generated by the PHY (MII 0).	I	5V tolerant 3.3V LVTTL	1, 4
PHY0RxD0[PHY0Rx0D0][PHY0Rx0D] PHY0RxD1[PHY0Rx0D1][PHY0Rx1D] PHY0RxD2[PHY0Rx1D0] PHY0RxD3[PHY0Rx1D1]	Received Data. This is a nibble wide bus from the PHY. The data is synchronous with PHY0RxClk (MII 0[RMII 0, 1][SMII 0, 1]).	I	5V tolerant 3.3V LVTTL	1, 4
PHY0RxDV[PHY0CrS1DV]	Receive Data Valid. Data on the Data Bus is valid when this signal is activated. Deassertion of this signal indicates end of the frame reception (MII 0). or Carrier sense data valid ([RMII 1])	I	5V tolerant 3.3V LVTTL	1, 5
PHY0RxErr[PHY0Rx0Er]	Receive Error. This signal comes from the PHY and is synchronous with PHY0RxClk (MII 0 [RMII 0]).	I	5V tolerant 3.3V LVTTL	1, 5
PHY0TxClk[PHY0RefClk]	Transmit medium clock. This signal is generated the PHY ([MII 0]). or Reference Clock [RMII and SMII].	I	5V tolerant 3.3V LVTTL	1, 4
SDRAM Interface				
MemAddr00:31	Memory Data bus **Notes:** 1. MemAddr00 is the most significant bit (msb). 2. MemData31 is the least significant bit (lsb).	I/O	3.3V LVTTL	
MemAddr12:00	Memory Address bus. **Notes:** 1. MemAddr12 is the most significant bit (msb). 2. MemAddr00 is the least significant bit (lsb).	O	3.3V LVTTL	
BA1:0	Bank Address supporting up to 4 internal banks	O	3.3V LVTTL	
$\overline{RAS}$	Row Address Strobe.	O	3.3V LVTTL	
$\overline{CAS}$	Column Address Strobe.	O	3.3V LVTTL	
DQM0:3	DQM for byte lane 0 (MemAddr00:7), 1 (MemAddr08:15), 2 (MemData16:23), and 3 (MemData24:31)	O	3.3V LVTTL	
DQMCB	DQM for ECC check bits.	O	3.3V LVTTL	

Signal Functional Description (Part 3 of 6)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 31.

Signal Name	Description	I/O	Type	Notes
ECC0:7	ECC check bits 0:7.	I/O	3.3V LVTTL	
$\overline{\text{BankSel0:3}}$	Select up to four external SDRAM banks.	O	3.3V LVTTL	
$\overline{\text{WE}}$	Write Enable.	O	3.3V LVTTL	
ClkEn0:1	SDRAM Clock Enable.	O	3.3V LVTTL	
MemClkOut0:1	Two copies of an SDRAM clock allows, in some cases, glueless SDRAM attachment without requiring this signal to be repowered by a PLL or zero-delay buffer.	O	3.3V LVTTL	
External Peripheral Bus Interface				
PerData00:15	External peripheral data bus . **Note:** PerData00 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
PerAddr04:31	External peripheral address bus .	O	5V tolerant 3.3V LVTTL	
PerPar0:1	External peripheral byte parity signals.	I/O	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerWBE0:1}}$	Peripheral write-bte enable. Byte-enables which are valid for an entire cycle or write-byte-enables which are valid for each byte on each data transfer, allowing partial word transactions. Used by either external bus controller or DMA controller depending upon the type of transfer involved.	O	5V tolerant 3.3V LVTTL	2, 7
[$\overline{\text{PerWE}}$]	Peripheral write enable. Low when any of the two $\overline{\text{PerWBE}}$ signals are low.	I/O	5V tolerant 3.3V LVTTL	7
$\overline{\text{PerCS0:3}}$	Peripheral Chip Selects	O	5V tolerant 3.3V LVTTL	
$\overline{\text{PerOE}}$	Peripheral output enable. Used by either the external bus controller or the DMA controller depending upon the type of transfer involved. When the NPe405L is the bus master, it enables the peripherals to drive the bus.	O	5V tolerant 3.3V LVTTL	7
PerR/$\overline{\text{W}}$	Peripheral read/write. Used by either the external bus controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory.	O	5V tolerant 3.3V LVTTL	
PerReady	Indicates peripheral is ready to transfer data.	I	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerBLast}}$	Peripheral burst last. Used to indicate the last transfer of a memory access.	O	5V tolerant 3.3V LVTTL	7
PerClk	Peripheral Clock. Used by synchronous peripherals.	O	5V tolerant 3.3V LVTTL	
PerErr	Used to indicate errors from peripherals.	I	5V tolerant 3.3V LVTTL	1, 5

Signal Functional Description (Part 4 of 6)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 31.

Signal Name	Description	I/O	Type	Notes
[$\overline{\text{DMAReq0:3}}$]	DMA request. Used by peripherals to request a data transfer. Following a system reset, the default mode of the signals is active-low. They may be programmed to active-high using the DMA0_POL register.	I	5V tolerant 3.3V LVTTL	1
[$\overline{\text{DMAAck0:3}}$]	DMA acknowledge. Used to indicate to peripherals that data transfer is complete. Following a system reset, the default mode of the signals is active-low. They may be programmed to active-high using the DMA0_POL register.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{EOT0:3}}$/$\overline{\text{TC0:3}}$]	End Of Transfer/Terminal Count. Indication by peripherals that all data has been transfered, or by DMA controller that programmed amount of data has been transfered. Following a system reset, the default mode of the signals is active-low. They may be programmed to active-high using the DMA0_POL register.	I/O	5V tolerant 3.3V LVTTL	1
Internal Peripheral Interface				
UARTSerClk	Serial Clock used to provide an alternative clock to the internally generated serial clock. Used in cases where the allowable internally generated baud rates are not satisfactory. This input can be individually connected to either or both UART0 and UART1.	I	5V tolerant 3.3V LVTTL	1
UART0_Rx	UART0 Receive data.	I	5V tolerant 3.3V LVTTL	1
UART0_Tx	UART0 Transmit data.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART0\_DCD}}$]	UART0 Data Carrier Detect.	I	5V tolerant 3.3V LVTTL	1
[$\overline{\text{UART0\_DSR}}$]	UART0 Data Set Ready.	I	5V tolerant 3.3V LVTTL	1
[$\overline{\text{UART0\_CTS}}$]	UART0 Clear To Send.	I	5V tolerant 3.3V LVTTL	1
[$\overline{\text{UART0\_DTR}}$]	UART0 Data Terminal Ready.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART0\_RTS}}$]	UART0 Request To Send.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART0\_RI}}$]	UART0 Ring Indicator.	I	5V tolerant 3.3V LVTTL r	1

Signal Functional Description (Part 5 of 6)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 31.

Signal Name	Description	I/O	Type	Notes
UART1_Rx	UART1 Receive data.	I	5V tolerant 3.3V LVTTL	1
UART1_Tx	UART1 Transmit data.	O	5V tolerant 3.3V LVTTL	6
[$\overline{\text{UART1\_DCD}}$]	UART1 Data Carrier Detect.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART1\_DSR}}$]	UART1 Data Set Ready.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART1\_CTS}}$]	UART1 Clear To Send.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART1\_DTR}}$]	UART1 Data Terminal Ready.	O	5V tolerant 3.3V LVTTL	6
[$\overline{\text{UART1\_RTS}}$]	UART1 Request To Send.	O	5V tolerant 3.3V LVTTL	6
[$\overline{\text{UART1\_RI}}$]	UART1 Ring Indicator.	I	5V tolerant 3.3V LVTTL	1, 4
IICSCL	IIC Serial Clock.	I/O	5V tolerant 3.3V LVTTL	1, 2
IICSDA	IIC Serial Data.	I/O	5V tolerant 3.3V LVTTL	1, 2
Interrupts Interface				
[IRQ0:6]	Interrupt Requests.	I	5V tolerant 3.3V LVTTL	1
JTAG Interface				
TDI	Test Data In.	I	5V tolerant 3.3V LVTTL	1, 4
TMS	Test Mode Select.	I	5V tolerant 3.3V LVTTL	1, 4
TDO	Test Data Out.	O	5V tolerant 3.3V LVTTL	
TCK	Test Clock.	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{TRST}}$	Test Reset. $\overline{\text{TRST}}$ must be low at power-on to reset the JTAG boundary scan state machine.	I	5V tolerant 3.3V LVTTL	5

Signal Functional Description (Part 6 of 6)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 30 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 31.

Signal Name	Description	I/O	Type	Notes
System Interface				
SysClk	Main System Clock input.	I	3.3V Analog Wire w/ESD	
$\overline{\text{SysReset}}$	Main System Reset.	I/O	5V tolerant 3.3V LVTTL	1, 2
SysErr	Set to 1 when a Machine Check is generated.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{Halt}}$	Halt from external debugger.	I	5V tolerant 3.3V LVTTL	1
GPIO00:31	General Purpose I/O. To access this function, software must toggle a DCR bit.	I/O	5V tolerant 3.3V LVTTL	1
TestEn	Test Enable. Used only for manufacturing tests. Pull down for normal operation.	I	3.3V LVTTL Rcvr w/PD	
TmrClk	This input must toggle at a rate of less than one half the CPU core frequency (less than 100MHz in most cases). In most cases this input toggles much slower (in the 1MHz to 10MHz range).	I	5V tolerant 3.3V LVTTL	1
Trace Interface				
[TS1E] [TS2E]	Even Trace execution status.To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
[TS1O] [TS2O]	Odd Trace execution status. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
[TS3:6]	Trace Status. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
[TrcClk]	Trace interface clock. A toggling signal that is always half of the CPU core frequency. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	1
Power Pins				
GND	Ground **Note:** J09-J14, K09-K14, L09-L14, M09-M14, N09-N14, and P09-P14 are also thermal balls.	I	Hardwire	
V_{DD}	Logic voltage—2.5V	I	Hardwire	
OV_{DD}	Output driver voltage—3.3V	I	Hardwire	
AV_{DD}	Filtered PLL voltage—2.5V	I	3.3V DC Wire w/ESD	
Other Pins				
Reserved	Do not connect signals, voltage, or ground to these pins.	n/a	n/a	

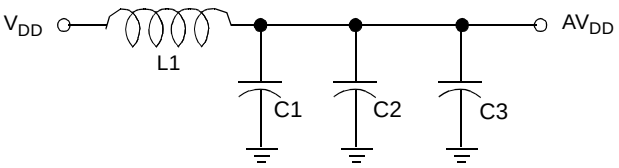
Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Characteristic	Symbol	Value	Unit
Supply Voltage (Internal Logic)	V_{DD}	0 to +2.7	V
Supply Voltage (I/O Interface)	OV_{DD}	0 to +3.6	V
PLL Supply Voltage [2]	AV_{DD}	0 to +2.7	V
Input Voltage (3.3V LVTTL receivers)	V_{IN}	-0.6 to (OV_{DD} + 0.6)	V
Input Voltage (5.0V LVTTL receivers)	V_{IN}	-0.6 to (OV_{DD} + 2.4)	V
Storage Temperature Range	T_{STG}	-55 to +150	°C
Case temperature under bias	T_C	-40 to +120	°C

Notes:

1. All voltages are specified with respect to ground (GND).
2. AV_{DD} should be derived from V_{DD} using the following circuit:



L1 – 2.2µH SMT inductor (equivalent to MuRata LQH3C2R2M34) or SMT chip ferrite bead (equivalent to MuRata BLM31A700S)

C1 – 3.3 µF SMT tantalum

C2 – 0.1µF SMT monolithic ceramic capacitor with X7R dielectric or equivalent

C3 – 0.01µF SMT monolithic ceramic capacitor with X7R dielectric or equivalent

Package Thermal Specifications

The NPe405L is designed to operate within a case temperature range of -40°C to 85°C. Thermal resistance values for the E-PBGA packages in a convection environment are as follows:

Package—Thermal Resistance	Symbol	Airflow ft/min (m/sec)			Unit
		0 (0)	100 (0.51)	200 (1.02)	
23mm, 324-balls—Junction-to-Case	θ_{JC}	2	2	2	°C/W
23mm, 324-balls—Case-to-Ambient[1]	θ_{CA}	17	15	14	°C/W

Notes:

1. For a chip mounted on a JEDEC 2S2P card without a heat sink.
2. For a chip mounted on a card with at least one signal and two power planes, the following relationships exist:
   a. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
   b. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
   c. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.

Recommended DC Operating Conditions

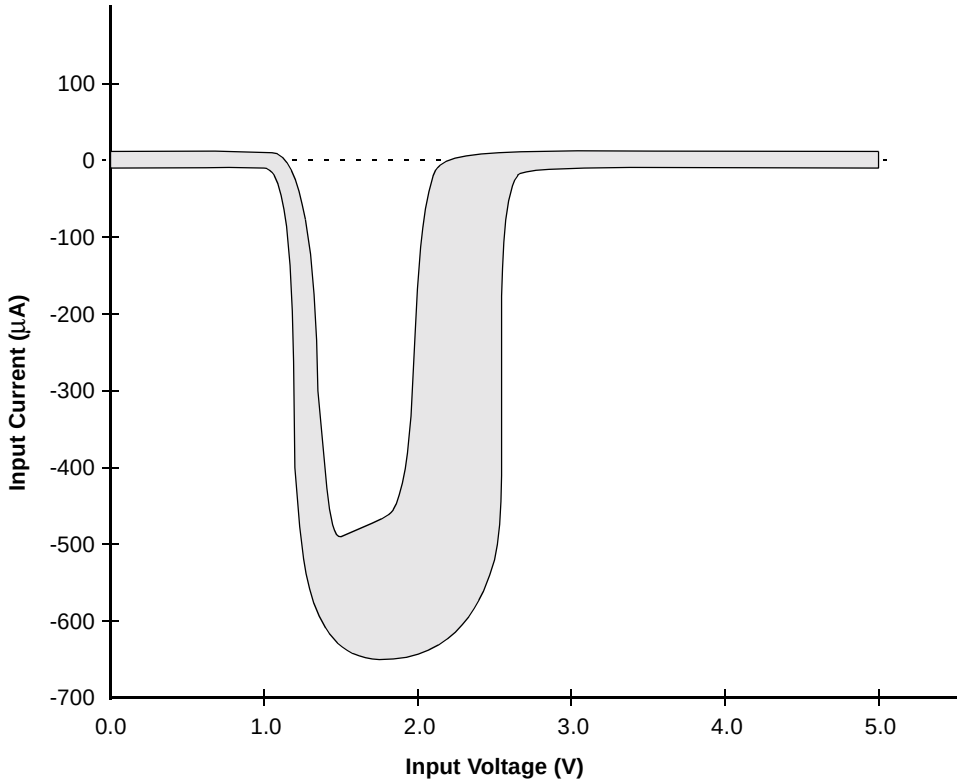
Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	+2.3	+2.5	+2.7	V	
I/O Supply Voltage	OV_{DD}	+3.0	+3.3	+3.6	V	
PLL Supply Voltage	AV_{DD}	+2.3	+2.5	+2.7	V	
Input Logic High (3.3V LVTTL receivers)	V_{IH}	+2.0		OV_{DD}	V	
Input Logic High (2.5V CMOS receivers)	V_{IH}	+1.7		V_{DD}	V	
Input Logic High (5.0V LVTTL receivers)	V_{IH}	+2.0		+5.5	V	
Input Logic Low	V_{IL}	0		+0.8	V	
Output Logic High	V_{OH}	+2.4		OV_{DD}	V	
Output Logic Low	V_{OL}	0		+0.4	V	
3.3V I/O input current (no pull-up or pull-down)	I_{IL1}			±10	µA	
Input Current (with internal pull-down)	I_{IL2}	±10 (@ 0V)		400 (@ 3.6V)	µA	
Input Current (with internal pull-up)	I_{IL3}	-250 (@ 0V)		±10 (@ 3.6V)	µA	
Input Max Allowable Overshoot (2.5V CMOS receivers)	V_{IMAO25}			V_{DD} + 0.6	V	
Input Max Allowable Overshoot (3.3V LVTTL receivers)	V_{IMAO3}			OV_{DD} + 0.6	V	
Input Max Allowable Overshoot (5.0V LVTTL receivers)	V_{IMAO5}			+5.5	V	
Input Max Allowable Undershoot (3.3V or 5.0V receivers)	V_{IMAU}	– 0.6			V	
Output Max Allowable Overshoot (3.3V or 5.0V receivers)	V_{OMAO}			OV_{DD} + 0.3	V	
Output Max Allowable Undershoot (3.3V and 5.0V receivers)	V_{OMAU3}	– 0.6			V	
Case Temperature	T_C	– 40		+85	°C	

Notes:

1. See “5V-Tolerant I/O Input Current” on page 40

5V-Tolerant I/O Input Current



Input Capacitance

Parameter	Symbol	Maximum	Unit	Notes
3.3V LVTTL I/O)	C_{IN1}	2.5	pF	
5V tolerant LVTTL I/O	C_{IN2}	3.5	pF	
RX only pins	C_{IN4}	0.75	pF	

DC Electrical Characteristics

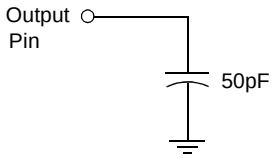
Parameter	Symbol	Minimum	Typical	Maximum	Unit
Active Operating Current for V_{DD} @ 133MHz	I_{DD}	444	497	543	mA
Active Operating Current for V_{DD} @ 200MHz	I_{DD}	468	565	676	mA
Active Operating Current for V_{DD} @ 266MHz	I_{DD}	490	590	700	mA
Active Operating Current for OV_{DD} @ 133MHz	I_{ODD}	17	23	36	mA
Active Operating Current for OV_{DD} @ 200MHz	I_{ODD}	24	36	51	mA
Active Operating Current for OV_{DD} @ 266MHz	I_{ODD}	27	44	61	mA
Active Operating Current for AV_{DD}	I_{ADD}	5.5	6	6.5	mA
Active Operating Power @ 133MHz	P_{DD}	1.1	1.3	1.6[1]	W
Active Operating Power @ 200MHz	P_{DD}	1.4	1.7	2[1]	W
Active Operating Power @ 266MHz	P_{DD}	1.5	1.8	2.1[1]	W

Notes:

1. Maximum power is characterized at V_{DD}=2.7V, OV_{DD}=3.6V, T_C=85°C, across the silicon process (worse case to best case), while running an application designed to maximize power consumption. The maximum power values are measured with the following clock rate combinations:
   a. CPU=133.33MHz, PLB=66.66MHz, OPB=66.66MHz, EBC=33.33MHz
   b. CPU=200 MHz, PLB=100MHz, OPB=50MHz, EBC=50MHz
   c. CPU=266.66MHz, PLB=66.66MHz, OPB=66.66MHz, EBC=33.33MHz

Test Conditions

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized at OV_{DD} = 3.00V and T_J = 85°C with the 50pF test load shown in the figure at right.

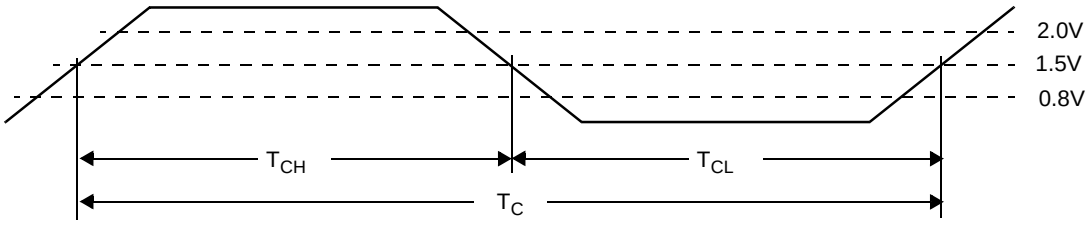


Clocking Specifications

Symbol	Parameter	Min	Max	Units
SysClk Input				
F_C	SysClk clock input frequency	25	66.66	MHz
T_C	SysClk clock period	15	40	ns
T_{CS}	Clock edge stability (phase jitter, cycle to cycle)		0.15	ns
T_{CH}	Clock input high time	40% of nominal period	60% of nominal period	ns
T_{CL}	Clock input low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate > 2V/ns				
MemClkOut Output				
F_C	MemClkOut clock output frequency–133MHz		66.66	MHz
T_C	MemClkOut clock period–133MHz	15		ns
F_C	MemClkOut clock output frequency–200MHz		100	MHz
T_C	MemClkOut clock period–200MHz	10		ns
F_C	MemClkOut clock output frequency–266MHz		133.33	MHz
T_C	MemClkOut clock period–266MHz	7.5		ns
T_{CH}	Clock output high time	45% of nominal period	55% of nominal period	ns
T_{CL}	Clock output low time	45% of nominal period	55% of nominal period	ns
Other Clocks				
F_C	VCO frequency	400	800	MHz
F_C	PLB frequency–133MHz		66.66	MHz
F_C	PLB frequency–200MHz		100	MHz
F_C	PLB frequency–266MHz		133.33	MHz
F_C	OPB frequency–133MHz		50[1]	MHz
F_C	OPB frequency–200MHz		50	MHz
F_C	OPB frequency–266MHz		50[1]	MHz

Notes:
1. If HDLCEX is not used, the maximum OPB frequency is 66.66MHz.

Clocking Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the NPe405L. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the NPe405L the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the NPe405L with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board NPe405L peripherals impose more stringent requirements (see Note 1).
- Use the peripheral bus clock (PerClk) for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the SDRAM MemClkOut since it also tracks the modulation.

Please refer to the application note *Using a Spread Spectrum Clock Generator with the PowerPC 405GP* for additional details. This application note is available on the IBM Microelectronics web site at http://www.chips.ibm.com.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates. If an external serial clock is used the baud rate is unaffected by the modulation
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.

Caution: It is up to the system designer to ensure that any SSCG used with the NPe405L meets the above requirements and does not adversely affect other aspects of the system.

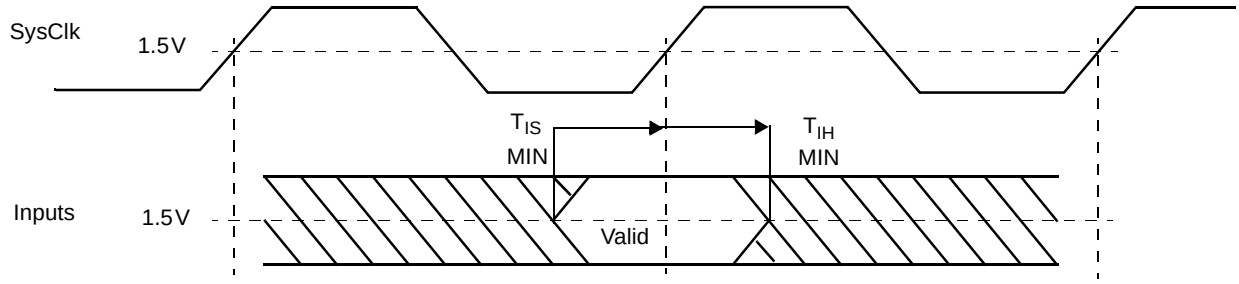
Peripheral Interface Clock Timings

Parameter	Min	Max	Units
EMC0MDClk output frequency	–	2.5	MHz
EMC0MDClk period	400	–	ns
EMC0MDClk output high time	160	–	ns
EMC0MDClk output low time	160	–	ns
PHY0TxClk input frequency	2.5	25	MHz
PHY0TxClk period	40	400	ns
PHY0TxClk input high time	35% of nominal period	–	ns
PHY0TxClk input low time	35% of nominal period	–	ns
PHY0RxClk input frequency	2.5	25	MHz
PHY0RxClk period	40	400	ns
PHY0RxClk input high time	35% of nominal period	–	ns
PHY0RxClk input low time	35% of nominal period	–	ns
PerClk output frequency–133MHz	–	33.33	MHz
PerClk period–133MHz	30	–	ns
PerClk output frequency–200MHz	–	50	MHz
PerClk period–200MHz	20	–	ns
PerClk output frequency–266MHz)	–	66.66	MHz
PerClk period–266MHz	15	–	ns
PerClk output high time	45% of nominal period	55% of nominal period	ns
PerClk output low time	45% of nominal period	55% of nominal period	ns
UARTSerClk input frequency (Note 1)	–	$1000/(2T_{OPB} + 2ns)$	MHz
UARTSerClk period	$2T_{OPB} + 2$	–	ns
UARTSerClk input high time	$T_{OPB} + 1$	–	ns
UARTSerClk input low time	$T_{OPB} + 1$	–	ns
TmrClk input frequency–133MHz	–	33.33	MHz
TmrClk period–133MHz	30	–	ns
TmrClk input frequency–200MHz	–	50	MHz
TmrClk period–200MHz	20	–	ns
TmrClk input frequency–266MHz	–	66.66	MHz
TmrClk period–266MHz	15	–	ns
TmrClk input high time	40% of nominal period	60% of nominal period	ns
TmrClk input low time	40% of nominal period	60% of nominal period	ns
HDLCEXTxClk, HDLCEXRxClk	0	8.192	MHz

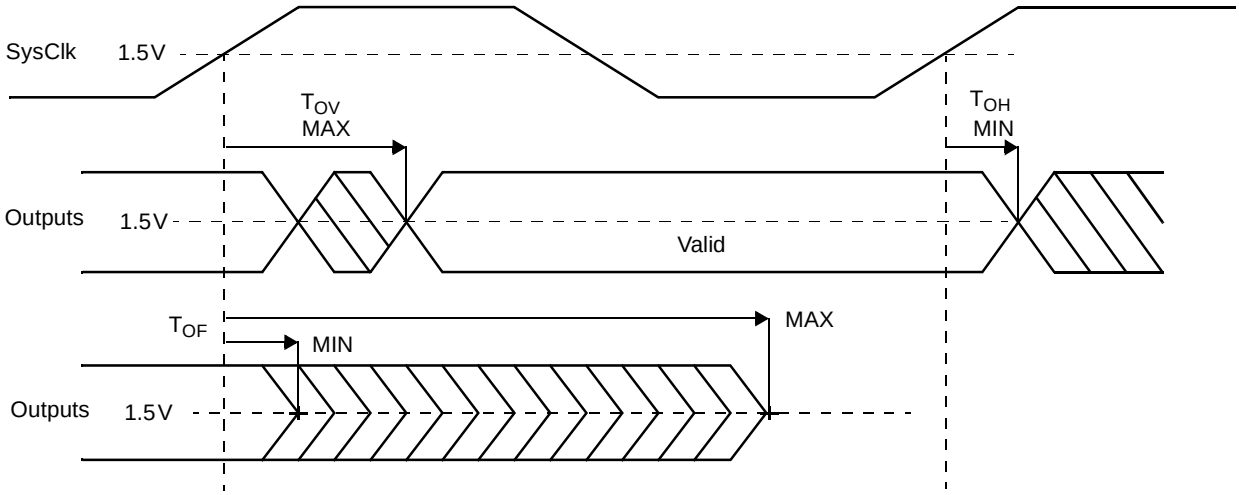
Notes:

1. T_{OPB} is the period in ns of the OPB clock. The maximum OPB clock frequency is 33.33 MHz for 133MHz parts, 50 MHz for 200MHz parts, and 66.66MHz for 266MHz parts.

Input Setup and Hold Waveform



Output Delay and Float Timing Waveform



I/O Specifications—All

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (maximum)	I/O L (minimum)		
Internal Peripheral Interface								
IICSCL	async	async	async	async	17	11		
IICSDA	async	async	async	async	17	11		
UART0_CTS	async	async	n/a	n/a	n/a	n/a		
UART0_DCD	async	async	n/a	n/a	n/a	n/a		
UART0_DSR	async	async	n/a	n/a	n/a	n/a		
UART0_DTR	n/a	n/a	async	async	12	8		
UART0_RI	async	async	n/a	n/a	n/a	n/a		
UART0_RTS	n/a	n/a	async	async	12	8		
UART0_Rx	async	async	n/a	n/a	n/a	n/a		
UART0_Tx	n/a	n/a	async	async	12	8		
UART1_CTS	async	async	n/a	n/a	n/a	n/a		
[UART1_DCD]	[async]	[async]	n/a	n/a	n/a	n/a		
UART1_DSR	async	async	n/a	n/a	n/a	n/a		
UART1_DTR	n/a	n/a	async	async	12	8		
[UART1_RI]	[async]	[async]	n/a	n/a	n/a	n/a		
UART1_RTS	n/a	n/a	async	async	12	8		
UART1_Rx	async	async	n/a	n/a	n/a	n/a		
UART1_Tx	n/a	n/a	async	async	12	8		
UARTSerClk	async	async	n/a	n/a	n/a	n/a		
Interrupts Interface								
[IRQ0:6]	async	async	n/a	n/a	n/a	n/a		
JTAG Interface								
TCK	async	async	n/a	n/a	n/a	n/a		
TDI	async	async	n/a	n/a	n/a	n/a		
TDO	n/a	n/a	async	async	12	8		
TMS	async	async	n/a	n/a	n/a	n/a		
TRST	async	async	n/a	n/a	n/a	n/a		
System Interface								
GPIO30	async	async	async	async	12	8		
Halt	async	async	n/a	n/a	n/a	n/a		
SysClk	n/a	n/a	n/a	n/a	n/a	n/a		
SysErr	n/a	n/a	5.5	1.7	12	8		
SysReset	n/a	n/a	n/a	n/a	12	8		
TestEn	dc	dc	n/a	n/a	n/a	n/a		
TmrClk	n/a	n/a	async	async	n/a	n/a		

I/O Specifications—133 and 200 MHz (Part 1 of 2)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM. Output times in table are in cycle 1.
3. SDRAM I/O timings are specified relative to a SysClk terminated in a lumped 10pF load.
4. SDRAM interface hold times are guaranteed at the NPe405L package pin. System designers must use the NPe405L IBIS model (available from **www.chips.ibm.com**) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (maximum)	I/O L (minimum)		
Ethernet Interface								
EMC0MDClk	n/a	n/a	7.4	1.5	12	8		1, async
EMC0MDIO	n/a	n/a	8.8	1.2	12	8	EMC0MDClk	1
EMC0TxD0:3 [EMC0Tx0:1D0:1] [EMC0Tx0:1D]	n/a	n/a	10.5 [7.3] [5.0]	3.0 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxEn [EMC0Tx0En] [EMC0Sync]	n/a	n/a	11.8 [7.2] [5.6]	2.9 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxErr[EMC0Tx1En]	n/a	n/a	11.8[7.4]	2.9[2.4]	12	8	PHYTX	1
PHY0Col[PHY0Rx1Er]	async[0.2]	async[1.7]	n/a	n/a	n/a	n/a		1
PHY0CrS[PHY0CrS0DV]	async[0.1]	async[1.9]	n/a	n/a	n/a	n/a		1
PHY0RxClk	n/a	n/a	n/a	n/a	n/a	n/a		1, async
PHY0RxD0:3 [PHY0Rx0:1D0:1] [PHY0Rx0:1D]	1.5 [0.8] [0.9]	1.7 [1.7] [0.3]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxDV[PHY0CRS1DV]	1.3[0.7]	1.7[1.7]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxErr[PHY0Rx0Er]	1.3[0.7]	1.8[1.9]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0TxClk[PHY0RefClk]	n/a	n/a	n/a	n/a	n/a	n/a		1, async
HDLCEX Interface								
HDLCEXRxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXRxDataA:B	23.8	2.1	n/a	n/a	n/a	n/a		
HDLCEXRxFS	24.2	1.1	n/a	n/a	n/a	n/a		
HDLCEXTxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXTxDataA:B	n/a	n/a	10.5	3.3	12	8		
HDLCEXTxFS	20.3	1.0	n/a	n/a	n/a	n/a		
[HDLCEXTxEnA]	n/a	n/a	11.3	3.5	12	8		
[HDLCEXTxEnB]]	n/a	n/a	11.8	3.8	12	8		
Trace Interface								
[TrcClk]GPIO00	n/a	n/a	11.2	1.2	12	8		
[TS1E]GPIO01	n/a	n/a	7.0	1.2	12	8		
[TS2E]GPIO02	n/a	n/a	7.0	1.2	12	8		
[TS1O]GPIO03	n/a	n/a	6.5	1.0	12	8		
[TS2O]GPIO04	n/a	n/a	6.4	1.0	12	8		
[TS3:6]GPIO05:08	n/a	n/a	6.4	1.0	12	8		

I/O Specifications—133 and 200MHz (Part 2 of 2)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM. Output times in table are in cycle 1.
3. SDRAM I/O timings are specified relative to a SysClk terminated in a lumped 10pF load.
4. SDRAM interface hold times are guaranteed at the NPe405L package pin. System designers must use the NPe405L IBIS model (available from **www.chips.ibm.com**) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (maximum)	I/O L (minimum)		
SDRAM Interface								
BA1:0	n/a	n/a	7.2	1.5	19	12	SysClk	2, 3
$\overline{\text{BankSel3:0}}$	n/a	n/a	5.8	1.0	19	12	SysClk	3
$\overline{\text{CAS}}$	n/a	n/a	7.0	1.4	19	12	SysClk	2, 3
ClkEn0:1	n/a	n/a	4.9	1.0	40	25	SysClk	3
DQM0:3	n/a	n/a	5.9	1.0	19	12	SysClk	3
DQMCB	n/a	n/a	5.9	1.0	19	12	SysClk	3
ECC0:7	2.0	0.3	5.7	1.0	19	12	SysClk	3
MemAddr12:00	n/a	n/a	7.2	1.4	19	12	SysClk	2, 3
MemClkOut0:1	n/a	n/a	0.4	-1.2	19	12	SysClk	3, 4
MemData00:31	2.0	0.3	5.6	1.0	19	12	SysClk	3
$\overline{\text{RAS}}$	n/a	n/a	7.4	1.6	19	12	SysClk	2, 3
$\overline{\text{WE}}$	n/a	n/a	7.1	1.4	19	12	SysClk	2, 3
External Peripheral Bus Interface								
[$\overline{\text{DMAReq0:3}}$]	[4.8]	[0.0]	[7.0]	[1.1]	n/a	n/a	PerClk	
[$\overline{\text{DMAAck0:3}}$]	n/a	n/a	[7.5]	[1.1]	12	8	PerClk	
[$\overline{\text{EOT0:3}}$/$\overline{\text{TC0:3}}$]	[4.3]	[-0.1]	[8.5]	[1.2]	12	8	PerClk	
PerAddr04:31	n/a	n/a	8.5	0.9	17	11	PerClk	
$\overline{\text{PerBLast}}$	n/a	n/a	7.4	1.4	12	8	PerClk	
$\overline{\text{PerCS0:3}}$	n/a	n/a	7.2	1.3	12	8	PerClk	
PerData00:15	4.8	1.0	9.3	1.0	17	11	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	7.6	1.4	12	8	PerClk	
PerPar0:1	3.1	0.0	8.3	0.9	17	11	PerClk	
PerR/$\overline{\text{W}}$	n/a	n/a	7.5	1.4	12	8	PerClk	
PerReady	7.5	-0.5	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWBE0:1}}$	n/a	n/a	7.5	1.3	12	8	PerClk	
PerClk	n/a	n/a	0.5	-0.9	17	11	PLB Clk	5
PerErr	4.0	-0.6	n/a	n/a	n/a	n/a	PerClk	
[$\overline{\text{PerWE}}$]	n/a	n/a	[8.3]	[1.3]	12	8		

I/O Specifications—266MHz (Part 1 of 2)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM. Output times in table are in cycle 1.
3. SDRAM I/O timings are specified relative to a SysClk terminated in a lumped 10pF load.
4. SDRAM interface hold times are guaranteed at the NPe405L package pin. System designers must use the NPe405L IBIS model (available from **www.chips.ibm.com**) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (maximum)	I/O L (minimum)		
Ethernet Interface								
EMC0MDClk	n/a	n/a	7.4	1.5	12	8		1, async
EMC0MDIO	n/a	n/a	6.7	1.2	12	8	EMC0MDClk	1
EMC0TxD0:3 [EMC0Tx0:1D0:1 [EMC0Tx0:1D]	n/a	n/a	7.7 [5.6] [4.6]	3 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxEn [EMC0Tx0En] [EMC0Sync]	n/a	n/a	9.4 [5.5] [4.2]	2.9 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxErr[EMC0Tx1En]	n/a	n/a	9.4[5.7]	2.9[2.4]	12	8	PHYTX	1
PHY0Col[PHY0Rx1Er]l	async[0.1]	async[1.4]	n/a	n/a	n/a	n/a		1
PHY0CrS[PHY0CrS0DV]	async[0.1]	async[1.5]	n/a	n/a	n/a	n/a		1
PHY0RxClk	n/a	n/a	n/a	n/a	n/a	n/a		1, async
PHY0RxD0:3 [PHY0Rx0:1D0:1] [PHY0Rx0:1D]	1.5 [0.8] [0.8]	1.4 [1.3] [0.2]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxDV[PHY0CRS1DV]	1.3[0.7]	1.3[1.3]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxErr[PHY0Rx0Er]	1.3[0.7]	1.4[1.5]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0TxClk[PHY0RefClk]	n/a	n/a	n/a	n/a	n/a	n/a		1, async
HDLCEX Interface								
HDLCEXRxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXRxDataA:B	23.9	1.6	n/a	n/a	n/a	n/a		
HDLCEXRxFS	24.2	0.8	n/a	n/a	n/a	n/a		
HDLCEXTxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXTxDataA:B	n/a	n/a	7.6	3.3	12	8		
HDLCEXTxFS	24.2	0.8	n/a	n/a	n/a	n/a		
[HDLCEXTxEnA]	n/a	n/a	[8.5]	[3.5]	12	8		
[HDLCEXTxEnB]	n/a	n/a	[8.9]	[3.8]	12	8		

I/O Specifications—266MHz (Part 2 of 2)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM. Output times in table are in cycle 1.
3. SDRAM I/O timings are specified relative to a SysClk terminated in a lumped 10pF load.
4. SDRAM interface hold times are guaranteed at the NPe405L package pin. System designers must use the NPe405L IBIS model (available from **www.chips.ibm.com**) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (maximum)	I/O L (minimum)		
Trace Interface								
[TrcClk]	n/a	n/a	8.7	1.2	12	8		
[TS1E]	n/a	n/a	5.8	1.2	12	8		
[TS2E]	n/a	n/a	5.7	1.2	12	8		
[TS1O]	n/a	n/a	5.3	1	12	8		
[TS2O]	n/a	n/a	5.3	1	12	8		
[TS3:6]	n/a	n/a	5.4	1	12	8		
SDRAM Interface								
BA1:0	n/a	n/a	5.5	1.5	19	12	SysClk	1, 2
$\overline{\text{BankSe3:0}}$	n/a	n/a	4.6	1	19	12	SysClk	2
$\overline{\text{CAS}}$	n/a	n/a	5.3	1.4	19	12	SysClk	1, 2
ClkEn0:1	n/a	n/a	3.9	1	40	25	SysClk	2
DQM0:3	n/a	n/a	4.7	1	19	12	SysClk	2
DQMCB	n/a	n/a	4.7	1	19	12	SysClk	2
ECC0:7	1.8	0.3	4.5	1	19	12	SysClk	2
MemAddr12:00	n/a	n/a	5.5	1.4	19	12	SysClk	1, 2
MemClkOut0:1	n/a	n/a	0.4	-1.2	19	12	SysClk	2, 3
MemData00:31	1.8	0.3	4.4	1	19	12	SysClk	2
$\overline{\text{RAS}}$	n/a	n/a	5.7	1.6	19	12	SysClk	1, 2
$\overline{\text{WE}}$	n/a	n/a	5.4	1.4	19	12	SysClk	1, 2
External Peripheral Bus Interface								
[$\overline{\text{DMAReq0:3}}$]	4.1	0	5.5	1.1	n/a	n/a	PerClk	
[$\overline{\text{DMAAck0:3}}$]	n/a	n/a	5.9	1.1	12	8	PerClk	
[$\overline{\text{EOT0:3}}$/$\overline{\text{TC0:3}}$]	3.7	-0.1	6.7	1.2	12	8	PerClk	
PerAddr04:31	n/a	n/a	6.5	0.9	17	11	PerClk	
$\overline{\text{PerBLast}}$	n/a	n/a	5.6	1.4	12	8	PerClk	
$\overline{\text{PerCS0:3}}$	n/a	n/a	5.5	1.3	12	8	PerClk	
PerData00:15	3.9	1	7.1	1	17	11	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	5.7	1.4	12	8	PerClk	
PerPar0:1	2.7	0	6.4	0.9	17	11	PerClk	
PerR/$\overline{\text{W}}$	n/a	n/a	5.7	1.4	12	8	PerClk	
PerReady	6.2	-0.5	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWBE0:1}}$	n/a	n/a	5.7	1.3	12	8	PerClk	
PerClk	n/a	n/a	0.5	-0.9	17	11	PLB Clk	4
PerErr	3.5	-0.6	n/a	n/a	n/a	n/a	PerClk	
[$\overline{\text{PerWE}}$]	n/a	n/a	7	1.3	12	8		

Initialization

The following describes the method by which initial chip settings are established when a system reset occurs.

Strapping

While the $\overline{\text{SysReset}}$ input pin is low (system reset), the state of certain I/O pins is read to enable default initial conditions prior to NPe405L start-up. The actual capture instant is the nearest SysClk edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. The recommended pull-up is 3kΩ to +3.3V or 10kΩ to +5V, the recommended pull-down is 1kΩ to GND.These pins are used for strap functions only during reset. They are used for other signals during normal operation. The following table lists the strapping pins along with their functions and strapping options.

Strapping Pin Assignments

Function	Option	Ball Strapping	
EXT_BootW Width of boot device on EBC data bus		**Y21** (UART1_Tx)	
	8 bits	0	
	16 bits	1	
ZMII_Mode Ethernet ZMII mode		**V21** ($\overline{\text{UART1\_RTS}}$)	**U20** ($\overline{\text{UART1\_DTR}}$)
	MII mode	0	0
	SMII mode	0	1
	RMII 10 Mbps mode	1	0
	RMII 100 Mbps mode	1	1

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