460GT

Preliminary Data Sheet

PowerPC 460GT Embedded Processor

Features

- PowerPC® 440 processor operating between 667MHz and 1GHz with 32KB I-cache and D-cache and 256KB L2/SRAM with parity checking
- On-chip memory (64KB)
- Processor Local Bus (PLB) with 128-bit width
- Floating Point unit
- Double Data Rate 2/1 (DDR2/1) Synchronous DRAM (SDRAM) interface
- One four-channel DMA (Direct Memory Access) for internal and external peripherals
- One single-channel, high-performance DMA for internal use
- External 32-bit peripheral bus (EBC) for up to six devices. Up to 100MHz
- Programmable Interrupt Controller (UIC) with up to 16 external interrupts
- Programmable General Purpose Timers (GPTs)
- Two PCI Express 1.1 interfaces—one 4-lane and one 1-lane
- PCI V2.3 interface. Thirty-two bits at up to 66MHz
- Four Ethernet 10/100/1000Mbps half- or full-duplex interfaces. Operational modes supported are MII, RMII, GMII, RGMII, and SGMIII with QoS, Jumbo frames, interrupt coalescing, and TCP/IP acceleration
- Up to four serial (UART) ports (16750 compatible)
- Two IIC interfaces (one with boot parameter read capability)
- NAND Flash interface
- SPI interface
- Serial Rapid I/O (SRIO) port
- General Purpose I/O (GPIO) interface
- JTAG interface for board level testing
- Boot from PCI memory, NOR Flash on the external peripheral bus, or NAND Flash on the NAND Flash interface
- Optional security feature (PPC460GT-S) with KASUMI.
- Available in RoHS compliant, lead-free package

Description

Designed specifically to address high-end embedded applications, the PowerPC 460GT (PPC460GT) provides a high-performance, low-power solution that interfaces to a wide range of peripherals and incorporates on-chip power management features.

This chip contains a high-performance RISC processor, a floating point unit, on-chip memory, a DDR2/1 SDRAM controller, PCI and PCI Express bus interfaces, control for external ROM and peripherals, DMA with scatter/gather support, Ethernet ports, serial ports, IIC interfaces, SPI interface, NAND Flash interface, SRIO support, an optional security feature with KASUMI (PPC460GT-S), and general purpose I/O.

Technology: CMOS Cu-08, 90nm.

Package: 35mm, 728-ball thermally and electrically enhanced plastic ball grid array (TE-EPBGA). RoHS compliant package available.

Typical power: Less than 6W at 1GHz.

Supply voltages required: 3.3V, 2.5V (DDR1, Ethernet), 1.8V (DDR2), 1.2V.

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Ordering and PVR Information

For information on the availability of the following parts, contact your local AMCC sales office. For additional information on the part number structure see *Figure 1*.

Product Name	Order Part Number (see **Notes**)	Package	Revision Level	PVR Value	JTAG ID
PPC460GT	PPC460GT-SpAfff(f)T	35mm 728-ball TE-EPBGA	A	0x130218A0	0x144101E1
PPC460GT	PPC460GT-NpAfff(f)T	35mm 728-ball TE-EPBGA	A	0x130218A1	0x144101E1

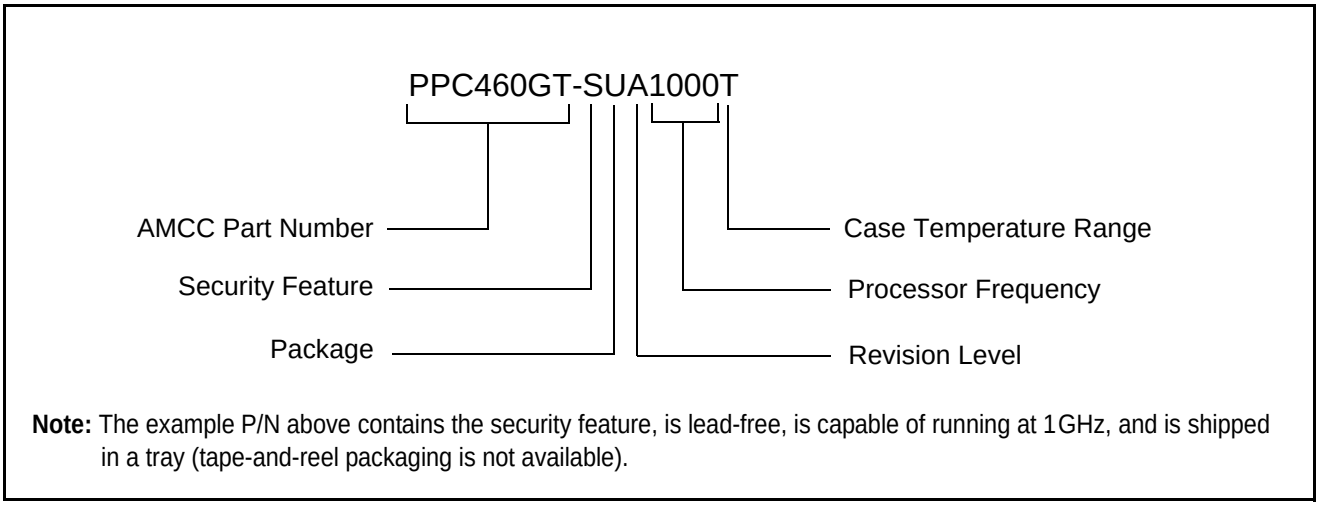
Notes: Characters following the dash (-):

1. S = Security feature present, N = Security feature not present
2. p = Package type: U = lead-free (RoHS compliant), T = contains lead.
3. A = Chip revision level A
4. fff(f) = Processor frequency: fff = 600 = 667MHz, fff = 800 = 800MHz, ffff = 1000 = 1GHz
5. T = Case temperature range of –40°C to +85°C.

Each part number contains a revision code. This is the die mask revision number and is included in the part number for identification purposes only.

The PVR (Processor Version Register) and the JTAG ID register are software accessible (read-only) and contain information that uniquely identifies the part. Refer to the *PowerPC 460GT Embedded Processor User's Manual* for details on accessing these registers.

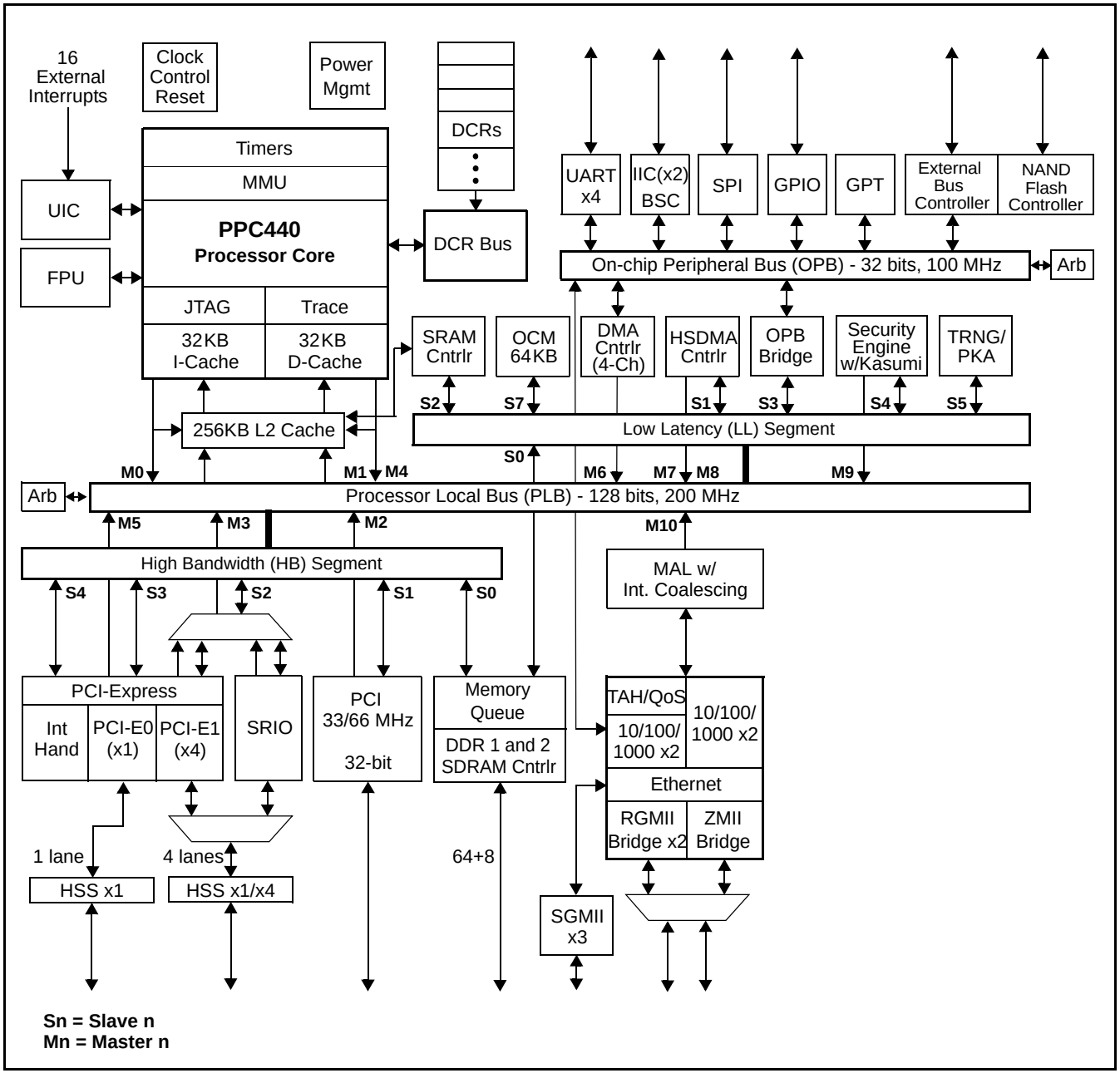
Figure 1. Order Part Number Key



Note: The example P/N above contains the security feature, is lead-free, is capable of running at 1GHz, and is shipped in a tray (tape-and-reel packaging is not available).

Block Diagram

Figure 2. PPC460GT Functional Block Diagram



The PPC460GT is a system on a chip (SOC).

Address Maps

The PPC460GT incorporates two address maps. The first is a fixed processor System Memory Address Map. This address map defines the possible contents of various address regions which the processor can access. The second is the DCR Address Map for Device Configuration Registers (DCRs). The DCRs are accessed by software running on the PPC460GT processor through the use of **mtdcr** and **mfdcr** instructions.

Table 1. System Memory Address Map (Part 1 of 3)

Function	Sub Function	Start Address	End Address	Size
Local Memory (LL)[1]	DDR SDRAM	0000 0000 0000 0000	0000 0003 FFFF FFFF	16GB
	SRAM (L2 Cache)	0000 0004 0000 0000	0000 0004 0003 FFFF	256KB
	On-Chip Memory (OCM)	0000 0004 0004 0000	0000 0004 0004 FFFF	64KB
	Reserved	0000 0004 0005 0000	0000 0004 000F FFFF	704KB
Internal PLB Interfaces (LL)[1]	I2O/DMA	0000 0004 0010 0000	0000 0004 0010 FFFF	64KB
	I2O Registers	0000 0004 0010 0000	0000 0004 0010 00FF	256B
	Reserved	0000 0004 0010 0100	0000 0004 0010 01FF	256B
	HSDMA Registers	0000 0004 0010 0200	0000 0004 0010 02FF	256B
	Reserved	0000 0004 0010 0300	0000 0004 0010 FFFF	63.25KB
	PKA & TRNG (EIPPKP)	0000 0004 0011 0000	0000 0004 0011 FFFF	64KB
	Reserved	0000 0004 0012 0000	0000 0004 0017 FFFF	384KB
	Security Function (EIP94)	0000 0004 0018 0000	0000 0004 001F FFFF	512KB
	Reserved	0000 0004 0020 0000	0000 0004 BFFF FFFF	~3GB

Table 1. System Memory Address Map (Part 2 of 3)

Function	Sub Function	Start Address	End Address	Size
Internal OPB Peripherals (LL)	EBC Memory except Bank 0 [6]	0000 0004 C000 0000	0000 0004 E7FF FFFF	640MB
	Reserved	0000 0004 E800 0000	0000 0004 EF5F FFFF	118MB
	General Purpose Timer	0000 0004 EF60 0000	0000 0004 EF60 01FF	512B
	Reserved	0000 0004 EF60 0200	0000 0004 EF60 02FF	256B
	UART0	0000 0004 EF60 0300	0000 0004 EF60 0307	8B
	Reserved	0000 0004 EF60 0308	0000 0004 EF60 03FF	248B
	UART1	0000 0004 EF60 0400	0000 0004 EF60 0407	8B
	Reserved	0000 0004 EF60 0408	0000 0004 EF60 04FF	248B
	UART2	0000 0004 EF60 0500	0000 0004 EF60 0507	8B
	Reserved	0000 0004 EF60 0508	0000 0004 EF60 05FF	248B
	UART3	0000 0004 EF60 0600	0000 0004 EF60 0607	8B
	Reserved	0000 0004 EF60 0608	0000 0004 EF60 06FF	248B
	IIC0	0000 0004 EF60 0700	0000 0004 EF60 071F	32B
	Reserved	0000 0004 EF60 0720	0000 0004 EF60 07FF	224B
	IIC1	0000 0004 EF60 0800	0000 0004 EF60 081F	32B
	Reserved	0000 0004 EF60 0820	0000 0004 EF60 08FF	224B
	SPI	0000 0004 EF60 0900	0000 0004 EF60 090F	16B
	Reserved	0000 0004 EF60 0910	0000 0004 EF60 09FF	240B
	OPB Arbiter	0000 0004 EF60 0A00	0000 0004 EF60 0A3F	64B
	Reserved	0000 0004 EF60 0A40	0000 0004 EF60 0AFF	192B
	GPIO0 Controller	0000 0004 EF60 0B00	0000 0004 EF60 0B7F	128B
	Reserved	0000 0004 EF60 0B80	0000 0004 EF60 0BFF	128B
	GPIO1 Controller	0000 0004 EF60 0C00	0000 0004 EF60 0C7F	128B
	Reserved	0000 0004 EF60 0C80	0000 0004 EF60 0CFF	128B
	Ethernet PHY ZMII	0000 0004 EF60 0D00	0000 0004 EF60 0D0F	16B
	Reserved	0000 0004 EF60 0D10	0000 0004 EF60 0DFF	240B
	EMAC0 Controller	0000 0004 EF60 0E00	0000 0004 EF60 0EFF	256B
	EMAC1 Controller	0000 0004 EF60 0F00	0000 0004 EF60 0FFF	256B
	Reserved	0000 0004 EF60 1000	0000 0004 EF60 10FF	256B
	EMAC2 Controller	0000 0004 EF60 1100	0000 0004 EF60 11FF	256B
	EMAC3 Controller	0000 0004 EF60 1200	0000 0004 EF60 12FF	256B
	TAHOE0 Accelerator	0000 0004 EF60 1300	0000 0004 EF60 13FF	256B
	TAHOE1 Accelerator	0000 0004 EF60 1400	0000 0004 EF60 14FF	256B
	RGMII0 Controller	0000 0004 EF60 1500	0000 0004 EF60 150F	16B
	Reserved	0000 0004 EF60 1510	0000 0004 FEFF FFFF	240B
	RGMII1 Controller	0000 0004 EF60 1600	0000 0004 EF60 160F	16B

Table 1. System Memory Address Map (Part 3 of 3)

Function	Sub Function	Start Address	End Address	Size
	Reserved	0000 0004 EF60 1610	0000 0004 FEFF FFFF	262B
Boot ROM [2, 3]	EBC Memory Bank 0	0000 0004 FF00 0000	0000 0004 FFFF FFFF	16MB
Internal PLB Interfaces (LL)	Reserved	0000 0005 0000 0000	0000 0007 FFFF FFFF	12GB
Local Memory Alias (HB)	Aliased DDR SDRAM	0000 0008 0000 0000	0000 000B FFFF FFFF	16GB
PCI/PCIE Space (HB)	PCI Express and SRIO Memory	0000 000C 0000 0000	0000 000C 07FF FFFF	128MB
	PCI I/O	0000 000C 0800 0000	0000 000C 0800 FFFF	64KB
	PC Express and SRIO Memory	0000 000C 0801 0000	0000 000C 087F FFFF	~8MB
	PCI Extra I/O	0000 000C 0880 0000	0000 000C 0BFF FFFF	~56MB
	PCI Express Memory and SRIO Memory	0000 000C 0C00 0000	0000 000C 0EBF FFFF	~44MB
	PCI Configuration Registers	0000 000C 0EC0 0000	0000 000C 0EC0 0007	8B
	Reserved	0000 000C 0EC0 0008	0000 000C 0EC7 FFFF	~512KB
	PCI Local Registers	0000 000C 0EC8 0000	0000 000C 0EC8 11FF	4.75KB
	Reserved	0000 000C 0EC8 1200	0000 000C 0ECF FFFF	~512KB
	PCI Special Cycle	0000 000C 0ED0 0000	0000 000C 0ED0 0003	4B
	Reserved	0000 000C 0ED0 0004	0000 000C 0FFF FFFF	~19MB
	PCI Express Interrupt Handler	0000 000C 1000 0000	0000 000C 1000 00FF	256B
	PCI, PCI-E and SRIO Memory	0000 000C 1000 0100	0000 000C FEFF FFFF	~3.8MB
	PCI Boot ROM (PCI Memory)	0000 000C FF00 0000	0000 000C FFFF FFFF	16MB
	PCI, PCI-E and SRIO Memory	0000 000D 0000 0000	0000 000F FFFF FFFF	12GB
	Reserved [4]	0000 0010 0000 0000	03FF FFFF FFFF FFFF	
	Reserved [5]	0400 0000 0000 0000	0FFF FFFF FFFF FFFF	
XOR Space (HB)	XOR	1000 0000 0000 0000	1FFF FFFF FFFF FFFF	
PCI/PCIE Space (HB)	PCI, PCI-E and SRIO Memory	2000 0000 0000 0000	FFFF FFFF FFFF FFFF	

Notes:

1. DDR SDRAM, SRAM (L2 Cache) and On-Chip Memory (OCM) can be located anywhere in the Local Memory area of the memory map.
2. The Boot ROM area of the memory map are intended for use by ROM or Flash-type devices. While locating volatile DDR SDRAM and SRAM in this region is supported, use of these regions for this purpose is not recommended.
3. When the optional boot from PCI Memory is selected, the PCI Boot ROM address space begins at 0000 000C FF00 0000 (16 MB).
4. Never decoded.
5. Unpredictable results on Read and Write operations.
6. Accessed by means of EBC Peripheral Bank Configuration Registers.

Table 2. DCR Address Map

Function	Base Address	Start Address	End Address	Size
Total DCR Address Space[1]		000	3FF	1KW (4KB)[1]
By function:				
Reserved		000	00B	12W
Clocking Power On Reset (CPR)	00 0000 110x	00C	00D	2W
System DCRs (SDR)	00 0000 111x	00E	00F	2W
Memory Controller	00 0001 000x	010	011	2W
External Bus Controller (EBC)	00 0001 001x	012	013	2W
Reserved		014	01F	12W
L2 Cache as SRAM	00 0010 xxxx	020	02F	16W
L2 Controller	00 0011 xxxx	030	03F	16W
Memory Queue	00 010x xxxx	040	04F	16W
Reserved		050	05F	16W
I2O/DMA Controller	00 011x xxxx	060	07F	32W
PLB Arbiter	00 1000 xxxx	080	08F	16W
PLB-to-OPB Bridge	00 1001 xxxx	090	09F	16W
Reserved		0A0	0AF	16W
On-Chip Memory (OCM)	00 1011 xxxx	0B0	0BF	16W
Universal Interrupt Controller 0	00 1100 xxxx	0C0	0CF	16W
Universal Interrupt Controller 1	00 1101 xxxx	0D0	0DF	16W
Universal Interrupt Controller 2	00 1110 xxxx	0E0	0EF	16W
Universal Interrupt Controller 3	00 1111 xxxx	0F0	0FF	16W
PCI Express 0	01 000x xxxx	100	11F	32W
PCI Express 1	01 001x xxxx	120	13F	32W
SRIO	01 010x xxxx	140	15F	32W
Power Management	01 011x xxxx	160	167	8W
Reserved		168	17F	24W
Ethernet MAL	01 1xxx xxxx	180	1FF	128W
DMA Controller	10 00xx xxxx	200	23F	64W
Reserved		240	3FF	448W

Notes:

1. DCR addresses are 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register. One kiloword (1024W) equals 4KB (4096 B).

PowerPC 440 Processor

The PowerPC 440 processor (in 90nm technology) is designed for high-end applications: RAID controllers, SAN, iSCSI, routers, switches, printers, set-top boxes, and so on. It implements the Book E PowerPC embedded architecture and uses the 128-bit version of IBM's on-chip CoreConnect Bus Architecture.

Features include:

- Up to 1GHz operation
- PowerPC Book E architecture
- 32KB I-cache, 32KB D-cache
  - UTLB Word Wide parity on data and tag address parity with exception force
- Three logical regions in D-cache: locked, transient, normal
- D-cache full line flush capability
- 41-bit virtual address, 36-bit (64GB) physical address
- Superscalar, out-of-order execution
- 7-stage pipeline
- Three execution pipelines
- Dynamic branch prediction
- Memory management unit
  - 64-entry, full associative, unified TLB with optional parity
  - Separate instruction and data micro-TLBs
  - Storage attributes for write-through, cache-inhibited, guarded, and big or little endian
- Debug facilities
  - Multiple instruction and data range breakpoints
  - Data value compare
  - Single step, branch, and trap events
  - Non-invasive real-time trace interface
- 24 DSP instructions
  - Single cycle multiply and multiply-accumulate
  - 32 x 32 integer multiply
  - 16 x 16 -> 32-bit MAC

Floating Point Unit (FPU)

The chip has a built-in super scalar FPU that supports both single- and double-precision operations, and offers single cycle through put on most instructions.

Features include:

- Five stages with 2 MFlops/MHz
- Hardware support for IEEE 754
- Single- and double-precision
- Single-cycle throughput on most instructions
- Thirty-two 64-bit floating point registers

L2 Cache/SRAM

The PPC460GT also provides a 256KB L2 cache between the Processor Local Bus and the processor's D- and I-caches. This memory unit can be alternatively programmed to function as 256KB of SRAM.

Features include:

- Four banks of 64KB each
- Memory cycles supported:
  - Single beat read and write, 1 to 16 bytes
  - Quadword Read and Write burst for 12-bit master
  - Guarded memory accesses on 4KB boundaries

- Sustainable 3.2GB/s peak bandwidth at 200MHz
- Use as an L2 cache improves processor performance and reduces the PLB load
  - Data Array and Tag Array parity
  - Unified data and instruction cache
  - Four-way set associative
  - 36-bit addressing
  - Full LRU replacement algorithm
  - Write through, look aside

On-Chip Memory (OCM)

The PPC460GT provides 64KB of on-chip memory.

Features include:
- Up to 128-bit bus width
- 128-bit slave attachment, addressable by any PLB master
- Transfers by PLB slave cycles:
  - Single-beat read and write (1 to 8 bytes for 64-bit masters, 1 to 16 bytes for 128-bit masters)
  - 4- and 8-word line reads and writes
  - Double word read and write bursts for 64-bit masters
  - Quadword read and write bursts for 128-bit masters
  - Slave-terminated double word and quadword fixed length bursts
  - Master-terminated variable length bursts
- Guarded memory access on 4KB boundaries
- Data parity checking
- Data transfers at PLB bus speeds
- Power management
- Use as storage area for DMA descriptors and packet data for processing by Ethernet and Security Function.

Internal Buses

The PowerPC 460GT features three standard internal buses: one Processor Local Bus (PLB), one On-chip Peripheral Bus (OPB), and the Device Control Register bus (DCR). The high performance, high bandwidth functions such as the PowerPC 440 processor, the DDR SDRAM memory controller, PCI Express, and PCI connect to the PLB. The OPB hosts lower data rate peripherals. The daisy-chained DCR provides a lower bandwidth path for passing status and control information between the processor and the other on-chip cores.

The PLB has a Crossbar arbiter that supports data transfer between the PLB master and two slave segments identified as the Low Latency (LL) and High Bandwidth (HB) segments. The LL segment allows PLB masters CPU and I2O, that are adversely affected by latency, to communicate with slave devices with minimal latency. The HB segment allows PLB masters DMA, PCI and PCI Express to exchange large blocks of data with SDRAM, PCI and PCI Express without interfering with the low latency PLB masters.

Features include:
- PLB4 (128-bit)
  - 128-bit implementation of the PLB architecture
  - Separate and simultaneous read and write data paths
  - 64-bit address
  - Simultaneous control, address, and data phases
  - Four levels of pipelining
  - Byte-enable capability supporting unaligned transfers
  - 32- and 64-byte burst transfers
  - 200MHz, maximum 12.8GB/s (simultaneous read and write)
  - Processor:bus clock ratios of N:1

- OPB
  - 32-bit data path with dynamic sizing for 32-, 16-, and 8-bit width
  - 32-bit address
  - 100MHz
- DCR
  - 32-bit data path
  - 10-bit address

Security Function (optional)

The built-in security function (PPC460GT-S only) is a cryptographic engine attached to the PLB with built-in DMA and interrupt controllers.

Features include:

- Federal Information Processing Standard (FIPS) 140-2 design
- Support for an unlimited number of Security Associations (SA)
- Different SA formats for each supported protocol (IPsec/SSL/TLS/sRTP)
- Internet Protocol Security (IPSec) features
  - Full packet transforms (ESP & AH)
  - Complete header and trailer processing (IPv4 and IPv6)
  - Multi-mode automatic padding
  - "Mutable bit" handler for AH, including IPv4 option and IPv6 extension headers
- Secure Socket Layer (SSL) and Transport Layer Security (TLS) features
  - Packet transforms
  - One-pass hash-then-encrypt for SSL and TLS packet transforms for inbound packet using Stream Cipher
- Secure Real-Time Protocol (sRTP) features
  - Packet transforms
  - ROC removal and TAG insertion
  - Variable bypass offset of header length per packet
- IPsec/SSL security acceleration engine
- DES, 3DES, AES, ARC-4, AES-GCM, and GMAC-AES encryption
- MD-5, SHA-1, and SHA-256 hashing, HMAC encrypt-hash and hash-decrypt
- KASUMI algorithm support
- Public key acceleration for RSA, DSA and Diffie-Hellman
- True or pseudo random number generators
  - Non-deterministic true random numbers
  - Pseudo random numbers with lengths of 8B or 16B
  - ANSI X9.17 Annex C compliant using a DES algorithm
- Interrupt controller
  - Fifteen programmable, maskable interrupts
  - Initiate commands via an input interrupt
  - Sixteen programmable interrupts indicating completion of certain operations
  - All interrupts mapped to one level- or edge-sensitive programmable interrupt output
- DMA controller
  - Autonomous, 4-channel
  - 1024-words (32 bits/word) per DMA transfer
  - Scatter/gather capability with byte aligned addressing

PCI Controller

The PCI interface allows connection of PCI devices to the PowerPC processor and local memory. This interface is designed to Version 2.3 of the PCI Specification and supports 32- bit PCI devices.

Reference Specifications:
- PCI Specification Version 2.3
- PCI Bus Power Management Interface Specification Version 1.1

Features include:
- Frequency to 66MHz
- 32-bit bus
- PCI Host Bus Bridge or an Adapter Device's PCI interface
- Internal PCI arbitration function, supporting up to four external devices, that can be disabled for use with an external arbiter
- Support for inbound and outbound Message Signaled Interrupts (MSI)
- Simple message passing capability
- Asynchronous to the PLB
- PCI Power Management 1.1
- PCI register set addressable both from on-chip processor and PCI device sides
- Ability to boot from PCI bus memory
- Error tracking/status
- Supports initiation of transfers of the following types:
  - Single beat I/O reads and writes
  - Single beat and burst memory reads and writes
  - Single beat configuration reads and writes (type 0 and type 1)
  - Single beat special cycles
- Vital Product Data (VPD) support

PCI Express Controller

There are two independent PCI Express interfaces compliant with PCI Express base specification 1.1. One interface can be configured as one to four lanes while the other functions as one-lane only. The four-lane interface shares a High-Speed SERDES with the Serial Rapid I/O (SRIO) interface. Both can be Root or Endpoint Ports.

Features include:
- Two independent PCI Express interfaces
  - One 4 lanes
  - One 1 lane
  - 2.5 GB/sec full duplex per lane
- Compliant with PCI Express base specification 1.1
- Each PCI Express port can be End Point or Root Complex. (Upstream & Downstream)
  - Applications compliant with MSI rules are limited to one Endpoint port per PPC460GT
- Power Management
- Supports one virtual channel (VC0) no Traffic Class (TC) filtering
- Maximum Payload block size 512 Bytes
- Supports up to 512 Bytes maximum Read request size
- Requests supported:
  - up to 4 (x4) or 2 (x1) posted outbound Write requests (memory and messages)
  - up to 4 (x4) or 2 (x1) posted inbound Write requests
  - up to 4 (x4) or 2 (x1) outbound Read requests outstanding on PCI Express
  - up to 4 (x4) or 2 (x1) inbound Read requests outstanding on PCI Express
  - Outbound I/O request as a PCI Express Root Port
  - Inbound I/O request as a PCI Express Endpoint

- Buffering in each PCI Express port for the following transaction types:
  - 2KB Replay buffer: up to 4 in flight transactions
  - 2KB (x4) or 1KB (x1) for Outbound posted Writes
  - 2KB (x4) or 1KB (x1) for Outbound Reads completion
  - 2KB (x4) or 1KB (x1) for Inbound posted Writes
  - 2KB (x4) or 1KB (x1) for Inbound Reads completion
- Parity checking on each buffer
- Programmable Outbound Memory (POM) regions: 3 memory, 1 I/O, 1 message, 1 configuration, 1 internal register
- Programmable Inbound Memory (PIM) regions: 4 memory, 1 I/O, 1 expansion ROM
- INTx Interrupts support (legacy PCI):
  - Up to four INTx Termination for Root Ports. A/B/C/D interrupts are wired to the UIC
  - A/B/C/D INTx types generation for Endpoints
- MSI - Message Signaled Interrupts
  - MSI generation for Endpoint
  - MSI termination for Root Ports
  - MSI_X termination for Root Ports

DDR2/1 SDRAM Memory Controller

The Double Data Rate 2/1 (DDR2/1) SDRAM memory controller supports industry standard 184-pin DIMMs, SO-DIMMs, and other discrete devices. Global memory timings, address and bank sizes, and memory addressing modes are programmable. This controller interfaces to the PLB through a Memory Queue (MQ) function that includes six high-speed 1KB FIFO buffers.

The correct I/O supply voltage must be provided for the two types of DDR devices: DDR1 devices require +2.5V and DDR2 devices require +1.8V.

Features include:
- Registered and non-registered industry standard DIMMs
- DDR2 333/400 support
- 64-and 32-bit memory interfaces with optional 8-bit ECC (SEC/DED)
- 3.2GB/s peak bandwidth for the 64-bit interface
- 1.6GB/s peak bandwidth for the 32-bit interface
- Four chip (bank) select signals supporting four external banks
- CAS latencies of 2, 3, 4, 5, 6, and 7
- Page mode accesses (up to 32 open pages) with configurable paging policy
- Look-ahead request queue with programmable depth of four commands
- Optional optimized command scheduling (activate/precharge non-conflicting banks while accessing the current bank)
- Up to 16GB in four external banks
- Up to two MemClkOut signals
- Programmable address mapping and timing
- Hardware and software initiated self-refresh
- Sync DRAM configuration by means of mode register and extended mode register set commands
- Power management (self-refresh, suspend, sleep)
- Low Latency and High Bandwidth PLB ports
- Selectable PLB read response (immediate or deferred)
- Programmable Low Latency and High Bandwidth arbitration schemes
- High Bandwidth port has four 1KB read buffers and two 1KB write buffers
- Low Latency port has four 128B read buffers and two 128B write buffers

External Peripheral Bus Controller (EBC)

The External Bus Controller (EBC) transfers data between the PLB and external memory or peripheral devices attached to the external peripheral bus. The EBC allows for direct attachment of memory devices such as ROM and SRAM, DMA device-paced memory devices, and DMA peripheral devices.

Features include:

- Up to six ROM, EPROM, SRAM, Flash memory, and slave peripheral I/O banks supported
- Up to 100 MHz operation
- Burst and non-burst devices
- 32-bit byte-addressable data bus
- Data parity
- 27-bit address
- Peripheral Device pacing with external Ready
- Latch data on Ready, synchronous or asynchronous
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to eight Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping
- External DMA Slave Support

Ethernet Controller

Four 10/100/1000 Ethernet ports are supported.

Features include:

- Compliant with ANSI/IEEE Standard 802.3 and IEEE 802.3u supplement
- Compliant with IEEE Standard 802.3z (Gigabit Ethernet)
- Four 10/100/1000 interfaces running in full- and half-duplex modes providing:
  - Two Gigabit Media Independent Interface (GMII)
  - Two Media Independent Interface (MII)
  - Four Reduced Media Independent Interface (RMII)
  - Four Serial MII (SMII) at 100/10 Mbps.
  - Four Reduced Gigabit MII (RGMII)
  - Three Serial Gigabit Media Independent Interface (SGMII).
- Quality of Service (QoS) support on two interfaces
  - Support of IEEE 802.1p priority queueing for up to 8 priorities
  - Recognizes TCI field in VLAN-tagged frames where the priority field is coded
- Jumbo frame support (9018 bytes)
  - Support for Ethernet II formatted frames (RFC894)
  - Support for IEEE formatted frames (RFC1042)
  - Handles VLAN-tagged frames (IEEE 802.2ac)
- TCP/IP Acceleration Hardware (TAH) support on two interfaces
  - Off loads Gigabit Ethernet protocol processing from the CPU
  - Checksum verification for TCP/UDP/IP headers in the receive path
  - Checksum generation for TCP/UDP/IP headers in the transmit path
  - TCP segmentation support in the transmit path
  - IPv4 and IPv6 support
  - IPv6 header extension support
- Wake On LAN handling
- 256-bit hash table to filter multicast frames
- DMA capability

- Interrupt coalescence

DMA 4-Channel Controller

The 4-channel DMA controller provides a DMA interface between the PLB memories and internal and external peripheral devices.

Features include:
- Supports the following transfers:
  - Memory-to-memory
  - Buffered peripheral to memory
  - Buffered memory to peripheral
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 64-bit addressing
- 128 byte FIFO buffer
- Address increment or decrement
- Support for:
  - Internal and external peripherals
  - Memory mapped peripherals
  - Peripherals running on slower frequency buses

Serial Rapid I/O (SRIO)

The Serial Rapid IO (SRIO) interface provides an interface to physical storage devices. It shares the High-Speed SERDES with the 4-lane PCI-Express interface.

Features include:
- Compliant with RapidIO Interconnect Specification, Revision 1.2
- Supports operation at 1.25 Gbps, 2.50 Gbps, and 3.125 Gbps
- Supports 1X/4X LP-SERIAL implementation of RapidIO (except GSM extensions)
- Supports RapidIO Multicast Event (TOD) reception and transmission
- Supports RapidIO Error Management Extensions and Software Error Recovery
- Supports interoperability class 3 (complex mastering device)
- Supports device hot-insertion/extraction
- Separate 4KB transmit and receive request/response queues

I20/DMA Controller

The I2O/DMA controller provides one High Speed DMA (HSDMA) interface to the PLB and support for I2O messaging. The HSDMA provides single-channel direct memory access support to ease the CPU burden. I2O manages Message Frame Address (MFA) FIFOs or queues in memory in response to I2O register reads and writes and transfers message frames.

DMA features include:
- Programmable Command Pointer FIFO and Completion FIFO size (up to 2048 DMA operations queued)
- Separate 512-byte buffering for transmit and receive
  - 1.4GB throughput (local read)
  - 1.0GB throughput (remote read)
- Simultaneous fill and drain (PLB read/write pipelining)
- Any source PLB address to any destination address
- No memory alignment restrictions on source or destination
- 32-byte command descriptor block
- Maximum transfer size of 16MB
- 64-bit addressing

- Prefetch indicators for PCI buffer management
- Supports initiation of transfer to the following address spaces:
  - Single beat I/O reads and writes
  - Single beat and burst memory reads and writes
  - Single beat configuration reads and writes (type 0 and type 1)
  - Single beat special cycles
- iSCSI CRC32 generation and checking

I2O features include:

- I2O pull- and push-messaging methods
- Dynamic message frame size
- Programmable FIFO size (4096 64-bit MFAs maximum)
- 64- and 32-bit MFA sizes
- Three interrupt gathering methods
- Registered MFA prefetch and posting
- 32-bit inbound and outbound doorbell registers
- Four 32-bit scratch pad registers

Serial Ports (UART)

The Universal Asynchronous Receiver/Transmitter (UART) interface provides one 8-signal port, or two 4-signal ports, or four 2-signal ports. The UART performs serial-to-parallel conversion on data received from a peripheral device or a modem, and parallel-to-serial conversion on data received from the processor.

Features include:

- Up to four ports in the following combinations:
  - One 8-pin (UART0)
  - Two 4-pin (UART0 and UART1)
  - Four 2-pin (UART0, UART1, UART2, and UART3)
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with 16750 register set
- Complete status reporting capability
- Fully programmable serial-interface characteristics
- Supports DMA using the 4-channel internal DMA function
- 64-byte FIFOs for buffering transmit and receive data

IIC Bus Controller

The Inter-Integrated Circuit (IIC) interface provides a Philips® I²C™ compatible interface operating up to 400 KHz either as a master, a slave, or both, with a Bootstrap Controller (BSC) included. During chip reset, the Bootstrap Controller can read configuration data from an IIC-compatible memory device (for example, EEPROM). This data can be used to replace the default configuration settings provided by the chip.

Features include:
- Two IIC interfaces
- Support for Philips Semiconductors I²C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocols
- Programmable error recovery
- Port 0 includes an integrated BSC that supports a serial Bootstrap ROM with default override parameters at initialization

Serial Peripheral Controller (SPI/SCP)

The Serial Peripheral Interface (also known as the Serial Communications Port) is a full-duplex, synchronous, character-oriented (byte) port that allows the exchange of data with other serial devices. The SPI is a master on the serial port supporting a 3-wire interface (receive, transmit, and clock), and is a slave on the OPB.

Features include:
- Three-wire serial port interface
- Full-duplex synchronous operation
- SPI bus master
- Programmable clock rate divider
- Clock inversion
- Reverse data
- Local data loop back for test

NAND Flash Controller

The NAND Flash controller provides a simple interface between the EBC and up to four separate external NAND Flash devices. It provides both direct command, address, and data access to the external device as well as a memory-mapped linear region that generates data accesses. NAND Flash data is transferred on the peripheral data bus.

Features include:
- One to four banks supported on EBC
- Direct interface to:
  - Discrete NAND Flash devices (up to four devices)
  - SmartMedia Card socket (22-pins)
- Device sizes:
  - 4MB and larger supported for read/write access
  - 4MB to 256MB supported for boot-from-NAND flash (size supported depends on addressing mode)

- (512 + 16)-B or (2K + 64)-B page sizes supported
- Boot from NAND supported with execution of up to 4KB of boot code out of block 0
- ECC provides single-bit error correction and double-bit error detection in each 256B of stored data
- Chip select pins are multiplexed with EBC

General Purpose Timers (GPT)

Provides a separate time base counter and additional system timers in addition to those defined in the processor.

Features include:
- Time Base Counter (32 bits) driven by the OPB bus clock
- Seven 32-bit compare timers

General Purpose IO (GPIO) Controller

Controller functions and GPIO registers are programmed and accessed by means of memory-mapped OPB bus master accesses.

Features include:
- Sixty-four GPIOs multiplexed with other functions. DCRs control whether a GPIO pin acts as a GPIO or is used for another purpose.
- Each GPIO output is separately programmable to emulate an open drain driver (that is, drives to zero, tri-stated if output bit is 1).

Universal Interrupt Controller (UIC)

Universal Interrupt Controllers (UICs) provide control, status, and communications necessary between the external and internal sources of interrupts and the on-chip PowerPC processor.

Note: Processor specific interrupts (for example, page faults) do not use UIC resources.

Features include:
- Sixteen external interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to the on-chip processor
- Programmable interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

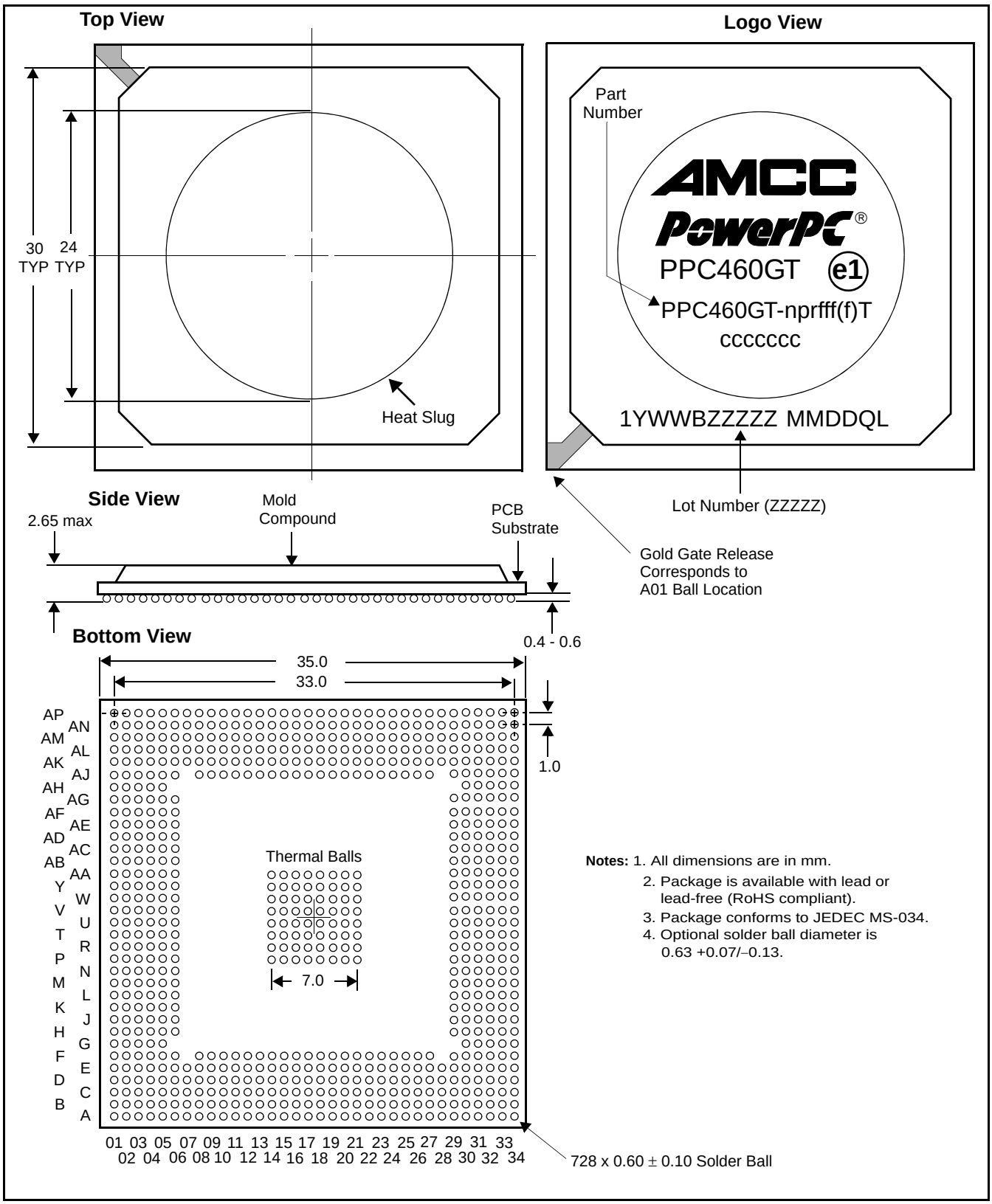
JTAG

Features include:
- IEEE 1149.1 Test Access Port
- JTAG Boundary Scan Description Language (BSDL)
- IBM RISCWatch support

Refer to **http://www.amcc.com/Embedded/Partners** for a list of AMCC partners supplying probes for use with this port.

Package Diagram

Figure 3. 35mm, 728-Ball TE-PBGA Package



Signal Lists

The following table lists all the external signals in alphabetical order and shows the ball (pin) number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and alternate signals in brackets. Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in *Table 7* on page 60 where the signals in the indicated interface group begin. In cases where signals in the same interface group (for example, Ethernet) have different names to distinguish variations in the mode of operation, the names are separated by a comma with the primary mode name appearing first. In cases where the signals have the same function but are associated with different ports (for example, UART), the signals are separated by a slash (/). These signals are listed only once, and appear alphabetically by the primary mode or primary port name.

Alphabetical Signal List

Table 3. Signals Listed Alphabetically (Part 1 of 27)

Signal Name	Ball	Interface Group	Page
AGND	L01		
AGND	L02		
AGND	M04		
AGND	M06		
AGND	P03		
AGND	P04		
AGND	P06		
AGND	R01		
AGND	R02	Power	69
AGND	R06		
AGND	U01		
AGND	U04		
AGND	U05		
AGND	Y01		
AGND	Y03		
AGND	Y05		
AGND	AA04		

Table 3. Signals Listed Alphabetically (Part 2 of 27)

Signal Name	Ball	Interface Group	Page
AV_{DD}	L03	Power	69
AV_{DD}	L06		
AV_{DD}	M03		
AV_{DD}	M05		
AV_{DD}	N03		
AV_{DD}	N06		
AV_{DD}	P05		
AV_{DD}	T03		
AV_{DD}	U02		
AV_{DD}	U03		
AV_{DD}	U06		
AV_{DD}	V03		
AV_{DD}	V06		
AV_{DD}	W03		
AV_{DD}	W06		
AV_{DD}	Y02		
AV_{DD}	Y04		
AV_{DD}	AB04		
BA0	AN32	DDR2/1 SDRAM	62
BA1	AP31		
BA2	AM31		
$\overline{\text{BankSel0}}$	AL28	DDR2/1 SDRAM	62
$\overline{\text{BankSel1}}$	AP29		
$\overline{\text{BankSel2}}$	AM29		
$\overline{\text{BankSel3}}$	AN29		
$\overline{\text{CAS}}$	AL29	DDR2/1 SDRAM	62
ClkEn0	AE29	DDR2/1 SDRAM	62
ClkEn1	AF34		
ClkEn2	AE33		
ClkEn3	AE31		
[DMAAck0]GPIO47[PerAddr06][IRQ14]	C31	DMA	66
[DMAAck1]GPIO44[$\overline{\text{PerCS4}}$][IRQ11]	E21		
[DMAAck2]GPIO31[PerPar1][IRQ8]	A16		
[DMAAck3]GPIO36[$\overline{\text{UART0CTS}}$][UART3Rx]	E31		
[DMAReq0]GPIO46[PerAddr05][IRQ13]	B32		
[DMAReq1]GPIO43[$\overline{\text{PerCS3}}$][$\overline{\text{NFCE3}}$][IRQ10]	A22		
[DMAReq2]GPIO30[PerPar0][IRQ7]	A20		
[DMAReq3]GPIO33[PerPar3][IRQ4]	F13		

Table 3. Signals Listed Alphabetically (Part 3 of 27)

Signal Name	Ball	Interface Group	Page
DM0	P31	DDR2/1 SDRAM	62
DM1	U30		
DM2	V30		
DM3	AB34		
DM4	AM25		
DM5	AP23		
DM6	AN20		
DM7	AM17		
DM8	AD34		
DQS0	P33		
$\overline{\text{DQS0}}$	P32	DDR2/1 SDRAM	62
DQS1	U32		
$\overline{\text{DQS1}}$	U31		
DQS2	W31		
$\overline{\text{DQS2}}$	W32		
DQS3	AA30		
$\overline{\text{DQS3}}$	AA31		
DQS4	AP25		
$\overline{\text{DQS4}}$	AN25		
DQS5	AN22		
$\overline{\text{DQS5}}$	AM22		
DQS6	AM19		
$\overline{\text{DQS6}}$	AL19		
DQS7	AK17		
$\overline{\text{DQS7}}$	AL17		
DQS8	AD32		
$\overline{\text{DQS8}}$	AD33		
$E1OV_{DD}$	Y14	Power	69
$E1OV_{DD}$	AA15		
$E1OV_{DD}$	AD06		
$E1OV_{DD}$	AF02		
$E1OV_{DD}$	AG05		
$E1OV_{DD}$	AJ11		
$E1OV_{DD}$	AK02		
$E1OV_{DD}$	AK08		
$E1OV_{DD}$	AN05		
$E1OV_{DD}$	AN09		
$E2OV_{DD}$	AK13	Power	69
$E2OV_{DD}$	AN16		

Table 3. Signals Listed Alphabetically (Part 4 of 27)

Signal Name	Ball	Interface Group	Page
EAGND	AP12	Power	69
EAVDD	AP11		
ECC0	AC31	DDR2/1 SDRAM	62
ECC1	AC30		
ECC2	AE32		
ECC3	AE34		
ECC4	AC34		
ECC5	AC32		
ECC6	AD31		
ECC7	AD30		
[EOT0/TC0]GPIO48[PerAddr07][IRQ15]	D30	DMA	66
[EOT1/TC1]GPIO45[$\overline{\text{PerCS5}}$][IRQ12]	D21		
[EOT2/TC2]GPIO32[PerPar2][IRQ9]	A14		
[EOT3/TC3]GPIO37[$\overline{\text{UART0RTS}}$][UART3Tx]	D33		
$\overline{\text{ExtReset}}$	F22	External Peripheral	66

Table 3. Signals Listed Alphabetically (Part 5 of 27)

Signal Name	Ball	Interface Group	Page
GMC0CD, GMC1RxClk, RMII1RxEr	AP05		
GMC0CrS, GMC1TxClk, RMII0CrSDV	AL07		
GMC0GTxClk, GMC0TxClk	AN06		
GMC0RxClk, GMC0RxClk	AM07		
GMC0RxD0, GMC0RxD0, RMII0RxD0, SMII0RxD	AL09		
GMC0RxD1, GMC0RxD1, RMII0RxD1, SMII1RxD	AK09		
GMC0RxD2, GMC0RxD2, RMII1RxD0, SMII2RxD	AP08		
GMC0RxD3, GMC0RxD3, RMII1RxD1, SMII3RxD	AJ09		
GMC0RxD4, GMC1RxD0	AN08		
GMC0RxD5, GMC1RxD1	AL08		
GMC0RxD6, GMC1RxD2	AM08		
GMC0RxD7, GMC1RxD3	AP07		
GMC0RxDV, GMC0RxCtl, RMII1CrSDV	AL06	Ethernet 0	63
GMC0RxEr, GMC1RxCtl, RMII0RxEr	AJ10		
GMC0TxClk,, RMII01RefClk, SMIIRefClk	AN04		
GMC0TxD0, GMC0TxD0, RMII0TxD0, SMII0TxD	AM02		
GMC0TxD1, GMC0TxD1, RMII0TxD1, SMII1TxD	AK04		
GMC0TxD2, GMC0TxD2, RMII1TxD0, SMII2TxD	AL02		
GMC0TxD3, GMC0TxD3, RMII1TxD1, SMII3TxD	AL01		
GMC0TxD4, GMC1TxD0	AK03		
GMC0TxD5, GMC1TxD1	AM01		
GMC0TxD6, GMC1TxD2	AH05		
GMC0TxD7, GMC1TxD3	AL03		
GMC0TxEn, GMC0TxCtl, RMII0TxEn, SMIISync	AM05		
GMC0TxEr, GMC1TxCtl, RMII1TxEn	AJ08		

Table 3. Signals Listed Alphabetically (Part 6 of 27)

Signal Name	Ball	Interface Group	Page
[GMC1CD, GMC3RxClk, RMII3RxEr]GPIO17	AG02		
[GMC1CrS, GMC3TxClk, RMII2CrSDV]GPIO20	AG03		
[GMC1GTxClk, GMC2TxClk]	AE06		
[GMC1RxClk, GMC2RxClk]	AF06		
[GMC1RxD0, GMC2RxD0, RMII2RxD0]GPIO08	AH04		
[GMC1RxD1, GMC2RxD1, RMII2RxD1]GPIO09	AJ05		
[GMC1RxD2, GMC2RxD2, RMII3RxD0]GPIO10	AG06		
[GMC1RxD3, GMC2RxD3, RMII3RxD1]GPIO11	AJ02		
[GMC1RxD4, GMC3RxD0]GPIO12	AJ04		
[GMC1RxD5, GMC3RxD1]GPIO13	AH03		
[GMC1RxD6, GMC3RxD2]GPIO14	AJ01		
[GMC1RxD7, GMC3RxD3]GPIO15	AH01		
[GMC1RxDV, GMC2RxCtll, RMII3CrSDV]GPIO21	AD04	Ethernet 1	64
[GMC1RxEr, GMC3RxCtl, RMII2RxEr]GPIO18	AG04		
GMC1TxClk, RMII23RefClk	AC06		
[GMC1TxD0, GMC2TxD0, RMII2TxD0]GPIO00	AG01		
[GMC1TxD1, GMC2TxD1, RMII2TxD1]GPIO01	AD05		
[GMC1TxD2, GMC2TxD2, RMII3TxD0]GPIO02	AE04		
[GMC1TxD3, GMC2TxD3, RMII3TxD1]GPIO03	AF01		
[GMC1TxD4, GMC3TxD0]GPIO04	AE02		
[GMC1TxD5, GMC3TxD1]GPIO05	AE01		
[GMC1TxD6, GMC3TxD2]GPIO06	AB05		
[GMC1TxD7, GMC3TxD3]GPIO07	AD03		
[GMC1TxEn, GMC2TxCtl, RMII2TxEn]GPIO19	AF03		
[GMC1TxEr, GMC3TxCtl, RMII3TxEn]GPIO16	AF04		
GMCMDClk	AJ03		
GMCMDIO	AK01	Ethernet 0	63
GMCRefClk	AP09		

Table 3. Signals Listed Alphabetically (Part 7 of 27)

Signal Name	Ball	Interface Group	Page
GND	A01	Power	69
GND	A02		
GND	A03		
GND	A33		
GND	A34		
GND	B01		
GND	B02		
GND	B03		
GND	B07		
GND	B12		
GND	B23		
GND	B28		
GND	B33		
GND	B34		
GND	C01		
GND	C02		
GND	C03		
GND	C16		
GND	C32		
GND	D04		
GND	D31		
GND	E05		
GND	E10		
GND	E23		
GND	E25		
GND	E28		
GND	E30		
GND	F06		
GND	F16		
GND	F19		
GND	F29		
GND	F30		
GND	F31		
GND	F32		

Table 3. Signals Listed Alphabetically (Part 8 of 27)

Signal Name	Ball	Interface Group	Page
GND	G02		
GND	G31		
GND	G33		
GND	H01		
GND	J01		
GND	J03		
GND	J30		
GND	J32		
GND	K02		
GND	K05		
GND	K06		
GND	K30		
GND	M30		
GND	M33		
GND	P14		
GND	P16		
GND	P19		
GND	P21	Power	69
GND	R15		
GND	R16		
GND	R19		
GND	R20		
GND	T14		
GND	T15		
GND	T16		
GND	T17		
GND	T18		
GND	T19		
GND	T20		
GND	T21		
GND	T30		
GND	U16		
GND	U17		
GND	U18		
GND	U19		

Table 3. Signals Listed Alphabetically (Part 9 of 27)

Signal Name	Ball	Interface Group	Page
GND	V16	Power	69
GND	V17		
GND	V18		
GND	V19		
GND	W14		
GND	W15		
GND	W16		
GND	W17		
GND	W18		
GND	W19		
GND	W20		
GND	W21		
GND	W29		
GND	Y15		
GND	Y16		
GND	Y19		
GND	Y20		
GND	AA14		
GND	AA16		
GND	AA19		
GND	AA21		
GND	AC01		
GND	AC03		
GND	AC04		
GND	AC05		
GND	AC33		
GND	AD01		
GND	AE03		
GND	AE05		
GND	AE30		
GND	AF05		
GND	AF29		
GND	AF30		
GND	AG29		
GND	AH02		
GND	AH33		

Table 3. Signals Listed Alphabetically (Part 10 of 27)

Signal Name	Ball	Interface Group	Page
GND	AJ06	Power	69
GND	AJ13		
GND	AJ16		
GND	AJ23		
GND	AJ25		
GND	AJ26		
GND	AJ27		
GND	AJ29		
GND	AJ30		
GND	AJ31		
GND	AK05		
GND	AK06		
GND	AK07		
GND	AK10		
GND	AK14		
GND	AK19		
GND	AK24		
GND	AK25		
GND	AK28		
GND	AK29		
GND	AK30		
GND	AL04		
GND	AL05		
GND	AL22		
GND	AL25		
GND	AL30		
GND	AL31		
GND	AL32		
GND	AL33		
GND	AL34		
GND	AM03		
GND	AM04		
GND	AM06		
GND	AM10		
GND	AM30		
GND	AM32		

Table 3. Signals Listed Alphabetically (Part 11 of 27)

Signal Name	Ball	Interface Group	Page
GND	AN01		
GND	AN02		
GND	AN03		
GND	AN07		
GND	AN12		
GND	AN23		
GND	AN28		
GND	AN31		
GND	AN33		
GND	AN34	Power	69
GND	AP01		
GND	AP02		
GND	AP03		
GND	AP04		
GND	AP06		
GND	AP16		
GND	AP17		
GND	AP33		
GND	AP34		

Table 3. Signals Listed Alphabetically (Part 12 of 27)

Signal Name	Ball	Interface Group	Page
GPIO00[GMC1TxD0, GMC2TxD0, RMII2TxD0]	AG01	System	68
GPIO01[GMC1TxD1, GMC2TxD1, RMII2TxD1]	AD05		
GPIO02[GMC1TxD2, GMC2TxD2, RMII3TxD0]	AE04		
GPIO03[GMC1TxD3, GMC2TxD3, RMII3TxD1]	AF01		
GPIO04[GMC1TxD4, GMC3TxD0]	AE02		
GPIO05[GMC1TxD5, GMC3TxD1]	AE01		
GPIO06[GMC1TxD6, GMC3TxD2]	AB05		
GPIO07[GMC1TxD7, GMC3TxD3]	AD03		
GPIO08[GMC1RxD0, GMC2RxD0, RMII2RxD0]	AH04		
GPIO09[GMC1RxD1, GMC2RxD1, RMII2RxD1]	AJ05		
GPIO10[GMC1RxD2, GMC2RxD2, RMII3RxD0]	AG06		
GPIO11[GMC1RxD3, GMC2RxD3, RMII3RxD1]	AJ02		
GPIO12[GMC1RxD4, GMC3RxD0]	AJ04		
GPIO13[GMC1RxD5, GMC3RxD1]	AH03		
GPIO14[GMC1RxD6, GMC3RxD2]	AJ01		
GPIO15[GMC1RxD7, GMC3RxD3]	AH01		
GPIO16[GMC1TxEr, GMC3TxCtl, RMII3TxEn]	AF04		
GPIO17[GMC1CD, GMC3RxClk, RMII3RxEr]	AG02		
GPIO18[GMC1RxEr, GMC3RxCtl, RMII2RxEr]	AG04		
GPIO19[GMC1TxEn, GMC2TxCtl, RMII2TxEn]	AF03		
GPIO20[GMC1CrS, GMC3TxClk, RMII2CrSDV]	AG03		
GPIO21[GMC1RxDV, GMC2RxCtl, RMII3CrSDV]	AD04		
GPIO22[$\overline{\text{NFRdyBusy}}$]	C24		
GPIO23[$\overline{\text{NFREn}}$]	B24		
GPIO24[$\overline{\text{NFWEn}}$]	A24		
GPIO25[NFCLE]	F26		
GPIO26[NFALE]	A25		
GPIO27[IRQ0]	D12		
GPIO28[IRQ1]	E12		
GPIO29[IRQ2]	F12		
GPIO30[PerPar0][DMAReq2][IRQ7]	A20		
GPIO31[PerPar1][DMAAck2][IRQ8]	A16		

Table 3. Signals Listed Alphabetically (Part 13 of 27)

Signal Name	Ball	Interface Group	Page
GPIO32[PerPar2][EOT2/TC2][IRQ9]	A14	System	68
GPIO33[PerPar3][DMAReq3][IRQ4]	F13		
GPIO34[$\overline{\text{UART0DCD}}$][$\overline{\text{UART1CTS}}$][UART2Tx]	E34		
GPIO35[$\overline{\text{UART0DSR}}$][$\overline{\text{UART1RTS}}$][UART2Rx]	E32		
GPIO36[$\overline{\text{UART0CTS}}$][DMAAck3][UART3Rx]	E31		
GPIO37[$\overline{\text{UART0RTS}}$][EOT3/TC3][UART3Tx]	D33		
GPIO38[$\overline{\text{UART0DTR}}$][UART1Tx][IRQ5]	D32		
GPIO39[$\overline{\text{UART0RI}}$][UART1Rx][IRQ6]	D34		
GPIO40[IRQ3]	C12		
GPIO41[$\overline{\text{PerCS1}}$][$\overline{\text{NFCE1}}$]	B22		
GPIO42[$\overline{\text{PerCS2}}$][$\overline{\text{NFCE2}}$]	D25		
GPIO43[$\overline{\text{PerCS3}}$][$\overline{\text{NFCE3}}$][DMAReq1][IRQ10]	A22		
GPIO44[$\overline{\text{PerCS4}}$][DMAAck1][IRQ11]	E21		
GPIO45[$\overline{\text{PerCS5}}$][EOT1/TC1][IRQ12]	D21		
GPIO46[PerAddr05][DMAReq0][IRQ13]	B32		
GPIO47[PerAddr06][DMAAck0][IRQ14]	C31		
GPIO48[PerAddr07][EOT0/TC0][IRQ15]	D30		
GPIO49[TrcBS0]	H33		
GPIO50[TrcBS1]	J34		
GPIO51[TrcBS2]	H34		
GPIO52[TrcES0]	L30		
GPIO53[TrcES1]	L31		
GPIO54[TrcES2]	K33		
GPIO55[TrcES3]	L32		
GPIO56[TrcES4]	K34		
GPIO57[TrcTS0]	L33		
GPIO58[TrcTS1]	N29		
GPIO59[TrcTS2]	M31		
GPIO60[TrcTS3]	L34		
GPIO61[TrcTS4]	M32		
GPIO62[TrcTS5]	M34		
GPIO63[TrcTS6]	N31		
$\overline{\text{Halt}}$	H32	System	68
$\overline{\text{HISRRst}}$	B11	DDR2/1 SDRAM	62
IIC0SClk	J31	IIC Peripheral	67
IIC0SData	H31		
[IIC1SClk]SPIClkOut	K31		
[IIC1SData]SPIDO	G34		

Table 3. Signals Listed Alphabetically (Part 14 of 27)

Signal Name	Ball	Interface Group	Page
[IRQ0]GPIO27	D12	Interrupt	67
[IRQ1]GPIO28	E12		
[IRQ2]GPIO29	F12		
[IRQ3]GPIO40	C12		
[IRQ4]GPIO33[PerPar3][DMAReq3]	F13		
[IRQ5]GPIO38[$\overline{\text{UART0DTR}}$][UART1Tx]	D32		
[IRQ6]GPIO39[$\overline{\text{UART0RI}}$][UART1Rx]	D34		
[IRQ7]GPIO30[PerPar0][DMAReq2]	A20		
[IRQ8]GPIO31[PerPar1][DMAAck2]	A16		
[IRQ9]GPIO32[PerPar2][EOT2/TC2]	A14		
[IRQ10]GPIO43[$\overline{\text{PerCS3}}$][$\overline{\text{NFCE3}}$][DMAReq1]	A22		
[IRQ11]GPIO44[$\overline{\text{PerCS4}}$][DMAAck1]	E21		
[IRQ12]GPIO45[$\overline{\text{PerCS5}}$][EOT1/TC1]	D21		
[IRQ13]GPIO46[PerAddr05][DMAReq0]	B32		
[IRQ14]GPIO47[PerAddr06][DMAAck0]	C31		
[IRQ15]GPIO48[PerAddr07][EOT0/TC0]	D30		
MemAddr00	AK34	DDR2/1 SDRAM	62
MemAddr01	AJ33		
MemAddr02	AJ32		
MemAddr03	AJ34		
MemAddr04	AH30		
MemAddr05	AH31		
MemAddr06	AH32		
MemAddr07	AG31		
MemAddr08	AH34		
MemAddr09	AG32		
MemAddr10	AG33		
MemAddr11	AF31		
MemAddr12	AG34		
MemAddr13	AC29		
MemAddr14	AF32		
MemClkOut0	AP27	DDR2/1 SDRAM	62
$\overline{\text{MemClkOut0}}$	AN27		
MemClkOut1	AK31		
$\overline{\text{MemClkOut1}}$	AK32		

Table 3. Signals Listed Alphabetically (Part 15 of 27)

Signal Name	Ball	Interface Group	Page
MemData00	P30	DDR2/1 SDRAM	62
MemData01	N34		
MemData02	R32		
MemData03	R30		
MemData04	N33		
MemData05	N32		
MemData06	P34		
MemData07	R31		
MemData08	R34		
MemData09	T34		
MemData10	V34		
MemData11	T32		
MemData12	R33		
MemData13	T31		
MemData14	U33		
MemData15	U34		
MemData16	V32		
MemData17	V31		
MemData18	Y32		
MemData19	W30		
MemData20	V33		
MemData21	W34		
MemData22	Y34		
MemData23	Y33		
MemData24	AA33		
MemData25	AA32		
MemData26	AB31		
MemData27	Y30		
MemData28	AA34		
MemData29	Y31		
MemData30	AB33		
MemData31	AB32		

Table 3. Signals Listed Alphabetically (Part 16 of 27)

Signal Name	Ball	Interface Group	Page
MemData32	AM26	DDR2/1 SDRAM	62
MemData33	AP26		
MemData34	AK21		
MemData35	AN24		
MemData36	AL26		
MemData37	AK26		
MemData38	AL24		
MemData39	AM24		
MemData40	AL23		
MemData41	AM23		
MemData42	AM21		
MemData43	AN21		
MemData44	AK23		
MemData45	AP24		
MemData46	AP22		
MemData47	AL21		
MemData48	AL20		
MemData49	AM20		
MemData50	AL18		
MemData51	AM18		
MemData52	AK20		
MemData53	AP21		
MemData54	AP20		
MemData55	AP19		
MemData56	AP18		
MemData57	AN17		
MemData58	AL16		
MemData59	AP15		
MemData60	AK18		
MemData61	AN18		
MemData62	AM16		
MemData63	AK16		
MemDCFdbkD	AM33	DDR2/1 SDRAM	62
MemDCFdbkR	AM34		
MemODT0	AP28	DDR2/1 SDRAM	62
MemODT1	AM27		
MemODT2	AM28		
MemODT3	AL27		

Table 3. Signals Listed Alphabetically (Part 17 of 27)

Signal Name	Ball	Interface Group	Page
MemVRef1A	AJ19	DDR2/1 SDRAM	62
MemVRef1B	AB29		
MemVRef2A	AJ22		
MemVRef2B	T29		
[NFALE]GPIO26	A25	NAND Flash	67
[$\overline{\text{NFCE0}}$]$\overline{\text{PerCS0}}$	E24		
[$\overline{\text{NFCE1}}$]GPIO41[$\overline{\text{PerCS1}}$]	B22		
[$\overline{\text{NFCE2}}$]GPIO42[$\overline{\text{PerCS2}}$]	D25		
[$\overline{\text{NFCE3}}$]GPIO43[$\overline{\text{PerCS3}}$][DMAReq1][IRQ10]	A22		
[NFCLE]GPIO25	F26		
[$\overline{\text{NFRdyBusy}}$]GPIO22	C24		
[$\overline{\text{NFREn}}$]GPIO23	B24		
[$\overline{\text{NFWEn}}$]GPIO24	A24		
OV_{DD}	B05	Power	69
OV_{DD}	B09		
OV_{DD}	B16		
OV_{DD}	B19		
OV_{DD}	B26		
OV_{DD}	B30		
OV_{DD}	E02		
OV_{DD}	E08		
OV_{DD}	E13		
OV_{DD}	E22		
OV_{DD}	E27		
OV_{DD}	E33		
OV_{DD}	F11		
OV_{DD}	F24		
OV_{DD}	H05		
OV_{DD}	H30		
OV_{DD}	J02		
OV_{DD}	J33		
OV_{DD}	L29		
OV_{DD}	P15		
OV_{DD}	P20		
OV_{DD}	R14		
OV_{DD}	R21		
PAV_{DD}	T06	Power	69
PAV_{DD}	AA05		

Table 3. Signals Listed Alphabetically (Part 18 of 27)

Signal Name	Ball	Interface Group	Page
PCI0AD00	D11	PCI	60
PCI0AD01	E11		
PCI0AD02	B10		
PCI0AD03	A10		
PCI0AD04	C10		
PCI0AD05	F10		
PCI0AD06	D10		
PCI0AD07	A09		
PCI0AD08	D09		
PCI0AD09	A08		
PCI0AD10	F09		
PCI0AD11	B08		
PCI0AD12	C08		
PCI0AD13	D08		
PCI0AD14	A07		
PCI0AD15	F08		
PCI0AD16	A05		
PCI0AD17	A04		
PCI0AD18	D05		
PCI0AD19	B04		
PCI0AD20	D02		
PCI0AD21	F04		
PCI0AD22	E03		
PCI0AD23	D03		
PCI0AD24	E01		
PCI0AD25	E04		
PCI0AD26	G05		
PCI0AD27	G04		
PCI0AD28	F02		
PCI0AD29	H06		
PCI0AD30	F01		
PCI0AD31	F05		
$\overline{\text{PCI0C/BE0}}$	C09	PCI	60
$\overline{\text{PCI0C/BE1}}$	C07		
$\overline{\text{PCI0C/BE2}}$	C05		
$\overline{\text{PCI0C/BE3}}$	F03		
PCI0Clk	K01	PCI	60
$\overline{\text{PCI0DevSel}}$	A06		
$\overline{\text{PCI0Frame}}$	E06		

Table 3. Signals Listed Alphabetically (Part 19 of 27)

Signal Name	Ball	Interface Group	Page
PCI0Gnt0/Req	G03	PCI	60
PCI0Gnt1	H04		
PCI0Gnt2	G01		
PCI0Gnt3	H03		
PCI0IDSel	D01	PCI	60
PCI0Int	J04		
PCI0IRdy	C04		
PCI0M66En	E09		
PCI0Par	D07		
PCI0PErr	B06		
PCI0Req0/Gnt	J06	PCI	60
PCI0Req1	H02		
PCI0Req2	K04		
PCI0Req3	J05		
PCI0Reset	K03	PCI	60
PCI0SErr	E07		
PCI0Stop	C06		
PCI0TRdy	D06		
PCIE0AVReg	AA01	PCI Express 0	61
PCIE0CalRN	AB02		
PCIE0CalRP	AB01		
PCIE0RefClk	AA02		
PCIE0RefClk	AA03		
PCIE0Rx0	W04		
PCIE0Rx0	W05		
PCIE0Tx0	W02		
PCIE0Tx0	W01		

Table 3. Signals Listed Alphabetically (Part 20 of 27)

Signal Name	Ball	Interface Group	Page
PCIE1AVReg[SRIO0AVReg]	R05	PCI Express 1	61
PCIE1CalRN[SRIO0CalRN]	P01		
PCIE1CalRP[SRIO0CalRP]	P02		
PCIE1RefClk[SRIO0RefClk]	R04		
$\overline{\text{PCIE1RefClk}}$[$\overline{\text{SRIO0RefClk}}$]	R03		
PCIE1Rx0[SRIO0Rx0]	L05	PCI Express 1	61
$\overline{\text{PCIE1Rx0}}$[$\overline{\text{SRIO0Rx0}}$]	L04		
PCIE1Rx1[SRIO0Rx1]	N05		
$\overline{\text{PCIE1Rx1}}$[$\overline{\text{SRIO0Rx1}}$]	N04		
PCIE1Rx2[SRIO0Rx2]	T04		
$\overline{\text{PCIE1Rx2}}$[$\overline{\text{SRIO0Rx2}}$]	T05		
PCIE1Rx3[SRIO0Rx3]	V05		
$\overline{\text{PCIE1Rx3}}$[$\overline{\text{SRIO0Rx3}}$]	V04		
PCIE1Tx0[SRIO0Tx0]	M02	PCI Express 1	61
$\overline{\text{PCIE1Tx0}}$[$\overline{\text{SRIO0Tx0}}$]	M01		
PCIE1Tx1[SRIO0Tx1]	N02		
$\overline{\text{PCIE1Tx1}}$[$\overline{\text{SRIO0Tx1}}$]	N01		
PCIE1Tx2[SRIO0Tx2]	T02		
$\overline{\text{PCIE1Tx2}}$[$\overline{\text{SRIO0Tx2}}$]	T01		
$\overline{\text{PCIE1Tx3}}$[$\overline{\text{SRIO0Tx3}}$]	V02		
PCIE1Tx3[SRIO0Tx3]	V01		

Table 3. Signals Listed Alphabetically (Part 21 of 27)

Signal Name	Ball	Interface Group	Page
[PerAddr05]GPIO46[DMAReq0][IRQ13]	B32	External Peripheral	66
[PerAddr06]GPIO47[DMAAck0][IRQ14]	C31		
[PerAddr07]GPIO48[EOT0/TC0][IRQ15]	D30		
PerAddr08	A32		
PerAddr09	E29		
PerAddr10	C30		
PerAddr11	B31		
PerAddr12	A30		
PerAddr13	A31		
PerAddr14	D29		
PerAddr15	C29		
PerAddr16	A29		
PerAddr17	D28		
PerAddr18	C28		
PerAddr19	B29		
PerAddr20	C27		
PerAddr21	A28		
PerAddr22	D26		
PerAddr23	F27		
PerAddr24	B27		
PerAddr25	D27		
PerAddr26	A27		
PerAddr27	C26		
PerAddr28	A26		
PerAddr29	C25		
PerAddr30	B25		
PerAddr31	D24		
$\overline{\text{PerBLast}}$	F25	External Peripheral	66
PerClk	F23	External Peripheral	66
$\overline{\text{PerCS0}}$[$\overline{\text{NFCE0}}$]	E24	External Peripheral	66
[$\overline{\text{PerCS1}}$]GPIO41[$\overline{\text{NFCE1}}$]	B22		
[$\overline{\text{PerCS2}}$]GPIO42[$\overline{\text{NFCE2}}$]	D25		
[$\overline{\text{PerCS3}}$]GPIO43[$\overline{\text{NFCE3}}$][DMAReq1][IRQ10]	A22		
[$\overline{\text{PerCS4}}$]GPIO44[DMAAck1][IRQ11]	E21		
[$\overline{\text{PerCS5}}$]GPIO45[EOT1/TC1][IRQ12]	D21		

Table 3. Signals Listed Alphabetically (Part 22 of 27)

Signal Name	Ball	Interface Group	Page
PerData00	C21	External Peripheral	66
PerData01	B21		
PerData02	A21		
PerData03	E20		
PerData04	D20		
PerData05	C20		
PerData06	D18		
PerData07	B20		
PerData08	E19		
PerData09	D19		
PerData10	E18		
PerData11	C19		
PerData12	A19		
PerData13	C18		
PerData14	B18		
PerData15	A18		
PerData16	D17		
PerData17	B17		
PerData18	A15		
PerData19	B15		
PerData20	E15		
PerData21	C15		
PerData22	D16		
PerData23	D15		
PerData24	E16		
PerData25	C14		
PerData26	E14		
PerData27	D14		
PerData28	B14		
PerData29	A13		
PerData30	B13		
PerData31	C13		
[PerPar0]GPIO30[DMAReq2][IRQ7]	A20	External Peripheral	66
[PerPar1]GPIO31[DMAAck2][IRQ8]	A16		
[PerPar2]GPIO32[EOT2/TC2][IRQ9]	A14		
[PerPar3]GPIO33[DMAReq3][IRQ4]	F13		
PerErr	D13	External Peripheral	66
$\overline{\text{PerOE}}$	E26	External Peripheral	66
PerR/$\overline{\text{W}}$	D23	External Peripheral	66

Table 3. Signals Listed Alphabetically (Part 23 of 27)

Signal Name	Ball	Interface Group	Page
PerReady	C17	External Peripheral	66
$\overline{\text{PerWBE0}}$	C23	External Peripheral	66
$\overline{\text{PerWBE1}}$	A23		
$\overline{\text{PerWBE2}}$	D22		
$\overline{\text{PerWBE3}}$	C22		
$\overline{\text{RAS}}$	AP30	DDR2/1 SDRAM	62
Reserved	A17	Other	68
Reserved	E17		
Reserved	AM15		
Reserved	AN15		
SGMII0RxClk	AK15	Ethernet SGMII 0	65
$\overline{\text{SGMII0RxClk}}$	AL15		
SGMII0RxD	AN14		
$\overline{\text{SGMII0RxD}}$	AP14		
SGMII0TxD	AM11		
$\overline{\text{SGMII0TxD}}$	AN11		
SGMII1RxClk	AL14	Ethernet SGMII 1	65
$\overline{\text{SGMII1RxClk}}$	AM14		
SGMII1RxD	AN13		
$\overline{\text{SGMII1RxD}}$	AP13		
SGMII1TxD	AK11		
$\overline{\text{SGMII1TxD}}$	AL11		
SGMII2RxClk	AL13	Ethernet SGMII 2	65
$\overline{\text{SGMII2RxClk}}$	AM13		
SGMII2RxD	AL12		
$\overline{\text{SGMII2RxD}}$	AM12		
SGMII2TxD	AP10		
$\overline{\text{SGMII2TxD}}$	AN10		
SGMIITxClk	AJ12		
$\overline{\text{SGMIITxClk}}$	AK12		

Table 3. Signals Listed Alphabetically (Part 24 of 27)

Signal Name	Ball	Interface Group	Page
SOV_{DD}	N30	Power	69
SOV_{DD}	T33		
SOV_{DD}	W33		
SOV_{DD}	Y21		
SOV_{DD}	AA20		
SOV_{DD}	AB30		
SOV_{DD}	AD29		
SOV_{DD}	AF33		
SOV_{DD}	AG30		
SOV_{DD}	AJ24		
SOV_{DD}	AK22		
SOV_{DD}	AK27		
SOV_{DD}	AK33		
SOV_{DD}	AN19		
SOV_{DD}	AN26		
SOV_{DD}	AN30		
SPAGND	A11	Power	69
$SPAV_{DD}$	A12		
SPIClkOut[IIC1SClk]	K31	Serial Peripheral	67
SPIDI	K32		
SPIDO[IIC1SData]	G34		

Table 3. Signals Listed Alphabetically (Part 25 of 27)

Signal Name	Ball	Interface Group	Page
[SRIO0AVReg]PCIE1AVReg	R05	Serial Rapid IO	65
[SRIO0CalRN]PCIE1CalRN	P01		
[SRIO0CalRP]PCIE1CalRP	P02		
[SRIO0RefClk]PCIE1RefClk	R04		
[$\overline{\text{SRIO0RefClk}}$]$\overline{\text{PCIE1RefClk}}$	R03		
[SRIO0Rx0]PCIE1Rx0	L05		
[$\overline{\text{SRIO0Rx0}}$]$\overline{\text{PCIE1Rx0}}$	L04		
[SRIO0Rx1]PCIE1Rx1	N05		
[$\overline{\text{SRIO0Rx1}}$]$\overline{\text{PCIE1Rx1}}$	N04		
[SRIO0Rx2]PCIE1Rx2	T04		
[$\overline{\text{SRIO0Rx2}}$]$\overline{\text{PCIE1Rx2}}$	T05		
[SRIO0Rx3]PCIE1Rx3	V05		
[$\overline{\text{SRIO0Rx3}}$]$\overline{\text{PCIE1Rx3}}$	V04		
[SRIO0Tx0]PCIE1Tx0	M02		
[$\overline{\text{SRIO0Tx0}}$]$\overline{\text{PCIE1Tx0}}$	M01		
[SRIO0Tx1]PCIE1Tx1	N02		
[$\overline{\text{SRIO0Tx1}}$]$\overline{\text{PCIE1Tx1}}$	N01		
[SRIO0Tx2]PCIE1Tx2	T02		
[$\overline{\text{SRIO0Tx2}}$]$\overline{\text{PCIE1Tx2}}$	T01		
[SRIO0Tx3]PCIE1Tx3	V02		
[$\overline{\text{SRIO0Tx3}}$]$\overline{\text{PCIE1Tx3}}$	V01		
SysClk	AD02	System	68
SysErr	AB03		
$\overline{\text{SysReset}}$	AC02		
TCK	J29	JTAG	68
TDI	F34		
TDO	F33		
TestEn	K29	System	68
TherMonA	AM09		
TherMonB	AL10		
TmrClk	C11	System	68
TMS	G32	JTAG	68
[TrcBS0]GPIO49	H33	Trace	68
[TrcBS1]GPIO50	J34		
[TrcBS2]GPIO51	H34		

Table 3. Signals Listed Alphabetically (Part 26 of 27)

Signal Name	Ball	Interface Group	Page
TrcClk	M29	Trace	68
[TrcES0]GPIO52	L30		
[TrcES1]GPIO53	L31		
[TrcES2]GPIO54	K33		
[TrcES3]GPIO55	L32		
[TrcES4]GPIO56	K34		
[TrcTS0]GPIO57	L33	Trace	68
[TrcTS1]GPIO58	N29		
[TrcTS2]GPIO59	M31		
[TrcTS3]GPIO60	L34		
[TrcTS4]GPIO61	M32		
[TrcTS5]GPIO62	M34		
[TrcTS6]GPIO63	N31		
$\overline{\text{TRST}}$	H29	JTAG	68
UARTSerClk	G30		
[$\overline{\text{UART0CTS}}$]GPIO36[DMAAck3][UART3Rx]	E31	UART Peripheral	67
[$\overline{\text{UART0DCD}}$]GPIO34[$\overline{\text{UART1CTS}}$][UART2Tx]	E34		
[$\overline{\text{UART0DSR}}$]GPIO35[$\overline{\text{UART1RTS}}$][UART2Rx]	E32		
[$\overline{\text{UART0DTR}}$]GPIO38[UART1Tx][IRQ5]	D32		
[$\overline{\text{UART0RI}}$]GPIO39[UART1Rx][IRQ6]	D34		
[$\overline{\text{UART0RTS}}$]GPIO37[EOT3/TC3][UART3Tx]	D33		
UART0Rx	C34		
UART0Tx	C33		
[$\overline{\text{UART1CTS}}$][$\overline{\text{UART0DCD}}$]GPIO34[UART2Tx]	E34	UART Peripheral	67
[$\overline{\text{UART1RTS}}$][$\overline{\text{UART0DSR}}$]GPIO35[UART2Rx]	E32		
[UART1Rx][$\overline{\text{UART0RI}}$]GPIO39[IRQ6]	D34		
[UART1Tx][$\overline{\text{UART0DTR}}$]GPIO38[IRQ5]	D32		
[UART2Rx][$\overline{\text{UART0DSR}}$]GPIO35[$\overline{\text{UART1RTS}}$]	E32		
[UART2Tx][$\overline{\text{UART0DCD}}$]GPIO34[$\overline{\text{UART1CTS}}$]	E34		
[UART3Rx][$\overline{\text{UART0CTS}}$]GPIO36[DMAAck3]	E31		
[UART3Tx][$\overline{\text{UART0RTS}}$]GPIO37[EOT3/TC3]	D33		

Table 3. Signals Listed Alphabetically (Part 27 of 27)

Signal Name	Ball	Interface Group	Page
V_{DD}	F14	Power	69
V_{DD}	F15		
V_{DD}	F17		
V_{DD}	F18		
V_{DD}	F20		
V_{DD}	F21		
V_{DD}	P17		
V_{DD}	P18		
V_{DD}	P29		
V_{DD}	R17		
V_{DD}	R18		
V_{DD}	R29		
V_{DD}	U14		
V_{DD}	U15		
V_{DD}	U20		
V_{DD}	U21		
V_{DD}	U29		
V_{DD}	V14		
V_{DD}	V15		
V_{DD}	V20		
V_{DD}	V21		
V_{DD}	V29		
V_{DD}	Y06		
V_{DD}	Y17		
V_{DD}	Y18		
V_{DD}	Y29		
V_{DD}	AA06	Power	69
V_{DD}	AA17		
V_{DD}	AA18		
V_{DD}	AA29		
V_{DD}	AB06		
V_{DD}	AJ14		
V_{DD}	AJ15		
V_{DD}	AJ17		
V_{DD}	AJ18		
V_{DD}	AJ20		
V_{DD}	AJ21		
$\overline{WE}$	AP32	DDR2/1 SDRAM	62

Signals in Ball Assignment Order

In the following table, only the default signal name is shown for each ball. Multiplexed or multifunction signals are marked with an asterisk (*). To determine what other signals or functions can be programmed to those balls, look up the default signal name in *Table 3* on page 21.

Table 4. Signals Listed by Ball Assignment (Part 1 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	GND	B01	GND	C01	GND	D01	PCI0IDSel
A02	GND	B02	GND	C02	GND	D02	PCI0AD20
A03	GND	B03	GND	C03	GND	D03	PCI0AD23
A04	PCI0AD17	B04	PCI0AD19	C04	$\overline{\text{PCI0IRdy}}$	D04	GND
A05	PCI0AD16	B05	OV_{DD}	C05	$\overline{\text{PCI0/CBE2}}$	D05	PCI0AD18
A06	$\overline{\text{PCI0DevSel}}$	B06	$\overline{\text{PCI0PErr}}$	C06	$\overline{\text{PCI0Stop}}$	D06	$\overline{\text{PCI0TRdy}}$
A07	PCI0AD14	B07	GND	C07	$\overline{\text{PCI0C/BE1}}$	D07	PCI0Par
A08	PCI0AD09	B08	PCI0AD11	C08	PCI0AD12	D08	PCI0AD13
A09	PCI0AD07	B09	OV_{DD}	C09	$\overline{\text{PCI0C/BE0}}$	D09	PCI0AD08
A10	PCI0AD03	B10	PCI0AD02	C10	PCI0AD04	D10	PCI0AD06
A11	SPAGND	B11	$\overline{\text{HISRRst}}$	C11	TmrClk	D11	PCI0AD00
A12	$SPAV_{DD}$ *	B12	GND	C12	GPIO40 *	D12	GPIO27 *
A13	PerData29	B13	PerData30	C13	PerData31	D13	PerErr
A14	GPIO32 *	B14	PerData28	C14	PerData25	D14	PerData27
A15	PerData18	B15	PerData19	C15	PerData21	D15	PerData23
A16	GPIO31 *	B16	OV_{DD}	C16	GND	D16	PerData22
A17	Reserved	B17	PerData17	C17	PerReady	D17	PerData16
A18	PerData15	B18	PerData14	C18	PerData13	D18	PerData06
A19	PerData12	B19	OV_{DD}	C19	PerData11	D19	PerData09
A20	GPIO30 *	B20	PerData07	C20	PerData05	D20	PerData04
A21	PerData02	B21	PerData01	C21	PerData00	D21	GPIO45 *
A22	GPIO43 *	B22	GPIO41 *	C22	$\overline{\text{PerWBE3}}$	D22	$\overline{\text{PerWBE2}}$
A23	$\overline{\text{PerWBE1}}$	B23	GND	C23	$\overline{\text{PerWBE0}}$	D23	PerR/$\overline{\text{W}}$
A24	GPIO24 *	B24	GPIO23 *	C24	GPIO22 *	D24	PerAddr31
A25	GPIO26 *	B25	PerAddr30	C25	PerAddr29	D25	GPIO42 *
A26	PerAddr28	B26	OV_{DD}	C26	PerAddr27	D26	PerAddr22
A27	PerAddr26	B27	PerAddr24	C27	PerAddr20	D27	PerAddr25
A28	PerAddr21	B28	GND	C28	PerAddr18	D28	PerAddr17
A29	PerAddr16	B29	PerAddr19	C29	PerAddr15	D29	PerAddr14
A30	PerAddr12	B30	OV_{DD}	C30	PerAddr10	D30	GPIO48 *
A31	PerAddr13	B31	PerAddr11	C31	GPIO47 *	D31	GND
A32	PerAddr08	B32	GPIO46 *	C32	GND	D32	GPIO38 *
A33	GND	B33	GND	C33	UART0Tx	D33	GPIO37 *
A34	GND	B34	GND	C34	UART0Rx	D34	GPIO39 *

Table 4. Signals Listed by Ball Assignment (Part 2 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	PCI0AD24	F01	PCI0AD30	G01	$\overline{\text{PCI0Gnt2}}$	H01	GND
E02	OV_{DD}	F02	PCI0AD28	G02	GND	H02	$\overline{\text{PCI0Req1}}$
E03	PCI0AD22	F03	$\overline{\text{PCI0C/BE3}}$	G03	$\overline{\text{PCI0Gnt0}}/\overline{\text{Req}}$	H03	$\overline{\text{PCI0Gnt3}}$
E04	PCI0AD25	F04	PCI0AD21	G04	PCI0AD27	H04	$\overline{\text{PCI0Gnt1}}$
E05	GND	F05	PCI0AD31	G05	PCI0AD26	H05	OV_{DD}
E06	$\overline{\text{PCI0Frame}}$	F06	GND	G06	No ball	H06	PCI0AD29
E07	$\overline{\text{PCI0SErr}}$	F07	No ball	G07	No Ball	H07	No Ball
E08	OV_{DD}	F08	PCI0AD15	G08	No Ball	H08	No Ball
E09	PCI0M66En	F09	PCI0AD10	G09	No Ball	H09	No Ball
E10	GND	F10	PCI0AD05	G10	No Ball	H10	No Ball
E11	PCI0AD01	F11	OV_{DD}	G11	No Ball	H11	No Ball
E12	GPIO28 *	F12	GPIO29 *	G12	No Ball	H12	No Ball
E13	OV_{DD}	F13	GPIO33 *	G13	No Ball	H13	No Ball
E14	PerData26	F14	V_{DD}	G14	No Ball	H14	No Ball
E15	PerData20	F15	V_{DD}	G15	No Ball	H15	No Ball
E16	PerData24	F16	GND	G16	No Ball	H16	No Ball
E17	Reserved	F17	V_{DD}	G17	No Ball	H17	No Ball
E18	PerData10	F18	V_{DD}	G18	No Ball	H18	No Ball
E19	PerData08	F19	GND	G19	No Ball	H19	No Ball
E20	PerData03	F20	V_{DD}	G20	No Ball	H20	No Ball
E21	GPIO44 *	F21	V_{DD}	G21	No Ball	H21	No Ball
E22	OV_{DD}	F22	$\overline{\text{ExtReset}}$	G22	No Ball	H22	No Ball
E23	GND	F23	PerClk	G23	No Ball	H23	No Ball
E24	$\overline{\text{PerCS0}}$	F24	OV_{DD}	G24	No Ball	H24	No Ball
E25	GND	F25	$\overline{\text{PerBLast}}$	G25	No Ball	H25	No Ball
E26	$\overline{\text{PerOE}}$	F26	GPIO25 *	G26	No Ball	H26	No Ball
E27	OV_{DD}	F27	PerAddr23	G27	No Ball	H27	No Ball
E28	GND	F28	No ball	G28	No Ball	H28	No Ball
E29	PerAddr09	F29	GND	G29	No ball	H29	$\overline{\text{TRST}}$
E30	GND	F30	GND	G30	UARTSerClk	H30	OV_{DD}
E31	GPIO36 *	F31	GND	G31	GND	H31	IIC0SData
E32	GPIO35 *	F32	GND	G32	TMS	H32	$\overline{\text{Halt}}$
E33	OV_{DD}	F33	TDO	G33	GND	H33	GPIO49 *
E34	GPIO34 *	F34	TDI	G34	SPIDO *	H34	GPIO51 *

Table 4. Signals Listed by Ball Assignment (Part 3 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	GND	K01	PCI0Clk	L01	AGND	M01	$\overline{\text{PCIE1Tx0}}$
J02	OV_{DD}	K02	GND	L02	AGND	M02	PCIE1Tx0
J03	GND	K03	$\overline{\text{PCI0Reset}}$	L03	AV_{DD}	M03	AV_{DD}
J04	$\overline{\text{PCI0Int}}$	K04	$\overline{\text{PCI0Req2}}$	L04	$\overline{\text{PCIE1Rx0}}$	M04	AGND
J05	$\overline{\text{PCI0Req3}}$	K05	GND	L05	PCIE1Rx0	M05	AV_{DD}
J06	$\overline{\text{PCI0Req0}}$/$\overline{\text{Gnt}}$	K06	GND	L06	AV_{DD}	M06	AGND
J07	No Ball	K07	No Ball	L07	No Ball	M07	No Ball
J08	No Ball	K08	No Ball	L08	No Ball	M08	No Ball
J09	No Ball	K09	No Ball	L09	No Ball	M09	No Ball
J10	No Ball	K10	No Ball	L10	No Ball	M10	No Ball
J11	No Ball	K11	No Ball	L11	No Ball	M11	No Ball
J12	No Ball	K12	No Ball	L12	No Ball	M12	No Ball
J13	No Ball	K13	No Ball	L13	No Ball	M13	No Ball
J14	No Ball	K14	No Ball	L14	No Ball	M14	No Ball
J15	No Ball	K15	No Ball	L15	No Ball	M15	No Ball
J16	No Ball	K16	No Ball	L16	No Ball	M16	No Ball
J17	No Ball	K17	No Ball	L17	No Ball	M17	No Ball
J18	No Ball	K18	No Ball	L18	No Ball	M18	No Ball
J19	No Ball	K19	No Ball	L19	No Ball	M19	No Ball
J20	No Ball	K20	No Ball	L20	No Ball	M20	No Ball
J21	No Ball	K21	No Ball	L21	No Ball	M21	No Ball
J22	No Ball	K22	No Ball	L22	No Ball	M22	No Ball
J23	No Ball	K23	No Ball	L23	No Ball	M23	No Ball
J24	No Ball	K24	No Ball	L24	No Ball	M24	No Ball
J25	No Ball	K25	No Ball	L25	No Ball	M25	No Ball
J26	No Ball	K26	No Ball	L26	No Ball	M26	No Ball
J27	No Ball	K27	No Ball	L27	No Ball	M27	No Ball
J28	No Ball	K28	No Ball	L28	No Ball	M28	No Ball
J29	TCK	K29	TestEn	L29	OV_{DD}	M29	TrcClk
J30	GND	K30	GND	L30	GPIO52 *	M30	GND
J31	IIC0SClk	K31	SPIClkOut *	L31	GPIO53 *	M31	GPIO59 *
J32	GND	K32	SPIDI *	L32	GPIO55 *	M32	GPIO61 *
J33	OV_{DD}	K33	GPIO54 *	L33	GPIO57 *	M33	GND
J34	GPIO50 *	K34	GPIO56 *	L34	GPIO60 *	M34	GPIO62 *

Table 4. Signals Listed by Ball Assignment (Part 4 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	$\overline{\text{PCIE1Tx1}}$	P01	PCIE1CalRN	R01	AGND	T01	$\overline{\text{PCIE1Tx2}}$
N02	PCIE1Tx1	P02	PCIE1CalRP	R02	AGND	T02	PCIE1Tx2
N03	AV_{DD}	P03	AGND	R03	$\overline{\text{PCIE1RefClk}}$	T03	AV_{DD}
N04	$\overline{\text{PCIE1Rx1}}$	P04	AGND	R04	PCIE1RefClk	T04	PCIE1Rx2
N05	PCIE1Rx1	P05	AV_{DD}	R05	PCIE1AVReg	T05	$\overline{\text{PCIE1Rx2}}$
N06	AV_{DD}	P06	AGND	R06	AGND	T06	PAV_{DD}
N07	No Ball	P07	No Ball	R07	No Ball	T07	No Ball
N08	No Ball	P08	No Ball	R08	No Ball	T08	No Ball
N09	No Ball	P09	No Ball	R09	No Ball	T09	No Ball
N10	No Ball	P10	No Ball	R10	No Ball	T10	No Ball
N11	No Ball	P11	No Ball	R11	No Ball	T11	No Ball
N12	No Ball	P12	No Ball	R12	No Ball	T12	No Ball
N13	No Ball	P13	No Ball	R13	No Ball	T13	No Ball
N14	No Ball	P14	GND	R14	OV_{DD}	T14	GND
N15	No Ball	P15	OV_{DD}	R15	GND	T15	GND
N16	No Ball	P16	GND	R16	GND	T16	GND
N17	No Ball	P17	V_{DD}	R17	V_{DD}	T17	GND
N18	No Ball	P18	V_{DD}	R18	V_{DD}	T18	GND
N19	No Ball	P19	GND	R19	GND	T19	GND
N20	No Ball	P20	OV_{DD}	R20	GND	T20	GND
N21	No Ball	P21	GND	R21	OV_{DD}	T21	GND
N22	No Ball	P22	No Ball	R22	No Ball	T22	No Ball
N23	No Ball	P23	No Ball	R23	No Ball	T23	No Ball
N24	No Ball	P24	No Ball	R24	No Ball	T24	No Ball
N25	No Ball	P25	No Ball	R25	No Ball	T25	No Ball
N26	No Ball	P26	No Ball	R26	No Ball	T26	No Ball
N27	No Ball	P27	No Ball	R27	No Ball	T27	No Ball
N28	No Ball	P28	No Ball	R28	No Ball	T28	No Ball
N29	GPIO58 *	P29	V_{DD}	R29	V_{DD}	T29	MEMVRef2B
N30	SOV_{DD}	P30	MemData00	R30	MemData03	T30	GND
N31	GPIO63 *	P31	DM0	R31	MemData07	T31	MemData13
N32	MemData05	P32	$\overline{\text{DQS0}}$	R32	MemData02	T32	MemData11
N33	MemData04	P33	DQS0	R33	MemData12	T33	SOV_{DD}
N34	MemData01	P34	MemData06	R34	MemData08	T34	MemData09

Table 4. Signals Listed by Ball Assignment (Part 5 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	AGND	V01	$\overline{\text{PCIE1Tx3}}$	W01	$\overline{\text{PCIE0Tx0}}$	Y01	AGND
U02	AV_{DD}	V02	PCIE1Tx3	W02	PCIE0Tx0	Y02	AV_{DD}
U03	AV_{DD}	V03	AV_{DD}	W03	AV_{DD}	Y03	AGND
U04	AGND	V04	$\overline{\text{PCIE1Rx3}}$	W04	PCIE0Rx0	Y04	AV_{DD}
U05	AGND	V05	PCIE1Rx3	W05	$\overline{\text{PCIE0Rx0}}$	Y05	AGND
U06	AV_{DD}	V06	AV_{DD}	W06	AV_{DD}	Y06	V_{DD}
U07	No Ball	V07	No Ball	W07	No Ball	Y07	No Ball
U08	No Ball	V08	No Ball	W08	No Ball	Y08	No Ball
U09	No Ball	V09	No Ball	W09	No Ball	Y09	No Ball
U10	No Ball	V10	No Ball	W10	No Ball	Y10	No Ball
U11	No Ball	V11	No Ball	W11	No Ball	Y11	No Ball
U12	No Ball	V12	No Ball	W12	No Ball	Y12	No Ball
U13	No Ball	V13	No Ball	W13	No Ball	Y13	No Ball
U14	V_{DD}	V14	V_{DD}	W14	GND	Y14	$E1OV_{DD}$
U15	V_{DD}	V15	V_{DD}	W15	GND	Y15	GND
U16	GND	V16	GND	W16	GND	Y16	GND
U17	GND	V17	GND	W17	GND	Y17	V_{DD}
U18	GND	V18	GND	W18	GND	Y18	V_{DD}
U19	GND	V19	GND	W19	GND	Y19	GND
U20	V_{DD}	V20	V_{DD}	W20	GND	Y20	GND
U21	V_{DD}	V21	V_{DD}	W21	GND	Y21	SOV_{DD}
U22	No Ball	V22	No Ball	W22	No Ball	Y22	No Ball
U23	No Ball	V23	No Ball	W23	No Ball	Y23	No Ball
U24	No Ball	V24	No Ball	W24	No Ball	Y24	No Ball
U25	No Ball	V25	No Ball	W25	No Ball	Y25	No Ball
U26	No Ball	V26	No Ball	W26	No Ball	Y26	No Ball
U27	No Ball	V27	No Ball	W27	No Ball	Y27	No Ball
U28	No Ball	V28	No Ball	W28	No Ball	Y28	No Ball
U29	V_{DD}	V29	V_{DD}	W29	GND	Y29	V_{DD}
U30	DM1	V30	DM2	W30	MemData19	Y30	MemData27
U31	$\overline{\text{DQS1}}$	V31	MemData17	W31	DQS2	Y31	MemData29
U32	DQS1	V32	MemData16	W32	$\overline{\text{DQS2}}$	Y32	MemData18
U33	MemData14	V33	MemData20	W33	SOV_{DD}	Y33	MemData23
U34	MemData15	V34	MemData10	W34	MemData21	Y34	MemData22

Table 4. Signals Listed by Ball Assignment (Part 6 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	PCIE0AVReg	AB01	PCIE0CalRP	AC01	GND	AD01	GND
AA02	PCIE0RefClk	AB02	PCIE0CalRN	AC02	$\overline{\text{SysReset}}$	AD02	SysClk
AA03	$\overline{\text{PCIE0RefClk}}$	AB03	SysErr	AC03	GND	AD03	GPIO07 *
AA04	AGND	AB04	AV_{DD}	AC04	GND	AD04	GPIO21 *
AA05	PAV_{DD}	AB05	GPIO06 *	AC05	GND	AD05	GPIO01 *
AA06	V_{DD}	AB06	V_{DD}	AC06	GMC1TxClk *	AD06	$E1OV_{DD}$
AA07	No Ball	AB07	No Ball	AC07	No Ball	AD07	No Ball
AA08	No Ball	AB08	No Ball	AC08	No Ball	AD08	No Ball
AA09	No Ball	AB09	No Ball	AC09	No Ball	AD09	No Ball
AA10	No Ball	AB10	No Ball	AC10	No Ball	AD10	No Ball
AA11	No Ball	AB11	No Ball	AC11	No Ball	AD11	No Ball
AA12	No Ball	AB12	No Ball	AC12	No Ball	AD12	No Ball
AA13	No Ball	AB13	No Ball	AC13	No Ball	AD13	No Ball
AA14	GND	AB14	No Ball	AC14	No Ball	AD14	No Ball
AA15	$E1OV_{DD}$	AB15	No Ball	AC15	No Ball	AD15	No Ball
AA16	GND	AB16	No Ball	AC16	No Ball	AD16	No Ball
AA17	V_{DD}	AB17	No Ball	AC17	No Ball	AD17	No Ball
AA18	V_{DD}	AB18	No Ball	AC18	No Ball	AD18	No Ball
AA19	GND	AB19	No Ball	AC19	No Ball	AD19	No Ball
AA20	SOV_{DD}	AB20	No Ball	AC20	No Ball	AD20	No Ball
AA21	GND	AB21	No Ball	AC21	No Ball	AD21	No Ball
AA22	No Ball	AB22	No Ball	AC22	No Ball	AD22	No Ball
AA23	No Ball	AB23	No Ball	AC23	No Ball	AD23	No Ball
AA24	No Ball	AB24	No Ball	AC24	No Ball	AD24	No Ball
AA25	No Ball	AB25	No Ball	AC25	No Ball	AD25	No Ball
AA26	No Ball	AB26	No Ball	AC26	No Ball	AD26	No Ball
AA27	No Ball	AB27	No Ball	AC27	No Ball	AD27	No Ball
AA28	No Ball	AB28	No Ball	AC28	No Ball	AD28	No Ball
AA29	V_{DD}	AB29	MemVRef1B	AC29	MemAddr13	AD29	SOV_{DD}
AA30	DQS3	AB30	SOV_{DD}	AC30	ECC1	AD30	ECC7
AA31	$\overline{\text{DQS3}}$	AB31	MemData26	AC31	ECC0	AD31	ECC6
AA32	MemData25	AB32	MemData31	AC32	ECC5	AD32	DQS8
AA33	MemData24	AB33	MemData30	AC33	GND	AD33	$\overline{\text{DQS8}}$
AA34	MemData28	AB34	DM3	AC34	ECC4	AD34	DM8

Table 4. Signals Listed by Ball Assignment (Part 7 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AE01	GPIO05 *	AF01	GPIO03 *	AG01	GPIO00 *	AH01	GPIO15 *
AE02	GPIO04 *	AF02	$E1OV_{DD}$	AG02	GPIO17 *	AH02	GND
AE03	GND	AF03	GPIO19 *	AG03	GPIO20 *	AH03	GPIO13 *
AE04	GPIO02 *	AF04	GPIO16 *	AG04	GPIO18 *	AH04	GPIO08 *
AE05	GND	AF05	GND	AG05	$E1OV_{DD}$	AH05	GMC0TxD6
AE06	GMC1GTxClk *	AF06	GMC1RxClk *	AG06	GPIO10 *	AH06	No ball
AE07	No Ball	AF07	No Ball	AG07	No Ball	AH07	No Ball
AE08	No Ball	AF08	No Ball	AG08	No Ball	AH08	No Ball
AE09	No Ball	AF09	No Ball	AG09	No Ball	AH09	No Ball
AE10	No Ball	AF10	No Ball	AG10	No Ball	AH10	No Ball
AE11	No Ball	AF11	No Ball	AG11	No Ball	AH11	No Ball
AE12	No Ball	AF12	No Ball	AG12	No Ball	AH12	No Ball
AE13	No Ball	AF13	No Ball	AG13	No Ball	AH13	No Ball
AE14	No Ball	AF14	No Ball	AG14	No Ball	AH14	No Ball
AE15	No Ball	AF15	No Ball	AG15	No Ball	AH15	No Ball
AE16	No Ball	AF16	No Ball	AG16	No Ball	AH16	No Ball
AE17	No Ball	AF17	No Ball	AG17	No Ball	AH17	No Ball
AE18	No Ball	AF18	No Ball	AG18	No Ball	AH18	No Ball
AE19	No Ball	AF19	No Ball	AG19	No Ball	AH19	No Ball
AE20	No Ball	AF20	No Ball	AG20	No Ball	AH20	No Ball
AE21	No Ball	AF21	No Ball	AG21	No Ball	AH21	No Ball
AE22	No Ball	AF22	No Ball	AG22	No Ball	AH22	No Ball
AE23	No Ball	AF23	No Ball	AG23	No Ball	AH23	No Ball
AE24	No Ball	AF24	No Ball	AG24	No Ball	AH24	No Ball
AE25	No Ball	AF25	No Ball	AG25	No Ball	AH25	No Ball
AE26	No Ball	AF26	No Ball	AG26	No Ball	AH26	No Ball
AE27	No Ball	AF27	No Ball	AG27	No Ball	AH27	No Ball
AE28	No Ball	AF28	No Ball	AG28	No Ball	AH28	No Ball
AE29	ClkEn0	AF29	GND	AG29	GND	AH29	No ball
AE30	GND	AF30	GND	AG30	SOV_{DD}	AH30	MemAddr04
AE31	ClkEn3	AF31	MemAddr11	AG31	MemAddr07	AH31	MemAddr05
AE32	ECC2	AF32	MemAddr14	AG32	MemAddr09	AH32	MemAddr06
AE33	ClkEn2	AF33	SOV_{DD}	AG33	MemAddr10	AH33	GND
AE34	ECC3	AF34	ClkEn1	AG34	MemAddr12	AH34	MemAddr08

Table 4. Signals Listed by Ball Assignment (Part 8 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AJ01	GPIO14 *	AK01	GMCMDIO *	AL01	GMC0TxD3	AM01	GMC0TxD5
AJ02	GPIO11 *	AK02	$E1OV_{DD}$	AL02	GMC0TxD2	AM02	GMC0TxD0
AJ03	GMCMDClk *	AK03	GMC0TxD4	AL03	GMC0TxD7	AM03	GND
AJ04	GPIO12 *	AK04	GMC0TxD1	AL04	GND	AM04	GND
AJ05	GPIO09 *	AK05	GND	AL05	GND	AM05	GMC0TxEn
AJ06	GND	AK06	GND	AL06	GMC0RxDV	AM06	GND
AJ07	No ball	AK07	GND	AL07	GMC0CrS	AM07	GMC0RxClk
AJ08	GMC0TxER	AK08	$E1OV_{DD}$	AL08	GMC0RxD5	AM08	GMC0RxD6
AJ09	GMC0RxD3	AK09	GMC0RxD1	AL09	GMC0RxD0	AM09	TherMonA
AJ10	GMC0RxER	AK10	GND	AL10	TherMonB	AM10	GND
AJ11	$E1OV_{DD}$	AK11	SGMII1TxD	AL11	$\overline{\text{SGMII1TxD}}$	AM11	SGMII0TxD
AJ12	SGMIITxClk	AK12	$\overline{\text{SGMIITxClk}}$	AL12	SGMII2RxD	AM12	$\overline{\text{SGMII2RxD}}$
AJ13	GND	AK13	$E2OV_{DD}$	AL13	SGMII2RxClk	AM13	$\overline{\text{SGMII2RxClk}}$
AJ14	V_{DD}	AK14	GND	AL14	SGMII1RxClk	AM14	$\overline{\text{SGMII1RxClk}}$
AJ15	V_{DD}	AK15	SGMII0RxClk	AL15	$\overline{\text{SGMII0RxClk}}$	AM15	Reserved
AJ16	GND	AK16	MemData63	AL16	MemData58	AM16	MemData62
AJ17	V_{DD}	AK17	DQS7	AL17	$\overline{\text{DQS7}}$	AM17	DM7
AJ18	V_{DD}	AK18	MemData60	AL18	MemData50	AM18	MemData51
AJ19	MemVRef1A	AK19	GND	AL19	$\overline{\text{DQS6}}$	AM19	DQS6
AJ20	V_{DD}	AK20	MemData52	AL20	MemData48	AM20	MemData49
AJ21	V_{DD}	AK21	MemData34	AL21	MemData47	AM21	MemData42
AJ22	MemVRef2A	AK22	SOV_{DD}	AL22	GND	AM22	$\overline{\text{DQS5}}$
AJ23	GND	AK23	MemData44	AL23	MemData40	AM23	MemData41
AJ24	SOV_{DD}	AK24	GND	AL24	MemData38	AM24	MemData39
AJ25	GND	AK25	GND	AL25	GND	AM25	DM4
AJ26	GND	AK26	MemData37	AL26	MemData36	AM26	MemData32
AJ27	GND	AK27	SOV_{DD}	AL27	MemODT3	AM27	MemODT1
AJ28	No ball	AK28	GND	AL28	$\overline{\text{BankSel0}}$	AM28	MemODT2
AJ29	GND	AK29	GND	AL29	$\overline{\text{CAS}}$	AM29	$\overline{\text{BankSel2}}$
AJ30	GND	AK30	GND	AL30	GND	AM30	GND
AJ31	GND	AK31	MemClkOut1	AL31	GND	AM31	BA2
AJ32	MemAddr02	AK32	$\overline{\text{MemClkOut1}}$	AL32	GND	AM32	GND
AJ33	MemAddr01	AK33	SOV_{DD}	AL33	GND	AM33	MemDCFdbkD
AJ34	MemAddr03	AK34	MemAddr00	AL34	GND	AM34	MemDCFdbkR

Table 4. Signals Listed by Ball Assignment (Part 9 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AN01	GND	AP01	GND				
AN02	GND	AP02	GND				
AN03	GND	AP03	GND				
AN04	GMC0TxClk *	AP04	GND				
AN05	$E1OV_{DD}$	AP05	GMC0CD				
AN06	GMC0GTxClk	AP06	GND				
AN07	GND	AP07	GMC0RxD7				
AN08	GMC0RxD4	AP08	GMC0RxD2				
AN09	$E1OV_{DD}$	AP09	GMCRefClk				
AN10	$\overline{\text{SGMII2TxD}}$	AP10	SGMII2TxD				
AN11	$\overline{\text{SGMII0TxD}}$	AP11	EAVDD				
AN12	GND	AP12	EAGND				
AN13	SGMII1RxD	AP13	$\overline{\text{SGMII1RxD}}$				
AN14	SGMII0RxD	AP14	$\overline{\text{SGMII0RxD}}$				
AN15	Reserved	AP15	MemData59				
AN16	$E2OV_{DD}$	AP16	GND				
AN17	MemData57	AP17	GND				
AN18	MemData61	AP18	MemData56				
AN19	SOV_{DD}	AP19	MemData55				
AN20	DM6	AP20	MemData54				
AN21	MemData43	AP21	MemData53				
AN22	DQS5	AP22	MemData46				
AN23	GND	AP23	DM5				
AN24	MemData35	AP24	MemData45				
AN25	$\overline{\text{DQS4}}$	AP25	DQS4				
AN26	SOV_{DD}	AP26	MemData33				
AN27	$\overline{\text{MemClkOut0}}$	AP27	MemClkOut0				
AN28	GND	AP28	MemODT0				
AN29	$\overline{\text{BankSel3}}$	AP29	$\overline{\text{BankSel1}}$				
AN30	SOV_{DD}	AP30	$\overline{\text{RAS}}$				
AN31	GND	AP31	BA1				
AN32	BA0	AP32	$\overline{\text{WE}}$				
AN33	GND	AP33	GND				
AN34	GND	AP34	GND				

Signal Descriptions

The PPC460GT embedded controller is packaged in a 728-ball thermally enhanced plastic ball grid array (TE-PBGA). The following tables describe the package level pin-out.

Table 5. Pin Summary

Group	No. of Pins
Total Signal Pins	**437**
V_{DD}	37
OV_{DD}	23
SOV_{DD}	16
$E1OV_{DD}$	10
$E2OV_{DD}$	2
GND	160
PAV_{DD}	2
AV_{DD}	18
AGND	17
EAV_{DD}	1
EAGND	1
$SPAV_{DD}$	1
SPAGND	1
Total Power Pins	**289**
Reserved	2
Total Pins	**728**

In the table *Table 7* on page 60, each I/O signal is listed along with a short description of its function. Active-low signals (for example, $\overline{RAS}$) are marked with an overline. Please see *Table 3* on page 21 for the pin (ball) number to which each signal is assigned.

Multiplexed Signals

Some signals are multiplexed on the same pin so that the pin can be used for different functions. In most cases, the signal names shown in the following table are not accompanied by signal names that might share the same pin. If you need to know what, if any, signals are multiplexed with a particular signal, look up the name in *Table 3* on page 21. It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

Multipurpose Signals

In addition to multiplexing, some pins such as those carrying the EOTx/TCx signals are also multipurpose. Control of which function a multipurpose pin has is determined by direction, register settings, and so on. Both functions are shown separated by a slash (/).

Multimode Signals

In some cases (for example, Ethernet) the function of a pin may vary with different modes of operation. When a pin has multiple signal names assigned to distinguish different modes of operation, all of the names are shown separated by a comma.

Strapping Pins

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 95). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

Reserved Pins

The balls marked *Reserved* on this chip are not functional. However, some of the reserved balls cannot be left unconnected. Connect the balls shown in Table 6 as indicated:

Table 6. Non-Functional Ball Connections

Ball	Connection
AM15	1kΩ to GND
AN15	1kΩ to GND

Table 7. Signal Functional Description (Part 1 of 10)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} or equivalent.
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ for LVTTL or 8.2kΩ for PCI to OV_{DD} or equivalent.
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCI Interface				
PCIAD00:31	Address/Data bus (bidirectional).	I/O	3.3V PCI	
PCIC0:3/$\overline{\text{BE0:3}}$	PCI Command/Byte Enables.	I/O	3.3V PCI	
PCI0Clk	Provides timing to the PCI interface for PCI transactions.	I	3.3V PCI	1
$\overline{\text{PCI0DevSel}}$	Indicates the driving device has decoded its address as the target of the current access.	I/O	3.3V PCI	4
$\overline{\text{PCI0Frame}}$	Driven by the current master to indicate beginning and duration of an access.	I/O	3.3V PCI	4
$\overline{\text{PCI0IRdy}}$	Indicates initiating agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	4
$\overline{\text{PCI0TRdy}}$	Indicates the target agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	4
$\overline{\text{PCI0Stop}}$	Indicates the current target is requesting the master to stop the current transaction.	I/O	3.3V PCI	4
$\overline{\text{PCI0PErr}}$	Reports data parity errors during all PCI transactions except a Special Cycle.	I/O	3.3V PCI	4
$\overline{\text{PCI0SErr}}$	Reports address parity errors, data parity errors on the Special Cycle command, or other catastrophic system errors.	I/O	3.3V PCI	4
$\overline{\text{PCI0Req0}}$/$\overline{\text{Gnt}}$	Indicates to the PCI arbiter that the specified agent wishes to use the bus. When the internal arbiter is enabled, input is Req0. When internal arbiter is disabled, input is Gnt.	I	3.3V PCI	4
$\overline{\text{PCI0Req1:3}}$	An indication to the PCI arbiter that the specified agent wishes to use the bus. Used only when internal PCI arbiter enabled.	I	3.3V PCI	4
$\overline{\text{PCI0Gnt0}}$/$\overline{\text{Req}}$	Indicates that the specified agent is granted access to the bus. When the internal arbiter is enabled, output is Gnt0. When the internal arbiter is disabled, output is Req.	O	3.3V PCI	
$\overline{\text{PCI0Gnt1:3}}$	Indicates that the specified agent is granted access to the bus. Used only when internal PCI arbiter enabled.	O	3.3V PCI	
PCI0IDSel	Used as a chip select during configuration read and write transactions.	I	3.3V PCI	5
$\overline{\text{PCI0INT}}$	Level sensitive PCI interrupt.	O	3.3V PCI	
PCI0M66En	Capable of 66MHz operation.	I	3.3V PCI	5
PCI0Par	Even parity across PCIAD00:31 and PCIC0:3/$\overline{\text{BE0:3}}$ buses.	I/O	3.3V PCI	
$\overline{\text{PCI0Reset}}$	Brings PCI device registers and logic to a consistent state.	O	3.3V PCI	

Table 7. Signal Functional Description (Part 2 of 10)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} or equivalent.
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ for LVTTL or 8.2kΩ for PCI to OV_{DD} or equivalent.
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCI Express Interface (n = 0 and 1)				
PCIEnRefClk PCIEnRefClk	Reference Clock: 100MHz differential pair.	I	2.5V LVDS Rcvr w/term	
PCIEnAVReg	Analog obvservation point for manufacturing test of internal voltage regulator. **Note:** For normal operation, do not terminate.	na	Analog	
PCIEnCalRN PCIEnCalRP	Connect a 1.37kΩ ± 1% external calibration resistor between these two pins.	na	Analog	
PCIEnRx0:3 PCIEnRx0:3	Differential receive signal pairs. PCIE0 is a single-channel (Rx0 only) interface. PCIE1 is a four-channel (Rx0:3) interface. Lane 0 is LSB. **Note:** DC couple only and bias to 0V common mode.	I	2.5V LVDS Rcvr w/term	
PCIEnTx0:3 PCIEnTx0:3	Differential transmit signal pairs. PCIE0 is a single-channel (Tx0 only) interface. PCIE1 is a four-channel (Tx0:3) interface. Lane 0 is LSB. **Note:** AC couple only.	O	2.5V LVDS Drvr w/term	

Table 7. Signal Functional Description (Part 3 of 10)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} or equivalent.
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ for LVTTL or 8.2kΩ for PCI to OV_{DD} or equivalent.
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
DDR2/1 SDRAM Interface				
BA0:2	Bank Address supporting up to eight internal banks.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
$\overline{\text{BankSel0:3}}$	Selects up to four external DDR SDRAM banks (a.k.a. ranks).	O	2.5V (1.8V) SSTL2 Dr/Rcv	
$\overline{\text{CAS}}$	Column Address Strobe.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
ClkEn0:3	Clock Enable.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
DM0:7 DM8	Memory write data byte lane masks. DM8 is the byte lane mask for the ECC byte lane.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
DQS0:7 $\overline{\text{DQS0:7}}$ DQS8 $\overline{\text{DQS8}}$	Differential byte lane data strobe. Differential byte lane data strobe for ECC.	I/O	2.5V (1.8V) SSTL2 Diff Dr/Rcv	
ECC0:7	ECC check bits 0:7.	I/O	2.5V (1.8V) SSTL2 Dr/Rcv	
MemAddr00:14	Memory address bus. MemAddr14 is the most significant bit (msb).	O	2.5V (1.8V) SSTL2 Dr/Rcv	
MemData00:63	Memory data bus (MemData32:63 available for DDR2 only). MemData00 is the most significant bit (msb).	I/O	2.5V (1.8V) SSTL2 Dr/Rcv	
MemClkOut0:1 $\overline{\text{MemClkOut0:1}}$	Subsystem clock outputs.	O	2.5V (1.8V) SSTL2 Dr/Rcv Diff Driver	
MemODT0:3	DDR2 On-die termination enable (not used with DDR1).	O	2.5V (1.8V) SSTL2 Dr/Rcv	
$\overline{\text{RAS}}$	Row Address Strobe.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
$\overline{\text{WE}}$	Write Enable.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
MemVRef1A:B	Memory voltage reference 1, A and B input.	I	Volt ref receiver (1.25V or 0.9V)	
MemVRef2A:B	Memory voltage reference 2, A and B input.	I	Volt ref driver (1.25V or 0.9V)	
MemDCFdbkD	Feedback driver for I/O timing measurements.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
MemDCFdbkR	Feedback receiver. Connect externally to MemDCFdbkD. **Note:** Connect directly to MemDCFdbkR. Use the shortest trace length possible. Do not include series termination or parallel termination to Vtt.	I	2.5V (1.8V) SSTL2 Dr/Rcv	
$\overline{\text{HISRRst}}$	SDRAM hardware initiated self-refresh reset control.	I	3.3V LVTTL	1, 2

Table 7. Signal Functional Description (Part 4 of 10)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} or equivalent.
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ for LVTTL or 8.2kΩ for PCI to OV_{DD} or equivalent.
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Ethernet 0 Interface				
GMCMDClk	GMII, MII, RGMII: Management data clock.	O	3.3V tolerant 2.5V CMOS	
GMCMDIO	GMII, MII, RGMII: Transfer command and status information between MII and PHY.	I/O	3.3V tolerant 2.5V CMOS	
GMCRefClk	GMII, SGMII, RGMII: 125MHz reference clock for 10/100/1000Mbps.	I	3.3V tolerant 2.5V CMOS	1, 5
GMC0GTxClk, GMC0TxClk	GMII 0: Transmit clock. RGMII 0: Transmit clock.	O	3.3V tolerant 2.5V CMOS	
GMC0TxClk, RMII01RefClk, SMIIRefClk	MII 0: Transmit clock. RMII 0 & 1: 50MHz reference clock for 10/100 Mbps. SMII: 125Mhz reference clock for 10/100 Mbps.	I	3.3V tolerant 2.5V CMOS	1, 5
GMC0TxD1:0, GMC0TxD1:0, RMII0TxD1:0, SMII1:0TxD	GMII/MII 0: Transmit data. RGMII 0: Transmit data. RMII 0: Transmit data. SMII 1:0: Transmit data.	O	3.3V tolerant 2.5V CMOS	
GMC0TxD3:2, GMC0TxD3:2, RMII1TxD1:0, SMII3:2TxD	GMII/MII 0: Transmit data. RGMII 0: Transmit data. RMII 1: Transmit data. SMII 3:2: Transmit data.	O	3.3V tolerant 2.5V CMOS	
GMC0TxD7:4, GMC1TxD3:0	GMII 0: Transmit data. RGMII 1: Transmit data.	O	3.3V tolerant 2.5V CMOS	
GMC0TxEn, GMC0TxCtl, RMII0TxEn, SMIISync	GMII/MII 0: Transmit enable. RGMII 0: Transmit control. RMII 0: Transmit enable. SMII: Synchronizing signal.	O	3.3V tolerant 2.5V CMOS	
GMC0TxEr, GMC1TxCtl, RMII1TxEn	GMII/MII 0: Transmit error. RGMII 1: Transmit control. RMII 1: Transmit enable.	O	3.3V tolerant 2.5V CMOS	
GMC0CD, GMC1RxClk RMII1RxEr	GMII/MII 0: Collision detection. RGMII 1: Receive clock. RMII 1: Receive error.	I	3.3V tolerant 2.5V CMOS	1, 5
GMC0CrS, GMC1TxClk, RMII0CrSDV	GMII/MII 0: Carrier sense. RGMII 1: Transmit clock. RMII 0: Carrier sense/Receive data valid.	I/O	3.3V tolerant 2.5V CMOS	
GMC0RxClk, GMC0RxClk	GMII/MII 0: Receive clock. RGMII 0: Receive clock.	I	3.3V tolerant 2.5V CMOS	1, 5
GMC0RxD1:0, GMC0RxD1:0, RMII0RxD1:0, SMII1:0RxD	GMII/MII 0: Receive data. RGMII 0: Receive data. RMII 0: Receive data. SMII 1:0: Receive data.	I	3.3V tolerant 2.5V CMOS	5
GMC0RxD3:2, GMC0RxD3:2, RMII1RxD1:0 SMII3:2RxD	GMII/MII 0: Receive data. RGMII 0: Receive data. RMII 1: Receive data. SMII 3:2: Receive data.	I	3.3V tolerant 2.5V CMOS	5

Table 7. Signal Functional Description (Part 5 of 10)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} or equivalent.
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ for LVTTL or 8.2kΩ for PCI to OV_{DD} or equivalent.
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
GMC0RxD7:4, GMC1RxD3:0	GMII/MII 0: Receive data. RGMII 1: Receive data.	I	3.3V tolerant 2.5V CMOS	5
GMC0RxDV, GMC0RxCtl, RMII1CrSDV	GMII/MII 0: Receive data valid. RGMII 0: Receive control. RMII 1: Carrier Sense/Receive Data Valid	I	3.3V tolerant 2.5V CMOS	5
GMC0RxEr, GMC1RxCtl, RMII0RxEr	GMII/MII 0: Receive error. RGMII 1: Receive control. RMII 0: Receive Error.	I	3.3V tolerant 2.5V CMOS	5
Ethernet 1 Interface				
GMC1GTxClk, GMC2TxClk	GMII 1: Transmit clock. RGMII 2: Transmit clock.	O	3.3V tolerant 2.5V CMOS	
GMC1TxClk, RMII23RefClk	MII 1: Transmit clock. RMII 2 & 3: 50MHz Reference clock for 10/100Mbps.	I	3.3V tolerant 2.5V CMOS	1, 5
GMC1TxD1:0, GMC2TxD1:0, RMII2TxD1:0	GMII/MII 1: Transmit data. RGMII 2: Transmit data. RMII 2: Transmit data.	O	3.3V tolerant 2.5V CMOS	
GMC1TxD3:2, GMC2TxD3:2, RMII3TxD1:0	GMII/MII 1: Transmit data. RGMII 2: Transmit data. RMII 3: Transmit data.	O	3.3V tolerant 2.5V CMOS	
GMC1TxD7:4, GMC3TxD3:0	GMII 1: Transmit data. RGMII 3: Transmit data.	O	3.3V tolerant 2.5V CMOS	
GMC1TxEn, GMC2TxCtl, RMII2TxEn	GMII/MII 1: Transmit enable. RGMII 2: Transmit control. RMII 2: Transmit enable.	O	3.3V tolerant 2.5V CMOS	
GMC1TxEr, GMC3TxCtl, RMII3TxEn	GMII/MII 1: Transmit error. RGMII 3: Transmit control. RMII 3: Transmit enable.	O	3.3V tolerant 2.5V CMOS	
GMC1CD, GMC3RxClk, RMII3RxEr	GMII/MII 1: Collision detection. RGMII 3: Receive clock. RMII 3: Receive error.	I	3.3V tolerant 2.5V CMOS	1, 5
GMC1Crs, GMC3TxClk, RMII2CrSDV	GMII/MII 1: Carrier sense. RGMII 3: Transmit clock. RMII 2: Carrier sense/Receive data valid.	I/O	3.3V tolerant 2.5V CMOS	
GMC1RxClk, GMC2RxClk	GMII/MII 1: Receive clock. RGMII 2: Receive clock.	I	3.3V tolerant 2.5V CMOS	1, 5
GMC1RxD2:0, GMC2RxD2:0, RMII2RxD1:0	GMII/MII 1: Receive data. RGMII 2: Receive data. RMII 2: Receive data.	I	3.3V tolerant 2.5V CMOS	
GMC1RxD3:2, GMC2RxD3:2, RMII3RxD1:0	GMII/MII 1: Receive data. RGMII 2: Receive data. RMII 3: Receive data.	I	3.3V tolerant 2.5V CMOS	

Table 7. Signal Functional Description (Part 6 of 10)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} or equivalent.
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ for LVTTL or 8.2kΩ for PCI to OV_{DD} or equivalent.
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
GMC1RxD4:7, GMC3RxD0:3	GMII/MII 1: Receive data. RGMII 3: Receive data.	I	3.3V tolerant 2.5V CMOS	5
GMC1RxDV, GMC2RxCtl, RMII3CrSDV	GMII/MII 1: Receive data valid. RGMII 2: Receive control. RMII 3: Carrier sense/Receive data valid.	I	3.3V tolerant 2.5V CMOS	5
GMC1RxEr, GMC3RxCtl, RMII2RxEr	GMII/MII 1: Receive error. RGMII 3: Receive control. RMII 2: Receive error.	I	3.3V tolerant 2.5V CMOS	5
Ethernet SGMII Gigabit Interface				
SGMIITxClk SGMIITxClk	Differential transmit clock: Common 625MHz to PHYs.	O	1.8V LVDS Drvr w/term	
SGMII0:2RxClk SGMII0:2RxClk	Differential receive clock: 625MHz from PHY. The differential receiver clock is required for SGMII. Clock recovery from the differential SGMII0:2RxD signals is not supported.	I	1.8V LVDS Rcvr w/term	
SGMII0:2RxD SGMII0:2RxD	Differential receive data.	I	1.8V LVDS Rcvr w/term	
SGMII0:2TxD SGMII0:2TxD	Differential transmit data.	O	1.8V LVDS Drvr w/term	
Serial Rapid IO Interface				
SRIO0RefClk SRIO0RefClk	Reference Clock: 100MHz differential clock pair.	I	CML	
SRIO0Rx0:3 SRIO0Rx0:3	Differential receive signal pairs.	I	CML	
SRIO0Tx0:3 SRIO0Tx0:3	Differential transmit signal pairs.	O	CML	
SRIO0AVREG	Analog observation point for manufacturing test. **Note:** For normal operation, do not terminate.	na	Analog	
SRIO0CalRP SRIO0CalRN	Attach a 1.37 kΩ, 1% resistor between these two pins to provide a reference for both the bias currents and the impedance calibration circuitry.	na	Analog	

Table 7. Signal Functional Description (Part 7 of 10)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} or equivalent.
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ for LVTTL or 8.2kΩ for PCI to OV_{DD} or equivalent.
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
DMA Interface				
DMAAck0:3	External peripheral DMA acknowledge. Used by the PPC460GT to indicate that data transfers have occurred.	O	3.3V LVTTL	
DMAReq0:3	External peripheral DMA request. Used by slave peripherals to indicate they are prepared to transfer data.	I	3.3V LVTTL	5
EOT0:3/TC0:3	End Of Transfer/Terminal Count.	I/O	3.3V LVTTL	5
External Peripheral Interface				
PerAddr05:31	Peripheral address bus used by the PPC460GT. PerAddr05 is the most significant bit (msb) on this bus.	I/O	3.3V LVTTL	
PerData00:31	Peripheral data bus used by the PPC460GT. PerData00 is the most significant bit (msb) on this bus.	I/O	3.3V LVTTL	
PerPar0:3	Peripheral data bus parity used by the PPC460GT.	I/O	3.3V LVTTL	
$\overline{\text{PerBLast}}$	Last burst transfer. Used by either the peripheral controller or DMA controller to indicates the last transfer of a memory access.	I/O	3.3V LVTTL	
$\overline{\text{PerCS0:5}}$	External peripheral device select.	O	3.3V LVTTL	
$\overline{\text{PerOE}}$	Output enable. Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the PPC460GT is the bus master, it enables the selected device to drive the bus.	O	3.3V LVTTL	
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	3.3V LVTTL Rcvr	1, 2
PerR/$\overline{\text{W}}$	Read/Write. Used by the PPC460GT as an output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory.	I/O	3.3V LVTTL	
$\overline{\text{PerWBE0:3}}$	External peripheral data bus byte enables.	I/O	3.3V LVTTL	
PerErr	External Error. Used as an input to record external slave peripheral errors.	I	3.3V LVTTL Rcvr	1, 5
$\overline{\text{ExtReset}}$	Peripheral Reset. Used by synchronous peripheral slaves. **Note:** The state of any external signals or clocks cannot be guaranteed until the ExtReset signal has been de-asserted.	O	3.3V LVTTL	
PerClk	Peripheral Clock. Used by synchronous peripheral slaves.	O	3.3V LVTTL	

Table 7. Signal Functional Description (Part 8 of 10)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} or equivalent.
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ for LVTTL or 8.2kΩ for PCI to OV_{DD} or equivalent.
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
UART Peripheral Interface The UART interface can be configured as follows: 1. One 8-pin, where n = 0 2. Two 4-pin, where n = 0 & 1 3. Four 2-pin, where n = 0 & 1 & 2 & 3				
UARTSerClk	This input provides an alternative to the internally generated serial clock. It is used in cases where the allowable internally generated clock rates are not satisfactory.	I	3.3V LVTTL w/pull-up	1
UARTnRx	Receive data.	I	3.3V LVTTL	
UARTnTx	Transmit data.	O	3.3V LVTTL	
$\overline{\text{UARTnDCD}}$	Data Carrier Detect.	I	3.3V LVTTL	6
$\overline{\text{UARTnDSR}}$	Data Set Ready.	I	3.3V LVTTL	6
$\overline{\text{UARTnCTS}}$	Clear To Send.	I	3.3V LVTTL	6
$\overline{\text{UARTnDTR}}$	Data Terminal Ready.	O	3.3V LVTTL	
$\overline{\text{UARTnRTS}}$	Request To Send.	O	3.3V LVTTL	
$\overline{\text{UARTnRI}}$	Ring Indicator.	I	3.3V LVTTL	
IIC Peripheral Interface (n = 0 and 1)				
IICnSClk	IIC0 Serial Clock.	I/O	3.3V LVTTL	1, 2
IICnSData	IIC0 Serial Data.	I/O	3.3V LVTTL	2
NAND Flash Interface				
NFALE	Address Latch Enable.	O	3.3V LVTTL	
NFCLE	Command Latch Enable. Latches operational commands into the NAND Flash.	O	3.3V LVTTL	
NFRdy$\overline{\text{Busy}}$	Ready/$\overline{\text{Busy}}$. Indicates status of device during program erase or page read. This signal is wire-OR connected from all NAND Flash devices.	I	3.3V LVTTL	
$\overline{\text{NFREn}}$	Read Enable. Data is latched on the rising edge.	O	3.3V LVTTL	
$\overline{\text{NFWEn}}$	Write Enable. Data is latched on the rising edge.	O	3.3V LVTTL	
$\overline{\text{NFCE0:3}}$	Chip enable.	O	3.3V LVTTL	
Serial Peripheral Interface				
SPIClkOut	Clock output.	O	3.3V LVTTL	1
SPIDI	Data input.	I	3.3V LVTTL w/pull-up	2
SPIDO	Data output.	O	3.3V LVTTL	
Interrupts Interface				
IRQ0:15	External interrupt requests 0 through 15.	I	3.3V LVTTL	1, 5

Table 7. Signal Functional Description (Part 9 of 10)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} or equivalent.
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ for LVTTL or 8.2kΩ for PCI to OV_{DD} or equivalent.
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
JTAG Interface				
TCK	Test Clock.	I	3.3V LVTTL w/pull-up	1
TDI	Test Data In.	I	3.3V LVTTL w/pull-up	
TDO	Test Data Out.	O	3.3V LVTTL	
TMS	Test Mode Select.	I	3.3V LVTTL w/pull-up	
$\overline{\text{TRST}}$	Test Reset. During chip power-up, this signal must be low from the start of V_{DD} ramp-up until at least 32 SysClk cycles after V_{DD} is stable in order to initialize the JTAG controller.	I	3.3V LVTTL w/pull-up	5
System Interface				
SysClk	Main system clock input.	I	3.3V tolerant 2.5V CMOS	1
SysErr	Set to 1 when a machine check is generated.	O	3.3V tolerant 2.5V CMOS	
$\overline{\text{SysReset}}$	Main system reset. External logic can drive this pin low (minimum of 16 cycles) to initiate a system reset. A system reset can also be initiated by software.	I	3.3V tolerant 2.5V CMOS	1, 2
TmrClk	Processor timer external input clock.	I	3.3V LVTTL w/pull-up	1
$\overline{\text{Halt}}$	Halt from external debugger.	I	3.3V LVTTL w/pull-up	1
TestEn	Test enable. **Note:** Do not connect for normal operation.	I	3.3V LVTTL w/pull-down	
GPIO00:21	General purpose I/O.	I/O	3.3V tolerant 2.5V CMOS	
GPIO22:63	General purpose I/O.	I/O	3.3V LVTTL	
TherMonA TherMonB	On-chip thermal monitor (P diffusion). On-chip thermal monitor (N diffusion).	I O	Thermal monitor	
Trace Interface				
TrcBS0:2	Trace branch execution status.	O	3.3V LVTTL	
TrcClk	Trace data capture clock; runs at 1/4 the frequency of the processor.	O	3.3V LVTTL	
TrcES0:4	Trace Execution Status is presented every fourth processor clock cycle.	O	3.3V LVTTL	
TrcTS0:6	Additional information on trace execution and branch status.	O	3.3V LVTTL	
Other				
Reserved	To avoid noise pickup problems, Some of these balls must be connected in the board design as shown *Table 6* on page 59. Otherwise, do not connect voltage, ground, or any signals to these pins.	na	na	

Table 7. Signal Functional Description (Part 10 of 10)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} or equivalent.
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ for LVTTL or 8.2kΩ for PCI to OV_{DD} or equivalent.
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Power				
V_{DD}	+1.25V—Logic voltage.	na	na	
OV_{DD}	+3.3V—I/O voltage (except DDR SDRAM, and Ethernet.	na	na	
SOV_{DD}	+1.8V (DDR2) or +2.5V (DDR1)—I/O voltage for DDR SDRAM.	na	na	
$E1OV_{DD}$	+2.5V—I/O voltage for Ethernet (except SGMII).	na	na	
$E2OV_{DD}$	+1.8V—I/O Ethernet (SGMII).	na	na	
GND	Ground for logic and I/O voltages.	na	na	
AV_{DD}	+1.25V—PCI-Express SerDes Analog Supply.	na	na	
PAV_{DD}	+2.5V—PCI-Express SerDes PLL Analog Supply.	na	na	
AGND	Ground for AV_{DD} and PAV_{DD}.	na	na	
EAV_{DD}	+2.5V—Filtered analog voltage for Ethernet PLLs.	na	na	
EAGND	Ground for EAV_{DD}.	na	na	
$SPAV_{DD}$	+2.5V—Filtered analog voltage for system PLL.	na	na	
SPAGND	Ground for $SPAV_{DD}$.	na	na	

Device Characteristics

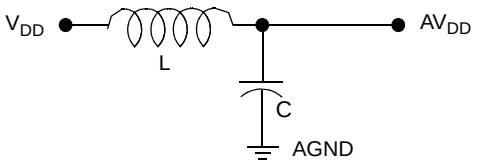
Table 8. Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. *Operation at or beyond these maximum ratings can cause permanent damage to the device. None of the performance specification contained in this document are guaranteed when operating at these maximum ratings.*

Characteristic	Symbol	Value	Unit	Notes
Internal logic supply voltage	V_{DD}	0 to +1.6	V	
I/O supply voltage	OV_{DD}	0 to +3.6	V	
Ethernet I/O supply voltage	$E1OV_{DD}$	0 to +2.7	V	
Ethernet SGMII supply voltage	$E2OV_{DD}$	0 to +1.9	V	
DDR2 (DDR1) SDRAM I/O supply voltage	SOV_{DD}	0 to +1.9 (+2.7V)	V	
PCI-Express SerDes analog supply voltage	AV_{DD}	0 to +1.6	V	1
System PLL analog supply voltage	$SPAV_{DD}$	0 to +2.7	V	1
Ethernet PLL analog supply voltage	EAV_{DD}	0 to +2.7	V	1
PCI-Express SerDes PLL analog supply voltage	PAV_{DD}	0 to +2.7	V	1
Storage Temperature Range	T_{STG}	–55 to +150	°C	
Case temperature under bias	T_C	–40 to +120	°C	2

Notes:

1. The analog voltages (AV_{DD}, EAV_{DD}, $SPAV_{DD}$, and PAV_{DD}) used for the on-chip functions can be derived from the logic voltages, but must be filtered before entering the PPC460GT. A separate filter for each analog voltage, as shown below, is recommended:



AV_{DD} L – SMT ferrite bead chip, Murata BLM18AG121SN1D
C – 0.1µF ceramic

EAV_{DD}, $SPAV_{DD}$, and PAV_{DD}
L – SMT ferrite bead chip, Murata BLM15AG102SN1
C – 1µF ceramic

2. This value is not a specification of the operational temperature range; it is a stress rating only.

Table 9. Recommended DC Operating Conditions (Part 1 of 2)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	+1.2	+1.25	+1.3	V	4
I/O Supply Voltage	OV_{DD}	+3.15	+3.3	+3.45	V	4
Ethernet 1 I/O Supply Voltage	$E1OV_{DD}$	+2.4	+2.5	+2.6	V	4
Ethernet 2 I/O Supply Voltage (SGMII)	$E2OV_{DD}$	+1.7	+1.8	+1.9	V	4
DDR2 (DDR1) SDRAM I/O Supply Voltage	SOV_{DD}	+1.7 (+2.4)	+1.8 (+2.5)	+1.9 (+2.6)	V	4
PCI-Express SerDes analog Supply Voltage	AV_{DD}	+1.2	+1.25	+1.3	V	3
System PLL Analog Supply Voltage	$SPAV_{DD}$	+2.4	+2.5	+2.6	V	3
Ethernet PLL analog supply voltage	EAV_{DD}	+2.4	+2.5	+2.6	V	3
PCI-Express SerDes PLL analog supply voltage	PAV_{DD}	+2.4	+2.5	+2.6	V	3
DDR2 (DDR1) SDRAM Reference Voltage	SV_{REF}	$0.49SOV_{DD}$	$0.50SOV_{DD}$	$0.51SOV_{DD}$	V	3
Input Logic High 3.3V LVTTL and PCI	V_{IH}	+2.0		+3.6	V	1
Input Logic High 2.5V CMOS, 3.3V tolerant		+1.7		+3.6	V	
Input Logic High 1.8V DDR2 (2.5V DDR1)		SV_{REF} + 0.125 (0.15)		2.2 (3.0)	V	2
Input Logic High (1.8V SGMII)		+1.1		+2.2	V	
Input Logic Low 3.3V LVTTL and PCI	V_{IL}	0		+0.8	V	1
Input Logic Low 2.5V CMOS		0		+0.7	V	
Input Logic Low 1.8V DDR2 (2.5V DDR1)		–0.3 (–0.3)		SV_{REF} – 0.125 (0.18)	V	2
Input Logic Low (1.8V SGMII)		+0.3		+0.8	V	
Output Logic High 3.3V LVTTL and PCI	V_{OH}	+2.4		+3.6	V	1
Output Logic High 2.5V CMOS		+2.0		+2.7	V	
Output Logic High 1.8V DDR2 (2.5V DDR1)		SOV_{DD}– 0.95 (+1.95)		SOV_{DD}	V	
Output Logic High (1.8V SGMII)		+1.23	+1.385	+1.534	V	
Output Logic Low 3.3V LVTTL and PCI	V_{OL}	0		+0.4	V	1
Output Logic Low 2.5V CMOS		0		+0.4	V	
Output Logic Low 1.8V DDR2 (2.5V DDR1)		0		+0.45	V	
Output Logic Low (1.8V SGMII)		+0.841	+0.961	+1.081	V	
Input Leakage Current (no pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current for pull-down	I_{IL2}	0 (LPDL)		200 (MPUL)	µA	5

Table 9. Recommended DC Operating Conditions (Part 2 of 2)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Input Leakage Current for pull-up	I_{IL3}	–150 (LPDL)		0 (MPUL)	µA	5
Input Max Allowable Overshoot 2.5V CMOS	V_{IMAO25}			+3.9	V	
Input Max Allowable Overshoot 3.3V LVTTL	V_{IMAO33}			+3.9	V	
Input Max Allowable Undershoot 2.5V CMOS	V_{IMAU25}	–0.6			V	
Input Max Allowable Undershoot 3.3V LVTTL	V_{IMAU33}	–0.6			V	
Output Max Allowable Overshoot 2.5V CMOS	V_{OMAO25}			+3.9	V	
Output Max Allowable Overshoot 3.3V LVTTL	V_{OMAO33}			+3.9	V	
Output Max Allowable Undershoot 2.5V CMOS	V_{OMAU25}	–0.6			V	
Output Max Allowable Undershoot 3.3V LVTTL	V_{OMAU33}	–0.6			V	
Case Temperature	T_C	–40		+85	°C	6

Notes:

1. PCI drivers meet PCI specifications.
2. $SV_{REF} = SOV_{DD}/2$. SOV_{DD} = +1.8V for DDR2 memory or +2.5V for DDR1 memory.
3. The analog voltages used for the on-chip PLLs can be derived from the logic voltages, but must be filtered before entering the PPC460GT. See “Absolute Maximum Ratings” on page 70.
4. LPDL is least positive down level; MPUL is most positive up level.
5. Case temperature, T_C, is measured at top center of case surface with device soldered to a circuit board.

Power Supply Sequencing

All the PPC460GT I/O designs are power supply sequence independent. There is no requirement that the power supplies power up in any particular order. The following items are power sequence considerations:

- Logic power (V_{DD}) is applied before the I/O supply voltages: The I/Os include internal supply sequencing circuitry which ensures the output of the receiver connected to internal chip logic is 0 until the I/O power is applied. When the logic power is on and the I/O power supplies are off, the I/O logic connected to the associated ball neither sinks or sources significant current unless influenced by an internal pull-up or pull-down resistor. While the I/O supply is ramping, the state of the I/O ball is not predictable. This power sequence is not destructive to the I/Os or internal logic and does not cause any functional problems.
- I/O power is applied before the logic power is applied: The output driver (connected the balls) comes up in an unknown state (driving 1, driving 0, or tri-state) until the internal logic voltage is stable within normal operating range. This power sequence is not destructive to the I/Os or internal logic and does not cause any functional problems.
- External voltage should not be applied to the chip I/O balls before the associated I/O power supply voltage is applied to the chip.
- A chip power-down cycle must complete (all I/O supply voltages and VDD are below +0.4V) before a new power-up cycle is started
- During a power-up cycle, $\overline{\text{SysReset}}$ and $\overline{\text{TRST}}$ inputs should be asserted low. $\overline{\text{SysReset}}$ and $\overline{\text{TRST}}$ should remain asserted until SysClock is stable and at least 32 SysClock times after all power supplies are stable within normal operating range. Failure to follow this reset sequence during the power-up cycle can result in unpredictable operation of the chip.

Table 10. Input Capacitance

Parameter	Symbol	Maximum	Unit	Notes
Group 1 (3.3V tolerant 2.5V CMOS I/O)	C_{IN1}	5.7	pF	
Group 2 (1.8V LVDS I/O)	C_{IN2}	5.0	pF	
Group 3 (2.5V SSTL2 I/O)	C_{IN3}	6.4	pF	
Group 4 (3.3V LVTTL I/O)	C_{IN5}	5.2	pF	
Group 5 (PCI I/O)	C_{IN6}	5.7	pF	
Group 6 (CML I/O)	C_{IN6}	5.0	pF	

Table 11. Typical DC Power Supply Requirements Using DDR2 Memory

Frequency (MHz)	+1.25V Supply (V_{DD}+AV_{DD})	+1.8V Supply (SOV_{DD}+$E2OV_{DD}$)	+2.5V Supply ($E1OV_{DD}$+EAV_{DD}+ $SPAV_{DD}$+PAV_{DD})	+3.3V Supply (OV_{DD})	Total	Unit	Notes
600	4.67	0.67	0.07	0.27	5.68	W	1
800	4.90	0.67	0.07	0.27	5.91	W	1
1000	5.34	0.67	0.07	0.27	6.35	W	1

Notes:
1. Typical power is estimated and is based on a nominal voltage of V_{DD} = +1.25V, T_C = 85°C, while running Linux and a test application that exercises each function with representative traffic.

Table 12. Typical DC Power Supply Requirements Using DDR1 Memory

Frequency (MHz)	+1.25V Supply (V_{DD}+AV_{DD})	+1.8V Supply ($E2OV_{DD}$)	+2.5V Supply ($E1OV_{DD}$+EAV_{DD}+ $SPAV_{DD}$+PAV_{DD} +SOV_{DD})	+3.3V Supply (OV_{DD})	Total	Unit	Notes
600	4.67	0	1.18	0.27		W	1
800	4.90	0	1.18	0.27		W	1
1000	5.34	0	1.18	0.27		W	1

Notes:
1. Typical power is estimated and is based on a nominal voltage of V_{DD} = +1.25V, T_C = 85°C, while running Linux and a test application that exercises each function with representative traffic.

Table 13. V_{DD} Supply Power Dissipation

Frequency (MHz)	+1.2V	+1.25V	+1.3V	Unit	Notes
600	4.46	4.67	4.89	W	1
800	4.70	4.90	5.14	W	1
1000	5.15	5.34	5.60	W	1

Notes:

1. Power is estimated and is based on V_{DD} specified in the table and T_C = 85°C, while running Linux and a test application that exercises each function with representative traffic.

Table 14. DC Power Supply Loads

Parameter	Symbol	Typical [4]	Maximum [3, 5]	Unit	Notes
V_{DD} (+1.25V) active operating current	I_{DD}	4270	5800	mA	
OV_{DD} (+3.3V) active operating current	I_{ODD}	70	80	mA	
$E1OV_{DD}$ (+2.5V) active operating current	I_{E1ODD}	30	30	mA	
$E2OV_{DD}$ (+1.8V) active operating current	I_{E2ODD}	40	40	mA	
SOV_{DD} (+1.8V) DDR2 active operating current [2]	I_{SODD2}	360	370	mA	
SOV_{DD} (+2.5V) DDR1 active operating current [2]	I_{SODD1}	450	470	mA	
AV_{DD} (+1.25V) input current [1]	I_{ADD}	50	50	mA	1
EAV_{DD} (+2.5V) active operating current [1]	I_{EADD}	30	30	mA	1
PAV_{DD} (+2.5V) active operating current [1]	I_{UADD}	180	180	mA	1
$SPAV_{DD}$ (+2.5V) active operating current [1]	I_{UADD}	50	50	mA	1

Notes:

1. See “Absolute Maximum Ratings” on page 70 for filter recommendations.
2. SOV_{DD} will be either +2.5V or +1.8V but not both.
3. The maximum current values listed above are not guaranteed to be the highest obtainable. These values are dependent on many factors including the type of applications running, clock rates, use of internal functional capabilities, external interface usage, case temperature, and the power supply voltages. Your specific application can produce significantly different results. V_{DD} (logic) current and power are primarily dependent on the applications running and the use of internal chip functions (DMA, PCI, Ethernet, and so on). OV_{DD} (I/O) current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses.
4. Typical current is estimated at 1GHz with V_{DD} = +1.25V, OV_{DD} = +3.3V, $E1OV_{DD}$ = +2.5V, SOV_{DD} = +2.5V (DDR1) or +1.8V (DDR2), and T_C = +85°C with a typical process.
5. Maximum current is estimated at 1GHz with V_{DD} = +1.3V, OV_{DD} = +3.45V, $E1OV_{DD}$ = +2.6V, SOV_{DD} = +2.6V (DDR1) or +1.9V (DDR2), and T_C = +85°C, and best-case process (which drives worst-case power).

Table 15. Package Thermal Specifications

Thermal resistance values for the TE-PBGA package in a convection environment at ?.?W are as follows:

Parameter	Symbol	Airflow ft/min (m/sec)						Unit	Notes
		0 (0)	100 (0.51)	200 (1.02)	300 (1.53	400 (2.04)	600 (2.55)		
Junction-to-ambient thermal resistance *without* heat sink	θ_{JA}	13.1	11.7	10.9	10.5	10.3	10		3
Junction-to-ambient thermal resistance *with* heat sink	θ_{JA}	10.3	7.3	6.1	5.6	5.4	5.1		3, 6
		Resistance Value							
Junction-to-case thermal resistance	θ_{JC}	3.5						°C/W	3
Junction-to-board thermal resistance	θ_{JB}	7.3						°C/W	3

Notes:

1. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
2. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
3. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature (+125°C) and P is power consumption.
4. The preceding equations assume that the chip is mounted on a board with at least one signal and two power planes.
5. Values in the table were achieved using a JEDEC standard board with the following characteristics: 114.5mm x 101.6mm x 1.6mm, 4 layers. The board has 100 thermal vias (same as the number of thermal balls on the TE-PBGA package).
6. Values for an attached heat sink were achieved with a 35mm x 35mm x 15mm unit (see Thermal Management below), attached with a 0.1mm thickness of adhesive having a thermal conductivity of 1.3W/mK.

Thermal Management

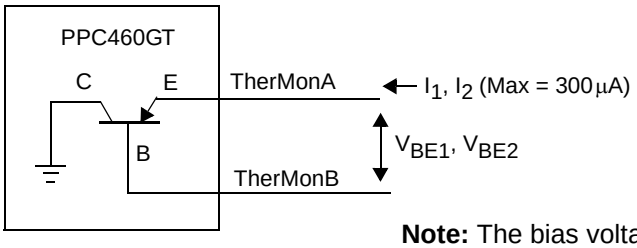
The following heat sink was used in the above thermal analysis:
35W x 35L x 15H (mm)
Base thickness = 1.5mm
Fin height = 13.5mm
Fin thickness = 1.0mm
Number of Fins: 11 aluminum

Thermal Monitor

Thermal monitoring of the chip is accomplished using the PNP transistor ($\beta \approx 2$) provided on the chip. The collector of the transistor is connected to ground (GND). The emitter (TherMonA) and base (TherMonB) are connected to chip pins. A voltage measurement (V_{BE1} and V_{BE2}) across the TherMonA and TherMonB pins at the two current values I_1 and I_2 provides the chip temperature in °K according to the equation:

$$T = (q/nk)(V_{BE2}-V_{BE1})/\ln(I_2/I_1)\ °K \quad \text{where } q = 1.602\ 176\ 53\times10^{-19},\ n = 0.99 \pm 0.05, \text{ and } k = 1.380\ 6505\times10^{-23}.$$

Note: V_{BE2} and V_{BE1} should be specified in Volts. I_1 and I_2 can be any units of measure provided they are the same. The small values require precision measurement and current sources.



Note: The bias voltage V_{EB} should be between +0.5V and +0.7V.

Test Conditions

Clock timing and switching characteristics are specified in accordance with operating conditions shown in *Table 9* on page 71. AC specifications are characterized with V_{DD} = +1.5V, T_C = +85 °C and a 50pF test load as shown in the figure to the right.

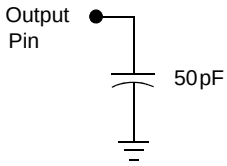


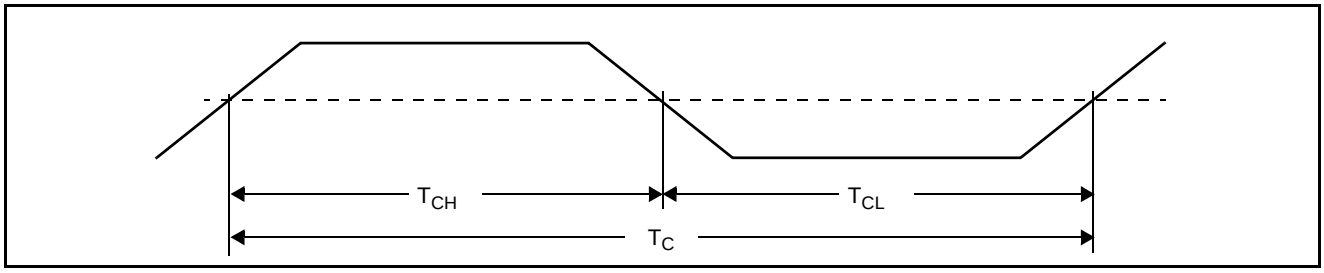
Table 16. Clocking Specifications

Symbol	Parameter	Min	Max	Units	Notes
SysClk Input					
F_C	Frequency	66.66	100	MHz	
T_C	Period	10	15	ns	
T_{CS}	Edge stability (cycle-to-cycle jitter)	–	±0.1	ns	
T_{CH}	High time	40% of nominal period	60% of nominal period	ns	
T_{CL}	Low time	40% of nominal period	60% of nominal period	ns	
Note: Input slew rate ≥ 1V/ns					
PLL VCO					
F_C	Frequency	600	2000	MHz	
T_C	Period	0.50	1.66	ns	
Processor (CPU) Clock					
F_C	Frequency	400	1000	MHz	1
T_C	Period	1	2.5	ns	
MemClkOut and PLB Clock					
F_C	Frequency	133.33	200	MHz	
T_C	Period	5	7.5	ns	
T_{CH}	High time	45% of nominal period	55% of nominal period	ns	
OPB Clock and PerClk					
F_C	Frequency	33	100	MHz	
T_C	Period	10	30	ns	

Notes:

1. The maximum supported processor clock frequency for any part is specified in the part number (see “Ordering and PVR Information” on page 4).

Figure 4. Timing Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC460GT. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as *tracking skew*. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC460GT the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC460GT with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed −1%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board PPC460GT peripherals impose more stringent requirements.
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the DDR SDRAM MemClkOut signal since it also tracks the modulation.
- For PCI Express, the maximum spread spectrum is -0.5%**,** modulated between 30kHz and 33kHz. The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates.
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.

Important: It is up to the system designer to ensure that any SSCG used with the PPC460GT meets the above requirements and does not adversely affect other aspects of the system.

I/O Specifications

Table 17. Peripheral Interface Clock Timings (Part 1 of 2)

Parameter	Minimum	Maximum	Units	Notes
PCI0Clk frequency	–	66.66	MHz	
PCI0Clk period	15	–	ns	
PCI0Clk high time	40% of nominal period	60% of nominal period	ns	
PCI0Clk low time	40% of nominal period	60% of nominal period	ns	
GMCMDClk frequency	–	2.5	MHz	
GMCMDClk period	400	–	ns	
GMCMDClk high time	160	–	ns	
GMCMDClk low time	160	–	ns	
GMCnGTxClk frequecy	2.5	125	MHz	
GMCnGTxClk period	8	400	ns	
GMCnTxClk frequency	2.5	25	MHz	
GMCnTxClk period	40	400	ns	
GMCnTxClk high time	35% of nominal period	–	ns	
GMCnTxClk low time	35% of nominal period	–	ns	
GMCnRxClk frequency	2.5	125	MHz	
GMCnRxClk period	8	400	ns	
GMCnRxClk high time	35% of nominal period	–	ns	
GMCnRxClk low time	35% of nominal period	–	ns	
GMCRefClk frequency	125	125	MHz	
GMCRefClk period	8	8	ns	
GMCRefClk high time	40% of nominal period	60% of nominal period	ns	
GMCRefClk low time	40% of nominal period	60% of nominal period	ns	
GMCRefClk rise time	–	1	ns	
GMCRefClk cycle-to-cycle jitter	–	±0.1	ns	
SGMIIRxClk frequency	625	625	MHz	
RMIIRefClk frequency	50	50	MHz	
RMIIRefClk accuracy	–	±50	ppm	
RMIIRefClk period	20	20	ns	
RMIIRefClk high time	35% of nominal period	–	ns	
RMIIRefClk low time	35% of nominal period	–	ns	
SMIIRefClk frequency	125	125	MHz	
SMIIRefClk accuracy	–	100	ppm	

Table 17. Peripheral Interface Clock Timings (Part 2 of 2)

Parameter	Minimum	Maximum	Units	Notes
PerClk frequency	33	100	MHz	
PerClk period	10	30	ns	
PerClk high time	50% of nominal period	66% of nominal period	ns	
PerClk low time	33% of nominal period	50% of nominal period	ns	
SPIClkOut frequency	??	??	MHz	
IICSClk frequency	–	400	kHz	
TmrClk frequency	–	100	MHz	
TmrClk period	10	–	ns	
TmrClk high time	40% of nominal period	60% of nominal period	ns	
TmrClk low time	40% of nominal period	60% of nominal period	ns	
TrcClk frequency	CPU $F_C/4$	CPU $F_C/4$	MHz	
UARTSerClk frequency	–	$1000/(2T_{OPB}^{1} + 2ns)$	MHz	1
UARTSerClk period	$2T_{OPB}^{1} + 2$	–	ns	1
UARTSerClk high time	$T_{OPB}^{1}+1$	–	ns	1
UARTSerClk low time	$T_{OPB}^{1}+1$	–	ns	1

Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at 1/2 the frequency of the PLB clock.

Figure 5. Input Setup and Hold Waveform

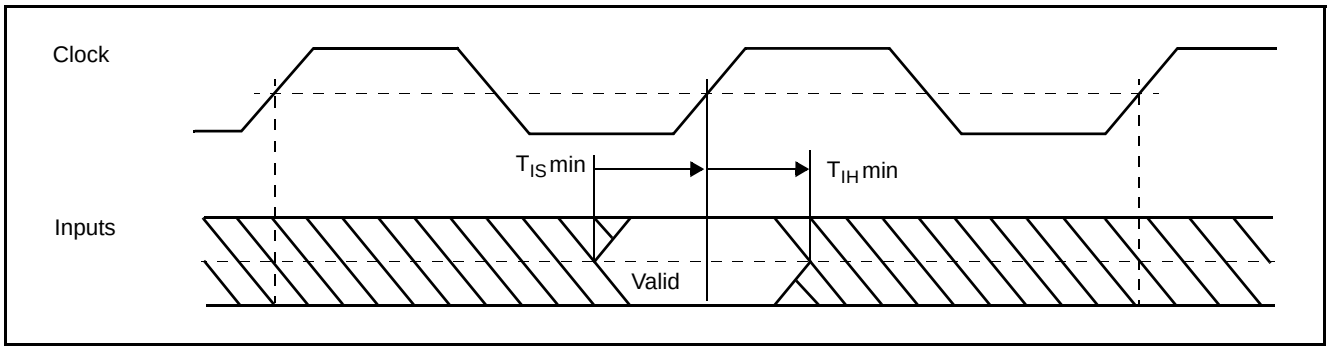


Figure 6. Output Delay and Float Timing Waveform

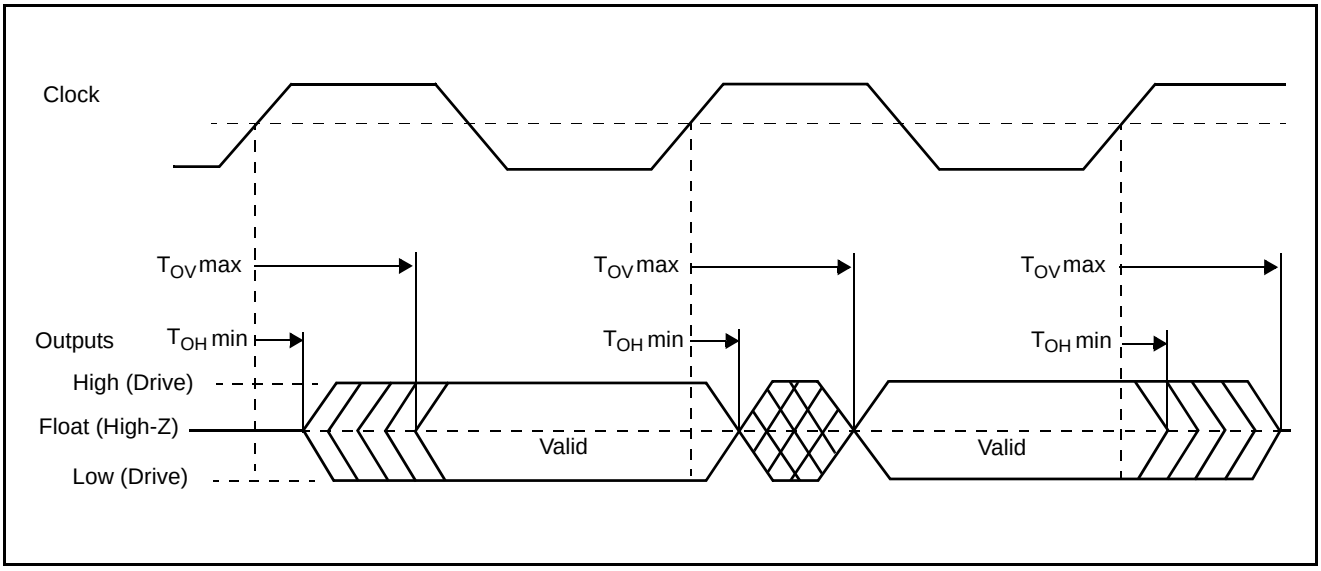
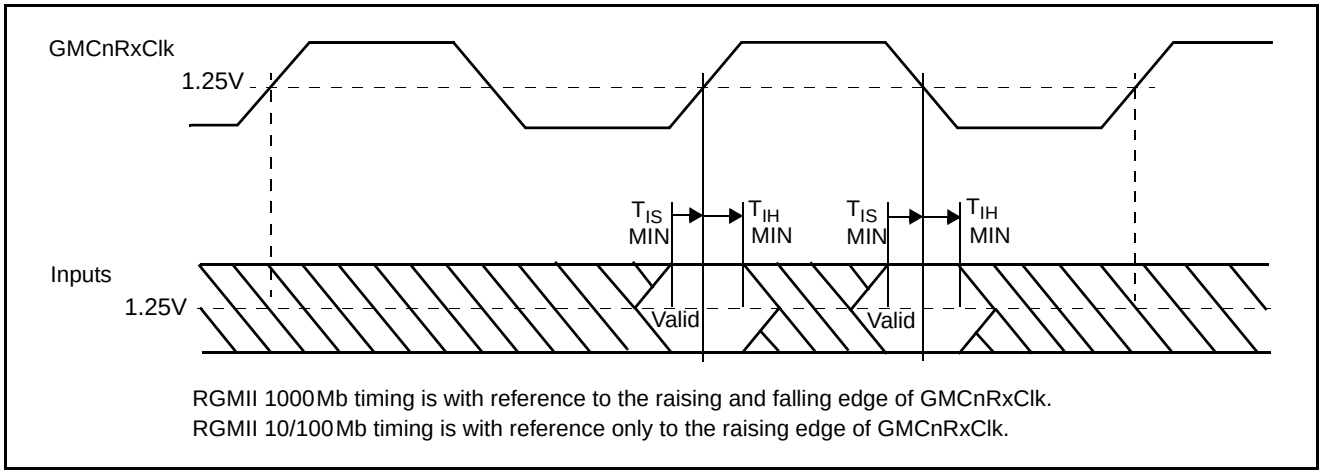
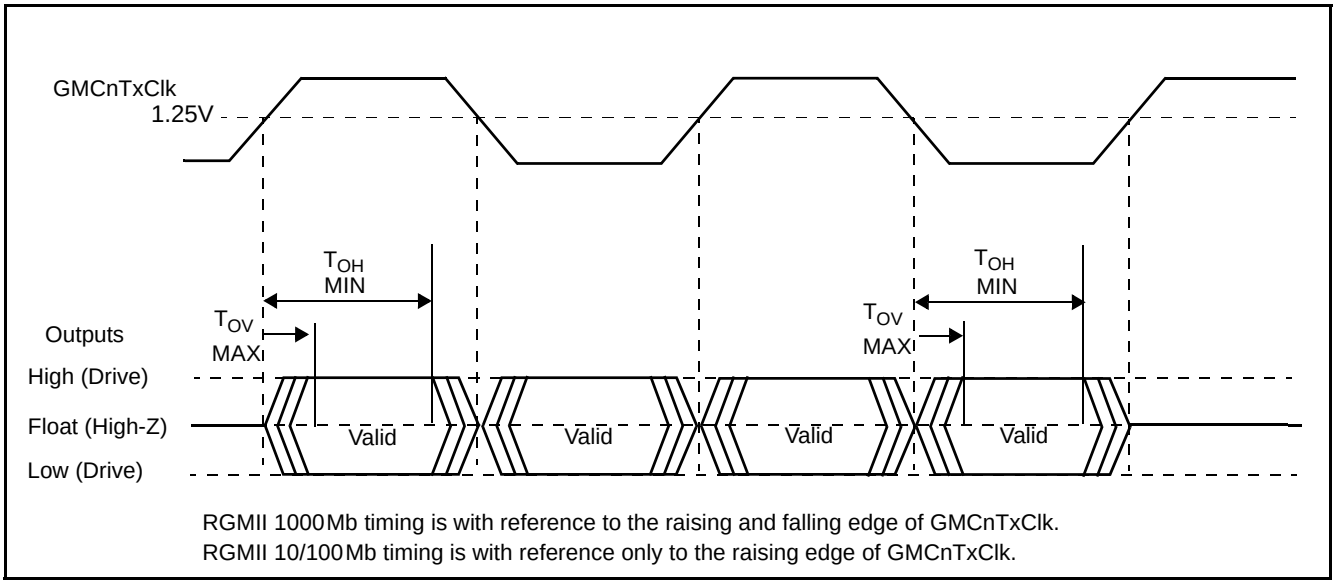


Figure 7. Input Setup and Hold Timing Waveform for RGMII Signals



RGMII 1000Mb timing is with reference to the raising and falling edge of GMCnRxClk.
RGMII 10/100Mb timing is with reference only to the raising edge of GMCnRxClk.

Figure 8. Output Delay and Hold Timing Waveform for RGMII Signals



RGMII 1000Mb timing is with reference to the raising and falling edge of GMCnTxClk.
RGMII 10/100Mb timing is with reference only to the raising edge of GMCnTxClk.

Table 18. I/O Specifications—All Speeds (Part 1 of 3)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. TDO timing is referenced to the falling edge of TCK.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
PCI Interface								
$\overline{\text{PCI0Reset}}$	n/a	n/a	n/a	n/a	0.5	1.5		async
PCI0Clk	dc	dc			na	na	66MHz	
PCI0AD00:31	2.5	0	5.5	2	0.5	1.5	PCI0Clk	
PCI0C0:3/$\overline{\text{BE0:3}}$	2.4	0	6	2	0.5	1.5	PCI0Clk	
PCI0Par	2.5	0	5.5	2	0.5	1.5	PCI0Clk	
$\overline{\text{PCI0Frame}}$	2.8	0	6	2	0.5	1.5	PCI0Clk	
$\overline{\text{PCI0DevSel}}$	2.1	0	6	2	0.5	1.5	PCI0Clk	
$\overline{\text{PCI0IRDY}}$	2.7	0	6	2	0.5	1.5	PCI0Clk	
$\overline{\text{PCI0TRDY}}$	2.9	0	6	2	0.5	1.5	PCI0Clk	
$\overline{\text{PCI0Stop}}$	2.5	0	6	2	0.5	1.5	PCI0Clk	
$\overline{\text{PCI0PErr}}$	2.4	0	6	2	0.5	1.5	PCI0Clk	
$\overline{\text{PCI0SErr}}$	2.1	0	6	2	0.5	1.5	PCI0Clk	
PCI0IDSel	2.2	0	n/a	n/a	na	na	PCI0Clk	
$\overline{\text{PCI0Req0:3}}$	2.3	0	n/a	n/a	na	na	PCI0Clk	
$\overline{\text{PCI0Gnt0:3}}$	n/a	n/a	6	2	0.5	1.5	PCI0Clk	
$\overline{\text{PCI0INT}}$	n/a	n/a	5.8	2	0.5	1.5		async
PCI Express Interface								
PCIEnRx0:3 $\overline{\text{PCIEnRx0:3}}$							PCIEnRefClk	
$\overline{\text{PCIEnTx0:3}}$ PCIEnTx0:3							PCIEnRefClk	
Ethernet MII Interface								
GMCMDIO	n/a	n/a	n/a	n/a	5.51	7.23	GMCMDClk	1
GMC0:1TxD3:0	n/a	n/a	7	1	5.51	7.23	GMC0:1TxClk	
GMC0:1TxEn	n/a	n/a	6	1	5.51	7.23	GMC0:1TxClk	
GMC0:1TxEr	n/a	n/a	6	1	5.51	7.23	GMC0:1TxClk	
GMC0:1CD	10	10	n/a	n/a	n/a	n/a	GMC0:1RxClk	
GMC0:1Crs	10	10	n/a	n/a	n/a	n/a	GMC0:1RxClk	
GMC0:1RxD3:0	6	10	n/a	n/a	n/a	n/a	GMC0:1RxClk	
GMC0:1RxDV	5	10	n/a	n/a	n/a	n/a	GMC0:1RxClk	
GMC0:1RxEr	6	10	n/a	n/a	n/a	n/a	GMC0:1RxClk	
Ethernet GMII Interface								
GMCMDIO	n/a	n/a	n/a	n/a	5.51	7.23	GMCMDClk	1
GMC0:1TxD7:0	n/a	n/a	3	2	5.51	7.23	GMC0:1GTxClk	
GMC0:1TxEn	n/a	n/a	3	2	5.51	7.23	GMC0:1GTxClk	
GMC0:1TxEr	n/a	n/a	2	2	5.51	7.23	GMC0:1GTxClk	
GMC0:1CD	2	0	n/a	n/a	n/a	n/a	GMC0:1RxClk	
GMC0:1Crs	2	0	n/a	n/a	n/a	n/a	GMC0:1RxClk	
GMC0:1RxD7:0	2	0	n/a	n/a	n/a	n/a	GMC0:1RxClk	
GMC0:1RxDV	1.9	0	n/a	n/a	n/a	n/a	GMC0:1RxClk	
GMC0:1RxEr	1.9	0	n/a	n/a	n/a	n/a	GMC0:1RxClk	

Table 18. I/O Specifications—All Speeds (Part 2 of 3)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. TDO timing is referenced to the falling edge of TCK.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
Ethernet RGMII Interface								
GMCMDIO	n/a	n/a	n/a	n/a	5.51	7.23	GMCMDClk	1
GMC0:3TxD3:0	n/a	n/a	0.5	3.5	5.51	7.23	GMC0:1TxClk	
GMC0:3TxCtl	n/a	n/a	0.5	3.5	5.51	7.23	GMC0:1TxClk	
GMC0:3RxD3:0	1	1	n/a	n/a	n/a	n/a	GMC0:1RxClk	
GMC0:3RxCtl	1	1	n/a	n/a	n/a	n/a	GMC0:1RxClk	
Ethernet SGMII Interface								
SGMII0:2RxD $\overline{\text{SGMII0:2RxD}}$	tbd	tbd	n/a	n/a	n/a	n/a	SGMII0RxClk	
SGMII0:2TxD $\overline{\text{SGMII0:2TxD}}$	n/a	n/a	tbd	tbd	3.35	3.35	SGMIITxClk	
Ethernet SMII Interface								
GMCMDIO	10	10	10	1.5	5.51	7.23	GMCMDClk	
SMIISync	na	na	4.8	1	5.51	7.23	SMIIRefClk	
SMII0:3TxD	n/a	n/a	4.9	1	5.51	7.23	SMIIRefClk	
SMII0:3RxD	1	1	n/a	n/a	n/a	n/a	SMIIRefClk	
Ethernet RMII Interface								
RMII0:3CrsDV			n/a	n/a			RMIIRefClk	
RMII0:3RxD1:0			n/a	n/a			RMIIRefClk	
RMII0:3TxD1:0	n/a	n/a			5.51	7.23	RMIIRefClk	
RMII0:3TxEn	n/a	n/a			5.51	7.23	RMIIRefClk	
RMII0:3Er			n/a	n/a			RMIIRefClk	
Internal Peripheral Interface								
IIC0:1SData	5	1.5	5	0	15.75	10.46	IIC0:1SClk	
SPIDI	5	1.5	n/a	n/a	n/a	n/a	SCPClkOut	
SPIDO	n/a	n/a	7	0	15.75	10.46	SCPClkOut	
$\overline{\text{UARTnDCD}}$	n/a	n/a	n/a	n/a	na	na	UARTSerClk	
$\overline{\text{UARTnDSR}}$	n/a	n/a	n/a	n/a	na	na	UARTSerClk	
$\overline{\text{UARTnCTS}}$	n/a	n/a	n/a	n/a	na	na	UARTSerClk	
$\overline{\text{UARTnRTS}}$	n/a	n/a	n/a	n/a	11.08	7.37	UARTSerClk	
$\overline{\text{UARTnDTR}}$	n/a	n/a	n/a	n/a	11.08	7.37	UARTSerClk	
$\overline{\text{UARTnRI}}$	n/a	n/a	n/a	n/a	na	na	UARTSerClk	
UARTnRx	n/a	n/a	n/a	n/a	na	na	UARTSerClk	
UARTnTx	n/a	n/a	n/a	n/a	11.08	7.37	UARTSerClk	
Interrupts Interface								
IRQ0:15	na	na	na	na	na	na		
JTAG Interface								
TCK	n/a	n/a	n/a	n/a	na	na	40 MHz	max
TDI	2	5.5	n/a	n/a	na	na	TCK	
TDO	n/a	n/a	9.5	1	11.08	7.37	TCK	2
TMS	2	5.5	n/a	n/a	na	na	TCK	
$\overline{\text{TRST}}$	n/a	n/a	n/a	n/a	na	na		async

Table 18. I/O Specifications—All Speeds (Part 3 of 3)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. TDO timing is referenced to the falling edge of TCK.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
System Interface								
SysClk	n/a	n/a	n/a	n/a	na	na		
$\overline{\text{SysReset}}$	n/a	n/a	n/a	n/a	na	na		async
SysErr	n/a	n/a	n/a	n/a	11.08	7.37		async
TmrClk	n/a	n/a	n/a	n/a	na	na		async
$\overline{\text{Halt}}$	n/a	n/a	n/a	n/a	na	na		async
$\overline{\text{TestEn}}$	n/a	n/a	n/a	n/a	na	na		async
Trace Interface								
TrcBS0:2	n/a	n/a	1.5	1	11.08	7.37	TrcClk	
TrcES0:4	n/a	n/a	1.6	1	11.08	7.37	TrcClk	
TrcTS0:6	n/a	n/a	1.7	1	11.08	7.37	TrcClk	

Table 19. I/O Specifications—400MHz to 1000MHz

Notes:
1. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 1.3ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
External Slave Peripheral Interface								
DMAReq0:3	4	1	n/a	n/a	na	na	PerClk	
DMAAck0:3	n/a	n/a	5.3	1	11.08	7.37	PerClk	
EOT0:3/TC0:3	4	1	5.3	1	11.08	7.37	PerClk	
PerAddr02:31	n/a	n/a	4.5	1	11.08	7.37	PerClk	
PerData00:31	2	1	4.9	1	11.08	7.37	PerClk	
PerPar0:3	2	1	4.9	1	11.08	7.37	PerClk	
$\overline{\text{PerWBE0:3}}$	n/a	n/a	4.8	1	11.08	7.37	PerClk	
$\overline{\text{PerCS0:5}}$	n/a	n/a	5.3	1	11.08	7.37	PerClk	
PerR/$\overline{\text{W}}$	n/a	n/a	4.5	1	11.08	7.37	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	4.5	1	11.08	7.37	PerClk	
PerReady	2	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerBLast}}$	n/a	n/a	4.5	1	11.08	7.37	PerClk	
PerErr	2	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{ExtReset}}$	n/a	n/a	n/a	n/a	11.08	7.37		async
NAND Flash Interface								
$\overline{\text{NFCE0:3}}$	n/a	n/a	5.3	1	11.08	7.37	PerClk	
NFCLE	n/a	n/a	5.3	1	11.08	7.37	PerClk	
NFALE	n/a	n/a	5.3	1	11.08	7.37	PerClk	
$\overline{\text{NFREn}}$	n/a	n/a	5.3	1	11.08	7.37	PerClk	
$\overline{\text{NFWEn}}$	n/a	n/a	5.3	1	11.08	7.37	PerClk	
$\overline{\text{NFRdyBusy}}$	2	1	n/a	n/a	na	na	PerClk	

DDR2/1 SDRAM I/O Specifications

The DDR SDRAM controller times its operation using the internal PLB clock signal and generates MemClkOut from the PLB clock. The PLB clock is an internal signal that cannot be directly observed. However MemClkOut is the same frequency as the PLB clock signal and is in phase with the PLB clock signal.

Note: MemClkOut can be advanced with respect to the PLB clock by means of the SDRAM0_CLKTR programming register. In a typical system, users advance MemClkOut by 90°. This depends on the specific application and requires a thorough understanding of the memory system in general (refer to the DDR SDRAM Controller chapter in the *PowerPC 460GT Embedded Processor User's Manual*).

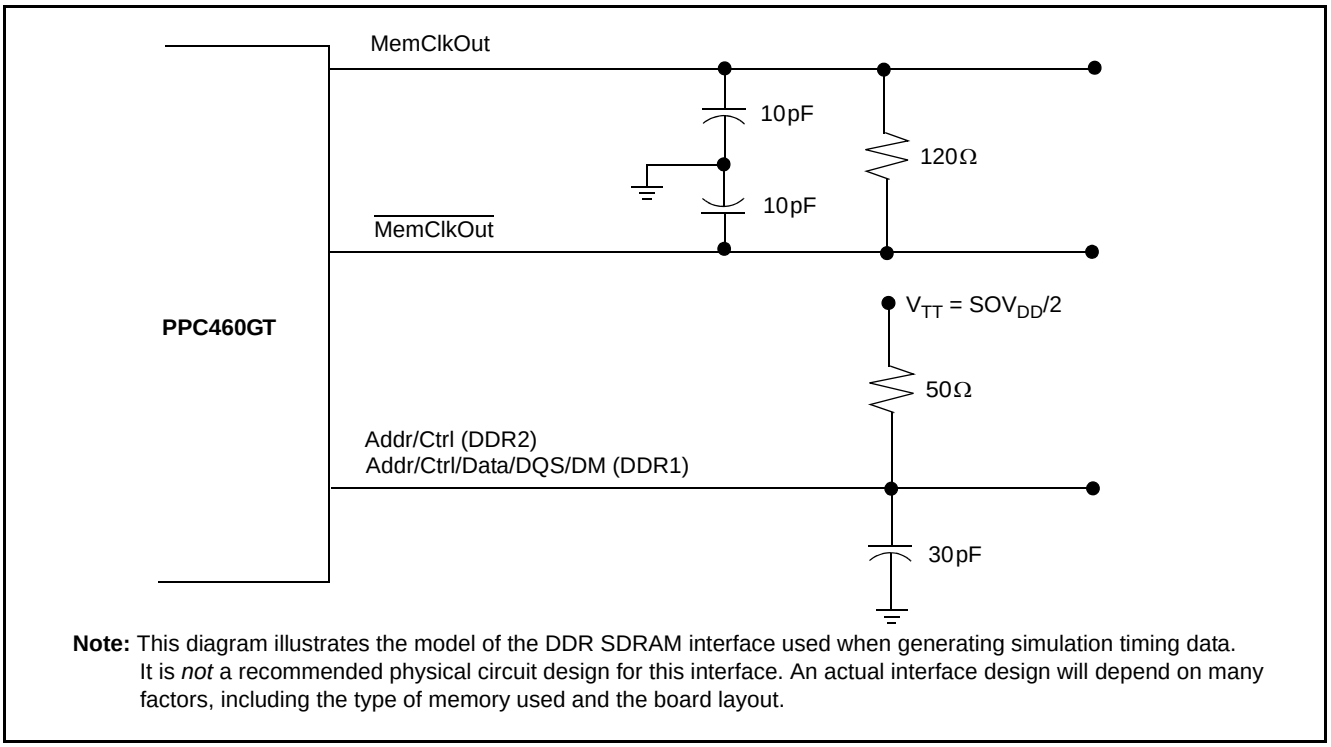
The following DDR data is generated by means of *simulation* and includes logic, driver, package RLC, and lengths. It is not to be used as a circuit design recommendation. Values are calculated over best case and worst case processes with speed, temperature, and voltage as follows:

Best Case = Fast process: -40°C, +1.3V

Worst Case = Slow process: +105°C, +1.2

Note: In all the following DDR tables and timing diagrams, *minimum* values are measured under best case conditions and *maximum* values are measured under worst case conditions. The signals are terminated as indicated in the figure below for the DDR timing data in the following sections.

Figure 9. DDR SDRAM Simulation Signal Termination Model



Note: This diagram illustrates the model of the DDR SDRAM interface used when generating simulation timing data. It is *not* a recommended physical circuit design for this interface. An actual interface design will depend on many factors, including the type of memory used and the board layout.

DDR2 SDRAM On-Die Termination Impedance Setting

For all DDR2 applications, the On-Die Termination (ODT) impedance value *must* be set to 75 ohms in the DIMM Extended Mode Register (EMR) in order to optimize the data transmission during memory write operations.

Table 20. DDR SDRAM Output Driver Specifications

Signal Path	Output Current (mA)	
	I/O H (maximum)	I/O L (maximum)
Write Data		
MemData00:63	10	10
ECC0:7	10	10
DM0:8	10	10
MemClkOut	10	10
MemAddr00:13	10	10
BA0:2	10	10
$\overline{\text{RAS}}$	10	10
$\overline{\text{CAS}}$	10	10
$\overline{\text{WE}}$	10	10
$\overline{\text{BankSel0:1}}$	10	10
ClkEn	10	10
DQS0:8	10	10
MemODT0:1	10	10

DDR SDRAM Write Operation

The rising edge of MemClkOut aligns with the first rising edge of the DQS signal on writes. The following data is generated by means of simulation and includes logic, driver, package RLC, and lengths. Values are calculated over best case and worst case processes with speed, junction temperature, and voltage as follows:

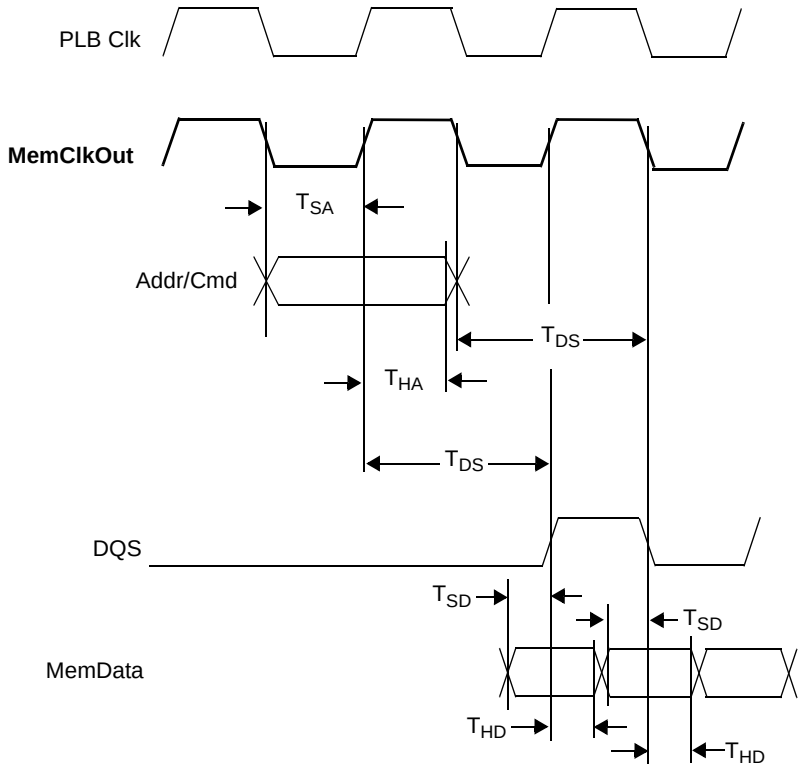
Table 21. DDR SDRAM Write Operation Conditions

Case	Process Speed	Junction Temperature (°C)	Voltage (V)
Best	Fast	–40	+1.3
Worst	Slow	+105	+1.2

Note: In the following tables and timing diagrams, minimum values are measured under best case conditions and maximum values are measured under worst case conditions. The timing numbers in the following sections are obtained using a simulation that assumes a model as shown in *Figure 9*.

The following diagram illustrates the relationship among the signals involved with a DDR write operation.

Figure 10. DDR SDRAM Write Cycle Timing



T_{SA} = Setup time for address and command signals to MemClkOut
T_{HA} = Hold time for address and command signals from MemClkOut
T_{SD} = Setup time for data signals (minimum time data is valid *before* rising/falling edge of DSQ)
T_{HD} = Hold time for data signals (minimum time data is valid *after* rising/falling edge of DSQ)
T_{DS} = Delay from rising/falling edge of clock to the rising/falling edge of DQS

Note: The timing data in the following tables is based on simulation runs using Einstimer.

Table 22. I/O Timing—DDR SDRAM T_{DS}

Notes:
1. All of the DQS signals are referenced to MemClkOut with the DQS delay line programmed to 1 cycle.
2. Clock speed is 200MHz.

Signal Name	T_{DS} (ns)	
	Minimum	Maximum
DQS0	4.9	5.1
DQS1	4.9	5.1
DQS2	4.9	5.1
DQS3	4.9	5.1
DQS4	4.9	5.1
DQS5	4.9	5.1
DQS6	4.9	5.1
DQS7	4.9	5.1
DQS8	4.9	5.1

Table 23. I/O Timing—DDR SDRAM T_{SA}, and T_{HA}

Notes:
1. Clock speed is 200MHz. T_{SA} and T_{HA} are referenced to MemClkOut rising edge.
2. The timing in this table assumes a single registered DIMM load on the outputs.
3. To obtain adjusted T_{SA} values for lower clock frequencies, use 1/2 of the cycle time for the lower clock frequency.
4. To obtain adjusted T_{HA} values for lower clock frequencies, use 1/2 of the cycle time for the lower clock frequency.

Signal Name	T_{SA} (ns)	T_{HA} (ns)
	Minimum	Minimum
MemAddr00:13	+2.3	+2.3
BA0:2		
BankSel0:1		
ClkEn		
$\overline{CAS}$		
$\overline{RAS}$		
$\overline{WE}$		

Table 24. I/O Timing—DDR SDRAM Write Timing T_{SD} and T_{HD}

Notes:
1. T_{SD} and T_{HD} are measured under worst case conditions.
2. Clock speed for the values in the table is 200MHz.
3. The time values in the table include 1/4 of a cycle at 200MHz.
4. To obtain adjusted T_{SD} and T_{HD} values for lower clock frequencies, subtract 1.25 ns from the values in the table and add 1/4 of the cycle time for the lower clock frequency (for example, $T_{SD} - 1.25 + 0.25T_{CYC}$).

Signal Names	Reference Signal	T_{SD} (ns)	T_{HD} (ns)
MemData00:07, DM0	DQS0	0.96	0.995
MemData08:15, DM1	DQS1	0.97	0.990
MemData16:23, DM2	DQS2	0.98	0.980
MemData24:31, DM3	DQS3	0.98	0.980
MemData32:39, DM4	DQS4	0.98	0.980
MemData40:47, DM5	DQS5	0.97	0.983
MemData48:55, DM6	DQS6	0.96	0.985
MemData56:63, DM7	DQS7	0.96	0.982
ECC0:7, DM8	DQS8	0.96	0.980

DDR SDRAM Read Operation

Data on a read is edge aligned with the DQS. To capture the incoming data on the rising and falling edges, DQS is delayed by the DDR controller in order to center a DQS edge on valid data.

Figure 11 shows the data read path of a single data bit. Data entering on the left is captured in the Stage 1 Flip Flops. The four Flip Flops in Stage 1 capture a 4-beat burst on the DDR interface. Data captured on the rising edge of DQS is stored in the even numbered Flip Flops. Likewise, data captured on the falling edge of DQS is stored in the odd numbered Flips Flops. To latch the data in Stage 1, a delayed version of DQS is used. Initialization software is responsible for tuning the DQS delay timing so that DQS is centered on valid data. Since there is process variation between parts and possible voltage variations on boards, read tuning is required. Fixed DQS delay values should not be used on production systems.

The Feedback Data Capture Window in *Figure 11* selects which Flip Flop is used to store the data sampled by DQS. Each output of this block generates a pulse to an input multiplexer. The series of four pulses selecting the input multiplexer is initiated by a feedback signal pulse on the input of the Feedback Data Capture Window. The DDR controller calculates when to assert the feedback signal based on when the data should be present after a read command.

The width of the feedback pulse is one DDR 1X clock period. The internal DDR 1X clock is the same frequency as MemClkOut0:1.

The feedback signal to the Feedback Data Capture Window is adjusted for propagation delay by the fine/coarse delays and is able to automatically track variations in the DDR I/O due to supply voltage and temperature. Compensation for driver/receiver variations is accomplished by driving and receiving the feedback signal on the external MemDCFdbkD and MemDCFdbkR pins. When properly tuned, the feedback pulse is aligned to the first DQS in a 4-beat burst such that the rising edge of DQS is nominally centered on the feedback pulse.

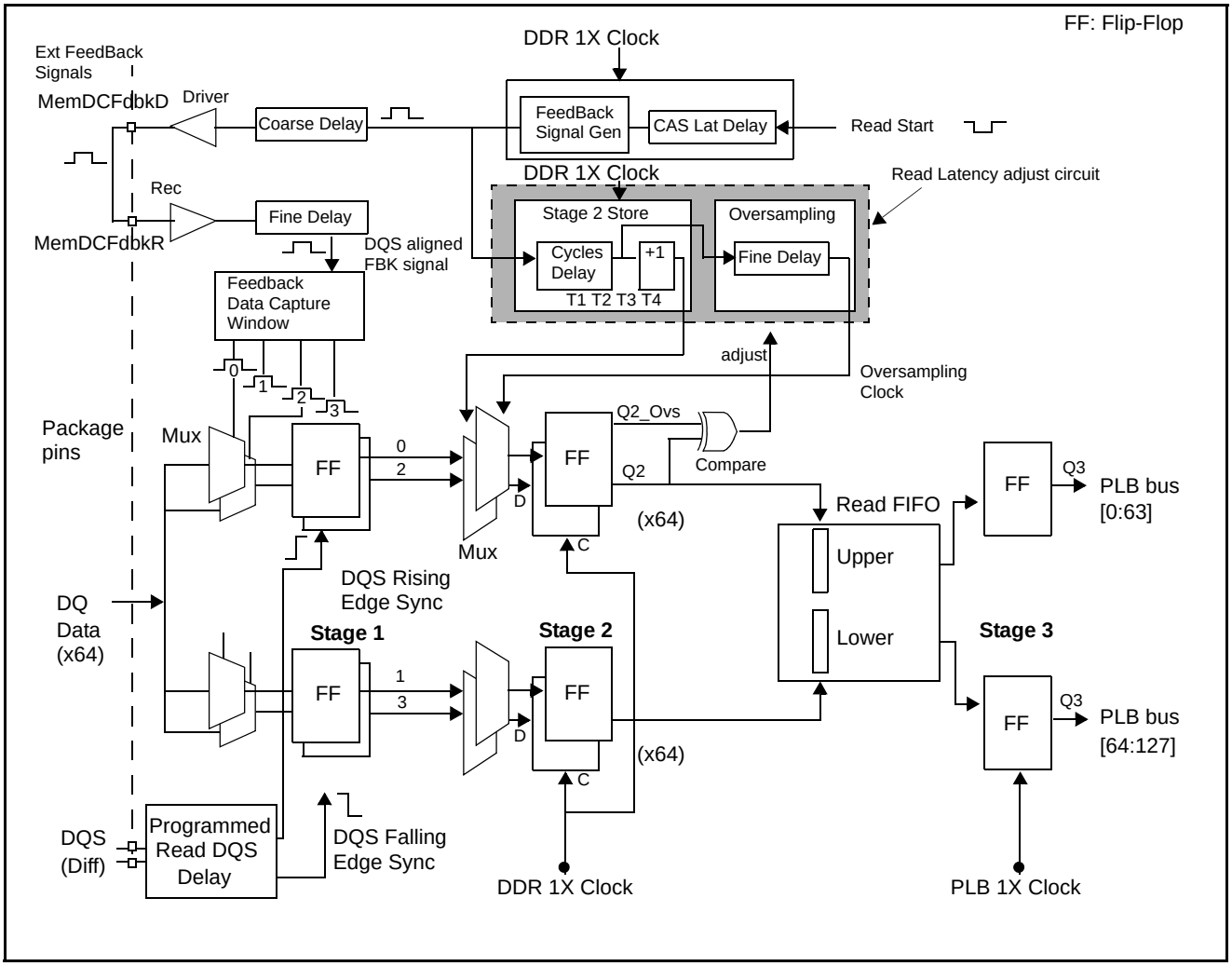
Note: Using minimum trace length, connect MemDCFdbkD directly to MemDCFdbkR

The data captured in Stage 1 is relative to the DQS timing domain and is held for four MemClkOut clock cycles. Stage 2 samples the data in Stage 1 attempting to capture the data in the DDR 1x domain. The on-time-sample clock from the Stage 2 Store block samples the Stage 1 data at sample cycle T1, T2, T3 or T4. The sample cycle is either selected by initialization software or can be automatically selected and adjusted by the DDR controller. The Stage 1 data is sampled a second time by the over sample clock at a delayed sample point. The delay between the on-time-sample and over sample clocks is the Over-Sampling-Guard-Band.

The feedback pulse is sampled with the data captured by the first DQS in the 4-beat burst. Capturing the data with the feedback pulse is considered a hit. The DDR controller based on hits or misses by the on-time sample and over sample clocks adjust the sample cycle in order to track variations in DQS. Burst data from a sample hit is passed to Stage 3.

In Stage 3 data is synchronized to the PLB clock domain and eventually driven onto the PLB bus. The data captured on the rising and falling DQS edges is unpacked into the correct bit locations on the upper (0:63) and lower (64:127) PLB bus. When ECC is enable, ECC checking and corrections is done after Stage 3.

Figure 11. DDR SDRAM Read Data Path



DDR SDRAM Read Cycle Timing

The following diagram illustrates the relationship of the signals involved with a DDR read operation.

Figure 12. DDR SDRAM Memory Data and DQS

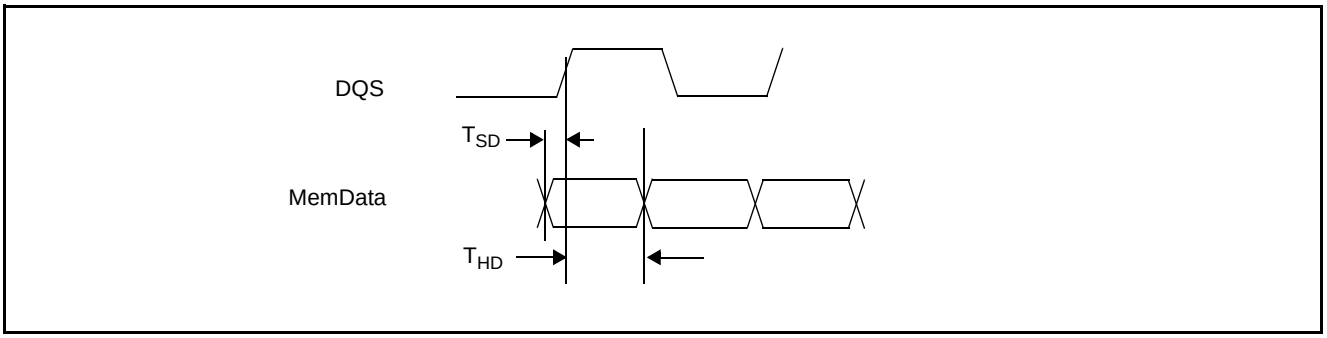


Table 25. I/O Timing—DDR SDRAM Read Timing T_{SD} and T_{HD}

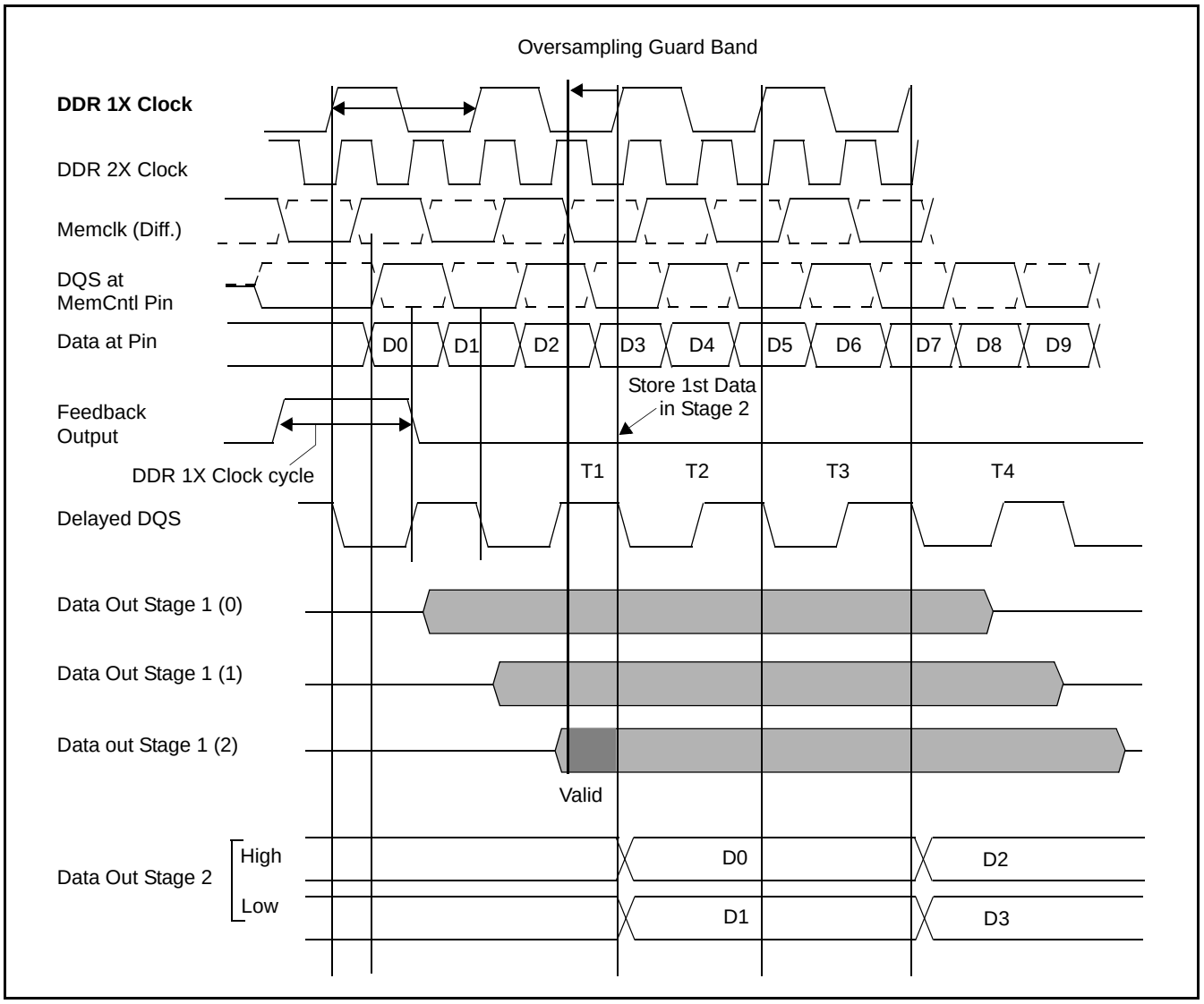
1. T_{SD} and T_{HD} are measured under worst case conditions.
2. Clock speed for the values in the table is 200 MHz.
3. The time values in the table include 1/4 of a cycle at 200 MHz (5 ns x 0.25 = 1.25 ns).
4. To obtain adjusted T_{SD} and T_{HD} values for lower clock frequencies, subtract 0.75 ns from the values in the table and add 1/4 of the cycle time for the lower clock frequency (e.g., T_{SD} - 1.25 + 0.25T_{CYC}).

Signal Names	Reference Signal	Read Data vs DQS Set up T_{SD} (ns)	Read Data vs DQS Hold T_{HD} (ns)
MemData00:07	DQS0	0.393	0311
MemData08:15	DQS1	0.398	0314
MemData16:23	DQS2	0.397	0307
MemData24:31	DQS3	0.396	0309
MemData32:39	DQS4	0.394	0291
MemData40:47	DQS5	0.395	0291
MemData48:55	DQS6	0.393	0295
MemData56:63	DQS7	0.394	0308
ECC0:7	DQS8	0.389	0306

In the following example, the data strobes (DQS) and the data are shown to be coincident. There is actually a slight skew as specified by the SDRAM specifications, and there can be additional skew due to loading and signal routing. It is recommended that the signal length for all of the eight DQS signals be matched.

The following example shows the timing relationship between SDRAM DDR Data at the input pin and storing the data in Stage 1.

Figure 13. DDR SDRAM Read Cycle Timing—Example



Initialization

The PPC460GT provides the option for setting initial parameters based on default values or by reading them from a slave PROM attached to the IIC0 bus (see “Serial EEPROM” below). Some of the default values can be altered by strapping on external pins (see “Strapping” below).

Strapping

While the SysReset input pin is low (system reset), the state of certain I/O pins is read to enable certain default initial conditions prior to PPC460GT start-up. The actual capture instant is the nearest reference clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. These pins are used for strap functions only during reset. Following reset they are used for normal functions. The signal names assigned to the pins for normal operation are shown in parentheses following the pin number.

The following table lists the strapping pins along with their functions and strapping options:

Table 26. Strapping Pin Assignments

Function	Option	Pin Strapping		
		E31 (UART0CTS)	E34 (UART0DCD)	E32 (UART0DSR)
Serial device is disabled. Each of the six options (A–F) is a combination of boot source, boot-source width, and clock frequency specifications. Refer to the IIC Bootstrap Controller chapter in the *PPC460GT Embedded Processor User’s Manual* for details.	A	0	0	0
	B	0	0	1
	C	0	1	0
	D	0	1	1
	E	1	0	0
	F	1	0	1
Serial device is enabled. The option being selected is the IIC0 slave address that will respond with strapping data.	G (0xA8)	1	1	0
	H (0xA4)	1	1	1

Serial EEPROM

During reset, initial conditions other than those obtained from the strapping pins can be read from a ROM device connected to the IIC0 port. At the de-assertion of reset, if the Bootstrap Controller is enabled, the PPC460GT sequentially reads 16B from the ROM device on the IIC0 port and sets the SDR0_SDSTP0:3 registers accordingly.

The initialization settings and their default values are covered in detail in the *PowerPC 460GT Embedded Processor User’s Manual User’s Manual*.

Revision Log

Date	Version	Contents of Modification
10/01/2007	1.00	Initial creation of document.
11/20/2007	1.01	Change all occurrences of PerDataPar to PerPar. Correct signal-to-ball assignments. Remove reference to L2 snooping. Update I/O timing. Add KASUMI to Security features list.
01/04/2008	1.02	Implement Document Issue 441 including: - Add RMII. - Remove tape-and reel shipping option. - Change available CPU speeds.
01/14/2008	1.03	Change maximum case temperature from +105°C to +85°C.
01/30/2008	1.04	Doc issue 450. Doc issue 458.
04/14/2008	1.05	Add block diagram from R/C engineering specification. Reference 802.3 Ethernet spec for GMCMDIO timing. Remove Confidential status and change Advanced to Preliminary. Add FPU. Add power/current estimates. Add missing items to Contents.
05/05/2008	1.06	Delete SAV_{DD} voltage from analog voltage filter diagram (Doc Issue 503). Misc. updates including Doc Issue 512 and 526.
05/29/2008	1.07	Add power sequence information (Doc Issue 455).
07/17/2008	1.08	Doc Issues 530, 531, 536, 550.

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Preliminary Edition (July 17, 2008)
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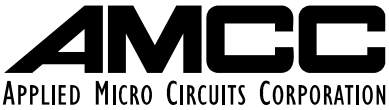

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