440GP

Data Sheet

Power PC 440GP Embedded Processor

Features

- PowerPC® 440 processor core operating up to 500 MHz with 32 KB I- and D-caches
- On-chip 8 KB SRAM
- Selectable processor:bus clock ratios of 3:1, 4:1, 5:1, 5:2, 7:2
- Double Data Rate (DDR) Synchronous DRAM (SDRAM) 32/64-bit interface operating up to 133 MHz
- External Peripheral Bus for up to eight devices with external mastering
- DMA support for external peripherals, internal UART and memory
- PCI-X V1.0a interface (32 or 64 bits, up to 133 MHz) with support for conventional PCI V2.2
- Two Ethernet 10/100 Mbps half- or full-duplex interfaces. Operational modes supported are MII and RMII.
- Programmable Interrupt Controller supports interrupts from a variety of sources.
- Programmable General Purpose Timers (GPT)
- Two serial ports (16750 compatible UART)
- Two IIC interfaces
- General Purpose I/O (GPIO) interface available
- JTAG interface for board level testing
- Internal Processor Local Bus (PLB) runs at DDR SDRAM interface frequency
- Processor can boot from PCI memory
- Available in ceramic (RoHs and non-RoHS compliant versions) and plastic packages.

Description

Designed specifically to address high-end embedded applications, the PowerPC 440GP (PPC440GP) provides a high-performance, low power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and lower power dissipation.

This chip contains a high-performance RISC processor core, DDR SDRAM controller,8KB SRAM, PCI-X bus interface, Ethernet interfaces, control for external ROM and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

Technology: CMOS SA-27E, 0.18 µm (0.11 L_{eff})

Packages: 25 mm, 552-ball Ceramic Ball Grid Array (CBGA) or Plastic Ball Grid Array (PBGA) in standard or RoHS compliant versions

Power (estimated): Less than:
4.0 W in normal mode
1.0 W in sleep mode

Supply voltages required: 3.3 V, 2.5 V, 1.8 V

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Ordering and PVR Information

For information on the availability of the following parts, contact your local AMCC sales office.

Order Part Numbers

Product Name	Order Part Number (See Notes and Key drawing)	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
PPC440GP	PPC440GP-3CC333C	333MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3CC400C	400MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3CC400CZ	400MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3CC400E	400MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3CC400EZ	400MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3CC466C	466MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3CC466CZ	466MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3CC500C	500MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3CC500CZ	500MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3FC400C	400MHz	25mm, 552 PBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3RC333C	333MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3RC400C	400MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3RC400CZ	400MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3RC400E	400MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3RC466C	466MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3RC466CZ	466MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3RC500C	500MHz	25mm, 552 CBGA	C	0x40120481	0x22052049
PPC440GP	PPC440GP-3RC500CZ	500MHz	25mm, 552 CBGA	C	0x40120481	0x22052049

Notes:

1. Package code: C = leaded ceramic, F = plastic, R = reduced-lead ceramic (RoHS compliant),.
2. Case Temperature Range code: C = -40 °C to +85 °C, E = -40 °C to +105 °C for C package and -40 °C to +100 °C for F package.
3. Z at the end of the Order Part Number indicates a tape-and-reel shipping package. Otherwise, the chips are shipped in a tray.
4. Revision code: C = rev 2.1.

Each part number contains a revision code. This is the die mask revision number and is included in the part number for identification purposes only.

The PVR (Processor Version Register) and the JTAG ID register are software accessible (read-only) and contain information that uniquely identifies the part. Refer to the *PPC440GP User's Manual* for details on accessing these registers.

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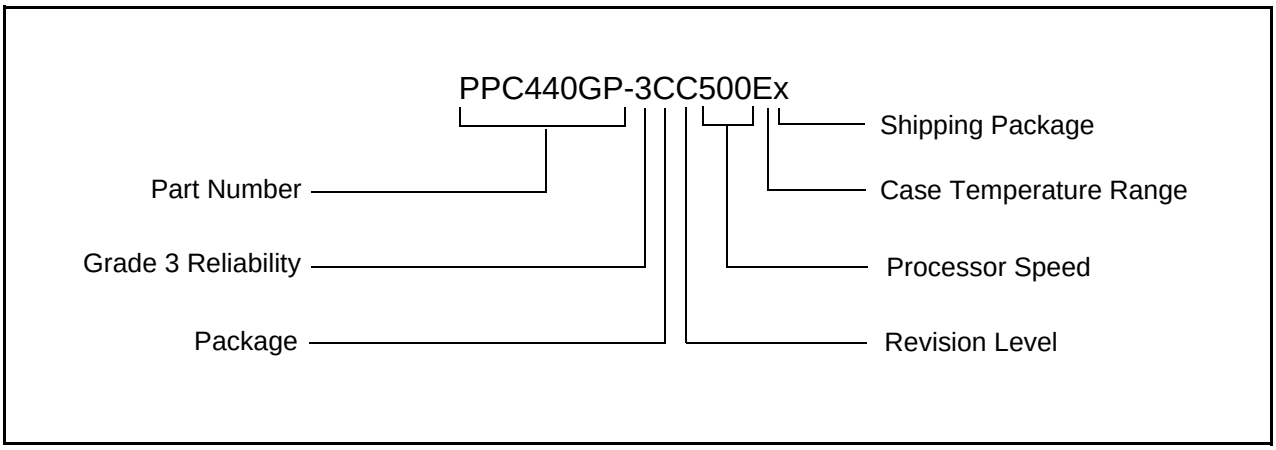
Order Part Number Key



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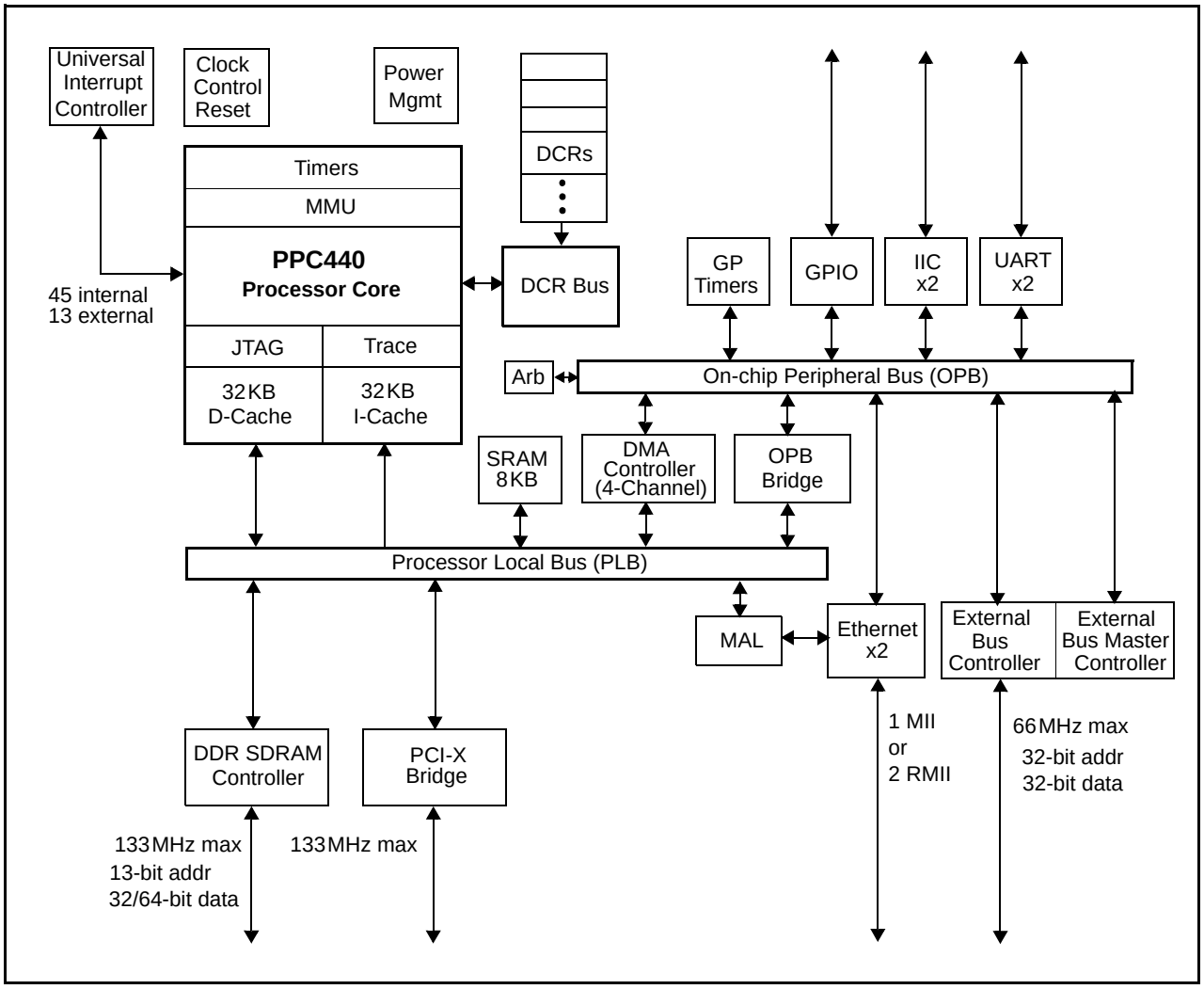
PPC440GP Functional Block Diagram



The PPC440GP is designed using the IBM® Microelectronics Blue Logic™ methodology in which major functional blocks are integrated together to create an application-specific product (ASIC). This approach provides a consistent way to create complex ASICs using IBM CoreConnect Bus™ Architecture.

Note: IBM CoreConnect buses provide:

- 128-bit PLB interfaces up to 133.33MHz
- 32-bit OPB interfaces up to 66.66MHz, 266MB/s

Address Maps

The PPC440GP incorporates two address maps. The first is a fixed processor system memory address map. This address map defines the possible contents of various address regions which the processor can access. The second address map is for Device Configuration Registers (DCRs). The DCRs are accessed by software running on the PPC440GP processor through the use of **mtdcr** and **mfdcr** instructions.

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System Memory Address Map (Sheet 1 of 2)

Function	Sub Function	Start Address	End Address	Size
Local Memory[1]	DDR SDRAM	0 0000 0000	0 7FFF FFFF	2GB
	SRAM	0 8000 0000	0 8000 1FFF	8KB
	Reserve	0 8000 2000	0 FFFF FFFF	
Internal Peripherals	EBC	1 0000 0000	1 3FFF FFFF	1GB
	Reserved	1 4000 0000	1 4000 01FF	
	UART0	1 4000 0200	1 4000 0207	8B
	Reserved	1 4000 0208	1 4000 02FF	
	UART1	1 4000 0300	1 4000 0307	8B
	Reserved	1 4000 0308	1 4000 03FF	
	IIC0	1 4000 0400	1 4000 041F	32B
	Reserved	1 4000 0420	1 4000 04FF	
	IIC1	1 4000 0500	1 4000 051F	32B
	Reserved	1 4000 0520	1 4000 05FF	
	OPB Arbiter	1 4000 0600	1 4000 063F	64B
	Reserved	1 4000 0640	1 4000 06FF	
	GPIO Controller	1 4000 0700	1 4000 077F	128B
	Ethernet PHY ZMII	1 4000 0780	1 4000 078F	16B
	Ethernet PHY GMII	1 4000 0790	1 4000 079F	16B
	Reserved	1 4000 0790	1 4000 07FF	
	Ethernet 0 Controller	1 4000 0800	1 4000 08FF	256B
	Ethernet 1 Controller	1 4000 0900	1 4000 09FF	256B
	General Purpose Timer	1 4000 0A00	1 4000 0AFF	256B
	Reserved	1 4000 0B00	1 EFFF FFFF	
Expansion ROM[2]		1 F000 0000	1 FFDF FFFF	254MB
Boot ROM[2, 3]		1 FFE0 0000	1 FFFF FFFF	2MB

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System Memory Address Map (Sheet 2 of 2)

Function	Sub Function	Start Address	End Address	Size
PCI-X	Reserved	2 0000 0000	2 07FF FFFF	
	PCI-X I/O	2 0800 0000	2 0BFF FFFF	64 MB
	Reserved	2 0C00 0000	2 0EBF FFFF	
	PCI-X External Configuration Registers	2 0EC0 0000	2 0EC0 0007	8 B
	Reserved	2 0EC0 0008	2 0EC7 FFFF	
	PCI-X Bridge Core Configuration Registers	2 0EC8 0000	2 0EC8 00FF	256 B
	Reserved	2 0EC8 0100	2 0EC8 00FF	
	PCI-X Special Cycle	2 0ED0 0000	2 0EDF FFFF	1 MB
	PCI-X Memory	2 0EE0 0000	F FFFF FFFF	55.76 GB

Notes:

1. DDR SDRAM and on-chip SRAM can be located anywhere in the Local Memory area of the memory map.
2. The Boot ROM and Expansion ROM areas of the memory map are intended for use by ROM or Flash-type devices. While locating volatile DDR SDRAM and SRAM in this region is supported, use of these regions for this purpose is not recommended.
3. When the optional boot from PCI-X memory is selected, the PCI-X Boot ROM address space begins at 2 FFFE 0000 (128 KB).

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DCR Address Map 4KB of Device Configuration Registers

Function	Start Address	End Address	Size
Total DCR Address Space[1]	000	3FF	1KW (4KB)[1]
By function:			
Reserved	000	00F	16W
Memory Controller	010	011	2W
External Bus Controller	012	013	2W
External Bus Master I/F	014	015	2W
PLB Performance Monitor	016	01F	10W
SRAM	020	02F	16W
Reserved	030	07F	80W
PLB	080	08F	16W
PLB to OPB Bridge Out	090	09F	16W
Reserved	0A0	0A7	8W
OPB to PLB Bridge In	0A8	0AF	8W
Power Management	0B0	0B7	8W
Reserved	0B8	0BF	8W
Interrupt Controller 0	0C0	0CF	16W
Interrupt Controller 1	0D0	0DF	16W
Clock, Control, and Reset	0E0	0EF	16W
Reserved	0F0	0FF	16W
DMA Controller	100	13F	64W
Reserved	140	17F	64W
Ethernet MAL	180	1FF	128W
Reserved	200	3FF	512W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register. One kiloword (1024W) equals 4KB (4096 bytes).

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PowerPC 440 Processor Core

The PowerPC 440 processor core is designed for high-end applications: RAID controllers, routers, switches, printers, set-top boxes, etc. It is the first processor core to implement the Book E PowerPC embedded architecture and the first to use the 128-bit version of IBM's on-chip CoreConnect Bus Architecture.

Features include:

- Up to 500 MHz operation
- PowerPC Book E architecture
- 32 KB I-cache, 32 KB D-cache
- Three logical regions in D-cache: locked, transient, normal
- D-cache full line flush capability
- 41-bit virtual address, 36-bit (64 GB) physical address
- Superscalar, out-of-order execution
- 7-stage pipeline
- 3 execution pipelines
- Dynamic branch prediction
- Memory management unit
  - 64-entry, full associative, unified TLB
  - Separate instruction and data micro-TLBs
  - Storage attributes for write-through, cache-inhibited, guarded, and big or little endian
- Debug facilities
  - Multiple instruction and data range breakpoints
  - Data value compare
  - Single step, branch, and trap events
  - Non-invasive real-time trace interface
- 24 DSP instructions
  - Single-cycle multiply and multiply-accumulate
  - 32 x 32 integer multiply
  - 16 x 16 -> 32-bit MAC

Internal Buses

The PowerPC 440GP features three IBM standard on-chip buses: the Processor Local Bus (PLB), the On-Chip Peripheral Bus (OPB), and the Device Control Register Bus (DCR). The high performance, high bandwidth cores such as the PowerPC 440 processor core, the DDR SDRAM memory controller, and the PCI-X bridge connect to the PLB. The OPB hosts lower data rate peripherals. The daisy-chained DCR provides a lower bandwidth path for passing status and control information between the processor core and the other on-chip cores.

Features include:

- PLB
  - 128-bit implementation of the PLB architecture
  - Separate and simultaneous read and write data paths
  - 36-bit address
  - Simultaneous control, address, and data phases
  - Four levels of pipelining
  - Byte enable capability supporting unaligned transfers
  - 32- and 64-byte burst transfers
  - 133 MHz, maximum 4.2 GB/s (simultaneous read and write)
  - Processor:bus clock ratios of 3:1, 4:1, 5:1, 5:2, and 7:2

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- OPB
  - Dynamic bus sizing 32-, 16-, and 8-bit data path
  - Separate and simultaneous read and write data paths
  - 36-bit address
  - 66.66MHz, maximum 266MB/s
- DCR
  - 32-bit data path
  - 10 bit address

On-Chip SRAM

Features include:

- One physical bank of 8KB
- Memory cycles supported:
  - Single beat read and write, 1 to 16 bytes
  - 32- and 64-byte burst transfers
  - Guarded memory accesses
- Sustainable 2.1GB/s peak bandwidth at 133MHz

PCI-X Interface

The PCI-X interface allows connection of PCI and PCI-X devices to the PowerPC processor and local memory. This interface is designed to Version 1.0a of the PCI-X Specification and supports 32- and 64-bit PCI-X buses. PCI 32/64-bit conventional mode, compatible with PCI Version 2.2, is also supported.

Reference Specifications:

- PowerPC CoreConnect Bus (PLB) version PLB4
- PCI Specification Version 2.2
- PCI Bus Power Management Interface Specification Version 1.1

Features include:

- PCI-X 1.0a
  - Split transactions
  - Frequency to 133MHz
  - 32- and 64-bit bus
- PCI 2.2 backward compatibility
  - Frequency to 66MHz
  - 32- and 64-bit bus
- Can be the PCI Host Bus Bridge or an Adapter Device's PCI interface
- Internal PCI arbitration function, supporting up to six external devices, that can be disabled for use with an external arbiter
- Support for Message Signaled Interrupts
- Simple message passing capability
- Asynchronous to the PLB
- PCI Power Management 1.1
- PCI register set addressable both from on-chip processor and PCI device sides
- Ability to boot from PCI-X bus memory
- Error tracking/status

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- Supports initiation of transfer to the following address spaces:
  - Single beat I/O reads and writes
  - Single beat and burst memory reads and writes
  - Single beat configuration reads and writes (type 0 and type 1)
  - Single beat special cycles

DDR SDRAM Memory Controller

The Double Data Rate (DDR) SDRAM memory controller supports industry standard 184-pin DIMMs and other discrete devices. Up to four 512MB logical banks are supported in limited configurations. Global memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:

- Registered and non-registered industry standard DIMMs and other discrete devices
- 32- or 64-bit memory interface with optional 8-bit ECC (SEC/DED)
- Sustainable 2.1GB/s peak bandwidth at 133MHz
- SSTL_2 logic
- 1 to 4 chip selects
- CAS latencies of 2, 2.5 and 3 supported
- PC200/266 support
- Page mode accesses (up to eight open pages) with configurable paging policy
- Programmable address mapping and timing
- Hardware and software initiated self-refresh
- Power management (self-refresh, suspend, sleep)

External Peripheral Bus Controller (EBC)

Features include:

- Up to eight ROM, EPROM, SRAM, Flash memory, and slave peripheral I/O banks supported
- Up to 66.66MHz operation (266MB/s)
- Burst and non-burst devices
- 8-, 16-, 32-bit byte-addressable data bus
- 32-bit address, 4GB address space
- Peripheral Device pacing with external “Ready”
- Latch data on Ready, synchronous or asynchronous
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping
- External master interface
  - Write posting from external master
  - Read prefetching on PLB for external master reads
  - Bursting capable from external master
  - Allows external master access to all non-EBC PLB slaves
  - External master can control EBC slaves for own access and control

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Ethernet Controller Interface

Ethernet support provided by the PPC440GP interfaces to the physical layer, but the PHY is not included on the chip.

Features include:

- One or two interfaces running in full- and half-duplex modes at 10Mb/s or 100Mb/s
  - One full Media Independent Interface (MII) with 4-bit parallel data transfer
  - Two Reduced Media Independent Interfaces (RMII) with 2-bit parallel data transfer

DMA Controller

Features include:

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 64-bit addressing
- Address increment or decrement
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

Serial Port

Features include:

- One 8-pin UART and one 4-pin UART interface provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with 16750 register set
- Complete status reporting capability
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

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IIC Bus Interface

Features include:

- Two IIC interfaces provided
- Support for Philips® Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocols
- Programmable error recovery

General Purpose Timers (GPT)

Provides a separate time base counter and additional system timers in addition to those defined in the processor core.

- 32-bit Time Base Counter driven by the OPB bus clock
- Five 32-bit compare timers

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses.
- 31 of the 32 GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose.
- Each GPIO output is separately programmable to emulate an open drain driver (that is, drives to zero, tri-stated if output bit is 1).

Universal Interrupt Controller (UIC)

TwoUniversal Interrupt Controllers (UIC) are available. They provide control, status, and communications necessary between the external and internal sources of interrupts and the on-chip PowerPC processor.

Note: Processor specific interrupts (for example, page faults) do not use UIC resources.

Features include:

- 13 external interrupts
- 45 internal interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to the on-chip processor core
- Programmable interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

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JTAG

Features include:

- IEEE 1149.1 Test Access Port
- IBM RISCWatch Debugger support
- JTAG Boundary Scan Description Language (BSDL)

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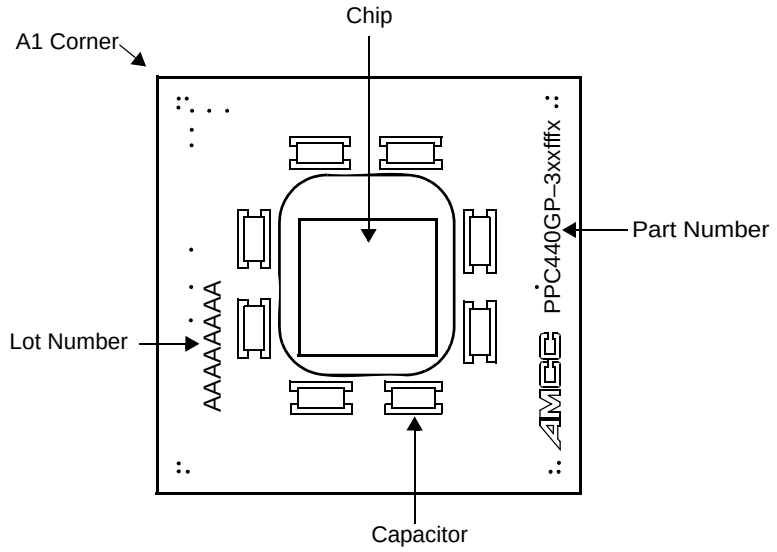
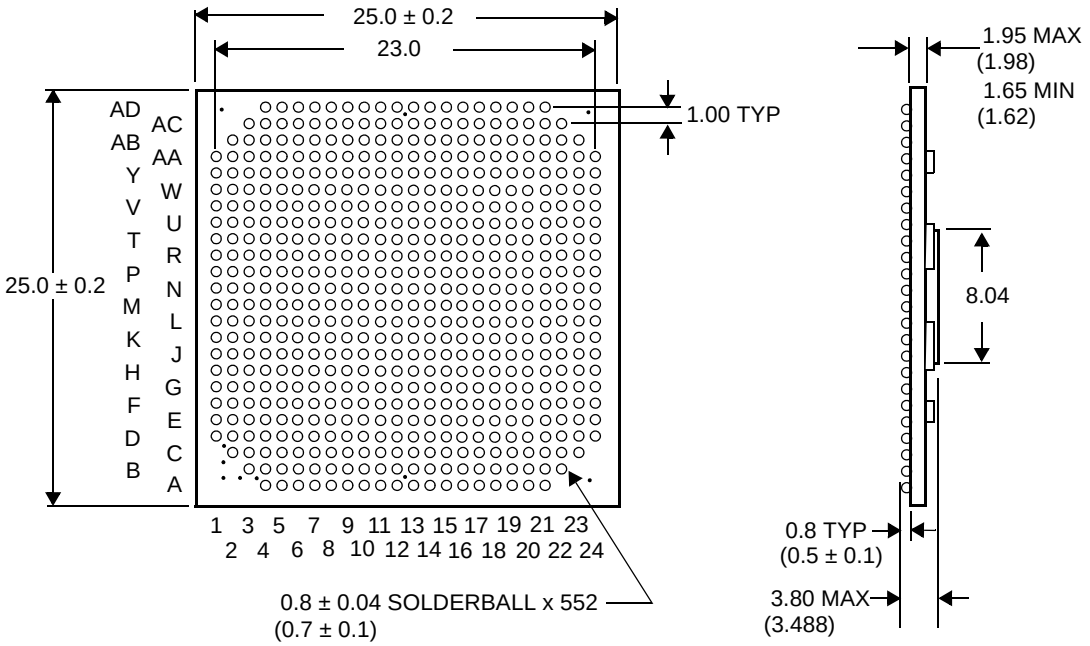
25mm, 552-Ball Ceramic (CBGA) Package

Top View



Notes: 1. All dimensions are in mm.
2. RoHS compliant reduced-lead package available.
3. Reduced-lead package dimensions are in parentheses (dimension).

Bottom View



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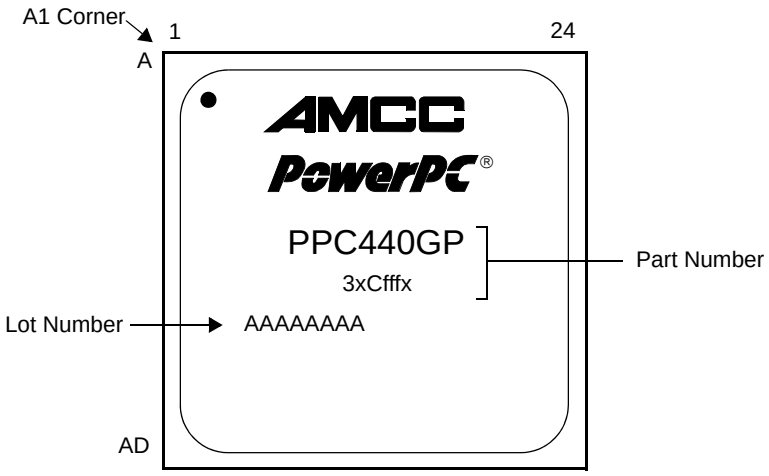
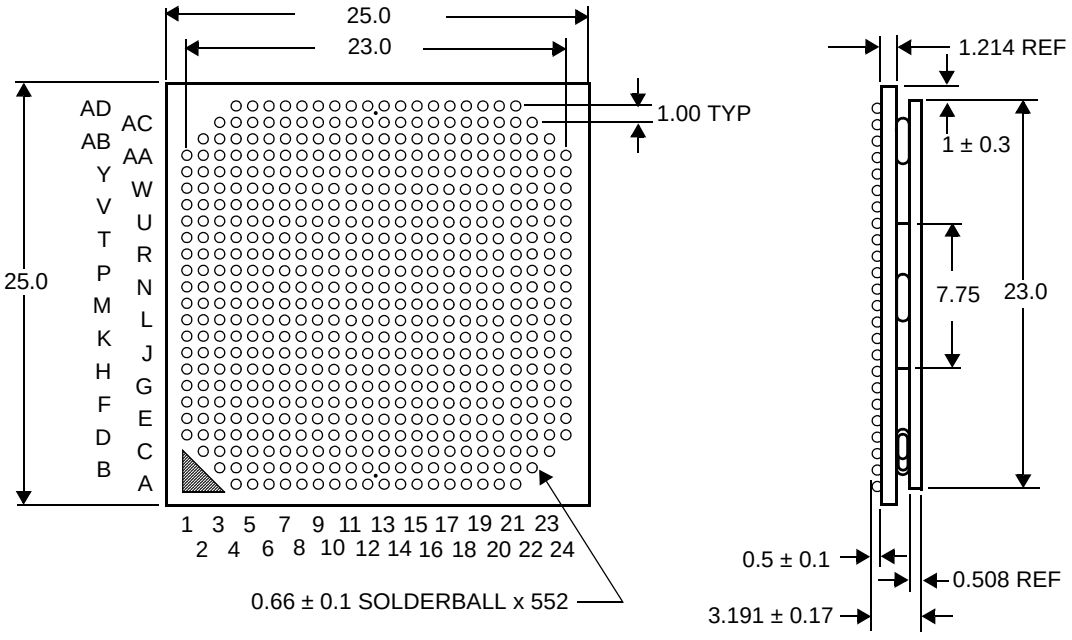
25mm, 552-Ball Plastic (FC-PBGA) Package

Top View



Note: All dimensions are in mm.

Bottom View



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Signal Lists

The following table lists all the external signals in alphabetical order and shows the ball (pin) number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal in brackets. Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in "Signal Functional Description" on page 48 where the signals in the indicated interface group begin. In cases where signals in the same interface group (for example, Ethernet) have different names to distinguish variations in the mode of operation, the names are separated by a comma with the primary name appearing first. These signals are listed only once, and appear alphabetically by the primary name.

Signals Listed Alphabetically (Sheet 1 of 22)

Signal Name	Ball	Interface Group	Page
AGND	J01	Power—Analog ground	54
AGND	J24		
AGND	AA11		
AMV_{DD}	AB11	Power—MemClkOut PLL analog voltage	54
APV_{DD}	G01	Power—PCI-X PLL analog voltage	54
ASV_{DD}	G24	Power—SysClk PLL analog voltage	54
BA0	AA16	DDR SDRAM	49
BA1	AD09		
$\overline{\text{BankSel0}}$	AB15	DDR SDRAM	49
$\overline{\text{BankSel1}}$	W14		
$\overline{\text{BankSel2}}$	AD11		
$\overline{\text{BankSel3}}$	AD05		
[$\overline{\text{BE0}}$]PCIXC0	F14	PCI-X	48
[$\overline{\text{BE1}}$]PCIXC1	E16		
[$\overline{\text{BE2}}$]PCIXC2	C19		
[$\overline{\text{BE3}}$]PCIXC3	F20		
[$\overline{\text{BE4}}$]PCIXC4	C08		
[$\overline{\text{BE5}}$]PCIXC5	C03		
[$\overline{\text{BE6}}$]PCIXC6	G09		
[$\overline{\text{BE7}}$]PCIXC7	F09		
BusReq	AA24	External Master Peripheral	51
$\overline{\text{CAS}}$	AB05	DDR SDRAM	49
ClkEn0	AD17	DDR SDRAM	49
ClkEn1	AB10		
ClkEn2	Y09		
ClkEn3	W09		

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Signals Listed Alphabetically (Sheet 2 of 22)

Signal Name	Ball	Interface Group	Page
DM0	T16	DDR SDRAM	49
DM1	AA18		
DM2	AB14		
DM3	P13		
DM4	AA09		
DM5	AA07		
DM6	Y03		
DM7	V03		
DM8	AC05		
DMAAck0	N05	External Slave Peripheral	50
DMAAck1	P07		
DMAAck2	P06		
DMAAck3	P11		
DMAReq0	R03	External Slave Peripheral	50
DMAReq1	M11		
DMAReq2	N11		
DMAReq3	P01		
DQS0	AC20	DDR SDRAM	49
DQS1	AC16		
DQS2	AC14		
DQS3	AB13		
DQS4	AC11		
DQS5	AC09		
DQS6	Y04		
DQS7	T01		
DQS8	AA05		
DrvrInh1	L07	System	53
DrvrInh2	A05	System	53

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Signals Listed Alphabetically (Sheet 3 of 22)

Signal Name	Ball	Interface Group	Page
ECC0	AB07	DDR SDRAM	49
ECC1	AB06		
ECC2	AD06		
ECC3	W07		
ECC4	U09		
ECC5	AC03		
ECC6	AB04		
ECC7	AD04		
EMCCD, EMC1RxErr	J07	Ethernet	49
EMCCrS, EMC0CrSDV	K07	Ethernet	49
EMCMDClk	J08	Ethernet	49
EMCMDIO	L05	Ethernet	49
EMCRxClk	J02	Ethernet	49
EMCRxD0, EMC0RxD0	G03	Ethernet	49
EMCRxD1, EMC0RxD1	E01		
EMCRxD2, EMC1RxD0	A07		
EMCRxD3, EMC1RxD1	H09		
EMCRxDV, EMC1CrSDV	K01	Ethernet	49
EMCRxErr, EMC0RxErr	K03	Ethernet	49
EMCTxClk, EMCRefClk	J06	Ethernet	49
EMCTxD0, EMC0TxD0	L09	Ethernet	49
EMCTxD1, EMC0TxD1	K05		
EMCTxD2, EMC1TxD0	J04		
EMCTxD3, EMC1TxD1	J03		
EMCTxEn, EMC0TxEn	L06	Ethernet	49
EMCTxErr, EMC1TxEn	C05	Ethernet	49
EOT0/TC0	R16	External Slave Peripheral	50
EOT1/TC1	P15		
EOT2/TC2	P16		
EOT3/TC3	M16		
$\overline{\text{ExtAck}}$	AA22	External Master Peripheral	51
$\overline{\text{ExtReq}}$	AB23	External Master Peripheral	51
$\overline{\text{ExtReset}}$	T17	External Master Peripheral	51

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Signals Listed Alphabetically (Sheet 4 of 22)

Signal Name	Ball	Interface Group	Page
GND	B06	Power	54
GND	B10		
GND	B13		
GND	B17		
GND	B21		
GND	D04		
GND	D08		
GND	D12		
GND	D15		
GND	D19		
GND	D23		
GND	F02		
GND	F06		
GND	F10		
GND	F13		
GND	F17		
GND	F21		
GND	H04		
GND	H08		
GND	H12		
GND	H15		
GND	H19		
GND	H23		
GND	K02		
GND	K06		
GND	K10		
GND	K13		
GND	K17		
GND	K21		
GND	M04		

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Signals Listed Alphabetically (Sheet 5 of 22)

Signal Name	Ball	Interface Group	Page
GND	M08		
GND	M12		
GND	M15		
GND	M19		
GND	M23		
GND	N02		
GND	N06		
GND	N10		
GND	N13		
GND	N17		
GND	N21		
GND	R04		
GND	R08		
GND	R12		
GND	R15	Power	54
GND	R19		
GND	R23		
GND	U02		
GND	U06		
GND	U10		
GND	U13		
GND	U17		
GND	U21		
GND	W04		
GND	W08		
GND	W12		
GND	W15		
GND	W19		
GND	W23		

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Signals Listed Alphabetically (Sheet 6 of 22)

Signal Name	Ball	Interface Group	Page
GND	AA02	Power	54
GND	AA06		
GND	AA10		
GND	AA13		
GND	AA17		
GND	AA21		
GND	AC04		
GND	AC08		
GND	AC12		
GND	AC15		
GND	AC19		

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Signals Listed Alphabetically (Sheet 7 of 22)

Signal Name	Ball	Interface Group	Page
[GPIO00]IRQ00	N18	System	53
[GPIO01]IRQ01	L20		
[GPIO02]IRQ02	P20		
[GPIO03]IRQ03	L18		
[GPIO04]IRQ04	N14		
[GPIO05]IRQ05	M20		
[GPIO06]IRQ06	M14		
[GPIO07]IRQ07	P18		
[GPIO08]IRQ08	N20		
[GPIO09]IRQ09	P22		
[GPIO10]IRQ10	V18		
GPIO11	P14		
[GPIO12]UART1_Rx	C18		
[GPIO13]UART1_Tx	J16		
[GPIO14]$\overline{\text{UART1\_DSR/CTS}}$	G06		
[GPIO15]$\overline{\text{UART1\_RTS/DTR}}$	E05		
[GPIO16]IIC1SClk	H11		
[GPIO17]IIC1SDA	H14		
[GPIO18]TrcBS0	N16		
[GPIO19]TrcBS1	P17		
[GPIO20]TrcBS2	T20		
[GPIO21]TrcES0	T21		
[GPIO22]TrcES1	P23		
[GPIO23]TrcES2	N09		
[GPIO24]TrcES3	P08		
[GPIO25]TrcES4	T05		
[GPIO26]TrcTS0	T04		
[GPIO27]TrcTS1	P03		
[GPIO28]TrcTS2	R07		
[GPIO29]TrcTS3	P09		
[GPIO30]TrcTS4	R09		
[GPIO31]TrcTS5	T06		
$\overline{\text{Halt}}$	V05	System	53
HoldAck	Y21	External Master Peripheral	51

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Signals Listed Alphabetically (Sheet 8 of 22)

Signal Name	Ball	Interface Group	Page
HoldReq	Y23	External Master Peripheral	51
IIC0SClk	G11	IIC Peripheral	52
IIC0SDA	G13	IIC Peripheral	52
IIC1SClk[GPIO16]	H11	IIC Peripheral	52
IIC1SDA[GPIO17]	H14	IIC Peripheral	52
IRQ00[GPIO00]	N18	Interrupts	52
IRQ01[GPIO01]	L20		
IRQ02[GPIO02]	P20		
IRQ03[GPIO03]	L18		
IRQ04[GPIO04]	N14		
IRQ05[GPIO05]	M20		
IRQ06[GPIO06]	M14		
IRQ07[GPIO07]	P18		
IRQ08[GPIO08]	N20		
IRQ09[GPIO09]	P22		
IRQ10[GPIO10]	V18		
[IRQ11]$\overline{\text{PCIReq1}}$	E21		
[IRQ12]$\overline{\text{PCIGnt1}}$	C22		
MemAddr00	Y19	DDR SDRAM	49
MemAddr01	AD20		
MemAddr02	Y20		
MemAddr03	AB20		
MemAddr04	AD18		
MemAddr05	AD16		
MemAddr06	AB18		
MemAddr07	Y14		
MemAddr08	V13		
MemAddr09	V11		
MemAddr10	W16		
MemAddr11	Y11		
MemAddr12	V10		
MemClkOut0	V09	DDR SDRAM	49
$\overline{\text{MemClkOut0}}$	V08		

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Signals Listed Alphabetically (Sheet 9 of 22)

Signal Name	Ball	Interface Group	Page
MemData00	AD21	DDR SDRAM	49
MemData01	AB21		
MemData02	AC22		
MemData03	AA20		
MemData04	U16		
MemData05	V17		
MemData06	AD19		
MemData07	AB19		
MemData08	W18		
MemData09	V16		
MemData10	Y17		
MemData11	AB16		
MemData12	AC18		
MemData13	Y18		
MemData14	R14		
MemData15	AB17		
MemData16	AA14		
MemData17	AD15		
MemData18	T15		
MemData19	V15		
MemData20	Y16		
MemData21	U14		
MemData22	T13		
MemData23	Y15		
MemData24	AD13		
MemData25	AD14		
MemData26	V14		
MemData27	Y13		
MemData28	P12		
MemData29	AB12		
MemData30	Y12		
MemData31	V12		

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Signals Listed Alphabetically (Sheet 10 of 22)

Signal Name	Ball	Interface Group	Page
MemData32	W11	DDR SDRAM	49
MemData33	AD12		
MemData34	Y10		
MemData35	T12		
MemData36	U11		
MemData37	T11		
MemData38	T10		
MemData39	AD10		
MemData40	AB08		
MemData41	AD08		
MemData42	R11		
MemData43	Y07		
MemData44	AC07		
MemData45	AB09		
MemData46	Y06		
MemData47	Y08		
MemData48	AA01		
MemData49	AA03		
MemData50	AB02		
MemData51	Y01		
MemData52	AB03		
MemData53	Y02		
MemData54	V07		
MemData55	V01		
MemData56	T08		
MemData57	U07		
MemData58	W01		
MemData59	W03		
MemData60	V06		
MemData61	T07		
MemData62	W05		
MemData63	U05		
MemVRef1	T14	DDR SDRAM	49
MemVRef2	T09		

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Signals Listed Alphabetically (Sheet 11 of 22)

Signal Name	Ball	Interface Group	Page
No ball	A01	A physical ball does not exist at these ball coordinates.	NA
No ball	A02		
No ball	A03		
No ball	A22		
No ball	A23		
No ball	A24		
No ball	B01		
No ball	B02		
No ball	B23		
No ball	B24		
No ball	C01		
No ball	C24		
No ball	AB01		
No ball	AB24		
No ball	AC01		
No ball	AC02		
No ball	AC23		
No ball	AC24		
No ball	AD01		
No ball	AD02		
No ball	AD03		
No ball	AD22		
No ball	AD23		
No ball	AD24		

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Signals Listed Alphabetically (Sheet 12 of 22)

Signal Name	Ball	Interface Group	Page
OV_{DD}	B04		
OV_{DD}	B12		
OV_{DD}	B19		
OV_{DD}	D02		
OV_{DD}	D10		
OV_{DD}	D17		
OV_{DD}	F08		
OV_{DD}	F15		
OV_{DD}	F23		
OV_{DD}	H06		
OV_{DD}	H10		
OV_{DD}	H13		
OV_{DD}	H21		
OV_{DD}	K04	Power	54
OV_{DD}	K08		
OV_{DD}	K19		
OV_{DD}	M02		
OV_{DD}	M17		
OV_{DD}	N08		
OV_{DD}	N23		
OV_{DD}	R06		
OV_{DD}	R17		
OV_{DD}	R21		
OV_{DD}	U04		
OV_{DD}	U19		
OV_{DD}	W02		
OV_{DD}	AA23		
PCIX133Cap	G08	PCI-X	48
$\overline{\text{PCIXAck64}}$	D09	PCI-X	48

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Signals Listed Alphabetically (Sheet 13 of 22)

Signal Name	Ball	Interface Group	Page
PCIXAD00	C17	PCI-X	48
PCIXAD01	B09		
PCIXAD02	G10		
PCIXAD03	E10		
PCIXAD04	C10		
PCIXAD05	A10		
PCIXAD06	F11		
PCIXAD07	G12		
PCIXAD08	G14		
PCIXAD09	A15		
PCIXAD10	C15		
PCIXAD11	E15		
PCIXAD12	G15		
PCIXAD13	B16		
PCIXAD14	C16		
PCIXAD15	D16		
PCIXAD16	E18		
PCIXAD17	E19		
PCIXAD18	F18		
PCIXAD19	G18		
PCIXAD20	D20		
PCIXAD21	A20		
PCIXAD22	A21		
PCIXAD23	C21		
PCIXAD24	F22		
PCIXAD25	B22		
PCIXAD26	G21		
PCIXAD27	E23		
PCIXAD28	C23		
PCIXAD29	F24		
PCIXAD30	D22		
PCIXAD31	D24		

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Signals Listed Alphabetically (Sheet 14 of 22)

Signal Name	Ball	Interface Group	Page
PCIXAD32	H03	PCI-X	48
PCIXAD33	H01		
PCIXAD34	L08		
PCIXAD35	F01		
PCIXAD36	D01		
PCIXAD37	J05		
PCIXAD38	H05		
PCIXAD39	G02		
PCIXAD40	E02		
PCIXAD41	C02		
PCIXAD42	A08		
PCIXAD43	G05		
PCIXAD44	F03		
PCIXAD45	D03		
PCIXAD46	B03		
PCIXAD47	H07		
PCIXAD48	G04		
PCIXAD49	E04		
PCIXAD50	C04		
PCIXAD51	A04		
PCIXAD52	F05		
PCIXAD53	D05		
PCIXAD54	B05		
PCIXAD55	C09		
PCIXAD56	E06		
PCIXAD57	C06		
PCIXAD58	A06		
PCIXAD59	F07		
PCIXAD60	E07		
PCIXAD61	D07		
PCIXAD62	B07		
PCIXAD63	E08		

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Signals Listed Alphabetically (Sheet 15 of 22)

Signal Name	Ball	Interface Group	Page
PCIXC0[BE0]	F14	PCI-X	48
PCIXC1[BE1]	E16		
PCIXC2[BE2]	C19		
PCIXC3[BE3]	F20		
PCIXC4[BE4]	C08		
PCIXC5[BE5]	C03		
PCIXC6[BE6]	G09		
PCIXC7[BE7]	F09		
PCIXCap	L23	PCI-X	48
PCIXClk	E03	PCI-X	48
PCIXDevSel	E13	PCI-X	48
PCIXFrame	A11	PCI-X	48
PCIXGnt0	E22	PCI-X	48
PCIXGnt1[IRQ12]	C22		
PCIXGnt2	N22		
PCIXGnt3	M18		
PCIXGnt4	R22		
PCIXGnt5	P19		
PCIXIDSel	G07	PCI-X	48
PCIXINT	M07	PCI-X	48
PCIXIRDY	E12	PCI-X	48
PCIXM66En	A14	PCI-X	48
PCIXParHigh	L04	PCI-X	48
PCIXParLow	F16	PCI-X	48
PCIXPErr	A17	PCI-X	48
PCIXReq0	E24	PCI-X	48
PCIXReq1[IRQ11]	E21		
PCIXReq2	E20		
PCIXReq3	R20		
PCIXReq4	G23		
PCIXReq5	R18		
PCIXReq64	E09	PCI-X	48
PCIXReset	M24	PCI-X	48
PCIXSErr	A18	PCI-X	48

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Signals Listed Alphabetically (Sheet 16 of 22)

Signal Name	Ball	Interface Group	Page
$\overline{\text{PCIXStop}}$	L12	PCI-X	48
$\overline{\text{PCIXTRDY}}$	C12	PCI-X	48
PerAddr00	D11	External Slave Peripheral **Note:** PerAddr00 is the most significant bit (msb) on this bus.	50
PerAddr01	C11		
PerAddr02	B11		
PerAddr03	A12		
PerAddr04	A19		
PerAddr05	D18		
PerAddr06	E11		
PerAddr07	M03		
PerAddr08	N01		
PerAddr09	E14		
PerAddr10	C20		
PerAddr11	A16		
PerAddr12	A13		
PerAddr13	B14		
PerAddr14	C14		
PerAddr15	D14		
PerAddr16	B20		
PerAddr17	L15		
PerAddr18	L21		
PerAddr19	L22		
PerAddr20	M22		
PerAddr21	M01		
PerAddr22	L24		
PerAddr23	P24		
PerAddr24	T19		
PerAddr25	R24		
PerAddr26	U22		
PerAddr27	U24		
PerAddr28	N03		
PerAddr29	V20		
PerAddr30	V23		
PerAddr31	V21		

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Signals Listed Alphabetically (Sheet 17 of 22)

Signal Name	Ball	Interface Group	Page
PerBLast	C07	External Slave Peripheral	50
PerClk	U18	External Master Peripheral	51
PerCS0	E17	External Slave Peripheral	50
PerCS1	L10		
PerCS2	V04		
PerCS3	T24		
PerCS4	L03		
PerCS5	T03		
PerCS6	L13		
PerCS7	U03		

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Signals Listed Alphabetically (Sheet 18 of 22)

Signal Name	Ball	Interface Group	Page
PerData00	H24	External Slave Peripheral **Note:** PerData00 is the most significant bit (msb) on this bus.	50
PerData01	H22		
PerData02	H20		
PerData03	G20		
PerData04	G19		
PerData05	H18		
PerData06	J23		
PerData07	J22		
PerData08	J21		
PerData09	J20		
PerData10	J19		
PerData11	J18		
PerData12	J17		
PerData13	J15		
PerData14	J14		
PerData15	J13		
PerData16	J12		
PerData17	J11		
PerData18	J10		
PerData19	J09		
PerData20	L14		
PerData21	K24		
PerData22	K22		
PerData23	K20		
PerData24	K18		
PerData25	K16		
PerData26	K14		
PerData27	K11		
PerData28	K09		
PerData29	L19		
PerData30	L17		
PerData31	L16		
PerErr	P21	External Master Peripheral	51
$\overline{\text{PerOE}}$	M09	External Slave Peripheral	50

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Signals Listed Alphabetically (Sheet 19 of 22)

Signal Name	Ball	Interface Group	Page
PerPar0	T23	External Slave Peripheral	50
PerPar1	T22		
PerPar2	W20		
PerPar3	U20		
PerReady[RcvrInh]	N07	External Slave Peripheral	50
PerR/$\overline{W}$	P05	External Slave Peripheral	50
$\overline{PerWBE0}$	T18	External Slave Peripheral	50
$\overline{PerWBE1}$	V19		
$\overline{PerWBE2}$	W22		
$\overline{PerWBE3}$	W24		
$\overline{PerWE}$	P02	External Slave Peripheral	50
$\overline{RAS}$	AD07	DDR SDRAM	49
[RcvrInh]PerReady	N07	System	53
RefVEn	L02	System	53
Reserved	L01	Reserved	54
Reserved	P04		
SV_{DD}	U12	Power	54
SV_{DD}	U15		
SV_{DD}	W10		
SV_{DD}	W17		
SV_{DD}	AA08		
SV_{DD}	AA15		
SV_{DD}	AC06		
SV_{DD}	AC13		
SV_{DD}	AC21		
SysClk	G22	System	53
SysErr	T02	System	53
$\overline{SysReset}$	P10	System	53
TCK	V22	JTAG	52
TDI	Y24	JTAG	52
TDO	Y22	JTAG	52
TestEn	M05	System	53
TmrClk	U01	System	53

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Signals Listed Alphabetically (Sheet 20 of 22)

Signal Name	Ball	Interface Group	Page
TMS	AB22	JTAG	52
TrcBS0[GPIO18]	N16	Trace	54
TrcBS1[GPIO19]	P17		
TrcBS2[GPIO20]	T20		
TrcClk	R05	Trace	54
TrcES0[GPIO21]	T21	Trace	54
TrcES1[GPIO22]	P23		
TrcES2[GPIO23]	N09		
TrcES3[GPIO24]	P08		
TrcES4[GPIO25]	T05		
TrcTS0[GPIO26]	T04	Trace	54
TrcTS1[GPIO27]	P03	Trace	54
TrcTS2[GPIO28]	R07	Trace	54
TrcTS3[GPIO29]	P09	Trace	54
TrcTS4[GPIO30]	R09	Trace	54
TrcTS5[GPIO31]	T06	Trace	54
TrcTS6	R01	Trace	54
$\overline{\text{TRST}}$	N24	JTAG	52
$\overline{\text{UART0\_CTS}}$	C13	UART Peripheral	51
$\overline{\text{UART0\_DCD}}$	V24	UART Peripheral **Note:** Used as initialization strapping input.	51
$\overline{\text{UART0\_DSR}}$	V02	UART Peripheral **Note:** Used as initialization strapping input.	51
$\overline{\text{UART0\_DTR}}$	B18	UART Peripheral	51
$\overline{\text{UART0\_RI}}$	H16	UART Peripheral	51
$\overline{\text{UART0\_RTS}}$	G16	UART Peripheral	51
UART0_Rx	G17	UART Peripheral	51
UART0_Tx	L11	UART Peripheral	51
$\overline{\text{UART1\_DSR/CTS}}$[GPIO14]	G06	UART Peripheral	51
$\overline{\text{UART1\_RTS/DTR}}$[GPIO15]	E05	UART Peripheral	51
UART1_Rx[GPIO12]	C18	UART Peripheral	51
UART1_Tx[GPIO13]	J16	UART Peripheral	51

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Signals Listed Alphabetically (Sheet 21 of 22)

Signal Name	Ball	Interface Group	Page
UARTSerClk	A09	UART Peripheral	51
V_{DD}	B08	Power	54
V_{DD}	B15		
V_{DD}	D06		
V_{DD}	D13		
V_{DD}	D21		
V_{DD}	F04		
V_{DD}	F12		
V_{DD}	F19		
V_{DD}	H02		
V_{DD}	H17		
V_{DD}	K12		
V_{DD}	K15		
V_{DD}	K23		
V_{DD}	M06		
V_{DD}	M10		
V_{DD}	M13		
V_{DD}	M21		
V_{DD}	N04		
V_{DD}	N12		
V_{DD}	N15		

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Signals Listed Alphabetically (Sheet 22 of 22)

Signal Name	Ball	Interface Group	Page
V_{DD}	N19	Power	54
V_{DD}	R02		
V_{DD}	R10		
V_{DD}	R13		
V_{DD}	U08		
V_{DD}	U23		
V_{DD}	W06		
V_{DD}	W13		
V_{DD}	W21		
V_{DD}	AA04		
V_{DD}	AA12		
V_{DD}	AA19		
V_{DD}	AC10		
V_{DD}	AC17		
$\overline{WE}$	Y05	DDR SDRAM	49

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In the following table, only the primary (default) signal name is shown for each pin. Multiplexed or multifunction signals are marked with an asterisk (*). To determine what signals or functions are multiplexed on those pins, look up the primary signal name in “Signals Listed Alphabetically” on page 18.

Signals Listed by Ball Assignment (Sheet 1 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	No ball	B01	No ball	C01	No ball	D01	PCIXAD36
A02	No ball	B02	No ball	C02	PCIXAD41	D02	OV_{DD}
A03	No ball	B03	PCIXAD46	C03	PCIXC5 *	D03	PCIXAD45
A04	PCIXAD51	B04	OV_{DD}	C04	PCIXAD50	D04	GND
A05	DrvrInh2	B05	PCIXAD54	C05	EMCTxErr *	D05	PCIXAD53
A06	PCIXAD58	B06	GND	C06	PCIXAD57	D06	V_{DD}
A07	EMCRxD2 *	B07	PCIXAD62	C07	$\overline{\text{PerBLast}}$	D07	PCIXAD61
A08	PCIXAD42	B08	V_{DD}	C08	PCIXC4 *	D08	GND
A09	UARTSerClk	B09	PCIXAD01	C09	PCIXAD55	D09	$\overline{\text{PCIXAck64}}$
A10	PCIXAD05	B10	GND	C10	PCIXAD04	D10	OV_{DD}
A11	$\overline{\text{PCIXFrame}}$	B11	PerAddr02	C11	PerAddr01	D11	PerAddr00
A12	PerAddr03	B12	OV_{DD}	C12	$\overline{\text{PCIXTRDY}}$	D12	GND
A13	PerAddr12	B13	GND	C13	$\overline{\text{UART0\_CTS}}$	D13	V_{DD}
A14	PCIXM66En	B14	PerAddr13	C14	PerAddr14	D14	PerAddr15
A15	PCIXAD09	B15	V_{DD}	C15	PCIXAD10	D15	GND
A16	PerAddr11	B16	PCIXAD13	C16	PCIXAD14	D16	PCIXAD15
A17	$\overline{\text{PCIXPErr}}$	B17	GND	C17	PCIXAD00	D17	OV_{DD}
A18	$\overline{\text{PCIXSErr}}$	B18	$\overline{\text{UART0\_DTR}}$	C18	UART1_Rx *	D18	PerAddr05
A19	PerAddr04	B19	OV_{DD}	C19	PCIXC2 *	D19	GND
A20	PCIXAD21	B20	PerAddr16	C20	PerAddr10	D20	PCIXAD20
A21	PCIXAD22	B21	GND	C21	PCIXAD23	D21	V_{DD}
A22	No ball	B22	PCIXAD25	C22	$\overline{\text{PCIXGnt1}}$ *	D22	PCIXAD30
A23	No ball	B23	No ball	C23	PCIXAD28	D23	GND
A24	No ball	B24	No ball	C24	No ball	D24	PCIXAD31

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Signals Listed by Ball Assignment (Sheet 2 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	EMCRxD1 *	F01	PCIXAD35	G01	APV_{DD} for PCI PLL	H01	PCIXAD33
E02	PCIXAD40	F02	GND	G02	PCIXAD39	H02	V_{DD}
E03	PCIXClk	F03	PCIXAD44	G03	EMCRxD0 *	H03	PCIXAD32
E04	PCIXAD49	F04	V_{DD}	G04	PCIXAD48	H04	GND
E05	$\overline{\text{UART1\_RTS/DTR}}$ *	F05	PCIXAD52	G05	PCIXAD43	H05	PCIXAD38
E06	PCIXAD56	F06	GND	G06	$\overline{\text{UART1\_DSR/CTS}}$ *	H06	OV_{DD}
E07	PCIXAD60	F07	PCIXAD59	G07	PCIXIDSel	H07	PCIXAD47
E08	PCIXAD63	F08	OV_{DD}	G08	PCIX133Cap	H08	GND
E09	$\overline{\text{PCIXReq64}}$	F09	PCIXC7 *	G09	PCIXC6 *	H09	EMCRxD3 *
E10	PCIXAD03	F10	GND	G10	PCIXAD02	H10	OV_{DD}
E11	PerAddr06	F11	PCIXAD06	G11	IIC0SClk	H11	IIC1SClk *
E12	$\overline{\text{PCIXIRDY}}$	F12	V_{DD}	G12	PCIXAD07	H12	GND
E13	$\overline{\text{PCIXDevSel}}$	F13	GND	G13	IIC0SDA	H13	OV_{DD}
E14	PerAdd09	F14	PCIXC0 *	G14	PCIXAD08	H14	IIC1SDA *
E15	PCIXAD11	F15	OV_{DD}	G15	PCIXAD12	H15	GND
E16	PCIXC1 *	F16	PCIXParLow	G16	$\overline{\text{UART0\_RTS}}$	H16	$\overline{\text{UART0\_RI}}$
E17	$\overline{\text{PerCS0}}$	F17	GND	G17	UART0_Rx	H17	V_{DD}
E18	PCIXAD16	F18	PCIXAD18	G18	PCIXAD19	H18	PerData05
E19	PCIXAD17	F19	V_{DD}	G19	PerData04	H19	GND
E20	$\overline{\text{PCIXReq2}}$	F20	PCIXC3 *	G20	PerData03	H20	PerData02
E21	$\overline{\text{PCIXReq1}}$ *	F21	GND	G21	PCIXAD26	H21	OV_{DD}
E22	$\overline{\text{PCIXGnt0}}$	F22	PCIXAD24	G22	SysClk	H22	PerData01
E23	PCIXAD27	F23	OV_{DD}	G23	$\overline{\text{PCIXReq4}}$	H23	GND
E24	$\overline{\text{PCIXReq0}}$	F24	PCIXAD29	G24	ASV_{DD} for SysClk PLL	H24	PerData00

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Signals Listed by Ball Assignment (Sheet 3 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	AGND	K01	EMCRxDV *	L01	Reserved	M01	PerAddr21
J02	EMCRxClk	K02	GND	L02	RefVEn	M02	OV_{DD}
J03	EMCTxD3 *	K03	EMCRxErr *	L03	$\overline{\text{PerCS4}}$	M03	PerAddr07
J04	EMCTxD2 *	K04	OV_{DD}	L04	PCIXParHigh	M04	GND
J05	PCIXAD37	K05	EMCTxD1 *	L05	EMCMDIO	M05	TestEn
J06	EMCTxClk *	K06	GND	L06	EMCTxEn *	M06	V_{DD}
J07	EMCCD *	K07	EMCCrS *	L07	DrvrInh1	M07	$\overline{\text{PCIXINT}}$
J08	EMCMDClk	K08	OV_{DD}	L08	PCIXAD34	M08	GND
J09	PerData19	K09	PerData28	L09	EMCTxD0 *	M09	$\overline{\text{PerOE}}$
J10	PerData18	K10	GND	L10	$\overline{\text{PerCS1}}$	M10	V_{DD}
J11	PerData17	K11	PerData27	L11	UART0_Tx	M11	DMAReq1
J12	PerData16	K12	V_{DD}	L12	$\overline{\text{PCIXStop}}$	M12	GND
J13	PerData15	K13	GND	L13	$\overline{\text{PerCS6}}$	M13	V_{DD}
J14	PerData14	K14	PerData26	L14	PerData20	M14	IRQ06 *
J15	PerData13	K15	V_{DD}	L15	PerAddr17	M15	GND
J16	UART1_Tx *	K16	PerData25	L16	PerData31	M16	EOT3/TC3
J17	PerData12	K17	GND	L17	PerData30	M17	OV_{DD}
J18	PerData11	K18	PerData24	L18	IRQ03 *	M18	$\overline{\text{PCIXGnt3}}$
J19	PerData10	K19	OV_{DD}	L19	PerData29	M19	GND
J20	PerData9	K20	PerData23	L20	IRQ01 *	M20	IRQ05 *
J21	PerData8	K21	GND	L21	PerAddr18	M21	V_{DD}
J22	PerData7	K22	PerData22	L22	PerAddr19	M22	PerAddr20
J23	PerData6	K23	V_{DD}	L23	PCIXCap	M23	GND
J24	AGND	K24	PerData21	L24	PerAddr22	M24	$\overline{\text{PCIXReset}}$

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Signals Listed by Ball Assignment (Sheet 4 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	PerAddr08	P01	DMAReq3	R01	TrcTS6	T01	DQS7
N02	GND	P02	$\overline{\text{PerWE}}$	R02	V_{DD}	T02	SysErr
N03	PerAddr28	P03	TrcTS1 *	R03	DMAReq0	T03	$\overline{\text{PerCS5}}$
N04	V_{DD}	P04	Reserved	R04	GND	T04	TrcTS0 *
N05	DMAAck0	P05	PerR/$\overline{\text{W}}$	R05	TrcClk	T05	TrcES4 *
N06	GND	P06	DMAAck2	R06	OV_{DD}	T06	TrcTS5 *
N07	PerReady *	P07	DMAAck1	R07	TrcTS2 *	T07	MemData61
N08	OV_{DD}	P08	TrcES3 *	R08	GND	T08	MemData56
N09	TrcES2 *	P09	TrcTS3 *	R09	TrcTS4 *	T09	MemVRef2
N10	GND	P10	$\overline{\text{SysReset}}$	R10	V_{DD}	T10	MemData38
N11	DMAReq2	P11	DMAAck3	R11	MemData42	T11	MemData37
N12	V_{DD}	P12	MemData28	R12	GND	T12	MemData35
N13	GND	P13	DM3	R13	V_{DD}	T13	MemData22
N14	IRQ04 *	P14	GPIO11	R14	MemData14	T14	MemVRef1
N15	V_{DD}	P15	EOT1/TC1	R15	GND	T15	MemData18
N16	TrcBS0 *	P16	EOT2/TC2	R16	EOT0/TC0	T16	DM0
N17	GND	P17	TrcBS1 *	R17	OV_{DD}	T17	$\overline{\text{ExtReset}}$
N18	IRQ00 *	P18	IRQ07 *	R18	$\overline{\text{PCIXReq5}}$	T18	$\overline{\text{PerWBE0}}$
N19	V_{DD}	P19	$\overline{\text{PCIXGnt5}}$	R19	GND	T19	PerAddr24
N20	IRQ08 *	P20	IRQ02 *	R20	$\overline{\text{PCIXReq3}}$	T20	TrcBS2 *
N21	GND	P21	PerErr	R21	OV_{DD}	T21	TrcES0 *
N22	$\overline{\text{PCIXGnt2}}$	P22	IRQ09 *	R22	$\overline{\text{PCIXGnt4}}$	T22	PerPar1
N23	OV_{DD}	P23	TrcES1 *	R23	GND	T23	PerPar0
N24	$\overline{\text{TRST}}$	P24	PerAddr23	R24	PerAddr25	T24	$\overline{\text{PerCS3}}$

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Signals Listed by Ball Assignment (Sheet 5 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	TmrClk	V01	MemData55	W01	MemData58	Y01	MemData51
U02	GND	V02	UART0_DSR	W02	OV_{DD}	Y02	MemData53
U03	PerCS7	V03	DM7	W03	MemData59	Y03	DM6
U04	OV_{DD}	V04	PerCS2	W04	GND	Y04	DQS6
U05	MemData63	V05	Halt	W05	MemData62	Y05	WE
U06	GND	V06	MemData60	W06	V_{DD}	Y06	MemData46
U07	MemData57	V07	MemData54	W07	ECC3	Y07	MemData43
U08	V_{DD}	V08	MemClkOut0	W08	GND	Y08	MemData47
U09	ECC4	V09	MemClkOut0	W09	ClkEn3	Y09	ClkEn2
U10	GND	V10	MemAddr12	W10	SV_{DD}	Y10	MemData34
U11	MemData36	V11	MemAddr9	W11	MemData32	Y11	MemAddr11
U12	SV_{DD}	V12	MemData31	W12	GND	Y12	MemData30
U13	GND	V13	MemAddr8	W13	V_{DD}	Y13	MemData27
U14	MemData21	V14	MemData26	W14	BankSel1	Y14	MemAddr7
U15	SV_{DD}	V15	MemData19	W15	GND	Y15	MemData23
U16	MemData04	V16	MemData09	W16	MemAddr10	Y16	MemData20
U17	GND	V17	MemData05	W17	SV_{DD}	Y17	MemData10
U18	PerClk	V18	IRQ10 *	W18	MemData08	Y18	MemData13
U19	OV_{DD}	V19	PerWBE1	W19	GND	Y19	MemAddr00
U20	PerPar3	V20	PerAddr29	W20	PerPar2	Y20	MemAddr02
U21	GND	V21	PerAddr31	W21	V_{DD}	Y21	HoldAck
U22	PerAddr26	V22	TCK	W22	PerWBE2	Y22	TDO
U23	V_{DD}	V23	PerAddr30	W23	GND	Y23	HoldReq
U24	PerAddr27	V24	UART0_DCD	W24	PerWBE3	Y24	TDI

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Signals Listed by Ball Assignment (Sheet 6 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	MemData48	AB01	No ball	AC01	No ball	AD01	No ball
AA02	GND	AB02	MemData50	AC02	No ball	AD02	No ball
AA03	MemData49	AB03	MemData52	AC03	ECC5	AD03	No ball
AA04	V_{DD}	AB04	ECC6	AC04	GND	AD04	ECC7
AA05	DQS8	AB05	$\overline{CAS}$	AC05	DM8	AD05	$\overline{BankSel3}$
AA06	GND	AB06	ECC1	AC06	SV_{DD}	AD06	ECC2
AA07	DM5	AB07	ECC0	AC07	MemData44	AD07	$\overline{RAS}$
AA08	SV_{DD}	AB08	MemData40	AC08	GND	AD08	MemData41
AA09	DM4	AB09	MemData45	AC09	DQS5	AD09	BA1
AA10	GND	AB10	ClkEn1	AC10	V_{DD}	AD10	MemData39
AA11	AGND	AB11	AMV_{DD} for MemClk PLL	AC11	DQS4	AD11	$\overline{BankSel2}$
AA12	V_{DD}	AB12	MemData29	AC12	GND	AD12	MemData33
AA13	GND	AB13	DQS3	AC13	SV_{DD}	AD13	MemData24
AA14	MemData16	AB14	DM2	AC14	DQS2	AD14	MemData25
AA15	SV_{DD}	AB15	$\overline{BankSel0}$	AC15	GND	AD15	MemData17
AA16	BA0	AB16	MemData11	AC16	DQS1	AD16	MemAddr5
AA17	GND	AB17	MemData15	AC17	V_{DD}	AD17	ClkEn0
AA18	DM1	AB18	MemAddr6	AC18	MemData12	AD18	MemAddr4
AA19	V_{DD}	AB19	MemData07	AC19	GND	AD19	MemData06
AA20	MemData03	AB20	MemAddr3	AC20	DQS0	AD20	MemAddr01
AA21	GND	AB21	MemData01	AC21	SV_{DD}	AD21	MemData00
AA22	$\overline{ExtAck}$	AB22	TMS	AC22	MemData02	AD22	No ball
AA23	OV_{DD}	AB23	$\overline{ExtReq}$	AC23	No ball	AD23	No ball
AA24	BusReq	AB24	No ball	AC24	No ball	AD24	No ball

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Signal Description

The PPC440GP embedded controller is provided in a 552-ball, ball grid array package. The following tables describe the package level pinout.

Pin Summary

Group	No. of Pins
Signal pins, non-multiplexed	347
Signal pins, multiplexed	57
Total Signal Pins	**404**
AxV_{DD}	3
AGnd	3
OV_{DD}	27
SV_{DD}	9
V_{DD}	34
Gnd	70
Total Power Pins	**146**
Reserved	2
Total Pins	**552**

In the table “Signal Functional Description” on page 48, each I/O signal is listed along with a short description of its function. Active-low signals (for example, $\overline{RAS}$) are marked with an overline. Please see “Signals Listed Alphabetically” on page 18 for the pin (ball) number to which each signal is assigned.

Multiplexed Signals

Some signals are multiplexed on the same pin so that the pin can be used for different functions. In most cases, the signal names shown in this table are not accompanied by signal names that may be multiplexed on the same pin. If you need to know what, if any, signals are multiplexed with a particular signal, look up the name in “Signals Listed Alphabetically” on page 18. It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

Multipurpose Signals

In addition to multiplexing, some pins are also multi-purpose. For example, the EBC peripheral controller address pins (PerAddr00:31) are used as outputs by the PPC440GP to broadcast an address to external slave devices when the PPC440GP has control of the external bus. When during the course of normal chip operation an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the PPC440GP. In this example, the pins are also bidirectional, serving both as inputs and outputs.

Multimode Signals

In some cases (for example, Ethernet) the function of a pin may vary with different modes of operation. When a pin has multiple signal names assigned to distinguish different modes of operation, all of the names are shown.

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Strapping Pins

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 80). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

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Signal Functional Description (Sheet 1 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCI-X Interface				
PCIXAD00:63	Address/Data bus (bidirectional).	I/O	3.3V PCI	
PCIXC0:7[$\overline{\text{BE0:7}}$]	PCI-X Command[Byte Enables].	I/O	3.3V PCI	
PCIXCap	Capable of PCI-X operation.	I	5V tolerant 3.3V LVTTL	5
PCIX133Cap	PCI-X devices are 133 MHz capable.	O	3.3V PCI	
PCIXClk	Provides timing to the PCI interface for PCI transactions. **Note:** If the PCI-X interface is not being used, drive this pin with a 3.3V clock signal at a frequency between 1 and 66MHz	I	3.3V PCI	
$\overline{\text{PCIXDevSel}}$	Indicates the driving device has decoded its address as the target of the current access.	I/O	3.3V PCI	4
$\overline{\text{PCIXFrame}}$	Driven by the current master to indicate beginning and duration of an access.	I/O	3.3V PCI	4
$\overline{\text{PCIXGnt0}}$	Indicates that the specified agent is granted access to the bus.	I/O	3.3V PCI	4
$\overline{\text{PCIXGnt1}}$	Indicates that the specified agent is granted access to the bus.	I/O	3.3V PCI	4
$\overline{\text{PCIXGnt2:5}}$	Indicates that the specified agent is granted access to the bus.	O	3.3V PCI	
PCIXIDSel	Used as a chip select during configuration read and write transactions.	I	3.3V PCI	5
$\overline{\text{PCIXINT}}$	Level sensitive PCI interrupt.	O	3.3V PCI	
$\overline{\text{PCIXIRDY}}$	Indicates initiating agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	4
PCIXM66En	Capable of 66MHz operation.	I	5V tolerant 3.3V LVTTL	5
PCIXParHigh	Even parity across PCIAD32:63 and PCIXC0:3[BE4:7].	I/O	3.3V PCI	
PCIXParLow	Even parity across PCIAD0:31 and PCIXC0:3[BE0:3].	I/O	3.3V PCI	
$\overline{\text{PCIXPErr}}$	Reports data parity errors during all PCI transactions except a Special Cycle.	I/O	3.3V PCI	4
$\overline{\text{PCIXReq0}}$	An indication to the PCI-X arbiter that the specified agent wishes to use the bus.	I/O	3.3V PCI	4
$\overline{\text{PCIXReq1:5}}$	An indication to the PCI-X arbiter that the specified agent wishes to use the bus.	I	3.3V PCI	4
$\overline{\text{PCIXReq64}}$	Asserted by the current bus master, indicating a 64-bit transfer.	I/O	3.3V PCI	4
$\overline{\text{PCIXAck64}}$	Indicates the target can transfer data using 64 bits.	I/O	3.3V PCI	4
$\overline{\text{PCIXReset}}$	Brings PCI device registers and logic to a consistent state.	O	3.3V PCI	
$\overline{\text{PCIXSErr}}$	Reports address parity errors, data parity errors on the Special Cycle command, or other catastrophic system errors.	I/O	3.3V PCI	4
$\overline{\text{PCIXStop}}$	Indicates the current target is requesting the master to stop the current transaction.	I/O	3.3V PCI	4
$\overline{\text{PCIXTRDY}}$	Indicates the target agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	4

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Signal Functional Description (Sheet 2 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
DDR SDRAM Interface				
BA0:1	Bank Address supporting up to four internal banks.	O	2.5V SSTL_2	
$\overline{\text{BankSel0:3}}$	Selects up to four external DDR SDRAM banks.	O	2.5V SSTL_2	
$\overline{\text{CAS}}$	Column Address Strobe.	O	2.5V SSTL_2	
ClkEn0:3	Clock Enable. One for each bank.	O	2.5V SSTL_2	
DM0:8	Memory write data byte lane masks. MEMDM8 is the byte lane mask for the ECC byte lane.	O	2.5V SSTL_2	
DQS0:8	Byte lane data strobe. DQS8 is the data strobe for the ECC byte lane.	I/O	2.5V SSTL_2	
ECC0:7	ECC check bits 0:7.	I/O	2.5V SSTL_2	
MemAddr00:12	Memory address bus.	O	2.5V SSTL_2	
MemClkOut0 $\overline{\text{MemClkOut0}}$	Subsystem clock.	O	2.5V SSTL_2	
MemData00:63	Memory data bus.	I/O	2.5V SSTL_2	
MemVRef1:2	Memory reference voltage (SV_{REF}) input.	I	Voltage Ref Receiver	
$\overline{\text{RAS}}$	Row Address Strobe.	O	2.5V SSTL_2	
$\overline{\text{WE}}$	Write Enable.	O	2.5V SSTL_2	
Ethernet Interface				
EMCCD, EMC1RxErr	MII: Collision detection RMII 1: Receive error	I/O	5V tolerant 3.3V LVTTL	
EMCCrS, EMC0CrSDV	MII: Carrier sense RMII 0: Carrier sense data valid	I/O	5V tolerant 3.3V LVTTL	
EMCMDClk	MII and RMII: Management data clock	O	5V tolerant 3.3V LVTTL	
EMCMDIO	MII and RMII: Transfer command and status information between MII and PHY	I/O	5V tolerant 3.3V LVTTL	
EMCRxD0:3, EMC0RxD0:1, EMC1RxD0:1	MII: Receive data RMII 0: Receive data RMII 1: Receive data	I/O	5V tolerant 3.3V LVTTL	
EMCRxDV, EMC1CrSDV	MII: Receive data valid RMII 1: Carrier sense data valid	I	5V tolerant 3.3V LVTTL	
EMCRxClk	MII: Receive clock	I	5V tolerant 3.3V LVTTL	
EMCRxErr, EMC0RxErr	MII: Receive error RMII 0: Receive error	I	5V tolerant 3.3V LVTTL	
EMCTxClk, EMCRefClk	MII: Transmit clock RMII: Reference clock	I	5V tolerant 3.3V LVTTL	5
EMCTxD0:3, EMC0TxD0:1, EMC1TxD0:1	MII: Transmit data RMII 0: Transmit data RMII 1: Transmit data	O	5V tolerant 3.3V LVTTL	

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Signal Functional Description (Sheet 3 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
EMCTxEn, EMC0TxEn	MII: Transmit data enabled RMII 0: Transmit data enabled	O	5V tolerant 3.3V LVTTL	
EMCTxErr, EMC1TxEn	MII: Transmit error: RMII: Transmit data enabled	O	5V tolerant 3.3V LVTTL	
External Slave Peripheral Interface				
DMAAck0:3	Used by the PPC440GP to indicate that data transfers have occurred.	O	5V tolerant 3.3V LVTTL	
DMAReq0:3	Used by slave peripherals to indicate they are prepared to transfer data.	I	5V tolerant 3.3V LVTTL	1, 5
EOT0:3/TC0:3	End Of Transfer/Terminal Count.	I/O	5V tolerant 3.3V LVTTL	1, 5
PerAddr00:31	Peripheral address bus used by PPC440GP when not in external master mode, otherwise used by external master. **Note:** PerAddr00 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerWBE0:3}}$	External peripheral data bus byte enables.	I/O	5V tolerant 3.3V LVTTL	1, 2
$\overline{\text{PerBLast}}$	Used by either the peripheral controller, DMA controller, or external master to indicates the last transfer of a memory access.	I/O	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{PerCS0:7}}$	External peripheral device select.	O	5V tolerant 3.3V LVTTL	2
PerData00:31	Peripheral data bus used by PPC440GP when not in external master mode, otherwise used by external master. **Note:** PerData00 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerOE}}$	Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the PPC440GP is the bus master, it enables the selected device to drive the bus.	O	5V tolerant 3.3V LVTTL	2
PerPar0:3	External peripheral data bus byte parity.	I/O	5V tolerant 3.3V LVTTL	1
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	5V tolerant 3.3V LVTTL	
PerR/$\overline{\text{W}}$	Used by the PPC440GP when not in external master mode, as output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory. Otherwise, it used by the external master as an input to indicate the direction of transfer.	I/O	5V tolerant 3.3V LVTTL	1, 2
$\overline{\text{PerWE}}$	Write Enable. Low when any of the four $\overline{\text{PerWBE0:3}}$ signals are low.	O	5V tolerant 3.3V LVTTL	2

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Signal Functional Description (Sheet 4 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
External Master Peripheral Interface				
BusReq	Bus Request. Used when the PPC440GP needs to regain control of peripheral interface from an external master.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{ExtAck}}$	External Acknowledgement. Used by the PPC440GP to indicate that a data transfer occurred.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{ExtReq}}$	External Request. Used by an external master to indicate it is prepared to transfer data.	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{ExtReset}}$	Peripheral Reset. Used by an external master and by synchronous peripheral slaves.	O	5V tolerant 3.3V LVTTL	
HoldAck	Hold Acknowledge. Used by the PPC440GP to transfer ownership of peripheral bus to an external master.	O	5V tolerant 3.3V LVTTL	
HoldReq	Hold Request. Used by an external master to request ownership of the peripheral bus.	I	5V tolerant 3.3V LVTTL	1, 5
PerClk	Peripheral Clock. Used by an external master and by synchronous peripheral slaves.	O	5V tolerant 3.3V LVTTL	
PerErr	External Error. Used as an input to record external master errors and external slave peripheral errors.	I/O	5V tolerant 3.3V LVTTL	1, 5
UART Peripheral Interface				
UARTSerClk	Serial clock input that provides an alternative to the internally generated serial clock. Used in cases where the allowable internally generated clock rates are not satisfactory. This input can be individually connected to either or both UART0 and UART1.	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Rx	UART0 Receive data.	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Tx	UART0 Transmit data.	O	5V tolerant 3.3V LVTTL	4
$\overline{\text{UART0\_DCD}}$	UART0 Data Carrier Detect.	I	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_DSR}}$	UART0 Data Set Ready.	I	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_CTS}}$	UART0 Clear To Send.	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{UART0\_DTR}}$	UART0 Data Terminal Ready.	O	5V tolerant 3.3V LVTTL	4
$\overline{\text{UART0\_RTS}}$	UART0 Request To Send.	O	5V tolerant 3.3V LVTTL	4
$\overline{\text{UART0\_RI}}$	UART0 Ring Indicator.	I	5V tolerant 3.3V LVTTL	1, 4
UART1_Rx	UART1 Receive data.	I/O	5V tolerant 3.3V LVTTL	1, 4
UART1_Tx	UART1 Transmit data.	I/O	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{UART1\_DSR}}$/$\overline{\text{CTS}}$	UART1 Data Set Ready or Clear To Send. The choice is determined by a DCR register bit setting.	I/O	5V tolerant 3.3V LVTTL	1, 4

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Signal Functional Description (Sheet 5 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
$\overline{\text{UART1\_RTS/DTR}}$	UART1 Request To Send or Data Terminal Ready. The choice is determined by a DCR register bit setting.	I/O	5V tolerant 3.3V LVTTL	1, 4
IIC Peripheral Interface				
IIC0SClk	IIC0 Serial Clock.	I/O	5V tolerant 3.3V LVTTL	1, 2
IIC0SDA	IIC0 Serial Data.	I/O	5V tolerant 3.3V LVTTL	1, 2
IIC1SClk	IIC1 Serial Clock.	I/O	5V tolerant 3.3V LVTTL	1, 2
IIC1SDA	IIC1 Serial Data.	I/O	5V tolerant 3.3V LVTTL	1, 2
Interrupts Interface				
IRQ00:10	External interrupt Requests 0 through 10.	I	5V tolerant 3.3V LVTTL	1, 5
IRQ11:12	External interrupt Requests 11 through 12.	I	3.3V PCI	
JTAG Interface				
TCK	Test Clock.	I	3.3V CMOS w/pull-up	1
TDI	Test Data In.	I	3.3V CMOS w/pull-up	4
TDO	Test Data Out.	O	3.3V LVTTL	
TMS	Test Mode Select.	I	3.3V CMOS w/pull-up	1
$\overline{\text{TRST}}$	Test Reset. During chip power-up, this signal must be low from the start of V_{DD} ramp-up until at least 16 SysClk cycles after V_{DD} is stable in order to initialize the JTAG controller.	I	3.3V CMOS w/pull-up	5

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Signal Functional Description (Sheet 6 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
System Interface				
SysClk	Main system clock input.	Clock	5V tolerant 3.3V LVTTL	
SysErr	Set to 1 when a machine check is generated.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{SysReset}}$	Main system reset. External logic can drive this bidirectional pin low (minimum of 16 cycles) to initiate a system reset. A system reset can also be initiated by software. The signal is implemented as an open-drain output (two states; 0 or open circuit). During chip power-up, this signal must be low from the start of V_{DD} ramp-up until at least 16 SysClk cycles after V_{DD} is stable.	I/O	5V tolerant 3.3V LVTTL	1, 2
TmrClk	Processor timer external input clock.	I	5V tolerant 3.3V LVTTL	
$\overline{\text{Halt}}$	Halt from external debugger.	I	5V tolerant 3.3V LVTTL	1, 4
GPIO00:31	General purpose I/O 0 through 10. To access these functions, software must set DCR register bits.	I/O	5V tolerant 3.3V LVTTL	
TestEn	Test Enable.	I	1.8V CMOS w/pull-down	3
RcvrInh	Receiver Inhibit. Active only when TestEn is active.	I	5V tolerant 3.3V LVTTL	
RefVEn	Reference Voltage Enable. Do not connect for normal operation. Pull up for Boundary Scan Description Language (BSDL) testing.	I	1.8V CMOS w/pull-down	
DrvrInh1:2	Driver Inhibit. Used for test purposes only. Tie up for normal operation	I	5V tolerant 3.3V LVTTL	2

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Signal Functional Description (Sheet 7 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Trace Interface				
TrcBS0:2	Trace branch execution status.	I/O	5V tolerant 3.3V LVTTL	
TrcClk	Trace data capture clock, runs at 1/4 the frequency of the processor.	O	5V tolerant 3.3V LVTTL	
TrcES0:4	Trace Execution Status is presented every fourth processor clock cycle.	I/O	5V tolerant 3.3V LVTTL	
TrcTS0:6	Additional information on trace execution and branch status.	I/O	5V tolerant 3.3V LVTTL	
Power Pins				
AGND	PLL (analog) voltage ground.	na	na	
GND	Ground.	na	na	
AxV_{DD}	1.8V—Filtered voltages input for PLLs (analog circuits) **Note:** A separate filter for each of the three voltages is recommended.	na	na	
OV_{DD}	3.3V supply—I/O (except DDR SDRAM)	na	na	
SV_{DD}	2.5V supply—DDR SDRAM	na	na	
V_{DD}	1.8V supply—Logic voltage.	na	na	
Reserved Pins				
Reserved	Do not connect signals, voltage, or ground to these balls.	na	na	

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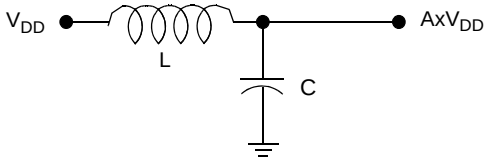
Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. *Operation at or beyond these maximum ratings can cause permanent damage to the device. None of the performance specification contained in this document are guaranteed when operating at these maximum ratings.*

Characteristic	Symbol	Value	Unit	Notes
Supply Voltage (Internal Logic)	V_{DD}	0 to +1.95	V	
Supply Voltage (I/O Interface, except DDR SDRAM)	OV_{DD}	0 to +3.6	V	
PLL Supply Voltages	AxV_{DD}	0 to +1.95	V	1
Supply Voltage (DDR SDRAM Logic)	SV_{DD}	0 to +2.7	V	
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to +3.6	V	
Input Voltage (5.0V LVTTL receivers)	V_{IN}	0 to +5.5	V	
Storage Temperature Range	T_{STG}	-55 to +150	°C	
Case Temperature under bias	T_C	-40 to +120	°C	2

Notes:

1. The analog voltages used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440GP. A separate filter, as shown below, is recommended for each voltage:



L – SMT ferrite bead chip, Murata BLM31A700S or equivalent.

C – 0.1µF ceramic

2. This value is not a specification of the operational temperature range; it is a stress rating only.

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Package Thermal Specifications

Thermal resistance values for the CBGA and PBGA packages in a convection environment are as follows:

Parameter	Symbol	Package	Airflow ft/min (m/sec)			Unit	Notes
			0 (0)	100 (0.51)	200 (1.02)		
Junction-to-case thermal resistance	θ_{JC}	Ceramic	<0.1	<0.1	<0.1	°C/W	1
		Plastic	1.2	1.2	1.2	°C/W	1, 3
Case-to-ambient thermal resistance (w/o heat sink)	θ_{CA}	Ceramic	18.9	17.7	16.3	°C/W	2
		Plastic		20.8		°C/W	2, 3
Junction-to-ball (typical)	θ_{JB}	Ceramic				°C/W	
		Plastic		8.0		°C/W	3

Notes:

1. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
2. The case-to-ambient thermal resistance is measured in a JEDEC JESD51-6 standard environment; and may not accurately predict thermal performance in production equipment environments. The operational case temperature must be maintained.
3. Modeled on standard JEDEC 2S2P card, 50x50mm

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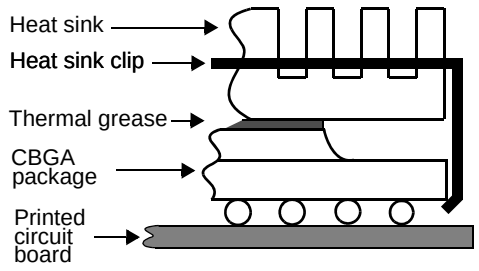
Heat Sink Mounting Information (Ceramic Package Only)

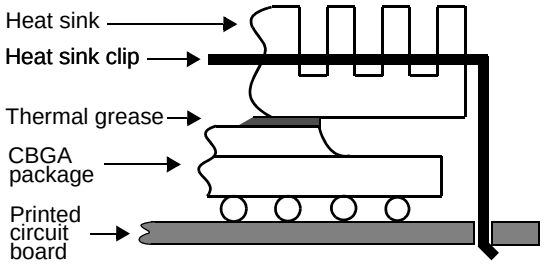
Proper thermal design is primarily dependent upon multiple system-level effects; that is, the effects of the heat sink, the air flow, and the thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods: adhesive, spring clips to the printed-circuit board or package, or a mounting clip and screw assembly. When attaching heat sinks, it is important to avoid placing excessive mechanical stress on bonding of the chip to the substrate and the package to the board.

Heat Sink Attached With Spring Clip



Spring clip to package

Static compression (spring force)—2.27kg maximum

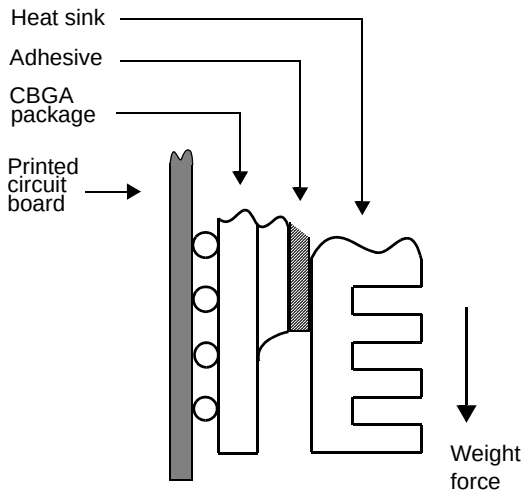


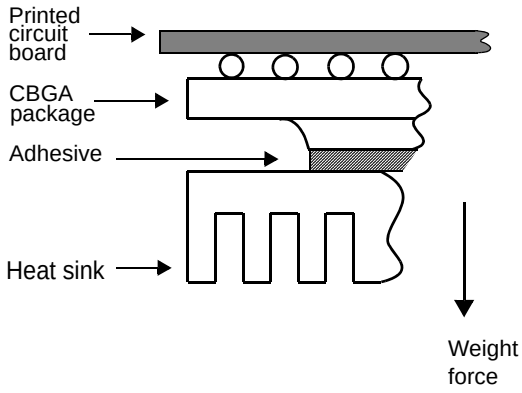
Spring clip to board

Static compression (spring force)—2.27kg maximum[1]

Note 1: Force is limited by allowable compression on the die. Allowable package compression force is 4.4kg.

Heat Sink Attached With Adhesive





Heat sink weight force—60g maximum

Important: All of the guidelines indicated in the above diagrams must be evaluated and adjusted to account for the shock and vibration effects of any particular application.

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Recommended DC Operating Conditions

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	+1.7	+1.8	+1.9	V	4
I/O Supply Voltage	OV_{DD}	+3.0	+3.3	+3.6	V	4
DDR SDRAM Supply Voltage (DDR clock up to 166 MHz)	SV_{DD}	+2.3	+2.5	+2.7	V	4
PLL Supply Voltages	AxV_{DD}	+1.65	+1.8	+1.95	V	3
DDR SDRAM Reference Voltage	SV_{REF}	+1.15	+1.25	+1.35	V	3
Input Logic High (2.5V SSTL)	V_{IH}	SV_{REF}+0.18		SV_{DD}+0.3	V	2
Input Logic High (3.3V PCI-X)		$0.5OV_{DD}$		OV_{DD}+0.5	V	1
Input Logic High (3.3V LVTTL, 5V tolerant receiver)		+2.0		+5.5	V	
Input Logic Low (2.5V SSTL)	V_{IL}	-0.3		SV_{REF}-0.18	V	
Input Logic Low (3.3V PCI-X)		-0.5		$0.35OV_{DD}$	V	1
Input Logic Low (3.3V LVTTL, 5V tolerant receiver)		0		+0.8	V	
Output Logic High (2.5V SSTL)	V_{OH}	+1.95		SV_{DD}	V	
Output Logic High (3.3V PCI-X)		$0.9OV_{DD}$		OV_{DD}	V	1
Output Logic High (3.3V LVTTL, 5V tolerant receiver)		+2.4		OV_{DD}	V	
Output Logic Low (2.5V SSTL)	V_{OL}	0		0.55	V	
Output Logic Low (3.3V PCI-X)				$0.1OV_{DD}$	V	1
Output Logic Low (3.3V LVTTL, 5V tolerant receiver)		0		+0.4	V	
Input Leakage Current (No pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current for Pull-Down	I_{IL2}	0 (LPDL)		200 (MPUL)	µA	5
Input Leakage Current for Pull-Up	I_{IL3}	-150 (LPDL)		0 (MPUL)	µA	5
Input Max Allowable Overshoot (3.3V LVTTL, 5V tolerant receiver)	V_{IMAO}			+5.5	V	
Input Max Allowable Undershoot (3.3V LVTTL, 5V tolerant receiver)	V_{IMAU}	-0.6			V	
Output Max Allowable Overshoot (3.3V LVTTL, 5V tolerant receiver)	V_{OMAO}			+5.5	V	
Output Max Allowable Undershoot (3.3V LVTTL, 5V tolerant receiver)	V_{OMAU3}	-0.6			V	

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Recommended DC Operating Conditions (Continued)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Case Temperature rating for C package	T_C	-40		+85	°C	6
Case Temperature rating E for C package	T_C	-40		+105	°C	6
Case Temperature rating E for F package	T_C	-40		+100	°C	6

Notes:

1. PCI-X drivers meet PCI-X specifications.
2. $SV_{REF} = SV_{DD}/2$
3. The analog voltages used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440GP. See “Absolute Maximum Ratings” on page 55.
4. There are no OV_{DD}, V_{DD}, or SV_{DD} power supply power-up sequence requirements. However, external voltage should not be applied to the chip I/O pins before OV_{DD} is applied to the chip. A power-down cycle should complete (OV_{DD} and V_{DD} should both be below 0.4V) before a new power- up cycle is started.
5. LPDL is least positive down level; MPUL is most positive up level.
6. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.

Input Capacitance

Parameter	Symbol	Maximum	Unit	Notes
Group 1 (2.5V SSTL I/O)	C_{IN1}	12	pF	
Group 2 (5V tolerant LVTTL I/O)	C_{IN2}	12	pF	
Group 3 (PCI-X I/O)	C_{IN3}	12	pF	
Group 4 (Receivers)	C_{IN4}	9	pF	

DC Power Supply Loads

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
V_{DD} (1.8V) active operating current	I_{DD}		915		mA	2
OV_{DD} (3.3V) active operating current	I_{ODD}		125		mA	2
SV_{DD} (2.5V) active operating current	I_{SDD}		560		mA	2
AxV_{DD} (1.8 V) input current	I_{ADD}		33		mA	1, 2

Notes:

1. See “Absolute Maximum Ratings” on page 55 for filter recommendations.
2. The current values listed above are not guaranteed to be the highest obtainable. These values are dependent on many factors including the type of applications running, clock rates, use of internal functional capabilities, external interface usage, case temperature, and the power supply voltages. Your specific application can produce significantly different results. V_{DD} (logic) current and power are primarily dependent on the applications running and the use of internal chip functions (DMA, PCI, Ethernet, and so on). OV_{DD} (I/O) current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses.

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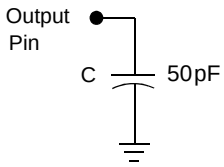
Test Conditions

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table "Recommended DC Operating Conditions." AC specifications are characterized with V_{DD} = 1.8V, T_C = rated temperature and a 50pF test load as shown in the figure to the right.



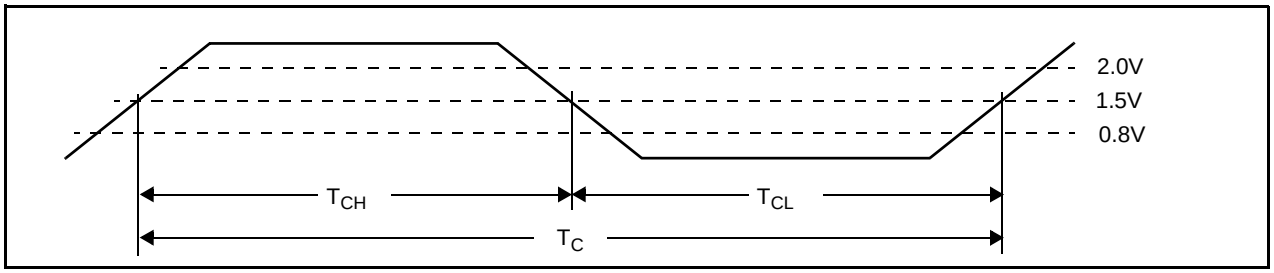
Clocking Specifications

Symbol	Parameter	Minimum	Maximum	Units	Notes
SysClk Input					
F_C	Frequency	33.33	66.66	MHz	
T_C	Period	15	30	ns	
T_{CS}	Edge stability (cycle-to-cycle jitter)	–	±0.15	ns	
T_{CH}	High time	40% of nominal period	60% of nominal period	ns	
T_{CL}	Low time	40% of nominal period	60% of nominal period	ns	
Note: Input slew rate ≥ 1V/ns					
PLL VCO					
F_C	Frequency	500	1000	MHz	
T_C	Period	1	2	ns	
Processor Clock (CPU Clock)					
F_C	Frequency	–	500	MHz	1
T_C	Period	2	–	ns	
MemClkOut					
F_C	Frequency	100	133.33	MHz	
T_C	Period	7.5	10	ns	
T_{CH}	High time	35% of nominal period	65% of nominal period	ns	

Notes:

1. The maximum supported processor clock frequency for any part is specified in the part number (see "Ordering and PVR Information" on page 4).

Timing Waveform



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Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC440GP. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC440GP the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC440GP with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board PPC440GP peripherals impose more stringent requirements.
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the DDR SDRAM MemClkOut since it also tracks the modulation.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates.
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.

Important: It is up to the system designer to ensure that any SSCG used with the PPC440GP meets the above requirements and does not adversely affect other aspects of the system.

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Peripheral Interface Clock Timings

Parameter	Min	Max	Units	Notes
PCIXClk input frequency (asynchronous mode)	–	133.33	MHz	2
PCIXClk period (asynchronous mode)	7.5	–	ns	
PCIXClk input high time	40% of nominal period	60% of nominal period	ns	
PCIXClk input low time	40% of nominal period	60% of nominal period	ns	
EMCMDClk output frequency	–	2.5	MHz	
EMCMDClk period	400	–	ns	
EMCMDClk output high time	160	–	ns	
EMCMDClk output low time	160	–	ns	
EMCTxClk input frequency MII(RMII)	2.5(5)	25(50)	MHz	
EMCTxClk period MII(RMII)	40(20)	400(200)	ns	
EMCTxClk input high time	35% of nominal period	–	ns	
EMCTxClk input low time	35% of nominal period	–	ns	
EMCRxClk input frequency MII(RMII)	2.5(5)	25(50)	MHz	
EMCRxClk period MII(RMII)	40(20)	400(200)	ns	
EMCRxClk input high time	35% of nominal period	–	ns	
EMCRxClk input low time	35% of nominal period	–	ns	
EMCRefClk input frequency	–	50	MHz	
EMCRefClk period	20		ns	
EMCRefClk input high time	45% of nominal period	55% of nominal period	ns	
EMCRefClk input low time	45% of nominal period	55% of nominal period	ns	
PerClk output frequency (for ext. master or sync. slaves)	–	66.66	MHz	
PerClk period	15	–	ns	
PerClk output high time	50% of nominal period	66% of nominal period	ns	
PerClk output low time	33% of nominal period	50% of nominal period	ns	
UARTSerClk input frequency	–	$1000/(2T_{OPB}^{1}+2ns)$	MHz	1
UARTSerClk period	$2T_{OPB}+2$	–	ns	1
UARTSerClk input high time	$T_{OPB}+1$	–	ns	1
UARTSerClk input low time	$T_{OPB}+1$	–	ns	1

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Peripheral Interface Clock Timings (Continued)

Parameter	Min	Max	Units	Notes
TmrClk input frequency	–	100	MHz	
TmrClk period	10	–	ns	
TmrClk input high time	40% of nominal period	60% of nominal period	ns	
TmrClk input low time	40% of nominal period	60% of nominal period	ns	

Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at 1/2the frequency of the PLB clock. The maximum OPB clock frequency is 66.66 MHz.
2. When the PCI-X interface is used to support a legacy PCI interface, the maximum PCIXClk frequency is 66.66MHz.

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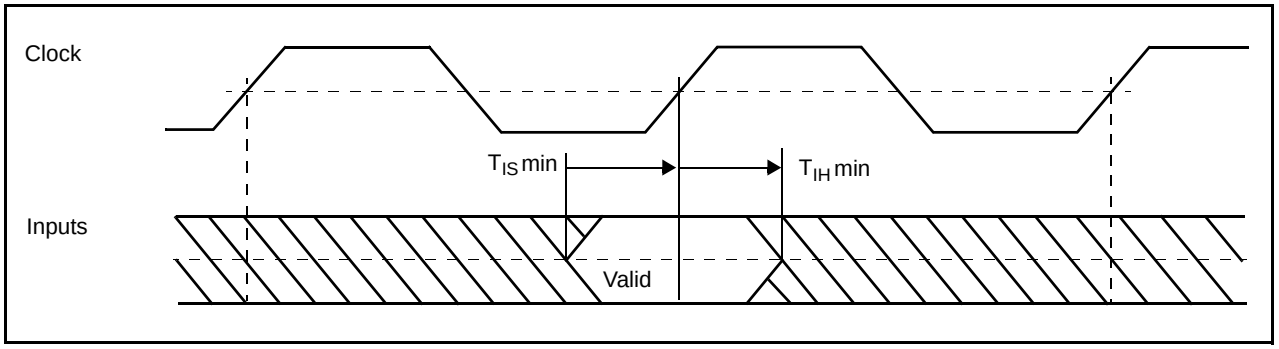
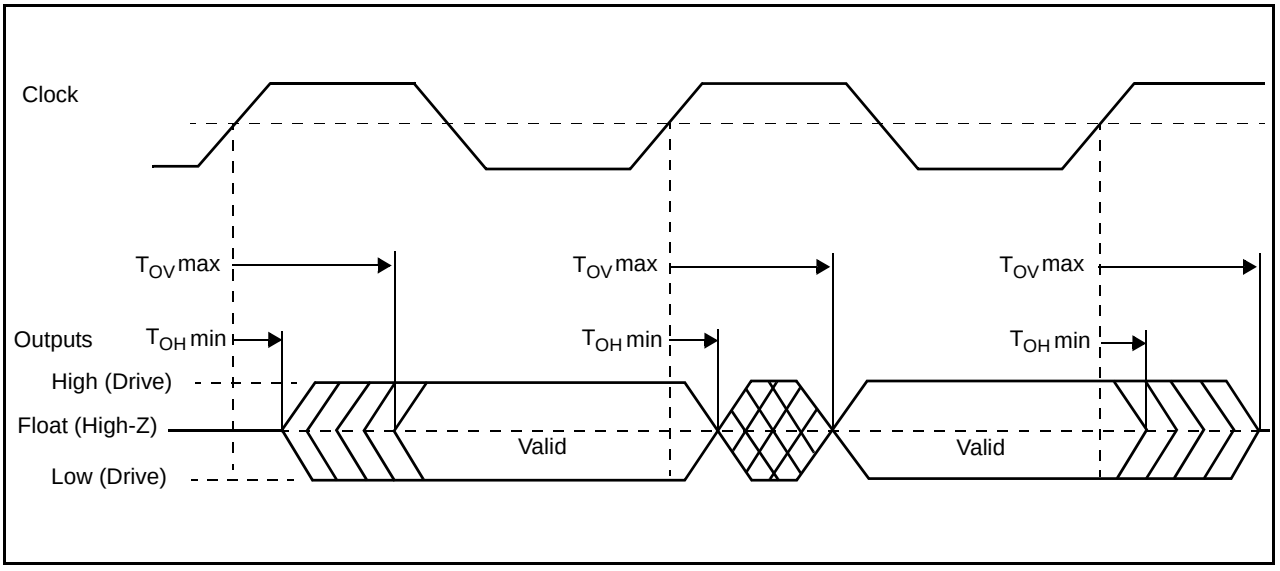
Input Setup and Hold Waveform



Output Delay and Float Timing Waveform



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I/O Specifications—All Speeds (Sheet 1 of 4)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
3. The clock frequency for RMII operation is 50MHz ± 100ppm.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
PCI-X Interface								
PCIXAD00:63	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIXC3:0[$\overline{\text{BE3:0}}$]	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIXParLow	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIParHigh	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXFrame}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXINT}}$	na	na	dc	dc	0.5	1.5	PCIXClk	async
$\overline{\text{PCIXIRDY}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXTRDY}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXStop}}$	Note 2 (3	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXDevSel}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIXIDSel	Note 2 (3)	0.5 (0)	na	na	na	na	PCIXClk	2
$\overline{\text{PCIXPErr}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXSErr}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIXClk	dc	dc	na	na	na	na		async
$\overline{\text{PCIXReset}}$	na	na	na	na	na	na	PCIXClk	
$\overline{\text{PCIXReq64}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXAck64}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIXCap	Note 2 (3)	0.5 (0)	na	na	na	na	PCIXClk	2
PCIX133Cap			3.8	0.7	0.5	1.5	PCIXClk	2
PCIXM66En	Note 2 (3)	0.5 (0)	na	na	na	na	PCIXClk	2
$\overline{\text{PCIXReq0:5}}$	Note 2 (3)	0.5 (0)	na	na	na	na	PCIXClk	2
$\overline{\text{PCIXGnt0:5}}$	na)	na	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2

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I/O Specifications—All Speeds (Sheet 2 of 4)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
3. The clock frequency for RMII operation is 50MHz ± 100ppm.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
Ethernet MII Interface								
EMCRxD0:3	4	1	na	na	n/a	n/a	EMCRxClk	1
EMCRxDV	4	1	na	na	n/a	n/a	EMCRxClk	1
EMCRxClk	na	na	na	na	n/a	n/a		1, async
EMCRxErr	4	1	na	na	n/a	n/a	EMCRxClk	1
EMCTxD0:3	na	na	15	2	10.3	7.1	EMCTxClk	1
EMCTxEn	na	na	15	2	10.3	7.1	EMCTxClk	1
EMCTxClk	na	na	na	na	na	na		1, async
EMCTxErr	na	na	15	2	10.3	7.1	EMCTxClk	1
EMCCrS			na	na	n/a	n/a		1, async
EMCCD			na	na	n/a	n/a		1, async
EMCMDIO					10.3	7.1	EMCMDClk	1
EMCMDClk	na	na	na	na	10.3	7.1		1, async
Ethernet RMII Interface								
EMC0RxD0:1	2	1	na	na	n/a	n/a	EMCRxClk	
EMC0RxErr	2	1	na	na	n/a	n/a	EMCRxClk	
EMC0CrSDV			na	na	n/a	n/a	EMCRxClk	
EMC0TxD0:1	na	na	11	2	10.3	7.1	EMCTxClk	
EMC0:1TxEn	na	na	11	2	10.3	7.1	EMCTxClk	
EMC1RxD0:1			na	na	10.3	7.1	EMCRxClk	
EMC1RxErr			na	na	n/a	n/a	EMCRxClk	
EMC1CrSDV			na	na	n/a	n/a	EMCRxClk	
EMC1TxD0:1	na	na	11	2	10.3	7.1	EMCTxClk	
EMCRefClk	na	na	na	na	10.3	7.1		3, async

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I/O Specifications—All Speeds (Sheet 3 of 4)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
3. The clock frequency for RMII operation is 50MHz ± 100ppm.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
Internal Peripheral Interface								
IICxSClk	na	na	na	na	15.3	10.2		
IICxSDA					15.3	10.2		
UARTSerClk	na	na	na	na	na	na		
UART0_Rx			na	na	na	na		
UART0_Tx	na	na			10.3	7.1		
$\overline{\text{UART0\_DCD}}$			na	na	na	na		
$\overline{\text{UART0\_DSR}}$			na	na	na	na		
$\overline{\text{UART0\_CTS}}$			na	na	na	na		
$\overline{\text{UART0\_DTR}}$	na	na			10.3	7.1		
$\overline{\text{UART0\_RI}}$			na	na	na	na		
$\overline{\text{UART0\_RTS}}$	na	na			10.3	7.1		
UART1_Rx			na	na	na	na		
UART1_Tx	na	na			10.3	7.1		
$\overline{\text{UART1\_DSR/CTS}}$			na	na	na	na		
$\overline{\text{UART1\_RTS/DTR}}$	na	na			10.3	7.1		
Interrupts Interface								
IRQ00:12					na	na		
JTAG Interface								
TDI					na	na		async
TMS					na	na		async
TDO					15.3	10.2		async
TCK					na	na		async
$\overline{\text{TRST}}$					na	na		async

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I/O Specifications—All Speeds (Sheet 4 of 4)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
3. The clock frequency for RMII operation is 50MHz ± 100ppm.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
System Interface								
SysClk			na	na	na	na		
TmrClk			na	na	na	na		async
$\overline{\text{SysReset}}$					na	na		async
$\overline{\text{Halt}}$			na	na	na	na		async
SysErr	na	na			10.3	7.1		async
$\overline{\text{TestEn}}$			na	na	na	na		async
DrvrInh1:2			na	na	na	na		
GPIO00:31					10.3	7.1		
Trace Interface								
TrcClk	na	na			10.3	7.1		
TrcBS0:2					10.3	7.1		
TrcES0:4					10.3	7.1		
TrcTS0:6					10.3	7.1		

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I/O Specifications—400, 466, and 500 MHz

Notes:

1. PerClk rising edge at package pin with a 10 pF load trails the internal PLB clock by approximately 1.3 ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
External Slave Peripheral Interface								
PerData00:31	3	1	9	0	15.3	10.2	PerClk	
PerAddr00:31	3	1	7.6	0	15.3	10.2	PerClk	
PerPar0:3	4	1	8.4	0	15.3	10.2	PerClk	
$\overline{\text{PerWBE0:3}}$	2.5	1	6.5	0	15.3	10.2	PerClk	
$\overline{\text{PerCS0:7}}$	na	na	6	0	15.3	10.2	PerClk	
$\overline{\text{PerOE}}$	na	na	6	0	15.3	10.2	PerClk	
$\overline{\text{PerWE}}$	na	na	7	0	15.3	10.2		
$\overline{\text{PerBLast}}$	2.5	1	5	na	15.3	10.2	PerClk	
PerReady[RcvrInh]	5	1	na	na	na	na	PerClk	
PerR/$\overline{\text{W}}$	2.5	1	5.6	na	15.3	10.2	PerClk	
DMAReq0:3	dc	dc	na	na	na	na	PerClk	
DMAAck0:3	na	na	7	0	15.3	10.2	PerClk	
EOT0:3/TC0:3	dc	dc	6.8	0	15.3	10.2	PerClk	
External Master Peripheral Interface								
PerClk	na	na	na	na	15.3	10.2	PLB Clk	1
$\overline{\text{ExtReset}}$	na	na	6.2	0	15.3	10.2	PerClk	
HoldReq	3.5	1	na	na	na	na	PerClk	
HoldAck	na	na	6.4	0	15.3	10.2	PerClk	
$\overline{\text{ExtReq}}$	2.5	1	na	na	na	na	PerClk	
$\overline{\text{ExtAck}}$	na	na	6.2	0	15.3	10.2	PerClk	
BusReq	na	na	6.2	0	15.3	10.2	PerClk	
PerErr	4.5	1	na	na	15.3	10.2	PerClk	

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DDR SDRAM I/O Specifications

The DDR SDRAM controller times its operation with internal PLB clock signals and generates MemClkOut0 from the PLB clock. The PLB clock is an internal signal that cannot be directly observed. However MemClkOut0 is the same frequency as the PLB clock signal and is in phase with the PLB clock signal.

Note: MemClkOut0 can be advanced with respect to the PLB clock by means of the SDRAM0_CLKTR programming register. In a typical system, users advance MemClkOut by 90°. This depends on the specific application and requires a thorough understanding of the memory system in general (refer to the DDR SDRAM controller chapter in the *PowerPC 440GP User's Manual*).

In the following sections, the label MemClkOut0(0) refers to MemClkOut0 when it has not been phase-shifted, and MemClkOut0(90) refers to MemClkOut0 when it has been phase-advanced 90°. Advancing MemClkOut0 by 90° creates a 3/4 cycle setup time and 1/4 cycle hold time for the address and control signals in relation to MemClkOut0(90). The rising edge of MemClkOut0(90) aligns with the first rising edge of the DQS signal.

The following DDR data is generated by means of simulation and includes logic, driver, package RLC, and lengths. Values are calculated over best case and worst case processes with speed, temperature, and voltage as follows:

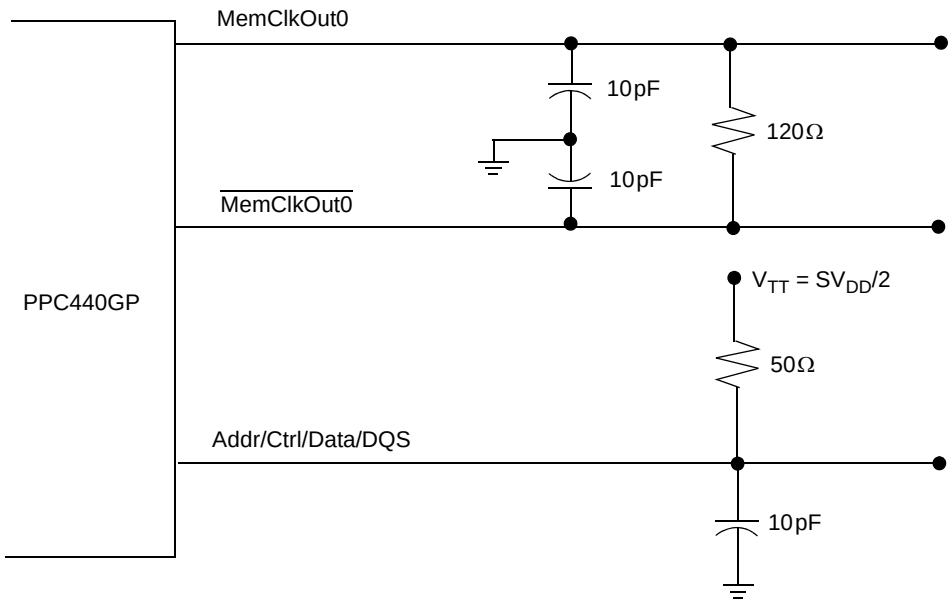
Best Case = Fast process, -40°C, +1.9V

Worst Case = Slow process, +85°C, +1.7V

Note: In all the following DDR tables and timing diagrams, the maximum values are measured under worst case conditions. The minimum values (best case) are estimates based on comparable timing in a similar chip of a different technology.

The signals are terminated as indicated in the figure below for the DDR timing data in the following sections.

DDR SDRAM Simulation Signal Termination Model



Note: This diagram illustrates the model of the DDR SDRAM interface used when generating simulation timing data. It is *not* a recommended physical circuit design for this interface. An actual interface design will depend on many factors, including the type of memory used and the board layout.

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DDR SDRAM Output Driver Specifications

Signal Path	Output Current (mA)	
	I/O H (maximum)	I/O L (minimum)
Write Data		
MemData00:07	15.2	15.2
MemData08:15	15.2	15.2
MemData16:23	15.2	15.2
MemData24:31	15.2	15.2
MemData32:39	15.2	15.2
MemData40:47	15.2	15.2
MemData48:55	15.2	15.2
MemData56:63	15.2	15.2
ECC0:7	15.2	15.2
DM0:8	15.2	15.2
MemClkOut0	15.2	15.2
MemAddr00:12	15.2	15.2
BA0:1	15.2	15.2
$\overline{\text{RAS}}$	15.2	15.2
$\overline{\text{CAS}}$	15.2	15.2
$\overline{\text{WE}}$	15.2	15.2
$\overline{\text{BankSel0:3}}$	15.2	15.2
ClkEn0:3	15.2	15.2
DQS0:8	15.2	15.2

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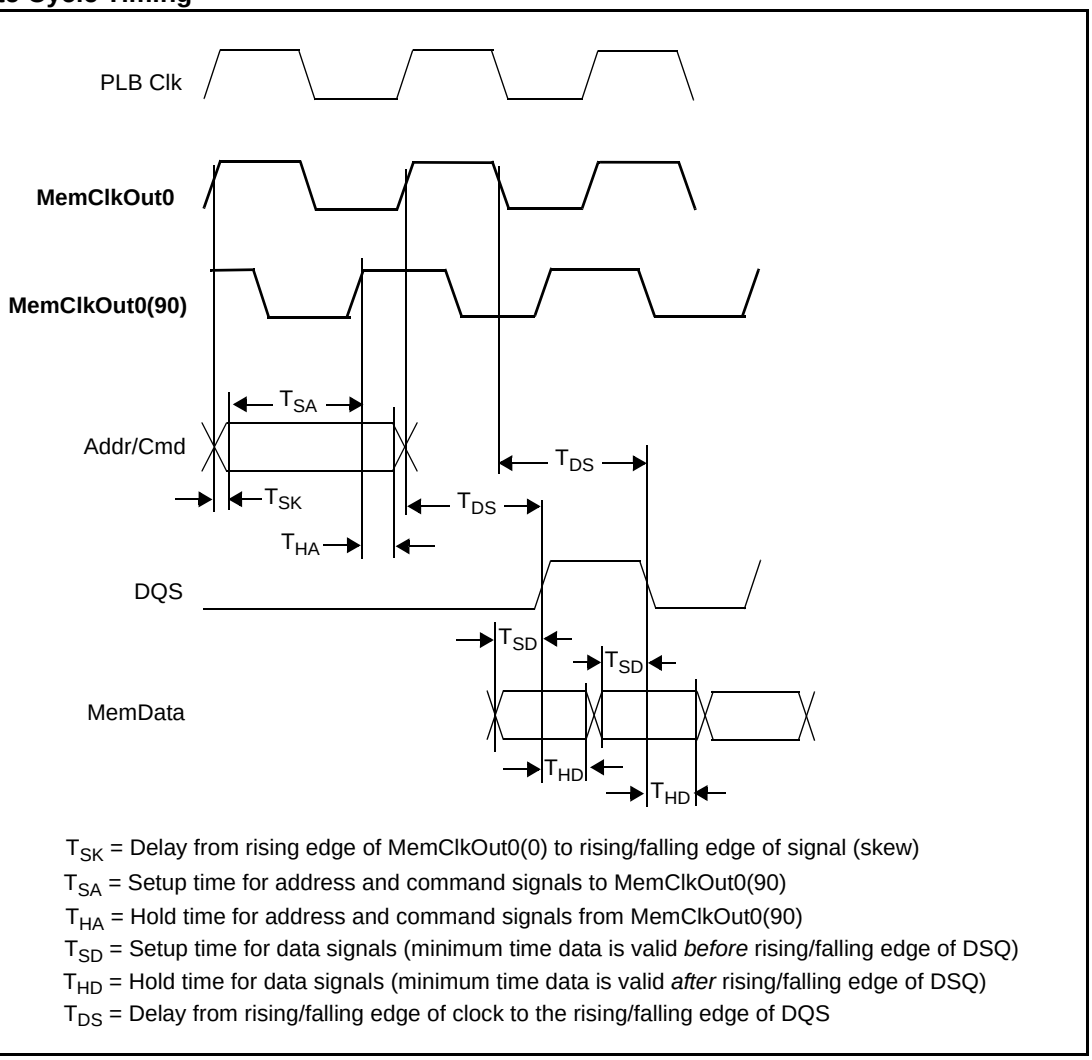
DDR SDRAM Write Operation

The following diagram illustrates the relationship among the signals involved with a DDR write operation.

DDR SDRAM Write Cycle Timing



T_{SK} = Delay from rising edge of MemClkOut0(0) to rising/falling edge of signal (skew)
T_{SA} = Setup time for address and command signals to MemClkOut0(90)
T_{HA} = Hold time for address and command signals from MemClkOut0(90)
T_{SD} = Setup time for data signals (minimum time data is valid *before* rising/falling edge of DSQ)
T_{HD} = Hold time for data signals (minimum time data is valid *after* rising/falling edge of DSQ)
T_{DS} = Delay from rising/falling edge of clock to the rising/falling edge of DQS

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I/O Timing—DDR SDRAM T_{DS}

Notes:
1. All of the DQS signals are referenced to MemClkOut0(0).
2. The T_{DS} values in the table include 3/4 of a cycle at the indicated clock speed.
3. To obtain adjusted values for lower clock frequencies, subtract 5.625 ns from the values in the table and add 3/4 of the cycle time for the lower clock frequency (T_{DS} - 5.625 + 0.75T_{CYC}).

Clock Speed (MHz)	Signal Name	T_{DS} (ns)	
		Minimum	Maximum
133	DQS0	na	6.25
133	DQS1	na	6.25
133	DQS2	na	6.25
133	DQS3	na	6.25
133	DQS4	na	6.25
133	DQS5	na	6.25
133	DQS6	na	6.25
133	DQS7	na	6.25
133	DQS8	na	6.25

I/O Timing—DDR SDRAM T_{SK}, T_{SA}, and T_{HA}

Notes:
1. T_{SK} is referenced to MemClkOut0(0). T_{SA} and T_{HA} are referenced to MemClkOut0(90).
2. To obtain adjusted T_{SA} values for lower clock frequencies, use 3/4 of the cycle time for the lower clock frequency and subtract T_{SK} maximum (0.75T_{CYC} - T_{SK}max).
3. To obtain adjusted T_{HA} values for lower clock frequencies, use 1/4 of the cycle time for the lower clock frequency and add T_{SK} minimum (0.25T_{CYC} + T_{SK}min).

Clock Speed (MHz)	Signal Name	T_{SK} (ns)		T_{SA} (ns)	T_{HA} (ns)
		Minimum	Maximum	Minimum	Minimum
133	MemAddr00:12	0.4	1.2	4.425	2.275
133	BA0:1	0.4	1.2	4.425	2.275
133	BankSel0:3	0.4	1.2	4.425	2.275
133	ClkEn0:3	0.4	1.2	4.425	2.275
133	$\overline{\text{CAS}}$	0.4	1.2	4.425	2.275
133	$\overline{\text{RAS}}$	0.4	1.2	4.425	2.275
133	$\overline{\text{WE}}$	0.4	1.2	4.425	2.275

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I/O Timing—DDR SDRAM T_{SD} and T_{HD}

Notes:

1. T_{SD} and T_{HD} are measured under worst case conditions.
2. The time values in the table include 1/4 of a cycle at the indicated clock speed.
3. To obtain adjusted T_{SD} and T_{HD} values for lower clock frequencies, subtract 1.875 ns from the values in the table and add 1/4 of the cycle time for the lower clock frequency (e.g., T_{SD} - 1.875 + 0.25T_{CYC}).

Clock Speed (MHz)	Signal Names	Reference Signal	T_{SD} (ns)	T_{HD} (ns)
133	MemData00:07, DM0	DQS0	1.375	1.375
133	MemData08:15, DM1	DQS1	1.375	1.375
133	MemData16:23, DM2	DQS2	1.375	1.375
133	MemData24:31, DM3	DQS3	1.375	1.375
133	MemData32:39, DM4	DQS4	1.375	1.375
133	MemData40:47, DM5	DQS5	1.375	1.375
133	MemData48:55, DM6	DQS6	1.375	1.375
133	MemData56:63, DM7	DQS7	1.375	1.375
133	ECC0:7, DM8	DQS8	1.375	1.375

DDR SDRAM Read Operation

The following examples of timing for DDR SDRAM read operations are based on the relationship between the incoming data and the PLB clock signal. Since the PLB clock cannot be directly observed, the delay of MemClkOut(0) relative to the PLB clock (T_{MD}) is provided.

The internal Read Clock signal, like MemClkOut0, is derived from the PLB clock and can be delayed relative to the PLB clock by programming the RDCT and RDCD fields in the SDRAM0_TR1 register. The delay can be programmed from 0 to 1/2 cycle in steps using RDCT. Setting RDCD results in a 1/2 cycle delay plus the value set in RDCT. The delay of Read Clock relative to the PLB clock (T_{RD}) shown below assumes the programmable Read Clock delay is set to zero.

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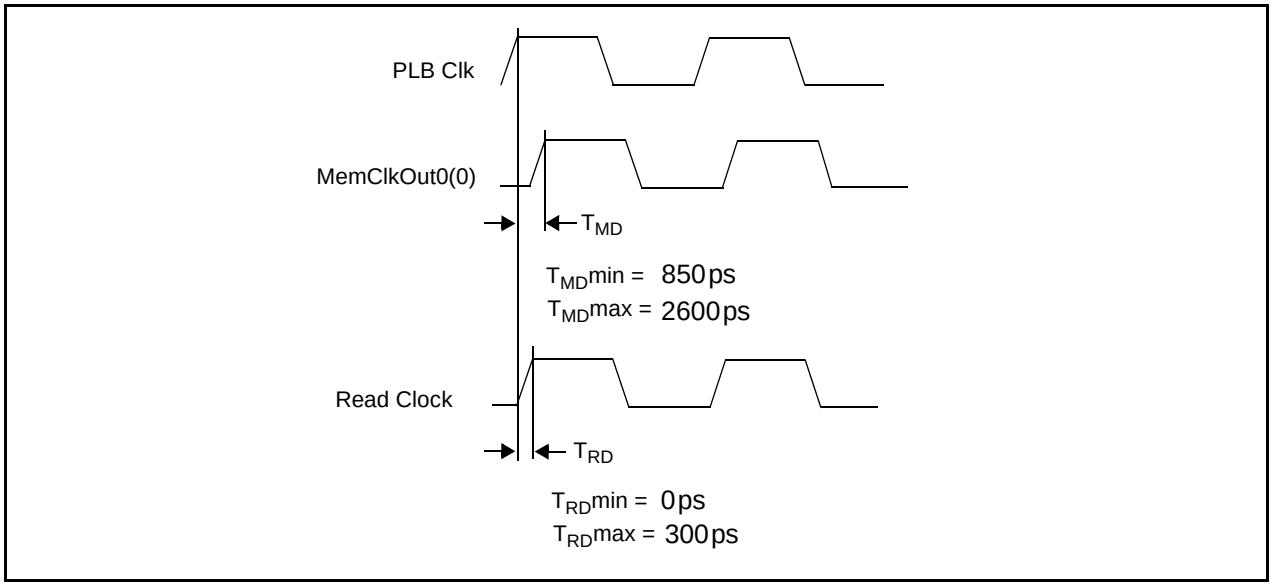
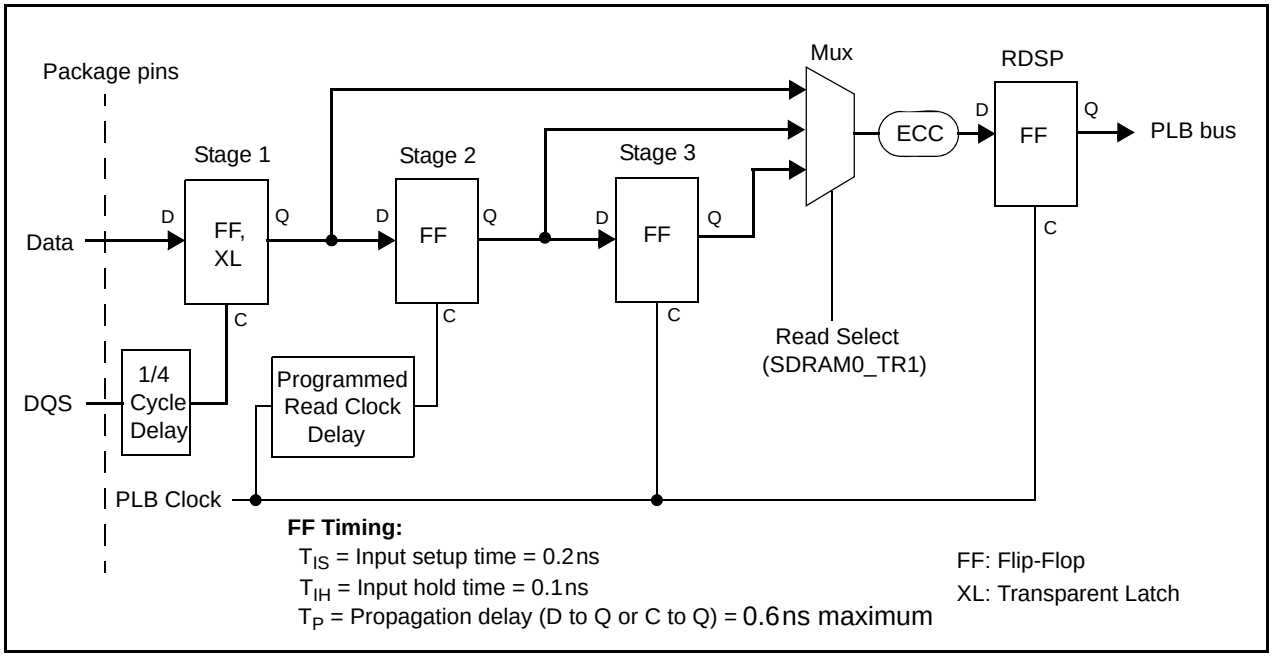
DDR SDRAM MemClkOut0 and Read Clock Delay



In operation, following the receipt of an address and read command from the PPC440GP, the SDRAM generates data and the DQS signals coincident with MemClkOut0. The data is latched into the PPC440GP using a DQS signal that is delayed 1/4 of a cycle. In order to accommodate timing variations introduced by the system designs using this chip, the three-stage data path shown below is used to eliminate metastability and allow data sampling to be adjusted for minimum latency. This adjustment requires programming the Read Clock delay and the selection of Stage 1, Stage 2, or Stage 3 data for sampling at RDSP.

DDR SDRAM Read Data Path



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I/O Timing—DDR SDRAM T_{SIN} and T_{DIN}

Notes:

1. T_{SIN} = Delay from DQS at package pin to C on Stage 1 FF.
2. T_{DIN} = Delay from data at package pin to D on Stage 1 FF.
3. The time values for T_{SIN} include 1/4 of a cycle at the indicated clock speed.

Clock Speed (MHz)	Signal Name	T_{SIN} (ns) minimum	T_{SIN} (ns) maximum	Signal Name	T_{DIN} (ns) minimum	T_{DIN} (ns) maximum
133	DQS0	2.775	3.775	MemData00:07	1.0	2.0
133	DQS1	2.775	3.775	MemData08:15	1.0	2.0
133	DQS2	2.775	3.775	MemData16:23	1.0	2.0
133	DQS3	2.775	3.775	MemData24:31	1.0	2.0
133	DQS4	2.775	3.775	MemData32:39	1.0	2.0
133	DQS5	2.775	3.775	MemData40:47	1.0	2.0
133	DQS6	2.775	3.775	MemData48:55	1.0	2.0
133	DQS7	2.775	3.775	MemData56:63	1.0	2.0
133	DQS8	2.775	3.775	ECC0:7	1.0	2.0

In the following examples, the data strobes (DQS) and the data are shown to be coincident. There is actually a slight skew as specified by the SDRAM specifications, and there can be additional skew due to loading and signal routing. It is recommended that the signal length for all of the eight DQS signals be matched.

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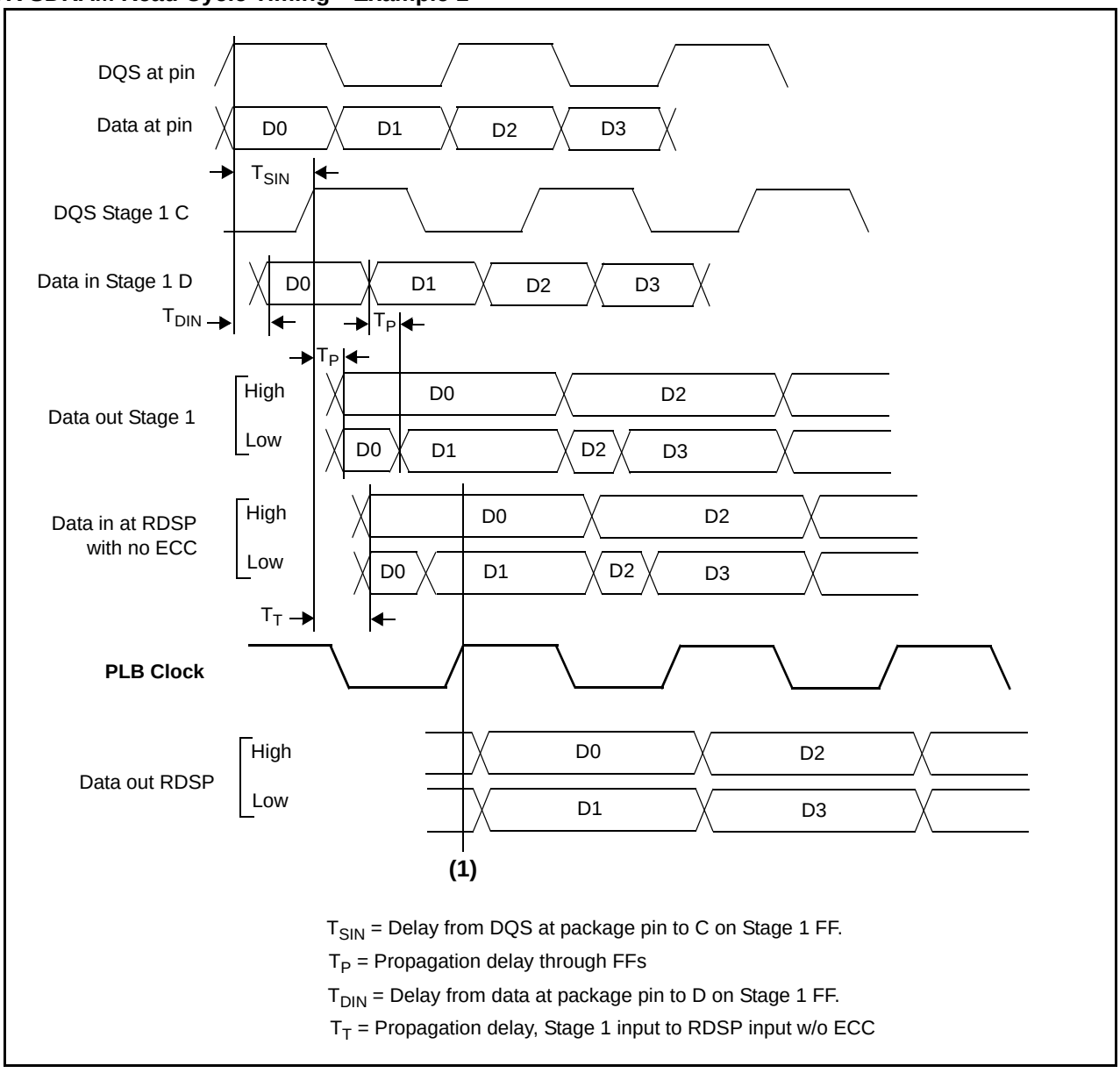
Example 1:

If the data-to-PLB clock timing is as shown in the example below, then the read clock is not delayed and the Stage 1 data is sampled at **(1)**. Except for small, low frequency memory systems with the memory located physically close to the PPC440GP, it is unlikely that Stage 1 data can be sampled. When the data comes later, it is necessary to sample Stage 2 or Stage 3 data. (see Examples 2 and 3). Another way to get the desired data-to-PLB timing to allow Stage 1 sampling is to buffer MemClkOut0 and skew it enough to guarantee the timing. In this example T_T = 1.5ns at worst case conditions.

DDR SDRAM Read Cycle Timing—Example 1



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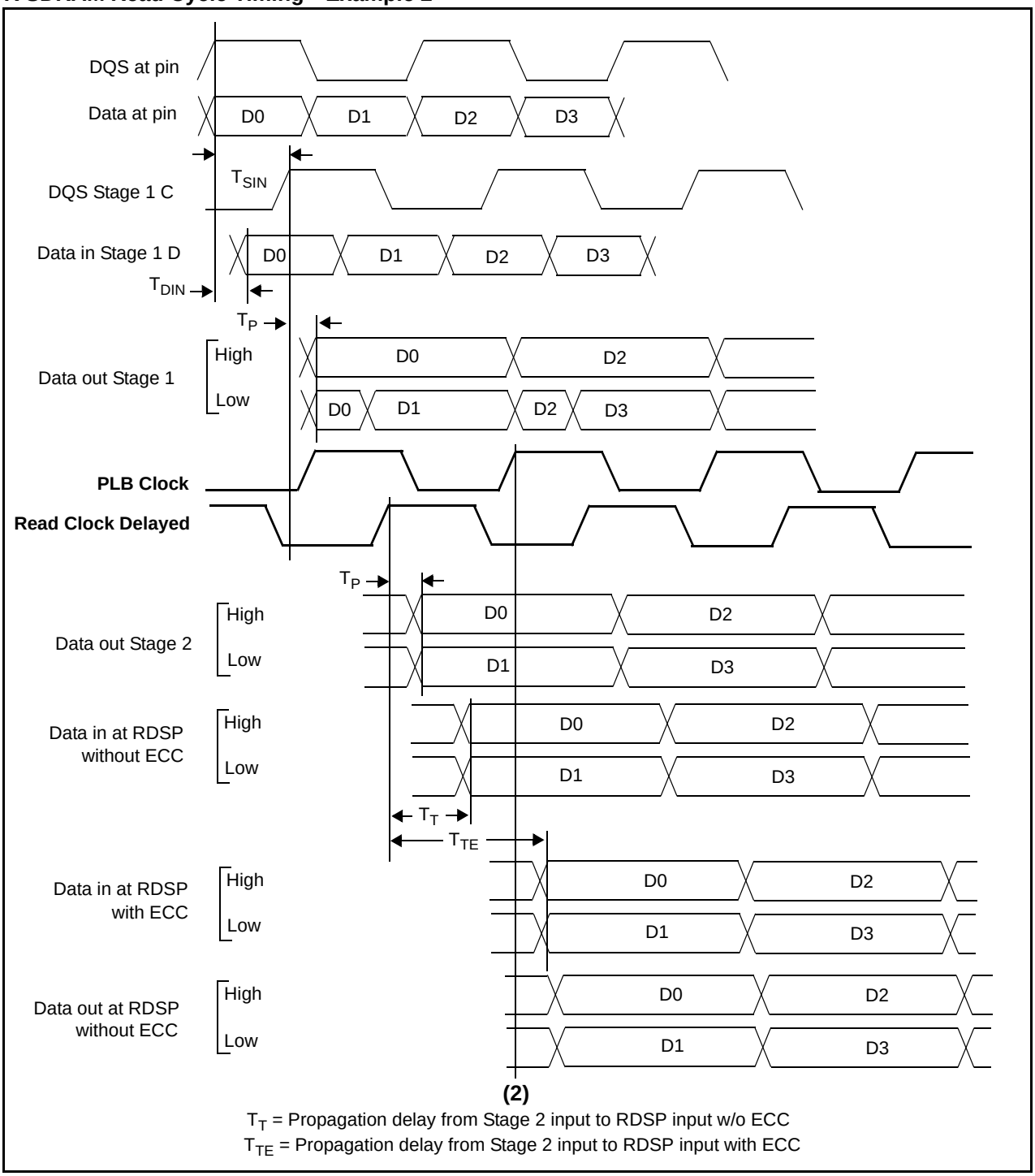
Example 2:

In this example Read Clock is delayed almost 1/2 cycle. Without ECC, Stage 2 data can be sampled at **(2)**. If ECC is enabled, Stage 3 data must be sampled (see Example 3). In this example, T_T = 1.5ns and T_{TE} = 4.3ns at worst case conditions.

DDR SDRAM Read Cycle Timing—Example 2



T_T = Propagation delay from Stage 2 input to RDSP input w/o ECC

T_{TE} = Propagation delay from Stage 2 input to RDSP input with ECC

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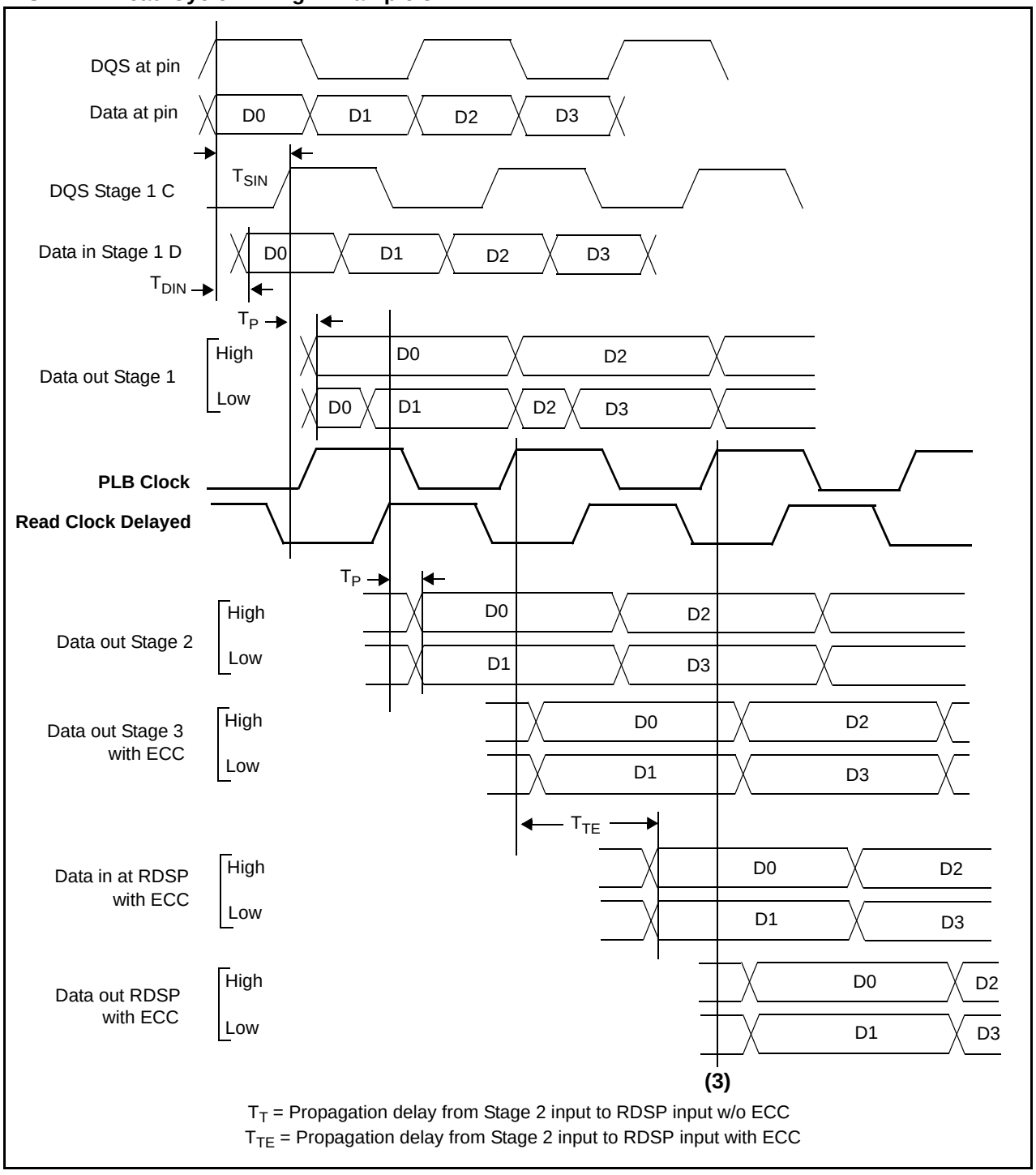
Example 3:

In this example, ECC is enabled. This requires that Stage 3 data be sampled at **(3)**. If ECC is disabled, the system will still work, but there will be more latency before the data is sampled into RDSP. Again, T_T = 1.5ns and T_{TE} = 4.3ns at worst case conditions.

DDR SDRAM Read Cycle Timing—Example 3



T_T = Propagation delay from Stage 2 input to RDSP input w/o ECC
T_{TE} = Propagation delay from Stage 2 input to RDSP input with ECC

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Initialization

The PPC440GP provides the option for setting initial parameters based on default values or by reading them from a slave PROM attached to the IIC0 bus (see “Serial EEPROM” below). Some of the default values can be altered by strapping on external pins (see “Strapping” below).

Strapping

While the SysReset input pin is low (system reset), the state of certain I/O pins is read to enable certain default initial conditions prior to PPC440GP start-up. The actual capture instant is the nearest reference clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. They are used for strap functions only during reset. Following reset they are used for normal functions.

The following table lists the strapping pins along with their functions and strapping options:

Strapping Pin Assignments

Function	Option	Ball Strapping
		V24 (UART0_DCD)
Bootstrap controller	Disabled	0
	Enabled	1
		V02 (UART0_DSR)
IIC0 slave address that will respond with boot data	0x54	0
	0x50	1

Serial EEPROM

During reset, initial conditions other than those obtained from the strapping pins can be read from a ROM device connected to the IIC0 port. At the de-assertion of reset, if the bootstrap controller is enabled, the PPC440GP sequentially reads 16 bytes from the ROM device on the IIC0 port and sets the SYS0and SYS1 registers accordingly. Otherwise, the default values set in the STRP0 and STRP1 registers are used for initialization.

The initialization settings and their default values are covered in detail in the *PowerPC 440GP Embedded Processor User’s Manual*.

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Revision Log

Date	Contents of Modification
08/07/2002	Add revision log.
08/30/2002	Change EMC0:1TxD0:1 and EMC0:1TxEn T_{OV} from 15 to 11 ns.
09/11/2002	Update for 466 and 500 MHz parts
10/22/2002	Add heat sink mounting information and additional part numbers for E temperature range.
11/20/2002	Update I/O timing data.
01/07/2003	Update PCI-X I/O voltage specification.
01/22/2003	Correct description of SysReset signal.
03/25/2003	Update DDR SDRAM timing.
06/16/2003	Change PCI setup specification from 2 to 3ns.
08/22/2003	Remove references to 2xPLB in DDR SDRAM timing section.
01/21/2004	Update DDR SDRAM timing section to be consistent 440GX presentation.
02/12/2004	Restore V_{DD}/OV_{DD} voltage sequence restriction.
05/12/2004	Add plastic package data and update part number list.
07/8/2004	Update supported part numbers.
11/01/2004	Add information on minimum SysClk and $\overline{\text{TRST}}$ duration during power-on reset. Remove power sequence restrictions note from Absolute Maximum Rating table. Restate power sequencing restrictions in Recommended DC Operating Conditions table. Convert to AMCC format.
12/09/2004	Remove references to Ethernet SMII mode.
06/07/2005	Add reduced-lead part numbers.
10/17/2005	Clarify DDR SDRAM interface diagram.
11/07/2005	Remove metal-layer specification from technology description. Add logo and number nomenclature to package drawing.
08/30/2007	Change the technical support telephone and fax number.
04/03/2008	Remove power supply power-up sequence requirements.

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