440GX

Data Sheet

Power PC 440GX Embedded Processor

Features

- PowerPC® 440 processor core operating up to 800 MHz with 32 KB I- and D-caches (with parity checking)
- On-chip 256 KB SRAM configurable as L2 Code store or Ethernet Packet store memory
- Selectable processor:bus clock ratios (Refer to the Clocking chapter in the *PPC440GX Embedded Processor User's Manual* for details)
- Double Data Rate (DDR) Synchronous DRAM (SDRAM) interface operating up to 166 MHz (200 MHz for 800 MHz Rev F parts)
- External Peripheral Bus (32 bits) for up to eight devices with external mastering
- DMA support for external peripherals, internal UART and memory
- PCI-X V1.0a interface (32 or 64 bits, up to 133 MHz) with support for conventional PCI V2.3
- Two Ethernet 10/100/1000 Mbps half- or full-duplex interfaces. Operational modes supported are SMII, GMII, RGMII, TBI and RTBI.
- TCP/IP Acceleration Hardware (TAH) provided for 10/100/1000 Mbps ports that performs checksum processing, TCP segmentation, and includes support for jumbo frames
- Programmable Interrupt Controller supports interrupts from a variety of sources.
- I2O Messaging unit for message transfer between the CPU and PCI-X
- Programmable General Purpose Timers (GPT)
- Two serial ports (16750 compatible UART)
- Two IIC interfaces
- General Purpose I/O (GPIO) interface available
- JTAG interface for board level testing
- Processor can boot from PCI memory
- Available in ceramic (RoHs and non-RoHS compliant versions) and plastic packages (RoHS and non-RoHS compliant versions).

Description

Designed specifically to address high-end embedded applications, the PowerPC 440GX (PPC440GX) provides a high-performance, low power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and lower power dissipation.

This chip contains a high-performance RISC processor core, DDR SDRAM controller, configurable 256 KB SRAM to be used as L2 cache or software-controlled on-chip memory, PCI-X bus interface, Gigabit Ethernet interfaces, TCP/IP acceleration hardware, I2O messaging unit, control for external ROM and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

Technology: CMOS Cu-11, 0.13 µm

Packages: 25 mm, 552-ball Ceramic Ball Grid Array (CBGA) or Plastic Ball Grid Array (PBGA) in standard or RoHS compliant versions

Power (estimated): Less than:
4 W typical @533 MHz
5 W typical @667 MHz
6 W typical @800 MHz (estimated)

Supply voltages required: 3.3 V, 2.5 V, 1.5 V

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Ordering and PVR Information

For information on the availability of the following parts, contact your local AMCC sales office.

Order Part Numbers

Product Name	Order Part Number (See Notes and Key drawing)	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
PPC440GX	PPC440GX-3CC533S	533MHz	25mm, 552 CBGA	C	0x51B21892	0x32054049
PPC440GX	PPC440GX-3CC667S	667MHz	25mm, 552 CBGA	C	0x51B21892	0x32054049
PPC440GX	PPC440GX-3CF400C	400MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3CF533C	533MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3CF533CZ	533MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3CF533E	533MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3CF667C	667MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3CF667CZ	667MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3CF800C	800MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3CF800CZ	800MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3FF533C	533MHz	25mm, 552 PBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3FF533E	533MHz	25mm, 552 PBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3FF667C	667MHz	25mm, 552 PBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3FF667E	667MHz	25mm, 552 PBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3RF400C	400MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3RF533C	533MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3RF533CZ	533MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3RF533E	533MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3RF667C	667MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3RF667CZ	667MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3RF800C	800MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3RF800CZ	800MHz	25mm, 552 CBGA	F	0x51B21894	0x52054049

Order Part Numbers (Continued)

Product Name	Order Part Number (See Notes and Key drawing)	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
PPC440GX	PPC440GX-3NF533C	533MHz	25mm, 552 PBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3NF533E	533MHz	25mm, 552 PBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3NF667C	667MHz	25mm, 552 PBGA	F	0x51B21894	0x52054049
PPC440GX	PPC440GX-3NF667E	667MHz	25mm, 552 PBGA	F	0x51B21894	0x52054049

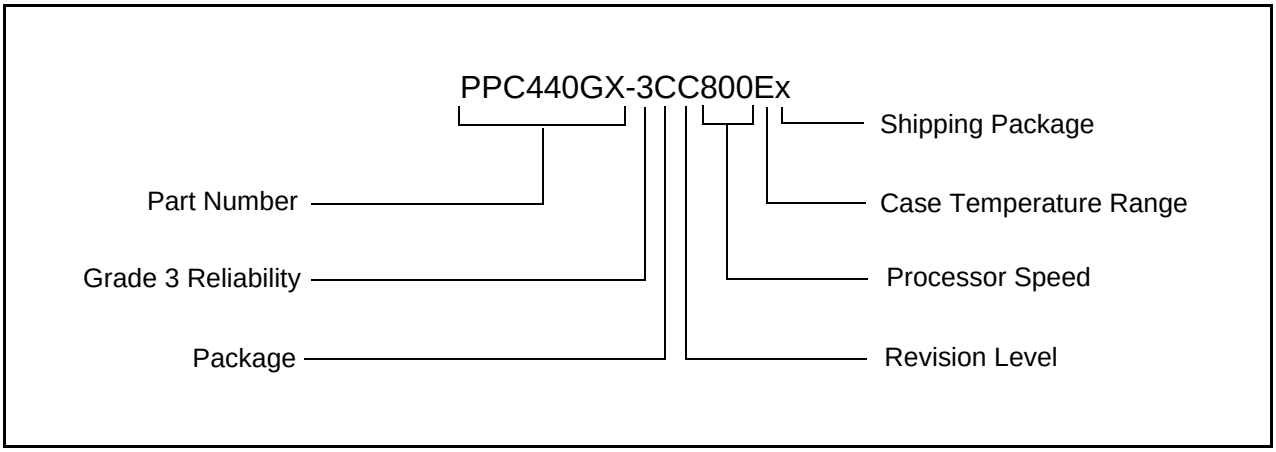
Notes:

1. Package code: C = leaded ceramic, F = plastic, R = reduced-lead ceramic (RoHS compliant), N = lead-free plastic (RoHS compliant).
2. Case Temperature Range code: C = -40 °C to +85 °C, E = -40 °C to +105 °C for C package and -40 °C to +100 °C for F package, S = -40 °C to +85 °C and no L2 cache support.
3. Z at the end of the Order Part Number indicates a tape-and-reel shipping package. Otherwise, the chips are shipped in a tray.
4. Revision code: C = rev 2.1, F = rev 3.1.

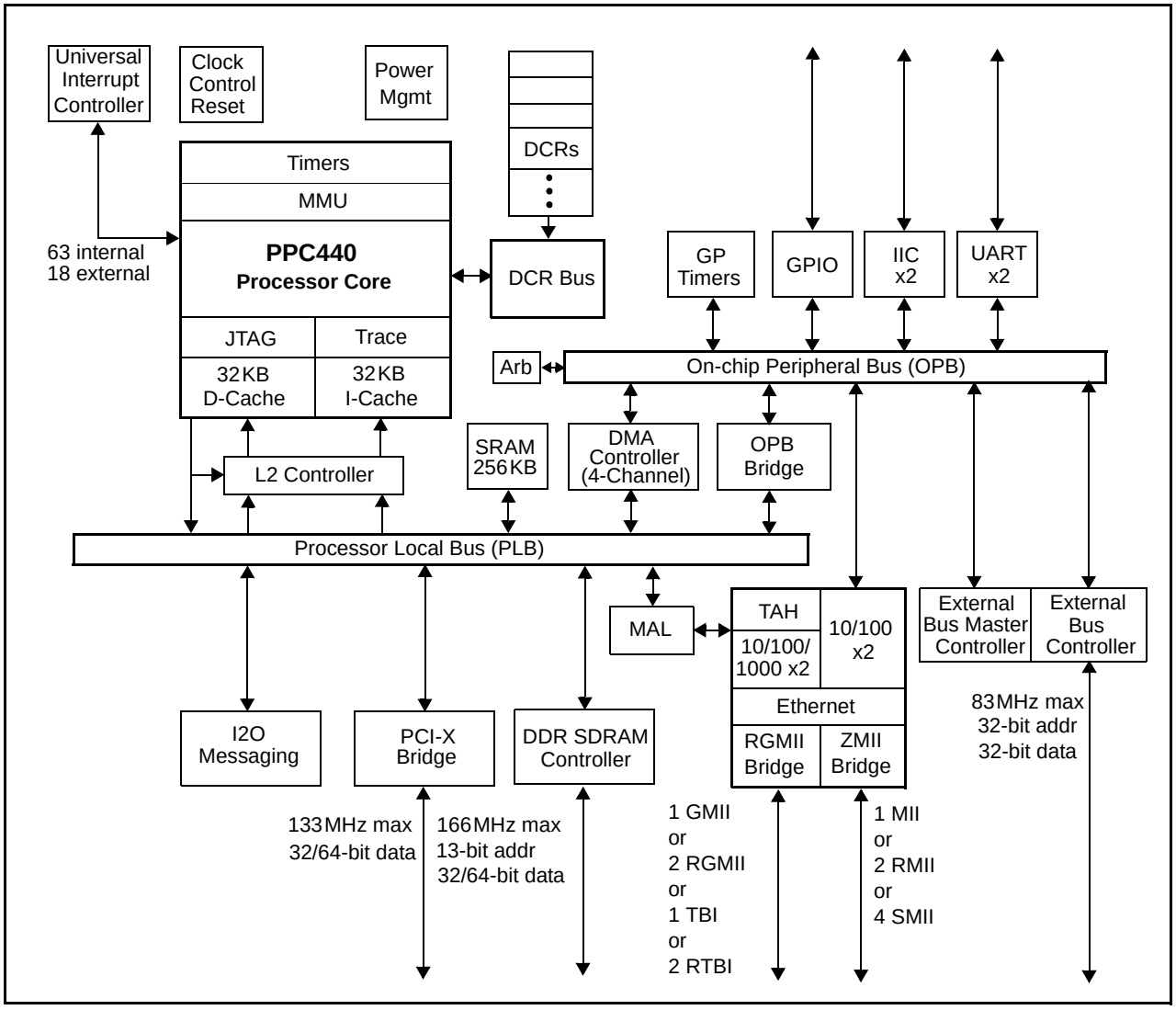
Each part number contains a revision code. This is the die mask revision number and is included in the part number for identification purposes only.

The PVR (Processor Version Register) and the JTAG ID register are software accessible (read-only) and contain information that uniquely identifies the part. Refer to the *PPC440GX User's Manual* for details on accessing these registers.

Order Part Number Key



PPC440GX Functional Block Diagram



The PPC440GX is designed using the IBM® Microelectronics Blue Logic™ methodology in which major functional blocks are integrated together to create an application-specific product (ASIC). This approach provides a consistent way to create complex ASICs using IBM CoreConnect Bus™ Architecture.

Note: IBM CoreConnect buses provide:

- 128-bit PLB interfaces up to 200MHz
- 32-bit OPB interfaces up to 83.33MHz, 333MB/s

Address Maps

The PPC440GX incorporates two address maps. The first is a fixed processor system memory address map. This address map defines the possible contents of various address regions which the processor can access. The second address map is for Device Configuration Registers (DCRs). The DCRs are accessed by software running on the PPC440GX processor through the use of **mtdcr** and **mfdcr** instructions.

System Memory Address Map (Sheet 1 of 2)

Function	Sub Function	Start Address	End Address	Size
Local Memory[1]	DDR SDRAM	0 0000 0000	0 7FFF FFFF	2GB
	SRAM	0 8000 0000	0 8000 3FFF	256KB
	Reserve	0 8000 4000	0 FFFE FFFF	
	IMU	0 FFFF 0000	0 FFFF FFFF	64KB
Internal Peripherals	EBC	1 0000 0000	1 3FFF FFFF	1GB
	Reserved	1 4000 0000	1 4000 01FF	
	UART0	1 4000 0200	1 4000 0207	8B
	Reserved	1 4000 0208	1 4000 02FF	
	UART1	1 4000 0300	1 4000 0307	8B
	Reserved	1 4000 0308	1 4000 03FF	
	IIC0	1 4000 0400	1 4000 041F	32B
	Reserved	1 4000 0420	1 4000 04FF	
	IIC1	1 4000 0500	1 4000 051F	32B
	Reserved	1 4000 0520	1 4000 05FF	
	OPB Arbiter	1 4000 0600	1 4000 063F	64B
	Reserved	1 4000 0640	1 4000 06FF	
	GPIO Controller	1 4000 0700	1 4000 077F	128B
	Ethernet PHY ZMII	1 4000 0780	1 4000 078F	16B
	Ethernet PHY GMII	1 4000 0790	1 4000 079F	16B
	Reserved	1 4000 07A0	1 4000 07FF	
	Ethernet 0 Controller	1 4000 0800	1 4000 08FF	256B
	Ethernet 1 Controller	1 4000 0900	1 4000 09FF	256B
	General Purpose Timer	1 4000 0A00	1 4000 0AFF	256B
	TCPIP Accelerator 0	1 4000 0B00	1 4000 0BFF	256B
	Ethernet 2 Controller	1 4000 0C00	1 4000 0CFF	256B
	TCPIP Accelerator 1	1 4000 0D00	1 4000 0DFF	256B
	Ethernet 3 Controller	1 4000 0E00	1 4000 0EFF	256B
	Reserved	1 4000 0F00	1 EFFF FFFF	
Expansion ROM[2]		1 F000 0000	1 FFDF FFFF	254MB
Boot ROM[2, 3]		1 FFE0 0000	1 FFFF FFFF	2MB

System Memory Address Map (Sheet 2 of 2)

Function	Sub Function	Start Address	End Address	Size
PCI-X	Reserved	2 0000 0000	2 07FF FFFF	
	PCI-X I/O	2 0800 0000	2 0BFF FFFF	64 MB
	Reserved	2 0C00 0000	2 0EBF FFFF	
	PCI-X External Configuration Registers	2 0EC0 0000	2 0EC0 0007	8 B
	Reserved	2 0EC0 0008	2 0EC7 FFFF	
	PCI-X Bridge Core Configuration Registers	2 0EC8 0000	2 0EC8 00FF	256 B
	Reserved	2 0EC8 0100	2 0EC8 00FF	
	PCI-X Special Cycle	2 0ED0 0000	2 0EDF FFFF	1 MB
	PCI-X Memory	2 0EE0 0000	F FFFF FFFF	55.76 GB

Notes:

1. DDR SDRAM and on-chip SRAM can be located anywhere in the Local Memory area of the memory map.
2. The Boot ROM and Expansion ROM areas of the memory map are intended for use by ROM or Flash-type devices. While locating volatile DDR SDRAM and SRAM in this region is supported, use of these regions for this purpose is not recommended.
3. When the optional boot from PCI-X memory is selected, the PCI-X Boot ROM address space begins at 2 FFFE 0000 (128 KB).

DCR Address Map 4KB of Device Configuration Registers

Function	Start Address	End Address	Size
Total DCR Address Space[1]	000	3FF	1KW (4KB)[1]
By function:			
Reserved	000	00B	12W
Clocking Power On Reset	00C	00D	2W
System DCRs	00E	00F	2W
Memory Controller	010	011	2W
External Bus Controller	012	013	2W
External Bus Master I/F	014	015	2W
PLB Performance Monitor	016	01F	10W
SRAM	020	02F	16W
L2 Controller	030	03F	16W
Reserved	040	07F	64W
PLB	080	08F	16W
PLB to OPB Bridge Out	090	09F	16W
Reserved	0A0	0A7	8W
OPB to PLB Bridge In	0A8	0AF	8W
Power Management	0B0	0B7	8W
Reserved	0B8	0BF	8W
Interrupt Controller 0	0C0	0CF	16W
Interrupt Controller 1	0D0	0DF	16W
Clock, Control, and Reset	0E0	0EF	16W
Reserved	0F0	0FF	16W
DMA Controller	100	13F	64W
Reserved	140	17F	64W
Ethernet MAL	180	1FF	128W
Base Interrupt Controller	200	20F	16W
Interrupt Controller 2	210	21F	16W
Reserved	220	3FF	480W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register. One kiloword (1024W) equals 4KB (4096 bytes).

PowerPC 440 Processor Core

The PowerPC 440 processor core is designed for high-end applications: RAID controllers, SAN, ISCSI, routers, switches, printers, set-top boxes, etc. It is the first processor core to implement the Book E PowerPC embedded architecture and the first to use the 128-bit version of IBM's on-chip CoreConnect Bus Architecture.

Features include:

- Up to 800 MHz operation
- PowerPC Book E architecture
- 32 KB I-cache, 32 KB D-cache
  - UTLB Word Wide parity on data and tag address parity with exception force
- Three logical regions in D-cache: locked, transient, normal
- D-cache full line flush capability
- 41-bit virtual address, 36-bit (64 GB) physical address
- Superscalar, out-of-order execution
- 7-stage pipeline
- 3 execution pipelines
- Dynamic branch prediction
- Memory management unit
  - 64-entry, full associative, unified TLB with parity
  - Separate instruction and data micro-TLBs
  - Storage attributes for write-through, cache-inhibited, guarded, and big or little endian
- Debug facilities
  - Multiple instruction and data range breakpoints
  - Data value compare
  - Single step, branch, and trap events
  - Non-invasive real-time trace interface
- 24 DSP instructions
  - Single-cycle multiply and multiply-accumulate
  - 32 x 32 integer multiply
  - 16 x 16 -> 32-bit MAC

Internal Buses

The PowerPC 440GX features three IBM standard on-chip buses: the Processor Local Bus (PLB), the On-Chip Peripheral Bus (OPB), and the Device Control Register Bus (DCR). The high performance, high bandwidth cores such as the PowerPC 440 processor core, the DDR SDRAM memory controller, and the PCI-X bridge connect to the PLB. The OPB hosts lower data rate peripherals. The daisy-chained DCR provides a lower bandwidth path for passing status and control information between the processor core and the other on-chip cores.

Features include:

- PLB
  - 128-bit implementation of the PLB architecture
  - Separate and simultaneous read and write data paths
  - 64-bit address
  - Simultaneous control, address, and data phases
  - Four levels of pipelining
  - Byte enable capability supporting unaligned transfers
  - 32- and 64-byte burst transfers
  - 166 MHz, maximum 5.2 GB/s (simultaneous read and write)(200 MHz for 800 MHz Rev F parts)
  - Processor:bus clock ratios of N:1 and N:2

- OPB
  - Dynamic bus sizing 32-, 16-, and 8-bit data path
  - 36-bit address
  - 83.33MHz, maximum 333MB/s
- DCR
  - 32-bit data path
  - 10 bit address

On-Chip SRAM

Features include:

- Four banks of 64KB each for a total of 256KB
- Configurable as either Code (L2) cache or software-controlled on-chip memory, or SRAM
- Memory cycles supported:
  - Single beat read and write, 1 to 16 bytes
  - 32- and 64-byte burst transfers
  - Guarded memory accesses
- Sustainable 2.6GB/s peak bandwidth at 166MHz
- Use as an L2 cache improves processor performance and reduces the PLB load
  - Cache coherency maintained by a hardware snoop mechanism or software
  - Data Array and Tag Array parity
  - Unified data and instruction cache
  - 4-way set associative
  - 36-bit addressing
  - Full LRU replacement algorithm
  - Write through, look aside
- Use as Ethernet packet store allows Ethernet packets to be held for processing by the TAH unit

PCI-X Interface

The PCI-X interface allows connection of PCI and PCI-X devices to the PowerPC processor and local memory. This interface is designed to Version 1.0a of the PCI-X Specification and supports 32- and 64-bit PCI-X buses. PCI 32/64-bit conventional mode, compatible with PCI Version 2.3, is also supported.

Reference Specifications:

- PowerPC CoreConnect Bus (PLB) Specification Version 3.1
- PCI Specification Version 2.3
- PCI Bus Power Management Interface Specification Version 1.1

Features include:

- PCI-X 1.0a
  - Split transactions
  - Frequency to 133MHz
  - 32- and 64-bit bus
- PCI 2.3 backward compatibility
  - Frequency to 66MHz
  - 32- and 64-bit bus
- Can be the PCI Host Bus Bridge or an Adapter Device's PCI interface
- Internal PCI arbitration function, supporting up to six external devices, that can be disabled for use with an external arbiter
- Support for Message Signaled Interrupts

- Simple message passing capability
- Asynchronous to the PLB
- PCI Power Management 1.1
- PCI register set addressable both from on-chip processor and PCI device sides
- Ability to boot from PCI-X bus memory
- Error tracking/status
- Supports initiation of transfer to the following address spaces:
  - Single beat I/O reads and writes
  - Single beat and burst memory reads and writes
  - Single beat configuration reads and writes (type 0 and type 1)
  - Single beat special cycles

DDR SDRAM Memory Controller

The Double Data Rate (DDR) SDRAM memory controller supports industry standard 184-pin DIMMs, SO-DIMMs, and other discrete devices. Up to four 512MB logical banks are supported in limited configurations. Global memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:

- Registered and non-registered industry standard DIMMs
- 64-bit memory interface with optional 8-bit ECC (SEC/DED)
- Sustainable 2.6GB/s peak bandwidth at 166MHz (200MHz for 800MHz Rev F parts)
- SSTL_2 logic
- 1 to 4 chip selects
- CAS latencies of 2, 2.5 and 3 supported
- DDR200/266/333 support
- Page mode accesses (up to eight open pages) with configurable paging policy
- Programmable address mapping and timing
- Hardware and software initiated self-refresh
- Power management (self-refresh, suspend, sleep)

External Peripheral Bus Controller (EBC)

Features include:

- Up to eight ROM, EPROM, SRAM, Flash memory, and slave peripheral I/O banks supported
- Up to 83.33MHz operation (333MB/s)
- Burst and non-burst devices
- 8-, 16-, 32-bit byte-addressable data bus
- 32-bit address, 4GB address space
- Peripheral Device pacing with external “Ready”
- Latch data on Ready, synchronous or asynchronous
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping
- External DMA Slave Support

- External master interface
  - Write posting from external master
  - Read prefetching on PLB for external master reads
  - Bursting capable from external master
  - Allows external master access to all non-EBC PLB slaves
  - External master can control EBC slaves for own access and control

Ethernet Controller Interface

Ethernet support provided by the PPC440GX interfaces to the physical layer, but the PHY is not included on the chip.

Features include:

- One to four 10/100 interfaces running in full- and half-duplex modes
  - One full Media Independent Interface (MII) with 4-bit parallel data transfer
  - Two Reduced Media Independent Interfaces (RMII) with 2-bit parallel data transfer
  - Four Serial Media Independent Interfaces (SMII)
- One or two GMII interfaces running in full- and half-duplex modes at 10Mb/s or 100Mb/s or 1000Mb/s
  - One full Gigabit Media Independent Interface (GMII) with 8-bit parallel data transfer
  - Two Reduced Gigabit Media Independent Interfaces (RGMII) with 4-bit parallel data transfer
- One or two TBI interfaces running in full- and half-duplex modes at 10Mb/s or 100Mb/s or 1000Mb/s
  - One full Ten Bit Interface (TBI) with 10-bit parallel data transfer
  - Two Reduced Ten Bit Interfaces (RTBI) with 4-bit parallel data transfer
- Jumbo frame support (9016 byte)
  - Support for Ethernet II formatted frames (RFC894)
  - Support for IEEE formatted frames (RFC1042)
  - Handles VLAN-tagged frames

TCP/IP Acceleration Hardware (TAH)

Features include:

- Offloads Gigabit Ethernet protocol processing from the CPU
- Checksum verification for TCP/UDP/IP headers in the receive path
- Checksum generation for TCP/UDP/IP headers in the transmit path
- TCP segmentation support in the transmit path

DMA Controller

Features include:

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 64-bit addressing
- 128 byte FIFO buffer
- Address increment or decrement
- Supports internal and external peripherals
- Support for memory mapped peripherals

- Support for peripherals running on slower frequency buses

Serial Port

Features include:

- One 8-pin UART and one 4-pin UART interface provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with 16750 register set
- Complete status reporting capability
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

IIC Bus Interface

Features include:

- Two IIC interfaces provided
- Support for Philips® Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocols
- Programmable error recovery

General Purpose Timers (GPT)

Provides a separate time base counter and additional system timers in addition to those defined in the processor core.

- 32-bit Time Base Counter driven by the OPB bus clock
- Seven 32-bit compare timers

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses.
- The 32 GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose.
- Each GPIO output is separately programmable to emulate an open drain driver (that is, drives to zero, tri-stated if output bit is 1).

Universal Interrupt Controller (UIC)

Four Universal Interrupt Controllers (UIC) are available. They provide control, status, and communications necessary between the external and internal sources of interrupts and the on-chip PowerPC processor.

Note: Processor specific interrupts (for example, page faults) do not use UIC resources.

Features include:

- 18 external interrupts
- 63 internal interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to the on-chip processor core
- Programmable interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

PLB Performance Monitor

The PLB Performance Monitor (PPM) provides hardware for counting certain events associated with PLB transactions. The contents of the counters can be read by software for analysis and enhancement of PLB performance, or software debug. The data includes identification and duration of the events.

I2O Messaging Unit (IMU)

The IMU interfaces to the PLB as a master or slave and allows messages to be transferred between two PLB masters (for example, the 440 CPU and PCI-X).

Features include:

- Three messaging methods
  - 4 Message registers—2 inbound, 2 outbound
  - 2 Doorbell registers—1 inbound, 1 outbound
  - 4 Circular queues—2 inbound, 2 outbound
- Up to 7 different interrupt outputs generated
- Support for interrupt masking

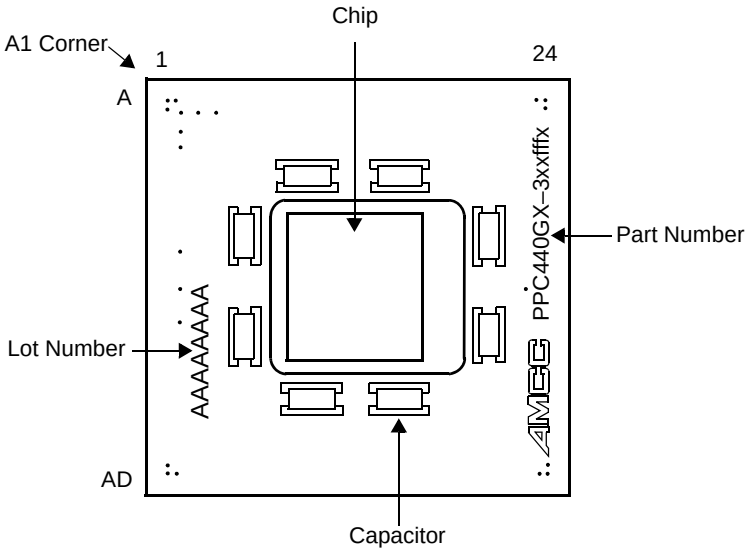
JTAG

Features include:

- IEEE 1149.1 Test Access Port
- IBM RISCWatch Debugger support
- JTAG Boundary Scan Description Language (BSDL)

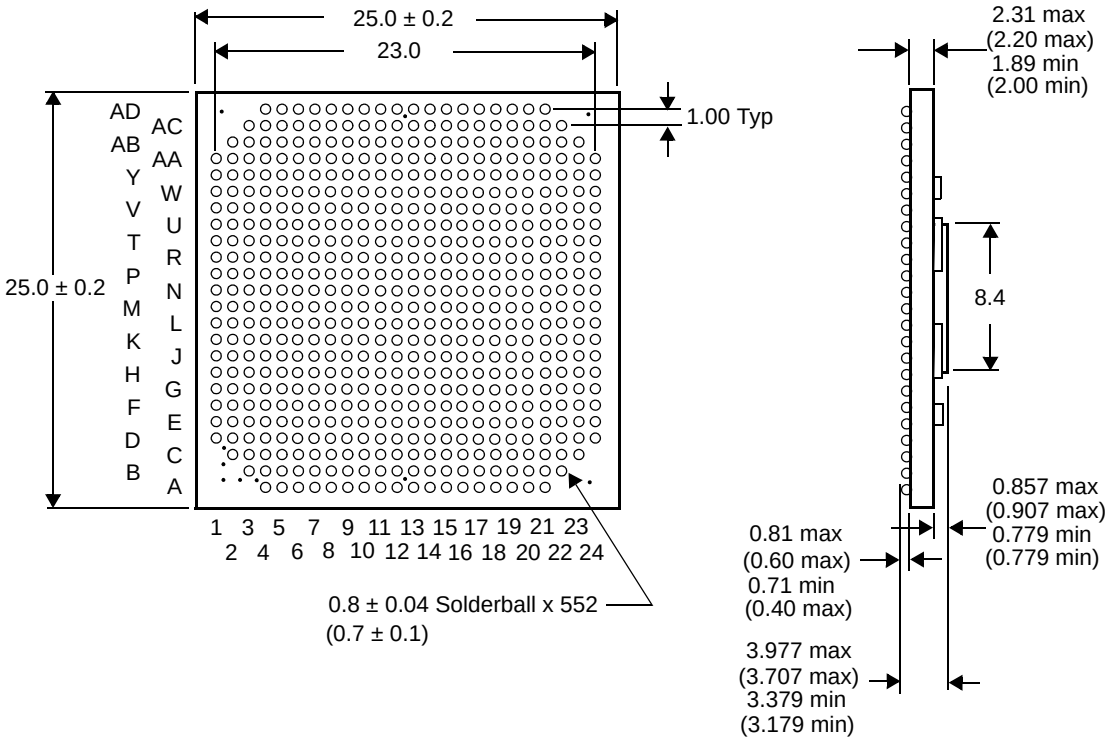
25mm, 552-Ball Ceramic (CBGA) Package

Top View



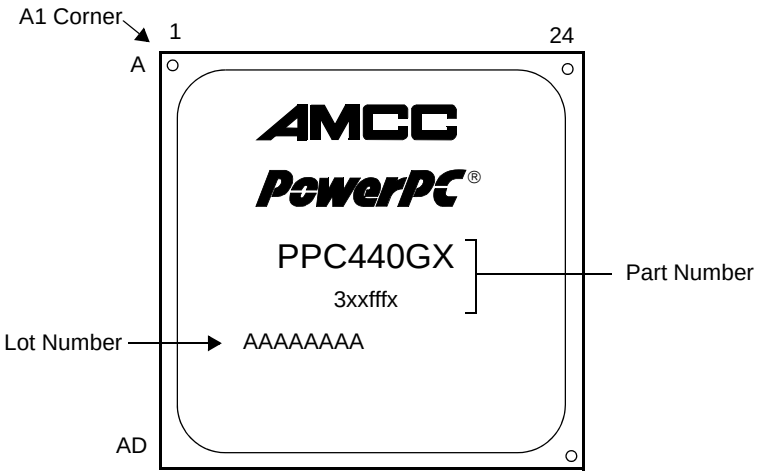
Notes: 1. All dimensions are in mm.
2. RoHS compliant reduced-lead package available.
3. Reduced-lead package dimensions are in parentheses (dimension).

Bottom View



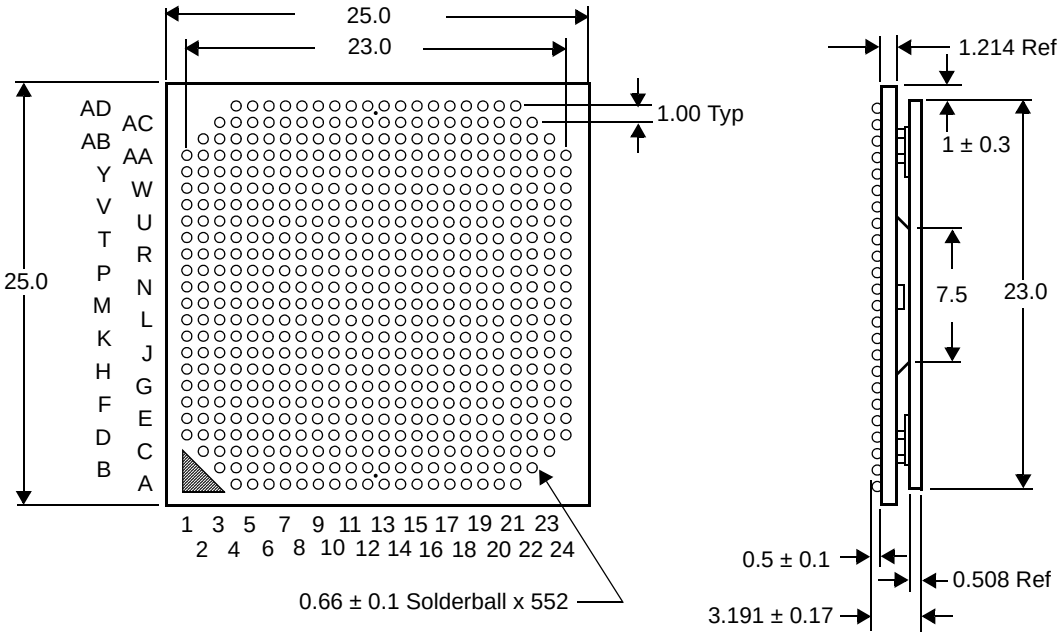
25mm, 552-Ball Plastic (FC-PBGA) Package

Top View



Notes: 1. All dimensions are in mm.
2. Available in lead-free, RoHS compliant version.

Bottom View



Signal Lists

The following table lists all the external signals in alphabetical order and shows the ball (pin) number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal in brackets. Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in "Signal Functional Description" on page 50 where the signals in the indicated interface group begin. In cases where signals in the same interface group (for example, Ethernet) have different names to distinguish variations in the mode of operation, the names are separated by a comma with the primary name appearing first. These signals are listed only once, and appear alphabetically by the primary name.

Signals Listed Alphabetically (Sheet 1 of 24)

Signal Name	Ball	Interface Group	Page
AGND	J01	Power—Analog ground	57
AGND	J24		
AGND	AA11		
AMV_{DD}	AB11	Power—MemClkOut PLL analog voltage	57
APV_{DD}	G01	Power—PCI-X PLL analog voltage	57
ASV_{DD}	G24	Power—SysClk PLL analog voltage	57
BA0	AA16	DDR SDRAM	51
BA1	AD09		
$\overline{\text{BankSel0}}$	AB15	DDR SDRAM	51
$\overline{\text{BankSel1}}$	W14		
$\overline{\text{BankSel2}}$	AD11		
$\overline{\text{BankSel3}}$	AD05		
[$\overline{\text{BE0}}$]PCIXC0	F14	PCI-X	50
[$\overline{\text{BE1}}$]PCIXC1	E16		
[$\overline{\text{BE2}}$]PCIXC2	C19		
[$\overline{\text{BE3}}$]PCIXC3	F20		
[$\overline{\text{BE4}}$]PCIXC4	C08		
[$\overline{\text{BE5}}$]PCIXC5	C03		
[$\overline{\text{BE6}}$]PCIXC6	G09		
[$\overline{\text{BE7}}$]PCIXC7	F09		
BusReq[TrcTS1]	AA24	External Master Peripheral	54
$\overline{\text{CAS}}$	AB05	DDR SDRAM	51
ClkEn0	AD17	DDR SDRAM	51
ClkEn1	AB10		
ClkEn2	Y09		
ClkEn3	W09		

Signals Listed Alphabetically (Sheet 2 of 24)

Signal Name	Ball	Interface Group	Page
DM0	T16	DDR SDRAM	51
DM1	AA18		
DM2	AB14		
DM3	P13		
DM4	AA09		
DM5	AA07		
DM6	Y03		
DM7	V03		
DM8	AC05		
DMAAck0	N05	External Slave Peripheral	53
DMAAck1	P07		
DMAAck2[GMCRxD0, GMC0RxD0, TBIRxD0, RTBI0RxD0]	P06		
DMAAck3[GMCRxD1, GMC0RxD1, TBIRxD1, RTBI0RxD1]	P11		
DMAReq0	R03	External Slave Peripheral	53
DMAReq1	M11		
DMAReq2[GMCRxDV, GMC0RxCtl, TBIRxD8, RTBI0RxD4]	N11		
DMAReq3[GMCTxEn, GMC0TxCtl, TBITxD8, RTBI0TxD4]	P01		
DQS0	AC20	DDR SDRAM	51
DQS1	AC16		
DQS2	AC14		
DQS3	AB13		
DQS4	AC11		
DQS5	AC09		
DQS6	Y04		
DQS7	T01		
DQS8	AA05		
DrvrInh2	A05	System	56

Signals Listed Alphabetically (Sheet 3 of 24)

Signal Name	Ball	Interface Group	Page
ECC0	AB07	DDR SDRAM	51
ECC1	AB06		
ECC2	AD06		
ECC3	W07		
ECC4	U09		
ECC5	AC03		
ECC6	AB04		
ECC7	AD04		
EMCCD, EMC1RxErr, GMCGTxClk, GMC0TxClk, TBITxClk, RTBI0TxClk	J07	Ethernet	51
EMCCrS, EMC0CrSDV, GMCTxD7, GMC1TxD3, TBITxD7, RTBI1TxD3	K07	Ethernet	51
EMCMDClk	J08	Ethernet	51
EMCMDIO	L05	Ethernet	51
EMCRxClk, GMCTxD5, GMC1TxD1, TBITxD5, RTBI1TxD1	J02	Ethernet	51
EMCRxD0, EMC0RxD0, EMC0RxD	G03	Ethernet	51
EMCRxD1, EMC0RxD1, EMC1RxD	E01		
EMCRxD2, EMC1RxD0, EMC2RxD, GMCTxD0, GMC0TxD0, TBITxD0, RTBI0TxD0	A07		
EMCRxD3, EMC1RxD1, EMC3RxD GMCTxD1, GMC0TxD1, TBITxD1, RTBI0TxD1	H09		
EMCRxDV, EMC1CrSDV, GMCTxD4, GMC1TxD0, TBITxD4, RTBI1TxD0	K01	Ethernet	51
EMCRxErr, EMC0RxErr, GMCTxD6, GMC1TxD2, TBITxD6, RTBI1TxD2	K03	Ethernet	51
EMCTxClk, EMCRefClk	J06	Ethernet	51
EMCTxD0, EMC0TxD0, EMC0TxD	L09	Ethernet	51
EMCTxD1, EMC0TxD1, EMC1TxD	K05		
EMCTxD2, EMC1TxD0, EMC2TxD, GMCTxD2, GMC0TxD2, TBITxD2, RTBI0TxD2	J04		
EMCTxD3, EMC1TxD1, EMC3TxD, GMCTxD3, GMC0TxD3, TBITxD3, RTBI0TxD3	J03		
EMCTxEn, EMC0TxEn, EMCSync	L06	Ethernet	51
EMCTxErr, EMC1TxEn, GMCRxClk, GMC0RxClk, TBIRxClk0, RTBI0RxClk	C05	Ethernet	51

Signals Listed Alphabetically (Sheet 4 of 24)

Signal Name	Ball	Interface Group	Page
EOT0/TC0	R16	External Slave Peripheral	53
EOT1/TC1	P15		
EOT2/TC2[GMCRxD2, GMC0RxD2, TBIRxD2, RTBI0RxD2]	P16		
EOT3/TC3[GMCRxD3, GMC0RxD3, TBIRxD3, RTBI0RxD3]	M16		
$\overline{\text{ExtAck}}$[TrcTS2]	AA22	External Master Peripheral	54
$\overline{\text{ExtReq}}$[TrcTS3]	AB23	External Master Peripheral	54
$\overline{\text{ExtReset}}$	T17	External Master Peripheral	54
[GMCCD, GMC1RxClk, RTBI1RxClk]TrcTS1[GPIO27]	P03	Ethernet	51
[GMCCrS, GMC1TxClk, RTBI1TxClk]TrcTS6	R01	Ethernet	51
GMCRefClk	L01	Ethernet	51
[GMCRxD0, GMC0RxD0, TBIRxD0, RTBI0RxD0]DMAAck2	P06	Ethernet	51
[GMCRxD1, GMC0RxD1, TBIRxD1, RTBI0RxD1]DMAAck3	P11		
[GMCRxD2, GMC0RxD2, TBIRxD2, RTBI0RxD2]EOT2/TC2	P16		
[GMCRxD3, GMC0RxD3, TBIRxD3, RTBI0RxD3]EOT3/TC3	M16		
[GMCRxD4, GMC1RxD0, TBIRxD4, RTBI1RxD0][GPIO28]TrcTS2	R07		
[GMCRxD5, GMC1RxD1, TBIRxD5, RTBI1RxD1][GPIO29]TrcTS3	P09		
[GMCRxD6, GMC1RxD2, TBIRxD6, RTBI1RxD2][GPIO30]TrcTS4	R09		
[GMCRxD7, GMC1RxD3, TBIRxD7, RTBI1RxD3][GPIO31]TrcTS5	T06		
[GMCRxDV, GMC0RxCtl, TBIRxD8, RTBI0RxD4]DMAReq2	N11	Ethernet	51
GMCRxEr, GMC1RxCtl, TBIRxD9, RTBI1RxD4	P04	Ethernet	51
GMCTxEr, GMC1TxCtl, TBITxD9, RTBI1TxD4	L07	Ethernet **Note:** Used as initialization strapping input.	51
[GMCTxEn, GMC0TxCtl, TBITxD8, RTBI0TxD4]DMAReq3	P01	Ethernet	51
[GMCTxClk, TBIRxClk1]GPIO11	P14	Ethernet	51

Signals Listed Alphabetically (Sheet 5 of 24)

Signal Name	Ball	Interface Group	Page
GND	B06	Power	57
GND	B10		
GND	B13		
GND	B17		
GND	B21		
GND	D04		
GND	D08		
GND	D12		
GND	D15		
GND	D19		
GND	D23		
GND	F02		
GND	F06		
GND	F10		
GND	F13		
GND	F17		
GND	F21		
GND	H04		
GND	H08		
GND	H12		
GND	H15		
GND	H19		
GND	H23		
GND	K02		
GND	K06		
GND	K10		
GND	K13		
GND	K17		
GND	K21		
GND	M04		

Signals Listed Alphabetically (Sheet 6 of 24)

Signal Name	Ball	Interface Group	Page
GND	M08		
GND	M12		
GND	M15		
GND	M19		
GND	M23		
GND	N02		
GND	N06		
GND	N10		
GND	N13		
GND	N17		
GND	N21		
GND	R04		
GND	R08		
GND	R12		
GND	R15	Power	57
GND	R19		
GND	R23		
GND	U02		
GND	U06		
GND	U10		
GND	U13		
GND	U17		
GND	U21		
GND	W04		
GND	W08		
GND	W12		
GND	W15		
GND	W19		
GND	W23		

Signals Listed Alphabetically (Sheet 7 of 24)

Signal Name	Ball	Interface Group	Page
GND	AA02	Power	57
GND	AA06		
GND	AA10		
GND	AA13		
GND	AA17		
GND	AA21		
GND	AC04		
GND	AC08		
GND	AC12		
GND	AC15		
GND	AC19		

Signals Listed Alphabetically (Sheet 8 of 24)

Signal Name	Ball	Interface Group	Page
[GPIO00]IRQ00	N18	System	56
[GPIO01]IRQ01	L20		
[GPIO02]IRQ02	P20		
[GPIO03]IRQ03	L18		
[GPIO04]IRQ04	N14		
[GPIO05]IRQ05	M20		
[GPIO06]IRQ06	M14		
[GPIO07]IRQ07	P18		
[GPIO08]IRQ08	N20		
[GPIO09]IRQ09	P22		
[GPIO10]IRQ10	V18		
GPIO11[GMCTxClk, TBIRxClk1]	P14		
[GPIO12]UART1_Rx	C18		
[GPIO13]UART1_Tx	J16		
[GPIO14]$\overline{\text{UART1\_DSR/CTS}}$	G06		
[GPIO15]$\overline{\text{UART1\_RTS/DTR}}$	E05		
[GPIO16]IIC1SClk	H11		
[GPIO17]IIC1SDA	H14		
[GPIO18]TrcBS0[IRQ13]	N16		
[GPIO19]TrcBS1[IRQ14]	P17		
[GPIO20]TrcBS2[IRQ15]	T20		
[GPIO21]TrcES0[IRQ16]	T21		
[GPIO22]TrcES1[IRQ17]	P23		
[GPIO23]TrcES2	N09		
[GPIO24]TrcES3	P08		
[GPIO25]TrcES4	T05		
[GPIO26]TrcTS0	T04		
[GPIO27]TrcTS1[GMCCD, GMC1RxClk, RTBI1RxClk]	P03		
[GPIO28]TrcTS2[GMCRxD4, GMC1RxD0, TBIRxD4, RTBI1RxD0]	R07		
[GPIO29]TrcTS3[GMCRxD5, GMC1RxD1, TBIRxD5, RTBI1RxD1]	P09		
[GPIO30]TrcTS4[GMCRxD6, GMC1RxD2, TBIRxD6, RTBI1RxD2]	R09		
[GPIO31]TrcTS5[GMCRxD7, GMC1RxD3, TBIRxD7, RTBI1RxD3]	T06		

Signals Listed Alphabetically (Sheet 9 of 24)

Signal Name	Ball	Interface Group	Page
$\overline{\text{Halt}}$	V05	System	56
HoldAck[TrcTS4]	Y21	External Master Peripheral	54
HoldReq[TrcTS5]	Y23	External Master Peripheral	54
IIC0SClk	G11	IIC Peripheral	55
IIC0SDA	G13	IIC Peripheral	55
IIC1SClk[GPIO16]	H11	IIC Peripheral	55
IIC1SDA[GPIO17]	H14	IIC Peripheral	55
IRQ00[GPIO00]	N18	Interrupts	55
IRQ01[GPIO01]	L20		
IRQ02[GPIO02]	P20		
IRQ03[GPIO03]	L18		
IRQ04[GPIO04]	N14		
IRQ05[GPIO05]	M20		
IRQ06[GPIO06]	M14		
IRQ07[GPIO07]	P18		
IRQ08[GPIO08]	N20		
IRQ09[GPIO09]	P22		
IRQ10[GPIO10]	V18		
[IRQ11]$\overline{\text{PCIReq1}}$	E21		
[IRQ12]$\overline{\text{PCIGnt1}}$	C22		
[IRQ13][GPIO18]TrcBS0	N16		
[IRQ14][GPIO19]TrcBS1	P17		
[IRQ15][GPIO20]TrcBS2	T20		
[IRQ16][GPIO21]TrcES0	T21		
[IRQ17][GPIO22]TrcES1	P23		

Signals Listed Alphabetically (Sheet 10 of 24)

Signal Name	Ball	Interface Group	Page
MemAddr00	Y19	DDR SDRAM	51
MemAddr01	AD20		
MemAddr02	Y20		
MemAddr03	AB20		
MemAddr04	AD18		
MemAddr05	AD16		
MemAddr06	AB18		
MemAddr07	Y14		
MemAddr08	V13		
MemAddr09	V11		
MemAddr10	W16		
MemAddr11	Y11		
MemAddr12	V10		
MemClkOut0	V09	DDR SDRAM	51
$\overline{\text{MemClkOut0}}$	V08		

Signals Listed Alphabetically (Sheet 11 of 24)

Signal Name	Ball	Interface Group	Page
MemData00	AD21	DDR SDRAM	51
MemData01	AB21		
MemData02	AC22		
MemData03	AA20		
MemData04	U16		
MemData05	V17		
MemData06	AD19		
MemData07	AB19		
MemData08	W18		
MemData09	V16		
MemData10	Y17		
MemData11	AB16		
MemData12	AC18		
MemData13	Y18		
MemData14	R14		
MemData15	AB17		
MemData16	AA14		
MemData17	AD15		
MemData18	T15		
MemData19	V15		
MemData20	Y16		
MemData21	U14		
MemData22	T13		
MemData23	Y15		
MemData24	AD13		
MemData25	AD14		
MemData26	V14		
MemData27	Y13		
MemData28	P12		
MemData29	AB12		
MemData30	Y12		
MemData31	V12		

Signals Listed Alphabetically (Sheet 12 of 24)

Signal Name	Ball	Interface Group	Page
MemData32	W11	DDR SDRAM	51
MemData33	AD12		
MemData34	Y10		
MemData35	T12		
MemData36	U11		
MemData37	T11		
MemData38	T10		
MemData39	AD10		
MemData40	AB08		
MemData41	AD08		
MemData42	R11		
MemData43	Y07		
MemData44	AC07		
MemData45	AB09		
MemData46	Y06		
MemData47	Y08		
MemData48	AA01		
MemData49	AA03		
MemData50	AB02		
MemData51	Y01		
MemData52	AB03		
MemData53	Y02		
MemData54	V07		
MemData55	V01		
MemData56	T08		
MemData57	U07		
MemData58	W01		
MemData59	W03		
MemData60	V06		
MemData61	T07		
MemData62	W05		
MemData63	U05		
MemVRef1	T14	DDR SDRAM	51
MemVRef2	T09		

Signals Listed Alphabetically (Sheet 13 of 24)

Signal Name	Ball	Interface Group	Page
No ball	A01	A physical ball does not exist at these ball coordinates.	NA
No ball	A02		
No ball	A03		
No ball	A22		
No ball	A23		
No ball	A24		
No ball	B01		
No ball	B02		
No ball	B23		
No ball	B24		
No ball	C01		
No ball	C24		
No ball	AB01		
No ball	AB24		
No ball	AC01		
No ball	AC02		
No ball	AC23		
No ball	AC24		
No ball	AD01		
No ball	AD02		
No ball	AD03		
No ball	AD22		
No ball	AD23		
No ball	AD24		

Signals Listed Alphabetically (Sheet 14 of 24)

Signal Name	Ball	Interface Group	Page
OV_{DD}	B04		
OV_{DD}	B12		
OV_{DD}	B19		
OV_{DD}	D02		
OV_{DD}	D10		
OV_{DD}	D17		
OV_{DD}	F08		
OV_{DD}	F15		
OV_{DD}	F23		
OV_{DD}	H06		
OV_{DD}	H10		
OV_{DD}	H13		
OV_{DD}	H21		
OV_{DD}	K04	Power	57
OV_{DD}	K08		
OV_{DD}	K19		
OV_{DD}	M02		
OV_{DD}	M17		
OV_{DD}	N08		
OV_{DD}	N23		
OV_{DD}	R06		
OV_{DD}	R17		
OV_{DD}	R21		
OV_{DD}	U04		
OV_{DD}	U19		
OV_{DD}	W02		
OV_{DD}	AA23		
PCIX133Cap	G08	PCI-X	50
$\overline{\text{PCIXAck64}}$	D09	PCI-X	50

Signals Listed Alphabetically (Sheet 15 of 24)

Signal Name	Ball	Interface Group	Page
PCIXAD00	C17	PCI-X	50
PCIXAD01	B09		
PCIXAD02	G10		
PCIXAD03	E10		
PCIXAD04	C10		
PCIXAD05	A10		
PCIXAD06	F11		
PCIXAD07	G12		
PCIXAD08	G14		
PCIXAD09	A15		
PCIXAD10	C15		
PCIXAD11	E15		
PCIXAD12	G15		
PCIXAD13	B16		
PCIXAD14	C16		
PCIXAD15	D16		
PCIXAD16	E18		
PCIXAD17	E19		
PCIXAD18	F18		
PCIXAD19	G18		
PCIXAD20	D20		
PCIXAD21	A20		
PCIXAD22	A21		
PCIXAD23	C21		
PCIXAD24	F22		
PCIXAD25	B22		
PCIXAD26	G21		
PCIXAD27	E23		
PCIXAD28	C23		
PCIXAD29	F24		
PCIXAD30	D22		
PCIXAD31	D24		

Signals Listed Alphabetically (Sheet 16 of 24)

Signal Name	Ball	Interface Group	Page
PCIXAD32	H03	PCI-X	50
PCIXAD33	H01		
PCIXAD34	L08		
PCIXAD35	F01		
PCIXAD36	D01		
PCIXAD37	J05		
PCIXAD38	H05		
PCIXAD39	G02		
PCIXAD40	E02		
PCIXAD41	C02		
PCIXAD42	A08		
PCIXAD43	G05		
PCIXAD44	F03		
PCIXAD45	D03		
PCIXAD46	B03		
PCIXAD47	H07		
PCIXAD48	G04		
PCIXAD49	E04		
PCIXAD50	C04		
PCIXAD51	A04		
PCIXAD52	F05		
PCIXAD53	D05		
PCIXAD54	B05		
PCIXAD55	C09		
PCIXAD56	E06		
PCIXAD57	C06		
PCIXAD58	A06		
PCIXAD59	F07		
PCIXAD60	E07		
PCIXAD61	D07		
PCIXAD62	B07		
PCIXAD63	E08		

Signals Listed Alphabetically (Sheet 17 of 24)

Signal Name	Ball	Interface Group	Page
PCIXC0[BE0]	F14	PCI-X	50
PCIXC1[BE1]	E16		
PCIXC2[BE2]	C19		
PCIXC3[BE3]	F20		
PCIXC4[BE4]	C08		
PCIXC5[BE5]	C03		
PCIXC6[BE6]	G09		
PCIXC7[BE7]	F09		
PCIXCap	L23	PCI-X	50
PCIXClk	E03	PCI-X	50
PCIXDevSel	E13	PCI-X	50
PCIXFrame	A11	PCI-X	50
PCIXGnt0	E22	PCI-X	50
PCIXGnt1[IRQ12]	C22		
PCIXGnt2	N22		
PCIXGnt3	M18		
PCIXGnt4	R22		
PCIXGnt5	P19		
PCIXIDSel	G07	PCI-X	50
PCIXINT	M07	PCI-X	50
PCIXIRDY	E12	PCI-X	50
PCIXM66En	A14	PCI-X	50
PCIXParHigh	L04	PCI-X	50
PCIXParLow	F16	PCI-X	50
PCIXPErr	A17	PCI-X	50
PCIXReq0	E24	PCI-X	50
PCIXReq1[IRQ11]	E21		
PCIXReq2	E20		
PCIXReq3	R20		
PCIXReq4	G23		
PCIXReq5	R18		
PCIXReq64	E09	PCI-X	50
PCIXReset	M24	PCI-X	50
PCIXSErr	A18	PCI-X	50

Signals Listed Alphabetically (Sheet 18 of 24)

Signal Name	Ball	Interface Group	Page
PCIXStop	L12	PCI-X	50
PCIXTRDY	C12	PCI-X	50
PerAddr00	D11	External Slave Peripheral **Note:** PerAddr00 is the most significant bit (msb) on this bus.	53
PerAddr01	C11		
PerAddr02	B11		
PerAddr03	A12		
PerAddr04	A19		
PerAddr05	D18		
PerAddr06	E11		
PerAddr07	M03		
PerAddr08	N01		
PerAddr09	E14		
PerAddr10	C20		
PerAddr11	A16		
PerAddr12	A13		
PerAddr13	B14		
PerAddr14	C14		
PerAddr15	D14		
PerAddr16	B20		
PerAddr17	L15		
PerAddr18	L21		
PerAddr19	L22		
PerAddr20	M22		
PerAddr21	M01		
PerAddr22	L24		
PerAddr23	P24		
PerAddr24	T19		
PerAddr25	R24		
PerAddr26	U22		
PerAddr27	U24		
PerAddr28	N03		
PerAddr29	V20		
PerAddr30	V23		
PerAddr31	V21		

Signals Listed Alphabetically (Sheet 19 of 24)

Signal Name	Ball	Interface Group	Page
PerBLast	C07	External Slave Peripheral	53
PerClk	U18	External Master Peripheral	54
PerCS0	E17	External Slave Peripheral	53
PerCS1	L10		
PerCS2	V04		
PerCS3	T24		
PerCS4	L03		
PerCS5	T03		
PerCS6	L13		
PerCS7	U03		

Signals Listed Alphabetically (Sheet 20 of 24)

Signal Name	Ball	Interface Group	Page
PerData00	H24	External Slave Peripheral **Note:** PerData00 is the most significant bit (msb) on this bus.	53
PerData01	H22		
PerData02	H20		
PerData03	G20		
PerData04	G19		
PerData05	H18		
PerData06	J23		
PerData07	J22		
PerData08	J21		
PerData09	J20		
PerData10	J19		
PerData11	J18		
PerData12	J17		
PerData13	J15		
PerData14	J14		
PerData15	J13		
PerData16	J12		
PerData17	J11		
PerData18	J10		
PerData19	J09		
PerData20	L14		
PerData21	K24		
PerData22	K22		
PerData23	K20		
PerData24	K18		
PerData25	K16		
PerData26	K14		
PerData27	K11		
PerData28	K09		
PerData29	L19		
PerData30	L17		
PerData31	L16		
[PerErr]TrcTS6	P21	External Master Peripheral	54
$\overline{\text{PerOE}}$	M09	External Slave Peripheral	53

Signals Listed Alphabetically (Sheet 21 of 24)

Signal Name	Ball	Interface Group	Page
PerPar0	T23	External Slave Peripheral	53
PerPar1	T22		
PerPar2	W20		
PerPar3	U20		
PerReady[RcvrInh]	N07	External Slave Peripheral	53
PerR/$\overline{W}$	P05	External Slave Peripheral	53
$\overline{PerWBE0}$	T18	External Slave Peripheral	53
$\overline{PerWBE1}$	V19		
$\overline{PerWBE2}$	W22		
$\overline{PerWBE3}$	W24		
$\overline{PerWE}$	P02	External Slave Peripheral	53
$\overline{RAS}$	AD07	DDR SDRAM	51
[RcvrInh]PerReady	N07	System	56
RefVEn	L02	System	56
SV_{DD}	U12	Power	57
SV_{DD}	U15		
SV_{DD}	W10		
SV_{DD}	W17		
SV_{DD}	AA08		
SV_{DD}	AA15		
SV_{DD}	AC06		
SV_{DD}	AC13		
SV_{DD}	AC21		
SysClk	G22	System	56
SysErr	T02	System	56
$\overline{SysReset}$	P10	System	56
TCK	V22	JTAG	55
TDI	Y24	JTAG	55
TDO	Y22	JTAG	55
TestEn	M05	System	56
TmrClk	U01	System	56
TMS	AB22	JTAG	55

Signals Listed Alphabetically (Sheet 22 of 24)

Signal Name	Ball	Interface Group	Page
TrcBS0[GPIO18][IRQ13]	N16	Trace	57
TrcBS1[GPIO19][IRQ14]	P17		
TrcBS2[GPIO20][IRQ15]	T20		
TrcClk	R05	Trace	57
TrcES0[GPIO21][IRQ16]	T21	Trace	57
TrcES1[GPIO22][IRQ17]	P23		
TrcES2[GPIO23]	N09		
TrcES3[GPIO24]	P08		
TrcES4[GPIO25]	T05		
TrcTS0[GPIO26]	T04	Trace	57
TrcTS1[GPIO27][GMCCD, GMC1RxClk, RTBI1RxClk]	P03	Trace	57
[TrcTS1]BusReq	AA24	Trace	57
TrcTS2[GPIO28][GMCRxD4, GMC1RxD0, TBIRxD4, RTBI1RxD0]	R07	Trace	57
[TrcTS2]$\overline{\text{ExtAck}}$	AA22	Trace	57
TrcTS3[GPIO29][GMCRxD5, GMC1RxD1, TBIRxD5, RTBI1RxD1]	P09	Trace	57
[TrcTS3]$\overline{\text{ExtReq}}$	AB23	Trace	57
TrcTS4[GPIO30][GMCRxD6, GMC1RxD2, TBIRxD6, RTBI1RxD2]	R09	Trace	57
[TrcTS4]HoldAck	Y21	Trace	57
TrcTS5[GPIO31][GMCRxD7, GMC1RxD3, TBIRxD7, RTBI1RxD3]	T06	Trace	57
[TrcTS5]HoldReq	Y23	Trace	57
TrcTS6[GMCCrS, GMC1TxClk, RTBI1TxClk]	R01	Trace	57
TrcTS6[PerErr]	P21	Trace	57
$\overline{\text{TRST}}$	N24	JTAG	55
$\overline{\text{UART0\_CTS}}$	C13	UART Peripheral	54
$\overline{\text{UART0\_DCD}}$	V24	UART Peripheral **Note:** Used as initialization strapping input.	54
$\overline{\text{UART0\_DSR}}$	V02	UART Peripheral **Note:** Used as initialization strapping input.	54
$\overline{\text{UART0\_DTR}}$	B18	UART Peripheral	54
$\overline{\text{UART0\_RI}}$	H16	UART Peripheral	54
$\overline{\text{UART0\_RTS}}$	G16	UART Peripheral	54
UART0_Rx	G17	UART Peripheral	54

Signals Listed Alphabetically (Sheet 23 of 24)

Signal Name	Ball	Interface Group	Page
UART0_Tx	L11	UART Peripheral	54
$\overline{\text{UART1\_DSR/CTS}}$[GPIO14]	G06	UART Peripheral	54
$\overline{\text{UART1\_RTS/DTR}}$[GPIO15]	E05	UART Peripheral	54
UART1_Rx[GPIO12]	C18	UART Peripheral	54
UART1_Tx[GPIO13]	J16	UART Peripheral	54
UARTSerClk	A09	UART Peripheral	54
V_{DD}	B08	Power	57
V_{DD}	B15		
V_{DD}	D06		
V_{DD}	D13		
V_{DD}	D21		
V_{DD}	F04		
V_{DD}	F12		
V_{DD}	F19		
V_{DD}	H02		
V_{DD}	H17		
V_{DD}	K12		
V_{DD}	K15		
V_{DD}	K23		
V_{DD}	M06		
V_{DD}	M10		
V_{DD}	M13		
V_{DD}	M21		
V_{DD}	N04		
V_{DD}	N12		
V_{DD}	N15		

Signals Listed Alphabetically (Sheet 24 of 24)

Signal Name	Ball	Interface Group	Page
V_{DD}	N19	Power	57
V_{DD}	R02		
V_{DD}	R10		
V_{DD}	R13		
V_{DD}	U08		
V_{DD}	U23		
V_{DD}	W06		
V_{DD}	W13		
V_{DD}	W21		
V_{DD}	AA04		
V_{DD}	AA12		
V_{DD}	AA19		
V_{DD}	AC10		
V_{DD}	AC17		
$\overline{WE}$	Y05	DDR SDRAM	51

In the following table, only the primary (default) signal name is shown for each pin. Multiplexed or multifunction signals are marked with an asterisk (*). To determine what signals or functions are multiplexed on those pins, look up the primary signal name in “Signals Listed Alphabetically” on page 18.

Signals Listed by Ball Assignment (Sheet 1 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	No ball	B01	No ball	C01	No ball	D01	PCIXAD36
A02	No ball	B02	No ball	C02	PCIXAD41	D02	OV_{DD}
A03	No ball	B03	PCIXAD46	C03	PCIXC5 *	D03	PCIXAD45
A04	PCIXAD51	B04	OV_{DD}	C04	PCIXAD50	D04	GND
A05	DrvrInh2	B05	PCIXAD54	C05	EMCTxErr *	D05	PCIXAD53
A06	PCIXAD58	B06	GND	C06	PCIXAD57	D06	V_{DD}
A07	EMCRxD2 *	B07	PCIXAD62	C07	$\overline{\text{PerBLast}}$	D07	PCIXAD61
A08	PCIXAD42	B08	V_{DD}	C08	PCIXC4 *	D08	GND
A09	UARTSerClk	B09	PCIXAD01	C09	PCIXAD55	D09	$\overline{\text{PCIXAck64}}$
A10	PCIXAD05	B10	GND	C10	PCIXAD04	D10	OV_{DD}
A11	$\overline{\text{PCIXFrame}}$	B11	PerAddr02	C11	PerAddr01	D11	PerAddr00
A12	PerAddr03	B12	OV_{DD}	C12	$\overline{\text{PCIXTRDY}}$	D12	GND
A13	PerAddr12	B13	GND	C13	$\overline{\text{UART0\_CTS}}$	D13	V_{DD}
A14	PCIXM66En	B14	PerAddr13	C14	PerAddr14	D14	PerAddr15
A15	PCIXAD09	B15	V_{DD}	C15	PCIXAD10	D15	GND
A16	PerAddr11	B16	PCIXAD13	C16	PCIXAD14	D16	PCIXAD15
A17	$\overline{\text{PCIXPErr}}$	B17	GND	C17	PCIXAD00	D17	OV_{DD}
A18	$\overline{\text{PCIXSErr}}$	B18	$\overline{\text{UART0\_DTR}}$	C18	UART1_Rx *	D18	PerAddr05
A19	PerAddr04	B19	OV_{DD}	C19	PCIXC2 *	D19	GND
A20	PCIXAD21	B20	PerAddr16	C20	PerAddr10	D20	PCIXAD20
A21	PCIXAD22	B21	GND	C21	PCIXAD23	D21	V_{DD}
A22	No ball	B22	PCIXAD25	C22	$\overline{\text{PCIXGnt1}}$ *	D22	PCIXAD30
A23	No ball	B23	No ball	C23	PCIXAD28	D23	GND
A24	No ball	B24	No ball	C24	No ball	D24	PCIXAD31

Signals Listed by Ball Assignment (Sheet 2 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	EMCRxD1 *	F01	PCIXAD35	G01	APV_{DD} for PCI PLL	H01	PCIXAD33
E02	PCIXAD40	F02	GND	G02	PCIXAD39	H02	V_{DD}
E03	PCIXClk	F03	PCIXAD44	G03	EMCRxD0 *	H03	PCIXAD32
E04	PCIXAD49	F04	V_{DD}	G04	PCIXAD48	H04	GND
E05	$\overline{\text{UART1\_RTS/DTR}}$ *	F05	PCIXAD52	G05	PCIXAD43	H05	PCIXAD38
E06	PCIXAD56	F06	GND	G06	$\overline{\text{UART1\_DSR/CTS}}$ *	H06	OV_{DD}
E07	PCIXAD60	F07	PCIXAD59	G07	PCIXIDSel	H07	PCIXAD47
E08	PCIXAD63	F08	OV_{DD}	G08	PCIX133Cap	H08	GND
E09	$\overline{\text{PCIXReq64}}$	F09	PCIXC7 *	G09	PCIXC6 *	H09	EMCRxD3 *
E10	PCIXAD03	F10	GND	G10	PCIXAD02	H10	OV_{DD}
E11	PerAddr06	F11	PCIXAD06	G11	IIC0SClk	H11	IIC1SClk *
E12	$\overline{\text{PCIXIRDY}}$	F12	V_{DD}	G12	PCIXAD07	H12	GND
E13	$\overline{\text{PCIXDevSel}}$	F13	GND	G13	IIC0SDA	H13	OV_{DD}
E14	PerAdd09	F14	PCIXC0 *	G14	PCIXAD08	H14	IIC1SDA *
E15	PCIXAD11	F15	OV_{DD}	G15	PCIXAD12	H15	GND
E16	PCIXC1 *	F16	PCIXParLow	G16	$\overline{\text{UART0\_RTS}}$	H16	$\overline{\text{UART0\_RI}}$
E17	$\overline{\text{PerCS0}}$	F17	GND	G17	UART0_Rx	H17	V_{DD}
E18	PCIXAD16	F18	PCIXAD18	G18	PCIXAD19	H18	PerData05
E19	PCIXAD17	F19	V_{DD}	G19	PerData04	H19	GND
E20	$\overline{\text{PCIXReq2}}$	F20	PCIXC3 *	G20	PerData03	H20	PerData02
E21	$\overline{\text{PCIXReq1}}$ *	F21	GND	G21	PCIXAD26	H21	OV_{DD}
E22	$\overline{\text{PCIXGnt0}}$	F22	PCIXAD24	G22	SysClk	H22	PerData01
E23	PCIXAD27	F23	OV_{DD}	G23	$\overline{\text{PCIXReq4}}$	H23	GND
E24	$\overline{\text{PCIXReq0}}$	F24	PCIXAD29	G24	ASV_{DD} for SysClk PLL	H24	PerData00

Signals Listed by Ball Assignment (Sheet 3 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	AGND	K01	EMCRxDV *	L01	GMCRefClk	M01	PerAddr21
J02	EMCRxClk *	K02	GND	L02	RefVEn	M02	OV_{DD}
J03	EMCTxD3 *	K03	EMCRxErr *	L03	$\overline{\text{PerCS4}}$	M03	PerAddr07
J04	EMCTxD2 *	K04	OV_{DD}	L04	PCIXParHigh	M04	GND
J05	PCIXAD37	K05	EMCTxD1 *	L05	EMCMDIO	M05	TestEn
J06	EMCTxClk *	K06	GND	L06	EMCTxEn *	M06	V_{DD}
J07	EMCCD *	K07	EMCCrS *	L07	GMCTxEr *	M07	$\overline{\text{PCIXINT}}$
J08	EMCMDClk	K08	OV_{DD}	L08	PCIXAD34	M08	GND
J09	PerData19	K09	PerData28	L09	EMCTxD0 *	M09	$\overline{\text{PerOE}}$
J10	PerData18	K10	GND	L10	$\overline{\text{PerCS1}}$	M10	V_{DD}
J11	PerData17	K11	PerData27	L11	UART0_Tx	M11	DMAReq1
J12	PerData16	K12	V_{DD}	L12	$\overline{\text{PCIXStop}}$	M12	GND
J13	PerData15	K13	GND	L13	$\overline{\text{PerCS6}}$	M13	V_{DD}
J14	PerData14	K14	PerData26	L14	PerData20	M14	IRQ06 *
J15	PerData13	K15	V_{DD}	L15	PerAddr17	M15	GND
J16	UART1_Tx *	K16	PerData25	L16	PerData31	M16	EOT3/TC3 *
J17	PerData12	K17	GND	L17	PerData30	M17	OV_{DD}
J18	PerData11	K18	PerData24	L18	IRQ03 *	M18	$\overline{\text{PCIXGnt3}}$
J19	PerData10	K19	OV_{DD}	L19	PerData29	M19	GND
J20	PerData9	K20	PerData23	L20	IRQ01 *	M20	IRQ05 *
J21	PerData8	K21	GND	L21	PerAddr18	M21	V_{DD}
J22	PerData7	K22	PerData22	L22	PerAddr19	M22	PerAddr20
J23	PerData6	K23	V_{DD}	L23	PCIXCap	M23	GND
J24	AGND	K24	PerData21	L24	PerAddr22	M24	$\overline{\text{PCIXReset}}$

Signals Listed by Ball Assignment (Sheet 4 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	PerAddr08	P01	DMAReq3 *	R01	TrcTS6 *	T01	DQS7
N02	GND	P02	$\overline{\text{PerWE}}$	R02	V_{DD}	T02	SysErr
N03	PerAddr28	P03	TrcTS1 *	R03	DMAReq0	T03	$\overline{\text{PerCS5}}$
N04	V_{DD}	P04	GMCRxEr *	R04	GND	T04	TrcTS0 *
N05	DMAAck0	P05	PerR/$\overline{\text{W}}$	R05	TrcClk	T05	TrcES4 *
N06	GND	P06	DMAAck2 *	R06	OV_{DD}	T06	TrcTS5 *
N07	PerReady *	P07	DMAAck1	R07	TrcTS2 *	T07	MemData61
N08	OV_{DD}	P08	TrcES3 *	R08	GND	T08	MemData56
N09	TrcES2 *	P09	TrcTS3 *	R09	TrcTS4 *	T09	MemVRef2
N10	GND	P10	$\overline{\text{SysReset}}$	R10	V_{DD}	T10	MemData38
N11	DMAReq2 *	P11	DMAAck3 *	R11	MemData42	T11	MemData37
N12	V_{DD}	P12	MemData28	R12	GND	T12	MemData35
N13	GND	P13	DM3	R13	V_{DD}	T13	MemData22
N14	IRQ04 *	P14	GPIO11 *	R14	MemData14	T14	MemVRef1
N15	V_{DD}	P15	EOT1/TC1	R15	GND	T15	MemData18
N16	TrcBS0 *	P16	EOT2/TC2 *	R16	EOT0/TC0	T16	DM0
N17	GND	P17	TrcBS1 *	R17	OV_{DD}	T17	$\overline{\text{ExtReset}}$
N18	IRQ00 *	P18	IRQ07 *	R18	$\overline{\text{PCIXReq5}}$	T18	$\overline{\text{PerWBE0}}$
N19	V_{DD}	P19	$\overline{\text{PCIXGnt5}}$	R19	GND	T19	PerAddr24
N20	IRQ08 *	P20	IRQ02 *	R20	$\overline{\text{PCIXReq3}}$	T20	TrcBS2 *
N21	GND	P21	TrcTS6 *	R21	OV_{DD}	T21	TrcES0 *
N22	$\overline{\text{PCIXGnt2}}$	P22	IRQ09 *	R22	$\overline{\text{PCIXGnt4}}$	T22	PerPar1
N23	OV_{DD}	P23	TrcES1 *	R23	GND	T23	PerPar0
N24	$\overline{\text{TRST}}$	P24	PerAddr23	R24	PerAddr25	T24	$\overline{\text{PerCS3}}$

Signals Listed by Ball Assignment (Sheet 5 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	TmrClk	V01	MemData55	W01	MemData58	Y01	MemData51
U02	GND	V02	UART0_DSR	W02	OV_{DD}	Y02	MemData53
U03	PerCS7	V03	DM7	W03	MemData59	Y03	DM6
U04	OV_{DD}	V04	PerCS2	W04	GND	Y04	DQS6
U05	MemData63	V05	Halt	W05	MemData62	Y05	WE
U06	GND	V06	MemData60	W06	V_{DD}	Y06	MemData46
U07	MemData57	V07	MemData54	W07	ECC3	Y07	MemData43
U08	V_{DD}	V08	MemClkOut0	W08	GND	Y08	MemData47
U09	ECC4	V09	MemClkOut0	W09	ClkEn3	Y09	ClkEn2
U10	GND	V10	MemAddr12	W10	SV_{DD}	Y10	MemData34
U11	MemData36	V11	MemAddr9	W11	MemData32	Y11	MemAddr11
U12	SV_{DD}	V12	MemData31	W12	GND	Y12	MemData30
U13	GND	V13	MemAddr8	W13	V_{DD}	Y13	MemData27
U14	MemData21	V14	MemData26	W14	BankSel1	Y14	MemAddr7
U15	SV_{DD}	V15	MemData19	W15	GND	Y15	MemData23
U16	MemData04	V16	MemData09	W16	MemAddr10	Y16	MemData20
U17	GND	V17	MemData05	W17	SV_{DD}	Y17	MemData10
U18	PerClk	V18	IRQ10 *	W18	MemData08	Y18	MemData13
U19	OV_{DD}	V19	PerWBE1	W19	GND	Y19	MemAddr00
U20	PerPar3	V20	PerAddr29	W20	PerPar2	Y20	MemAddr02
U21	GND	V21	PerAddr31	W21	V_{DD}	Y21	HoldAck *
U22	PerAddr26	V22	TCK	W22	PerWBE2	Y22	TDO
U23	V_{DD}	V23	PerAddr30	W23	GND	Y23	HoldReq *
U24	PerAddr27	V24	UART0_DCD	W24	PerWBE3	Y24	TDI

Signals Listed by Ball Assignment (Sheet 6 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	MemData48	AB01	No ball	AC01	No ball	AD01	No ball
AA02	GND	AB02	MemData50	AC02	No ball	AD02	No ball
AA03	MemData49	AB03	MemData52	AC03	ECC5	AD03	No ball
AA04	V_{DD}	AB04	ECC6	AC04	GND	AD04	ECC7
AA05	DQS8	AB05	$\overline{CAS}$	AC05	DM8	AD05	$\overline{BankSel3}$
AA06	GND	AB06	ECC1	AC06	SV_{DD}	AD06	ECC2
AA07	DM5	AB07	ECC0	AC07	MemData44	AD07	$\overline{RAS}$
AA08	SV_{DD}	AB08	MemData40	AC08	GND	AD08	MemData41
AA09	DM4	AB09	MemData45	AC09	DQS5	AD09	BA1
AA10	GND	AB10	ClkEn1	AC10	V_{DD}	AD10	MemData39
AA11	AGND	AB11	AMV_{DD} for MemClk PLL	AC11	DQS4	AD11	$\overline{BankSel2}$
AA12	V_{DD}	AB12	MemData29	AC12	GND	AD12	MemData33
AA13	GND	AB13	DQS3	AC13	SV_{DD}	AD13	MemData24
AA14	MemData16	AB14	DM2	AC14	DQS2	AD14	MemData25
AA15	SV_{DD}	AB15	$\overline{BankSel0}$	AC15	GND	AD15	MemData17
AA16	BA0	AB16	MemData11	AC16	DQS1	AD16	MemAddr5
AA17	GND	AB17	MemData15	AC17	V_{DD}	AD17	ClkEn0
AA18	DM1	AB18	MemAddr6	AC18	MemData12	AD18	MemAddr4
AA19	V_{DD}	AB19	MemData07	AC19	GND	AD19	MemData06
AA20	MemData03	AB20	MemAddr3	AC20	DQS0	AD20	MemAddr01
AA21	GND	AB21	MemData01	AC21	SV_{DD}	AD21	MemData00
AA22	$\overline{ExtAck}$ *	AB22	TMS	AC22	MemData02	AD22	No ball
AA23	OV_{DD}	AB23	$\overline{ExtReq}$ *	AC23	No ball	AD23	No ball
AA24	BusReq *	AB24	No ball	AC24	No ball	AD24	No ball

Signal Description

The PPC440GX embedded controller is provided in a 552-ball, ball grid array package. The following tables describe the package level pinout.

Pin Summary

Group	No. of Pins
Signal pins, non-multiplexed	343
Signal pins, multiplexed	63
Total Signal Pins	**406**
AxV_{DD}	3
AGnd	3
OV_{DD}	27
SV_{DD}	9
V_{DD}	34
Gnd	70
Total Power Pins	**146**
Reserved	0
Total Pins	**552**

In the table “Signal Functional Description” on page 50, each I/O signal is listed along with a short description of its function. Active-low signals (for example, $\overline{RAS}$) are marked with an overline. Please see “Signals Listed Alphabetically” on page 18 for the pin (ball) number to which each signal is assigned.

Multiplexed Signals

Some signals are multiplexed on the same pin so that the pin can be used for different functions. In most cases, the signal names shown in this table are not accompanied by signal names that may be multiplexed on the same pin. If you need to know what, if any, signals are multiplexed with a particular signal, look up the name in “Signals Listed Alphabetically” on page 18. It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

Multipurpose Signals

In addition to multiplexing, some pins are also multi-purpose. For example, the EBC peripheral controller address pins (PerAddr00:31) are used as outputs by the PPC440GX to broadcast an address to external slave devices when the PPC440GX has control of the external bus. When during the course of normal chip operation an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the PPC440GX. In this example, the pins are also bidirectional, serving both as inputs and outputs.

Multimode Signals

In some cases (for example, Ethernet) the function of a pin may vary with different modes of operation. When a pin has multiple signal names assigned to distinguish different modes of operation, all of the names are shown.

Strapping Pins

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 89). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

Signal Functional Description (Sheet 1 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCI-X Interface				
PCIXAD00:63	Address/Data bus (bidirectional).	I/O	3.3V PCI	
PCIXC0:7[$\overline{\text{BE0:7}}$]	PCI-X Command[Byte Enables].	I/O	3.3V PCI	
PCIXCap	Capable of PCI-X operation.	I	3.3V LVTTL	5
PCIX133Cap	PCI-X devices are 133 MHz capable.	O	3.3V PCI	
PCIXClk	Provides timing to the PCI interface for PCI transactions. **Note:** If the PCI-X interface is not being used, drive this pin with a 3.3V clock signal at a frequency between 1 and 66MHz	I	3.3V PCI	
$\overline{\text{PCIXDevSel}}$	Indicates the driving device has decoded its address as the target of the current access.	I/O	3.3V PCI	4
$\overline{\text{PCIXFrame}}$	Driven by the current master to indicate beginning and duration of an access.	I/O	3.3V PCI	4
$\overline{\text{PCIXGnt0}}$	Indicates that the specified agent is granted access to the bus. When using an external PCI/PCI-X arbiter, connect the external arbiter's Grant line to this signal.	I/O	3.3V PCI	4
$\overline{\text{PCIXGnt1}}$	Indicates that the specified agent is granted access to the bus.	I/O	3.3V PCI	4
$\overline{\text{PCIXGnt2:5}}$	Indicates that the specified agent is granted access to the bus.	O	3.3V PCI	
PCIXIDSel	Used as a chip select during configuration read and write transactions.	I	3.3V PCI	5
$\overline{\text{PCIXINT}}$	Level sensitive PCI interrupt.	O	3.3V PCI	
$\overline{\text{PCIXIRDY}}$	Indicates initiating agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	4
PCIXM66En	Capable of 66MHz operation.	I	3.3V LVTTL w/pull-up	5
PCIXParHigh	Even parity across PCIAD32:63 and PCIXC0:3[BE4:7].	I/O	3.3V PCI	
PCIXParLow	Even parity across PCIAD0:31 and PCIXC0:3[BE0:3].	I/O	3.3V PCI	
$\overline{\text{PCIXPErr}}$	Reports data parity errors during all PCI transactions except a Special Cycle.	I/O	3.3V PCI	4
$\overline{\text{PCIXReq0}}$	An indication to the PCI-X arbiter that the specified agent wishes to use the bus. When using an external PCI/PCI-X arbiter, connect the external arbiter's Request line to this signal.	I/O	3.3V PCI	4
$\overline{\text{PCIXReq1:5}}$	An indication to the PCI-X arbiter that the specified agent wishes to use the bus.	I	3.3V PCI	4
$\overline{\text{PCIXReq64}}$	Asserted by the current bus master, indicating a 64-bit transfer.	I/O	3.3V PCI	4
$\overline{\text{PCIXAck64}}$	Indicates the target can transfer data using 64 bits.	I/O	3.3V PCI	4
$\overline{\text{PCIXReset}}$	Brings PCI device registers and logic to a consistent state.	O	3.3V PCI	
$\overline{\text{PCIXSErr}}$	Reports address parity errors, data parity errors on the Special Cycle command, or other catastrophic system errors.	I/O	3.3V PCI	4
$\overline{\text{PCIXStop}}$	Indicates the current target is requesting the master to stop the current transaction.	I/O	3.3V PCI	4

Signal Functional Description (Sheet 2 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
$\overline{\text{PCIXTRDY}}$	Indicates the target agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	4
DDR SDRAM Interface				
BA0:1	Bank Address supporting up to four internal banks.	O	2.5V SSTL_2	
$\overline{\text{BankSel0:3}}$	Selects up to four external DDR SDRAM banks.	O	2.5V SSTL_2	
$\overline{\text{CAS}}$	Column Address Strobe.	O	2.5V SSTL_2	
ClkEn0:3	Clock Enable. One for each bank.	O	2.5V SSTL_2	
DM0:8	Memory write data byte lane masks. MEMDM8 is the byte lane mask for the ECC byte lane.	O	2.5V SSTL_2	
DQS0:8	Byte lane data strobe. DQS8 is the data strobe for the ECC byte lane.	I/O	2.5V SSTL_2	
ECC0:7	ECC check bits 0:7.	I/O	2.5V SSTL_2	
MemAddr00:12	Memory address bus.	O	2.5V SSTL_2	
MemClkOut0 $\overline{\text{MemClkOut0}}$	Subsystem clock.	O	2.5V SSTL_2	
MemData00:63	Memory data bus.	I/O	2.5V SSTL_2	
MemVRef1:2	Memory reference voltage (SV_{REF}) input.	I	Voltage Ref Receiver	
$\overline{\text{RAS}}$	Row Address Strobe.	O	2.5V SSTL_2	
$\overline{\text{WE}}$	Write Enable.	O	2.5V SSTL_2	
Ethernet Interface				
EMCCD, EMC1RxErr, GMCGTxClk, GMC0TxClk, TBITxClk, RTBI0TxClk	MII: Collision detection RMII 1: Receive error GMII: 1000Mbps Transmit clock RGMII: Transmit clock TBI: Transmit clock RTBI: Transmit clock	I/O	3.3V tolerant 2.5V CMOS	
EMCCrS, EMC0CrSDV, GMCTxD7, GMC1TxD3, TBITxD7, RTBI1TxD3	MII: Carrier sense RMII 0: Carrier sense data valid GMII: Transmit data RGMII 1: Transmit data TBI: Transmit data RTBI 1: Transmit data	I/O	3.3V tolerant 2.5V CMOS	
EMCMDClk	MII and RMII: Management data clock	O	3.3V tolerant 2.5V CMOS	
EMCMDIO	MII and RMII: Transfer command and status information between MII and PHY	I/O	3.3V tolerant 2.5V CMOS	

Signal Functional Description (Sheet 3 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
EMCRxD0:3, EMC0RxD0:1, EMC1RxD0:1, EMC0RxD, EMC1RxD, EMC2RxD, EMC3RxD, GMCTxD0:1, GMC0TxD0:1, TBITxD0:1, RTBI0TxD0:1	MII: Receive data RMII 0: Receive data RMII 1: Receive data SMII 0: Receive data SMII 1: Receive data SMII 2: Receive data SMII 3: Receive data GMII: Transmit data RGMII 0: Transmit data TBI: Transmit data RTBI 0: Transmit data	I/O	3.3V tolerant 2.5V CMOS	
EMCRxDV, EMC1CrSDV, GMCTxD4, GMC1TxD0, TBITxD4, RTBI1TxD0	MII: Receive data valid RMII 1: Carrier sense data valid GMII: Transmit data RGMII 1: Transmit data TBI: Transmit data RTBI 1: Transmit data	I/O	3.3V tolerant 2.5V CMOS	
EMCRxClk, GMCTxD5, GMC1TxD1, TBITxD5, RTBI1TxD1	MII: Receive clock GMII: Transmit data RGMII 1: Transmit data TBI: Transmit data RTBI 1: Transmit data	I/O	3.3V tolerant 2.5V CMOS	
EMCRxErr, EMC0RxErr, GMCTxD6, GMC1TxD2, TBITxD6, RTBI1TxD2	MII: Receive error RMII 0: Receive error GMII: Transmit data RGMII 1: Transmit data TBI: Transmit data RTBI 1: Transmit data	I/O	3.3V tolerant 2.5V CMOS	
EMCTxClk, EMCRefClk	MII: Transmit clock RMII and SMII: Reference clock	I	3.3V tolerant 2.5V CMOS	5
EMCTxD0:3, EMC0TxD0:1, EMC1TxD0:1, EMC0TxD, EMC1TxD, EMC2TxD, EMC3TxD, GMCTxD2:3, GMC0TxD2:3, TBITxD2:3, RTBI0TxD2:3	MII: Transmit data RMII 0: Transmit data RMII 1: Transmit data SMII 0: Transmit data SMII 1: Transmit data SMII 2: Transmit data SMII 3: Transmit data GMII: Transmit data RGMII 0: Transmit data TBI: Transmit data RTBI 0: Transmit data	O	3.3V tolerant 2.5V CMOS	
EMCTxEn, EMC0TxEn, EMCSync	MII: Transmit data enabled RMII 0: Transmit data enabled SMII: Sync signal	O	3.3V tolerant 2.5V CMOS	
EMCTxErr, EMC1TxEn, GMCRxClk, GMC0RxClk, TBIRxClk0, RTBI0RxClk	MII: Transmit error: RMII: Transmit data enabled GMII: Receive clock RGMII: Receive clock TBI: Receive clock 0 RTBI: Receive clock	I/O	3.3V tolerant 2.5V CMOS	
GMCCD, GMC1RxClk, RTBI1RxClk	GMII: Collision detection RGMII: Receive clock RTBI: Receive clock	I	3.3V tolerant 2.5V CMOS	5

Signal Functional Description (Sheet 4 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
GMCCrS, GMC1TxClk, RTBI1TxClk	GMII: Carrier sense RGMII: Transmit clock RTBI: Transmit clock	I/O	3.3V tolerant 2.5V CMOS	
GMCRefClk	GMII, RGMII, TBI and RTBI: Gigabit reference clock	I	3.3V tolerant 2.5V CMOS	5
GMCRxD0:3, GMC0RxD0:3, TBIRxD0:3, RTBI0RxD0:3	GMII: Receive data RGMII: Receive data TBI: Receive data RTBI: Receive data	I	3.3V tolerant 2.5V CMOS	
GMCRxD4:7, GMC1RxD0:3, TBIRxD4:7, RTBI1RxD0:3	GMII: Receive data RGMII: Receive data TBI: Receive data RTBI: Receive data	I	3.3V tolerant 2.5V CMOS	
GMCRxDV, GMC0RxCtl, TBIRxD8, RTBI0RxD4	GMII: Receive data valid RGMII: Receive control TBI: Receive data RTBI: Receive data	I	3.3V tolerant 2.5V CMOS	
GMCRxEr, GMC1RxCtl, TBIRxD9, RTBI1RxD4	GMII: Receive error RGMII: Receive control TBI: Receive data RTBI: Receive data	I/O	3.3V tolerant 2.5V CMOS	
GMCTxEn, GMC0TxCtl, TBITxD8, RTBI0TxD4	GMII: Transmit data enable RGMII: Transmit control TBI: Transmit data RTBI: Transmit data	O	3.3V tolerant 2.5V CMOS	
GMCTxEr, GMC1TxCtl, TBITxD9, RTBI1TxD4	GMII: Transmit error RGMII: Transmit control TBI: Transmit data RTBI: Transmit data	O	3.3V tolerant 2.5V CMOS	6
GMCTxClk TBIRxClk1	GMII: 10/100 Mbps Transmit clock TBI: Receive clock 1	I/O	3.3V LVTTL	5
External Slave Peripheral Interface				
DMAAck0:3	Used by the PPC440GX to indicate that data transfers have occurred.	O	3.3V tolerant 2.5V CMOS	
DMAReq0:3	Used by slave peripherals to indicate they are prepared to transfer data.	I	3.3V tolerant 2.5V CMOS	1, 5
EOT0:3/TC0:3	End Of Transfer/Terminal Count.	I/O	3.3V tolerant 2.5V CMOS	1, 5
PerAddr00:31	Peripheral address bus used by PPC440GX when not in external master mode, otherwise used by external master. **Note:** PerAddr00 is the most significant bit (msb) on this bus.	I/O	3.3V LVTTL	1
$\overline{\text{PerWBE0:3}}$	External peripheral data bus byte enables.	I/O	3.3V LVTTL	1, 2
$\overline{\text{PerBLast}}$	Used by either the peripheral controller, DMA controller, or external master to indicates the last transfer of a memory access.	I/O	3.3V LVTTL	1, 4
$\overline{\text{PerCS0:7}}$	External peripheral device select.	O	3.3V LVTTL	2
PerData00:31	Peripheral data bus used by PPC440GX when not in external master mode, otherwise used by external master. **Note:** PerData00 is the most significant bit (msb) on this bus.	I/O	3.3V LVTTL	1

Signal Functional Description (Sheet 5 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
$\overline{\text{PerOE}}$	Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the PPC440GX is the bus master, it enables the selected device to drive the bus.	O	3.3V LVTTL	2
PerPar0:3	External peripheral data bus byte parity.	I/O	3.3V LVTTL	1
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	3.3V LVTTL	
PerR/$\overline{\text{W}}$	Used by the PPC440GX when not in external master mode, as output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory. Otherwise, it used by the external master as an input to indicate the direction of transfer.	I/O	3.3V LVTTL	1, 2
$\overline{\text{PerWE}}$	Write Enable. Low when any of the four $\overline{\text{PerWBE0:3}}$ signals are low.	O	3.3V LVTTL	2
External Master Peripheral Interface				
BusReq	Bus Request. Used when the PPC440GX needs to regain control of peripheral interface from an external master.	O	3.3V LVTTL	
$\overline{\text{ExtAck}}$	External Acknowledgement. Used by the PPC440GX to indicate that a data transfer occurred.	O	3.3V LVTTL	
$\overline{\text{ExtReq}}$	External Request. Used by an external master to indicate it is prepared to transfer data.	I	3.3V LVTTL	1, 4
$\overline{\text{ExtReset}}$	Peripheral Reset. Used by an external master and by synchronous peripheral slaves.	O	3.3V LVTTL	
HoldAck	Hold Acknowledge. Used by the PPC440GX to transfer ownership of peripheral bus to an external master.	O	3.3V LVTTL	
HoldReq	Hold Request. Used by an external master to request ownership of the peripheral bus.	I	3.3V LVTTL	1, 5
PerClk	Peripheral Clock. Used by an external master and by synchronous peripheral slaves.	O	3.3V LVTTL	
PerErr	External Error. Used as an input to record external master errors and external slave peripheral errors.	I/O	3.3V LVTTL	1, 5
UART Peripheral Interface				
UARTSerClk	Serial clock input that provides an alternative to the internally generated serial clock. Used in cases where the allowable internally generated clock rates are not satisfactory. This input can be individually connected to either or both UART0 and UART1.	I	3.3V LVTTL	1, 4
UART0_Rx	UART0 Receive data.	I	3.3V LVTTL	1, 4
UART0_Tx	UART0 Transmit data.	O	3.3V LVTTL	4
$\overline{\text{UART0\_DCD}}$	UART0 Data Carrier Detect.	I	3.3V LVTTL	6
$\overline{\text{UART0\_DSR}}$	UART0 Data Set Ready.	I	3.3V LVTTL	6
$\overline{\text{UART0\_CTS}}$	UART0 Clear To Send.	I	3.3V LVTTL	1, 4
$\overline{\text{UART0\_DTR}}$	UART0 Data Terminal Ready.	O	3.3V LVTTL	4
$\overline{\text{UART0\_RTS}}$	UART0 Request To Send.	O	3.3V LVTTL	4
$\overline{\text{UART0\_RI}}$	UART0 Ring Indicator.	I	3.3V LVTTL	1, 4

Signal Functional Description (Sheet 6 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
UART1_Rx	UART1 Receive data.	I/O	3.3V LVTTL	1, 4
UART1_Tx	UART1 Transmit data.	I/O	3.3V LVTTL	1, 4
$\overline{\text{UART1\_DSR}}$/$\overline{\text{CTS}}$	UART1 Data Set Ready or Clear To Send. The choice is determined by a DCR register bit setting.	I/O	3.3V LVTTL	1, 4
$\overline{\text{UART1\_RTS/DTR}}$	UART1 Request To Send or Data Terminal Ready. The choice is determined by a DCR register bit setting.	I/O	3.3V LVTTL	1, 4
IIC Peripheral Interface				
IIC0SClk	IIC0 Serial Clock.	I/O	3.3V LVTTL	1, 2
IIC0SDA	IIC0 Serial Data.	I/O	3.3V LVTTL	1, 2
IIC1SClk	IIC1 Serial Clock.	I/O	3.3V IIC	1, 2
IIC1SDA	IIC1 Serial Data.	I/O	3.3V IIC	1, 2
Interrupts Interface				
IRQ00:10	External interrupt Requests 0 through 10.	I	3.3V LVTTL	1, 5
IRQ11:12	External interrupt Requests 11 through 12.	I	3.3V PCI	
IRQ13:17	External interrupt Requests 13 through 17.	I	3.3V LVTTL	
JTAG Interface				
TCK	Test Clock.	I	3.3V LVTTL w/pull-up	1
TDI	Test Data In.	I	3.3V LVTTL w/pull-up	4
TDO	Test Data Out.	O	3.3V LVTTL	
TMS	Test Mode Select.	I	3.3V LVTTL w/pull-up	1
$\overline{\text{TRST}}$	Test Reset. During chip power-up, this signal must be low from the start of V_{DD} ramp-up until at least 16 SysClk cycles after V_{DD} is stable in order to initialize the JTAG controller.	I	3.3V LVTTL w/pull-up	5

Signal Functional Description (Sheet 7 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
System Interface				
SysClk	Main system clock input.	Clock	3.3V LVTTL	
SysErr	Set to 1 when a machine check is generated.	O	3.3V LVTTL	
$\overline{\text{SysReset}}$	Main system reset. External logic can drive this bidirectional pin low (minimum of 16 cycles) to initiate a system reset. A system reset can also be initiated by software. The signal is implemented as an open-drain output (two states; 0 or open circuit). During chip power-up, this signal must be low from the start of V_{DD} ramp-up until at least 16 SysClk cycles after V_{DD} is stable.	I/O	3.3V LVTTL	1, 2
TmrClk	Processor timer external input clock.	I	3.3V LVTTL	
$\overline{\text{Halt}}$	Halt from external debugger.	I	3.3V LVTTL	1, 4
GPIO00:31	General purpose I/O 0 through 10. To access these functions, software must set DCR register bits.	I/O	3.3V LVTTL	
TestEn	Test Enable.	I	3.3V tolerant 2.5V CMOS	3
RcvrInh	Receiver Inhibit. Active only when TestEn is active.	I	3.3V LVTTL	
RefVEn	Reference Voltage Enable. Do not connect for normal operation. Pull up for Boundary Scan Description Language (BSDL) testing.	I	3.3V LVTTL w/pull-down	
DrvrInh2	Driver Inhibit. Used for test purposes only. Tie up for normal operation	I	3.3V LVTTL w/pull-up	2

Signal Functional Description (Sheet 8 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Trace Interface				
TrcBS0:2	Trace branch execution status.	I/O	3.3V LVTTL	
TrcClk	Trace data capture clock, runs at 1/4 the frequency of the processor.	O	3.3V LVTTL	
TrcES0:4	Trace Execution Status is presented every fourth processor clock cycle.	I/O	3.3V LVTTL	
TrcTS0:5 (multiplexed with GPIO signals)	Additional information on trace execution and branch status. **Note:** The trace signals, TrcTS0:6, are duplicated on two sets of chip balls and are multiplexed with other signals in both cases. This allows users to choose which set of multiplexed signals they wish to use along with the TrcTS0:6 signals. The trace signals in this set are *primary* signals.	I/O	3.3V tolerant 2.5V CMOS	
TrcTS1:5 (multiplexed with EBC signals)	Additional information on trace execution and branch status. **Note:** The trace signals in this set are *secondary* signals.	I/O	3.3V LVTTL	
TrcTS6 (multiplexed with EBC and Ethernet signals)	Additional information on trace execution and branch status. **Note:** This trace signal is the *primary* signal.	I/O	3.3V LVTTL	
Power Pins				
AGND	PLL (analog) voltage ground.	na	na	
GND	Ground.	na	na	
AxV_{DD}	1.5V—Filtered voltages input for PLLs (analog circuits) **Note:** A separate filter for each of the three voltages is recommended.	na	na	
OV_{DD}	3.3V supply—I/O (except DDR SDRAM, Ethernet)	na	na	
SV_{DD}	2.5V supply—DDR SDRAM, Ethernet	na	na	
V_{DD}	1.5V supply—Logic voltage.	na	na	

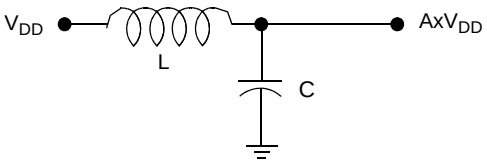
Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. *Operation at or beyond these maximum ratings can cause permanent damage to the device. None of the performance specification contained in this document are guaranteed when operating at these maximum ratings.*

Characteristic	Symbol	Value	Unit	Notes
Supply Voltage (Internal Logic)	V_{DD}	0 to +1.65	V	
Supply Voltage (I/O Interface, except DDR SDRAM)	OV_{DD}	0 to +3.6	V	
PLL Supply Voltages	AxV_{DD}	0 to +1.65	V	1
Supply Voltage (DDR SDRAM Logic)	SV_{DD}	0 to +2.7	V	
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to +3.6	V	
Storage Temperature Range	T_{STG}	-55 to +150	°C	
Case Temperature under bias	T_C	-40 to +120	°C	2

Notes:

1. The analog voltages used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440GX. A separate filter, as shown below, is recommended for each voltage:



L – SMT ferrite bead chip, Murata BLM31A700S or equivalent.

C – 0.1µF ceramic

2. This value is not a specification of the operational temperature range; it is a stress rating only.

Package Thermal Specifications

Thermal resistance values for the CBGA and PBGA packages in a convection environment are as follows:

Parameter	Symbol	Package	Airflow ft/min (m/sec)			Unit	Notes
			0 (0)	100 (0.51)	200 (1.02)		
Junction-to-case thermal resistance	θ_{JC}	Ceramic	<0.1	<0.1	<0.1	°C/W	1
		Plastic	1.2	1.2	1.2	°C/W	1, 3
Case-to-ambient thermal resistance (w/o heat sink)	θ_{CA}	Ceramic	18.9	17.7	16.3	°C/W	2
		Plastic		20.8		°C/W	2, 3
			Range				
			Min	Nom	Max		
Junction-to-ball (typical)	θ_{JB}	Ceramic	1.5		2.2	°C/W	4
		Plastic		8.2		°C/W	

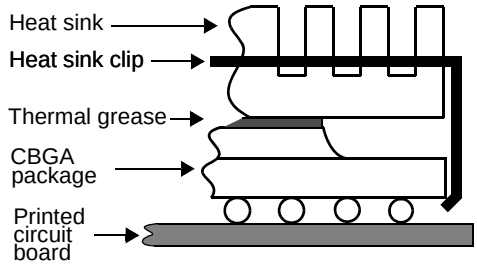
Notes:

1. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
2. The case-to-ambient thermal resistance is measured in a JEDEC JESD51-6 standard environment; and may not accurately predict thermal performance in production equipment environments. The operational case temperature must be maintained.
3. Modeled on standard JEDEC 2S2P card, 50x50mm
4. 1.5 °C/W is the theoretical θ_{JB} using an infinite heat sink. The larger number applies to the module mounted on a 1.8mm thick, 2P card using 1oz. copper power planes, with an effective heat transfer area of 75mm^2.

Heat Sink Mounting Information (Ceramic Package Only)

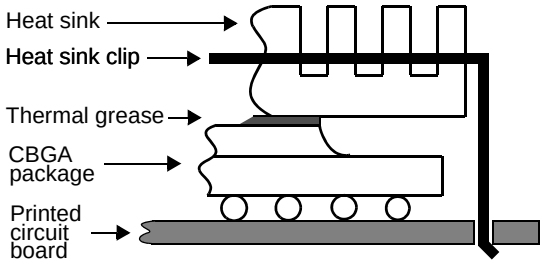
Proper thermal design is primarily dependent upon multiple system-level effects; that is, the effects of the heat sink, the air flow, and the thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods: adhesive, spring clips to the printed-circuit board or package, or a mounting clip and screw assembly. When attaching heat sinks, it is important to avoid placing excessive mechanical stress on bonding of the chip to the substrate and the package to the board.

Heat Sink Attached With Spring Clip



Spring clip to package

Static compression (spring force)—2.27kg maximum

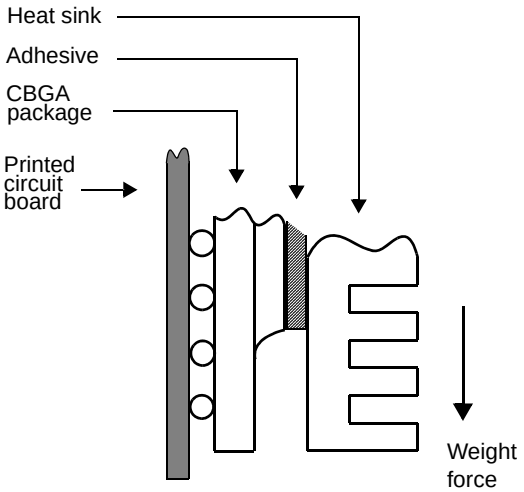


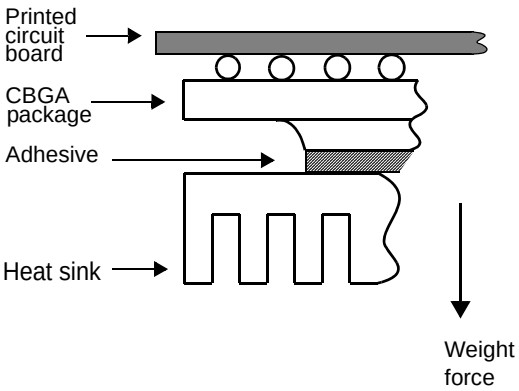
Spring clip to board

Static compression (spring force)—2.27kg maximum[1]

Note 1: Force is limited by allowable compression on the die. Allowable package compression force is 4.4kg.

Heat Sink Attached With Adhesive





Heat sink weight force—60g maximum

Important: All of the guidelines indicated in the above diagrams must be evaluated and adjusted to account for the shock and vibration effects of any particular application.

Recommended DC Operating Conditions

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage (500MHz Rev A and 533MHz)	V_{DD}	+1.4	+1.5	+1.6	V	4
Logic Supply Voltage (667MHz and 800MHz)	V_{DD}	+1.5	+1.55	+1.6	V	4
I/O Supply Voltage	OV_{DD}	+3.0	+3.3	+3.6	V	4
DDR SDRAM Supply Voltage (DDR clock up to 166MHz)	SV_{DD}	+2.3	+2.5	+2.7	V	4
DDR SDRAM Supply Voltage (DDR clock = 200MHz)	SV_{DD}	+2.5	+2.6	+2.7	V	4
PLL Supply Voltages (500MHz Rev A and 533MHz)	AxV_{DD}	+1.4	+1.5	+1.6	V	3
PLL Supply Voltage (667MHz and 800MHz)	AxV_{DD}	+1.5	+1.55	+1.6	V	3
DDR SDRAM Reference Voltage	SV_{REF}	+1.15	+1.25	+1.35	V	3
Input Logic High (2.5V SSTL)	V_{IH}	SV_{REF}+0.18		SV_{DD}+0.3	V	2
Input Logic High (2.5V CMOS, 3.3V tolerant receiver)		1.7			V	
Input Logic High (3.3V PCI-X)		$0.5OV_{DD}$		OV_{DD}+0.5	V	1
Input Logic High (3.3V LVTTL)		+2.0		+3.6	V	
Input Logic Low (2.5V SSTL)	V_{IL}	-0.3		SV_{REF}-0.18	V	
Input Logic Low (2.5V CMOS, 3.3V tolerant receiver)				0.7	V	
Input Logic Low (3.3V PCI-X)		-0.5		$0.35OV_{DD}$	V	1
Input Logic Low (3.3V LVTTL)		0		+0.8	V	
Output Logic High (2.5V SSTL)	V_{OH}	+1.95		SV_{DD}	V	
Output Logic High (2.5V CMOS, 3.3V tolerant receiver)		2.0			V	
Output Logic High (3.3V PCI-X)		$0.9OV_{DD}$		OV_{DD}	V	1
Output Logic High (3.3V LVTTL)		+2.4		OV_{DD}	V	
Output Logic Low (2.5V SSTL)	V_{OL}	0		0.55	V	
Output Logic Low (2.5V CMOS, 3.3V tolerant receiver)				0.4	V	
Output Logic Low (3.3V PCI-X)				$0.1OV_{DD}$	V	1
Output Logic Low (3.3V LVTTL)		0		+0.4	V	
Input Leakage Current (No pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current for Pull-Down	I_{IL2}	0 (LPDL)		200 (MPUL)	µA	5
Input Leakage Current for Pull-Up	I_{IL3}	-150 (LPDL)		0 (MPUL)	µA	5
Input Max Allowable Overshoot (3.3V LVTTL)	V_{IMAO}			+3.9	V	
Input Max Allowable Undershoot (3.3V LVTTL)	V_{IMAU}	-0.6			V	

Recommended DC Operating Conditions (Continued)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Output Max Allowable Overshoot (3.3V LVTTL)	V_{OMAO}			+3.9	V	
Output Max Allowable Undershoot (3.3V LVTTL)	V_{OMAU3}	-0.6			V	
Case Temperature rating for C package and S package	T_C	-40		+85	°C	6
Case Temperature rating E for C package	T_C	-40		+105	°C	6
Case Temperature rating E for F package	T_C	-40		+100	°C	6

Notes:

1. PCI-X drivers meet PCI-X specifications.
2. $SV_{REF} = SV_{DD}/2$
3. The analog voltages used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440GX. See “Absolute Maximum Ratings” on page 58.
4. There are no OV_{DD}, V_{DD}, or SV_{DD} power supply power-up sequence requirements. However, external voltage should not be applied to the chip I/O pins before OV_{DD} is applied to the chip. A power-down cycle should complete (OV_{DD} and V_{DD} should both be below 0.4V) before a new power- up cycle is started.
5. LPDL is least positive down level; MPUL is most positive up level.
6. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.

Input Capacitance

Parameter	Symbol	Maximum	Unit	Notes
Group 1 (2.5V SSTL I/O)	C_{IN1}	12	pF	
Group 2 (3.3V LVTTL I/O)	C_{IN2}	12	pF	
Group 3 (PCI-X I/O)	C_{IN3}	12	pF	
Group 4 (Receivers)	C_{IN4}	9	pF	
Group 5 (3.3V tolerant CMOS I/O)	C_{IN5}	16	pF	

DC Power Supply Loads

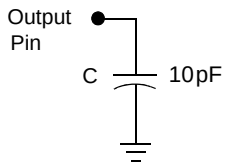
Parameter	Symbol	Frequency (MHz)	Typical	Maximum	Unit	Notes
V_{DD} active operating current	I_{DD}	533	1.37	1.69	A	2
		667	1.49	1.8	A	2
		800	1.77	2.2	A	2, 3
OV_{DD} active operating current	I_{ODD}	533	58	111	mA	2
		667	58	111	mA	2
		800	58	111	mA	2, 3
SV_{DD} active operating current	I_{SDD}	533	544	749	mA	2
		667	568	837	mA	2
		800	680	940	mA	2, 3
AxV_{DD} input current	I_{ADD}		33		mA	1, 2

Notes:

1. See “Absolute Maximum Ratings” on page 58 for filter recommendations.
2. The maximum current values listed above are not guaranteed to be the highest obtainable. These values are dependent on many factors including the type of applications running, clock rates, use of internal functional capabilities, external interface usage, case temperature, and the power supply voltages. Your specific application can produce significantly different results. V_{DD} (logic) current and power are primarily dependent on the applications running and the use of internal chip functions (DMA, PCI, Ethernet, and so on). OV_{DD} (I/O) current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses. The following information provides details about the conditions under which the listed values were obtained:
   a. In general, the values are measured using a PPC440GX Evaluation Board set for Ethernet mode 4, PCI-X running at 100MHz with an Intel Pro 1000, an Agilent Test card, an EBMI test card, a UART wrap plug, and one 128MB Micron DIMM while running applications designed to maximize CPU power consumption. An external PCI master heavily loads the PCI bus with transfers targeting SDRAM, while the internal DMA controller further increases SDRAM bus traffic.
   System clock rates are set as follows: SysClk = 33MHz, CPU = 667MHz, PLB = 167MHz, and OPB = EBC = 83MHz.
   b. Typical current is characterized at V_{DD} = +1.5V, OV_{DD} = +3.3V, SV_{DD} = +2.5V, and T_C = +47°C.
   c. Maximum current is characterized at V_{DD} = +1.6V, OV_{DD} = +3.6V, SV_{DD} = +2.7V, and T_C = +85°C.
3. Estimated values.

Test Conditions

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized with V_{DD} = 1.5V, T_C = +85 °C and a 10pF test load as shown in the figure to the right.



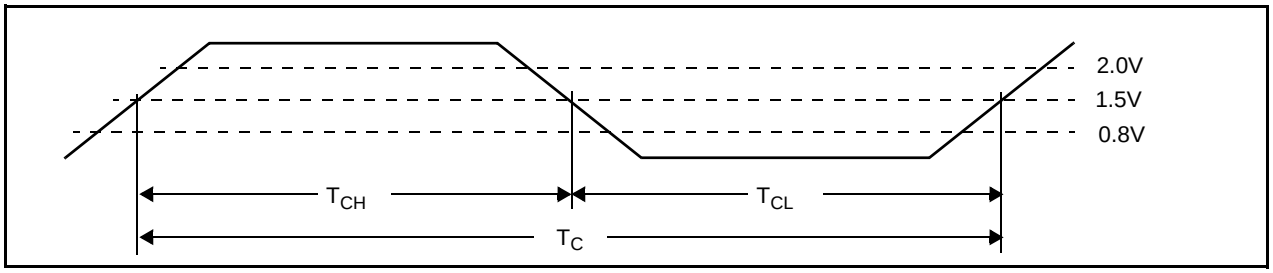
Clocking Specifications

Symbol	Parameter	Minimum	Maximum	Units	Notes
SysClk Input					
F_C	Frequency	33.33	83.33	MHz	
T_C	Period	12	30	ns	
T_{CS}	Edge stability (cycle-to-cycle jitter)	–	±0.15	ns	
T_{CH}	High time	40% of nominal period	60% of nominal period	ns	
T_{CL}	Low time	40% of nominal period	60% of nominal period	ns	
Note: Input slew rate ≥ 1 V/ns					
PLL VCO					
F_C	Frequency	600	1334	MHz	
T_C	Period	0.75	1.66	ns	
Processor Clock (CPU Clock)					
F_C	Frequency	333	800	MHz	1
T_C	Period	1.25	3	ns	
MemClkOut					
F_C	Frequency—533, 667, 800 MHz Rev C Frequency—800 MHz Rev F	100 100	166.66 200	MHz	
T_C	Period—533, 667, 800 MHz Rev C Period—800 MHz Rev F	6 5	10 10	ns	
T_{CH}	High time	45% of nominal period	55% of nominal period	ns	
OPB Clock					
F_C	Frequency	33.33	83.33	MHz	
T_C	Period	12	30	ns	
MAL Clock					
F_C	Frequency	45	83.33	MHz	
T_C	Period	12	22.22	ns	

Notes:

1. The maximum supported processor clock frequency for any part is specified in the part number (see “Ordering and PVR Information” on page 4).

Timing Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC440GX. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC440GX the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC440GX with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40kHz. In some cases, on-board PPC440GX peripherals impose more stringent requirements.
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the DDR SDRAM MemClkOut since it also tracks the modulation.
- For PCI-X and PCI 66 the maximum spread spectrum is -1% modulated between 30kHz and 33kHz.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates.
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.

Important: It is up to the system designer to ensure that any SSCG used with the PPC440GX meets the above requirements and does not adversely affect other aspects of the system.

Peripheral Interface Clock Timings

Parameter	Min	Max	Units	Notes
PCIXClk input frequency (asynchronous mode)	–	133.33	MHz	2
PCIXClk period (asynchronous mode)	7.5	–	ns	
PCIXClk input high time	40% of nominal period	60% of nominal period	ns	
PCIXClk input low time	40% of nominal period	60% of nominal period	ns	
EMCMDClk output frequency	–	2.5	MHz	
EMCMDClk period	400	–	ns	
EMCMDClk output high time	160	–	ns	
EMCMDClk output low time	160	–	ns	
EMCTxClk input frequency MII(RMII)	2.5(5)	25(50)	MHz	
EMCTxClk period MII(RMII)	40(20)	400(200)	ns	
EMCTxClk input high time	35% of nominal period	–	ns	
EMCTxClk input low time	35% of nominal period	–	ns	
EMCRxClk input frequency MII(RMII)	2.5(5)	25(50)	MHz	
EMCRxClk period MII(RMII)	40(20)	400(200)	ns	
EMCRxClk input high time	35% of nominal period	–	ns	
EMCRxClk input low time	35% of nominal period	–	ns	
GMCRefClk input frequency	–	125	MHz	
GMCRefClk period	8		ns	
GMCRefClk input high time	47% of nominal period	53% of nominal period	ns	
GMCRefClk input low time	47% of nominal period	53% of nominal period	ns	
PerClk output frequency (for ext. master or sync. slaves)	33.33	83.33	MHz	
PerClk period	12	30	ns	
PerClk output high time	50% of nominal period	66% of nominal period	ns	
PerClk output low time	33% of nominal period	50% of nominal period	ns	
UARTSerClk input frequency	–	$1000/(2T_{OPB}$[1]$+2ns)$	MHz	1
UARTSerClk period	$2T_{OPB}+2$	–	ns	1
UARTSerClk input high time	$T_{OPB}+1$	–	ns	1
UARTSerClk input low time	$T_{OPB}+1$	–	ns	1

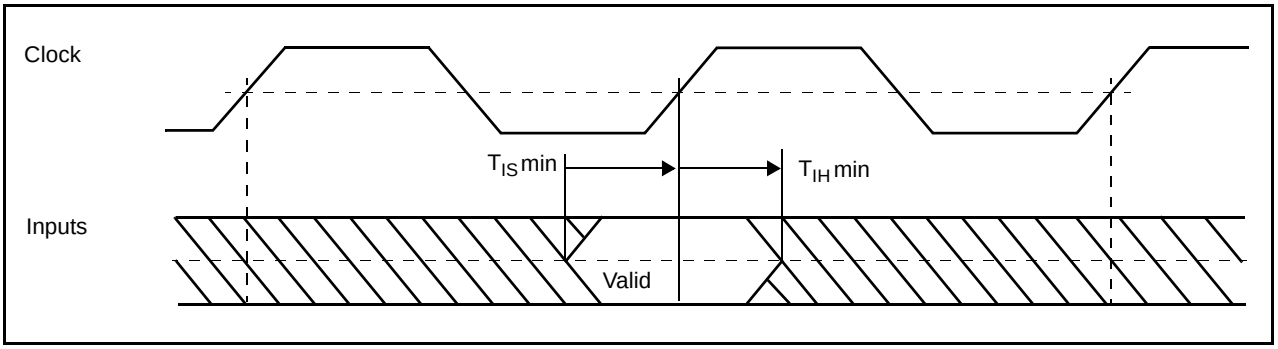
Peripheral Interface Clock Timings (Continued)

Parameter	Min	Max	Units	Notes
TmrClk input frequency	–	100	MHz	
TmrClk period	10	–	ns	
TmrClk input high time	40% of nominal period	60% of nominal period	ns	
TmrClk input low time	40% of nominal period	60% of nominal period	ns	

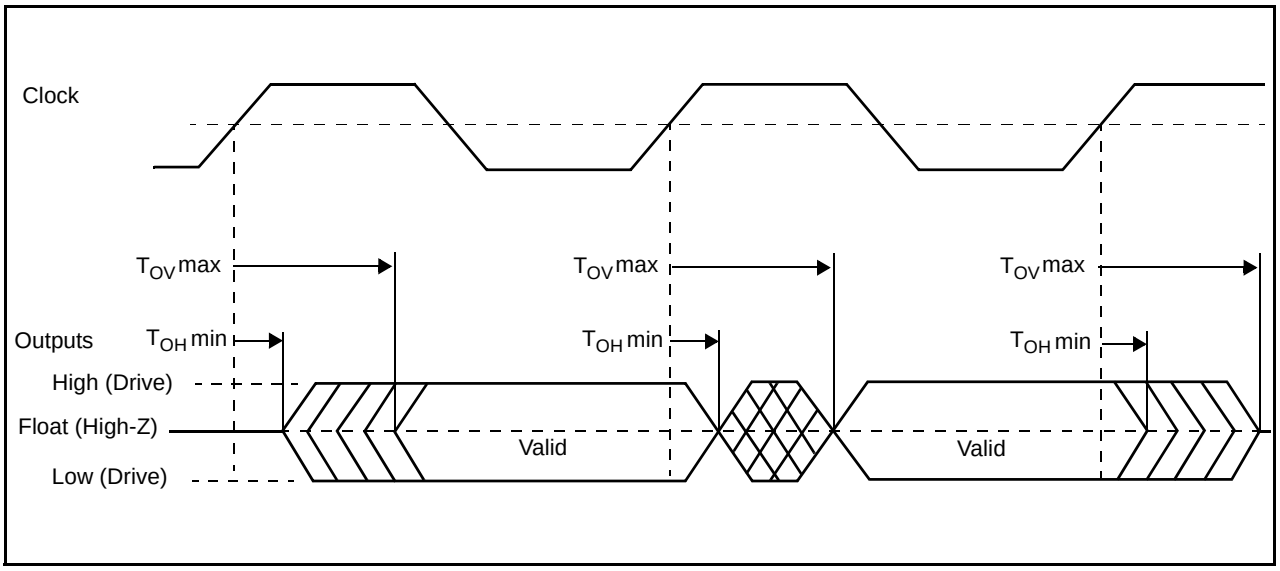
Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at an integral divisor ratio of the frequency of the PLB clock. The maximum OPB clock frequency is 83.33 MHz. Refer to the Clocking chapter of the *PPC440GX Embedded Processor User's Manual* for details.
2. When the PCI-X interface is used to support a legacy PCI interface, the maximum PCIXClk frequency is 66.66 MHz.

Input Setup and Hold Waveform



Output Delay and Float Timing Waveform



I/O Specifications—All Speeds (Sheet 1 of 7)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
3. The clock frequency for RMII operation is 50MHz ± 100ppm.
4. The clock frequency for SMII operation is 125MHz ± 100ppm.
5. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
PCI-X Interface								
PCIXAD00:63	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIXC3:0[$\overline{\text{BE3:0}}$]	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIXParLow	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIParHigh	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXFrame}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXINT}}$	na	na	dc	dc	0.5	1.5	PCIXClk	async
$\overline{\text{PCIXIRDY}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXTRDY}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXStop}}$	Note 2 (3	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXDevSel}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIXIDSel	Note 2 (3)	0.5 (0)	na	na	na	na	PCIXClk	2
$\overline{\text{PCIXPErr}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXSErr}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIXClk	dc	dc	na	na	na	na		async
$\overline{\text{PCIXReset}}$	na	na	na	na	na	na	PCIXClk	
$\overline{\text{PCIXReq64}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
$\overline{\text{PCIXAck64}}$	Note 2 (3)	0.5 (0)	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2
PCIXCap	Note 2 (3)	0.5 (0)	na	na	na	na	PCIXClk	2
PCIX133Cap			3.8	0.7	0.5	1.5	PCIXClk	2
PCIXM66En	Note 2 (3)	0.5 (0)	na	na	na	na	PCIXClk	2
$\overline{\text{PCIXReq0:5}}$	Note 2 (3)	0.5 (0)	na	na	na	na	PCIXClk	2
$\overline{\text{PCIXGnt0:5}}$	na)	na	3.8 (6)	0.7 (Note 2)	0.5	1.5	PCIXClk	2

I/O Specifications—All Speeds (Sheet 2 of 7)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
3. The clock frequency for RMII operation is 50MHz ± 100ppm.
4. The clock frequency for SMII operation is 125MHz ± 100ppm.
5. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
Ethernet MII Interface								
EMCRxD0:3	4	1	na	na	5.1	6.8	EMCRxClk	1
EMCRxDV	4	1	na	na	5.1	6.8	EMCRxClk	1
EMCRxClk	na	na	na	na	5.1	6.8		1, async
EMCRxErr	4	1	na	na	5.1	6.8	EMCRxClk	1
EMCTxD0:3	na	na	15	2	5.1	6.8	EMCTxClk	1
EMCTxEn	na	na	15	2	5.1	6.8	EMCTxClk	1
EMCTxClk	na	na	na	na	na	na		1, async
EMCTxErr	na	na	15	2	5.1	6.8	EMCTxClk	1
EMCCrS			na	na	5.1	6.8		1, async
EMCCD			na	na	5.1	6.8		1, async
EMCMDIO					5.1	6.8	EMCMDClk	1
EMCMDClk	na	na	na	na	5.1	6.8		1, async
Ethernet RMII Interface								
EMC0RxD0:1	2	1	na	na	5.1	6.8	EMCRefClk	
EMC0RxErr	2	1	na	na	5.1	6.8	EMCRefClk	
EMC0CrSDV			na	na	5.1	6.8	EMCRefClk	
EMC0TxD0:1	na	na	11	2	5.1	6.8	EMCRefClk	
EMC0:1TxEn	na	na	11	2	5.1	6.8	EMCRefClk	
EMC1RxD0:1			na	na	5.1	6.8	EMCRefClk	
EMC1RxErr			na	na	5.1	6.8	EMCRefClk	
EMC1CrSDV			na	na	5.1	6.8	EMCRefClk	
EMC1TxD0:1	na	na	11	2	5.1	6.8	EMCRefClk	
EMCRefClk	na	na	na	na	na	na		3, async

I/O Specifications—All Speeds (Sheet 3 of 7)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
3. The clock frequency for RMII operation is 50MHz ± 100ppm.
4. The clock frequency for SMII operation is 125MHz ± 100ppm.
5. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
Ethernet SMII Interface								
EMC0:1RxD	0.8	0.8	na	na	5.1	6.8	EMCRefClk	
EMC2:3RxD	0.8	0.8	na	na	5.1	6.8	EMCRefClk	
EMC0:1TxD	na	na	3.5	2	5.1	6.8	EMCRefClk	
EMC2:3TxD	na	na	3.5	2	5.1	6.8	EMCRefClk	
EMCRefClk	na	na	na	na	na	na		4, async
Ethernet GMII Interface								
GMCRxClk	na	na	na	na	na	na		1, async
GMCRxD0:7	2	0	na	na	5.1	6.8	GMCRxClk	
GMCRxEr	2	0	na	na	5.1	6.8	GMCRxClk	
GMCRxDV	2	0	na	na	5.1	6.8	GMCRxClk	
GMCCrS			na	na	5.1	6.8		1, async
GMCol			na	na	5.1	6.8		1, async
GMCGTxClk	na	na	na	na	na	na		1, async
GMCTxD0:7	na	na	5.5	0.5	5.1	6.8	GMCGTxClk	
GMCTxEr	na	na	5.5	0.5	5.1	6.8	GMCGTxClk	
GMCTxEn	na	na	5.5	0.5	5.1	6.8	GMCGTxClk	

I/O Specifications—All Speeds (Sheet 4 of 7)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
3. The clock frequency for RMII operation is 50MHz ± 100ppm.
4. The clock frequency for SMII operation is 125MHz ± 100ppm.
5. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
Ethernet RGMII Interface								
GMC0RxClk	na	na	na	na	na	na		1, async
GMC0RxCtl	1	1	na	na	na	na	GMC0RxClk	4, 5
GMC0RxD0:3	1	1	na	na	5.1	6.8	GMC0RxClk	4, 5
GMC0TxClk	na	na	na	na	5.1	6.8		1, async
GMC0TxCtl	na	na	0.5	3.5	5.1	6.8	GMC0TxClk	4, 5
GMC0TxD0:3	na	na	0.5	3.5	5.1	6.8	GMC0TxClk	4, 5
GMC1RxClk	na	na	na	na	na	na		1, async
GMC1RxCtl	1	1	na	na	na	na	GMC1RxClk	4, 5
GMC1RxD0:3	1	1	na	na	5.1	6.8	GMC1RxClk	4, 5
GMC1TxClk	na	na	na	na	5.1	6.8		1, async
GMC1TxCtl	na	na	0.5	3.5	5.1	6.8	GMC1TxClk	4, 5
GMC1TxD0:3	na	na	0.5	3.5	5.1	6.8	GMC1TxClk	4, 5
GMCRefClk	na	na	na	na	na	na		async
Ethernet TBI Interface								
TBIRxClk0	na	na	na	na	na	na		1, async
TBIRxClk1	na	na	na	na	na	na		1, async
TBIRxD0:9	2.5	1.5	na	na	5.1	6.8	TBIRxClkx	
TBITxClk	na	na	na	na	na	na		1, async
TBITxD0:9	na	na	6	1	5.1	6.8	TBITxClk	

I/O Specifications—All Speeds (Sheet 5 of 7)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
3. The clock frequency for RMII operation is 50MHz ± 100ppm.
4. The clock frequency for SMII operation is 125MHz ± 100ppm.
5. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
Ethernet RTBI Interface								
RTBI0RxClk	na	na	na	na	na	na		1, async
RTBI0RxD0:4	1	1	na	na	5.1	6.8	RTBI0RxClk	
RTBI0TxClk	na	na	na	na	5.1	6.8		1, async
RTBI0TxD0:4	na	na	3.5	5.1	5.1	6.8	RTBI0TxClk	
RTBI1RxClk	na	na	na	na	na	na		1, async
RTBI1RxD0:4	1	1	na	na	5.1	6.8	RTBI1RxClk	
RTBI1TxClk	na	na	na	na	5.1	6.8		1, async
RTBI1TxD0:4	na	na	3.5	5.1	5.1	6.8	RTBI1TxClk	
GMCRefClk	na	na	na	na	na	na		async

I/O Specifications—All Speeds (Sheet 6 of 7)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
3. The clock frequency for RMII operation is 50MHz ± 100ppm.
4. The clock frequency for SMII operation is 125MHz ± 100ppm.
5. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
Internal Peripheral Interface								
IIC0SClk	na	na	na	na	15.3	10.2		
IIC0SDA					15.3	10.2		
IIC1SClk	na	na	na	na	15.3	10.2		
IIC1SDA					15.3	10.2		
UARTSerClk	na	na	na	na	na	na		
UART0_Rx			na	na	na	na		
UART0_Tx	na	na			10.3	7.1		
$\overline{\text{UART0\_DCD}}$			na	na	na	na		
$\overline{\text{UART0\_DSR}}$			na	na	na	na		
$\overline{\text{UART0\_CTS}}$			na	na	na	na		
$\overline{\text{UART0\_DTR}}$	na	na			10.3	7.1		
$\overline{\text{UART0\_RI}}$			na	na	na	na		
$\overline{\text{UART0\_RTS}}$	na	na			10.3	7.1		
UART1_Rx			na	na	na	na		
UART1_Tx	na	na			10.3	7.1		
$\overline{\text{UART1\_DSR/CTS}}$			na	na	na	na		
$\overline{\text{UART1\_RTS/DTR}}$	na	na			10.3	7.1		
Interrupts Interface								
IRQ00:17					na	na		
JTAG Interface								
TDI					na	na		async
TMS					na	na		async
TDO					15.3	10.2		async
TCK					na	na		async
$\overline{\text{TRST}}$					na	na		async

I/O Specifications—All Speeds (Sheet 7 of 7)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
3. The clock frequency for RMII operation is 50MHz ± 100ppm.
4. The clock frequency for SMII operation is 125MHz ± 100ppm.
5. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
System Interface								
SysClk			na	na	na	na		
TmrClk			na	na	na	na		async
$\overline{\text{SysReset}}$					na	na		async
$\overline{\text{Halt}}$			na	na	na	na		async
SysErr	na	na			10.3	7.1		async
$\overline{\text{TestEn}}$			na	na	na	na		async
DrvrInh2			na	na	na	na		
GPIO00:31					10.3	7.1		
Trace Interface								
TrcClk	na	na			10.3	7.1		
TrcBS0:2					10.3	7.1		
TrcES0:4					10.3	7.1		
TrcTS0:5 (GPIO set)					10.3	7.1		
TrcTS1:5 (EBC set)					15.3	10.2		
TrcTS6					15.3	10.2		

I/O Specifications—500 MHz–800 MHz

Notes:

1. PerClk rising edge at package pin with a 10 pF load trails the internal PLB clock by approximately 1.3 ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
External Slave Peripheral Interface								
PerData00:31	2.8	1	6.6	0	15.3	10.2	PerClk	
PerAddr00:31	2.9	1	6.6	0	15.3	10.2	PerClk	
PerPar0:3	2.7	1	6.0	0	15.3	10.2	PerClk	
$\overline{\text{PerWBE0:3}}$	1.8	1	5.1	0	15.3	10.2	PerClk	
$\overline{\text{PerCS0:7}}$	na	na	5.8	0	15.3	10.2	PerClk	
$\overline{\text{PerOE}}$	na	na	5.5	0	15.3	10.2	PerClk	
$\overline{\text{PerWE}}$	na	na	5.5	0	15.3	10.2		
$\overline{\text{PerBLast}}$	3.3	1	5.7	na	15.3	10.2	PerClk	
PerReady[RcvrInh]	4.9	1	na	na	na	na	PerClk	
PerR/$\overline{\text{W}}$	2.5	1	5.7	na	15.3	10.2	PerClk	
DMAReq0:3	dc	dc	na	na	na	na	PerClk	
DMAAck0:3	na	na	6.0	0	5.1	6.8	PerClk	
EOT0:3/TC0:3	dc	dc	6.3	0	15.3	10.2	PerClk	
External Master Peripheral Interface								
PerClk	na	na	na	na	15.3	10.2	PLB Clk	1
$\overline{\text{ExtReset}}$	na	na	6.7	0	15.3	10.2	PerClk	
HoldReq	2.8	1	na	na	na	na	PerClk	
HoldAck	na	na	5.5	0	15.3	10.2	PerClk	
$\overline{\text{ExtReq}}$	1.5	1	na	na	na	na	PerClk	
$\overline{\text{ExtAck}}$	na	na	5.7	0	15.3	10.2	PerClk	
BusReq	na	na	5.7	0	15.3	10.2	PerClk	
PerErr	2.5	1	na	na	15.3	10.2	PerClk	

DDR SDRAM I/O Specifications

The DDR SDRAM controller times its operation with internal PLB clock signals and generates MemClkOut0 from the PLB clock. The PLB clock is an internal signal that cannot be directly observed. However MemClkOut0 is the same frequency as the PLB clock signal and is in phase with the PLB clock signal.

Note: MemClkOut0 can be advanced with respect to the PLB clock by means of the SDRAM0_CLKTR programming register. In a typical system, users advance MemClkOut by 90°. This depends on the specific application and requires a thorough understanding of the memory system in general (refer to the DDR SDRAM controller chapter in the *PowerPC 440GX User's Manual*).

In the following sections, the label MemClkOut0(0) refers to MemClkOut0 when it has not been phase-shifted, and MemClkOut0(90) refers to MemClkOut0 when it has been phase-advanced 90°. Advancing MemClkOut0 by 90° creates a 3/4 cycle setup time and 1/4 cycle hold time for the address and control signals in relation to MemClkOut0(90). The rising edge of MemClkOut0(90) aligns with the first rising edge of the DQS signal.

The following DDR data is generated by means of simulation and includes logic, driver, package RLC, and lengths. Values are calculated over best case and worst case processes with speed, temperature, and voltage as follows:

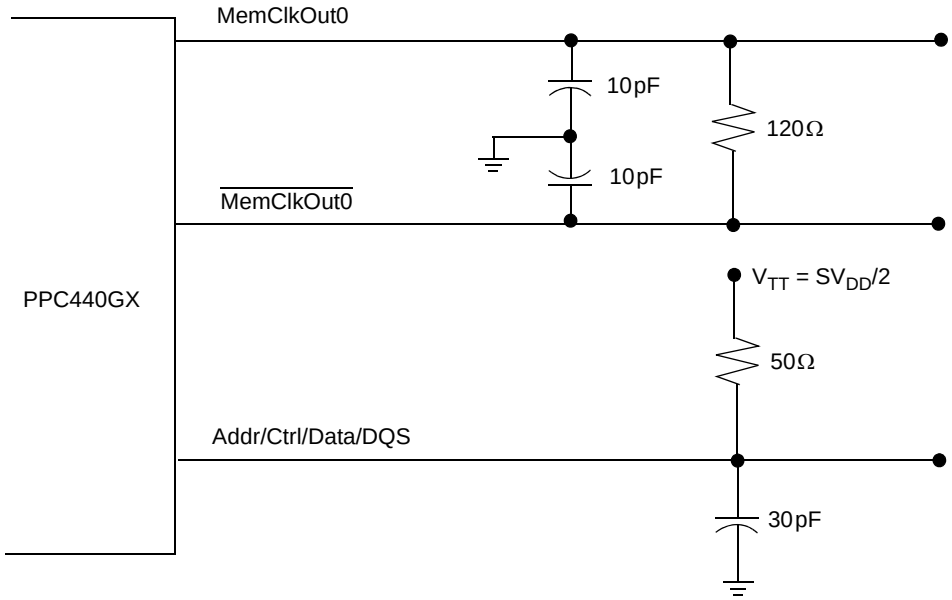
Best Case = Fast process, -40°C, +1.6V

Worst Case = Slow process, +85°C, +1.4V

Note: In all the following DDR tables and timing diagrams, *minimum* values are measured under *best* case conditions and *maximum* values are measured under *worst* case conditions.

The signals are terminated as indicated in the figure below for the DDR timing data in the following sections.

DDR SDRAM Simulation Signal Termination Model



Note: This diagram illustrates the model of the DDR SDRAM interface used when generating simulation timing data. It is *not* a recommended physical circuit design for this interface. An actual interface design will depend on many factors, including the type of memory used and the board layout.

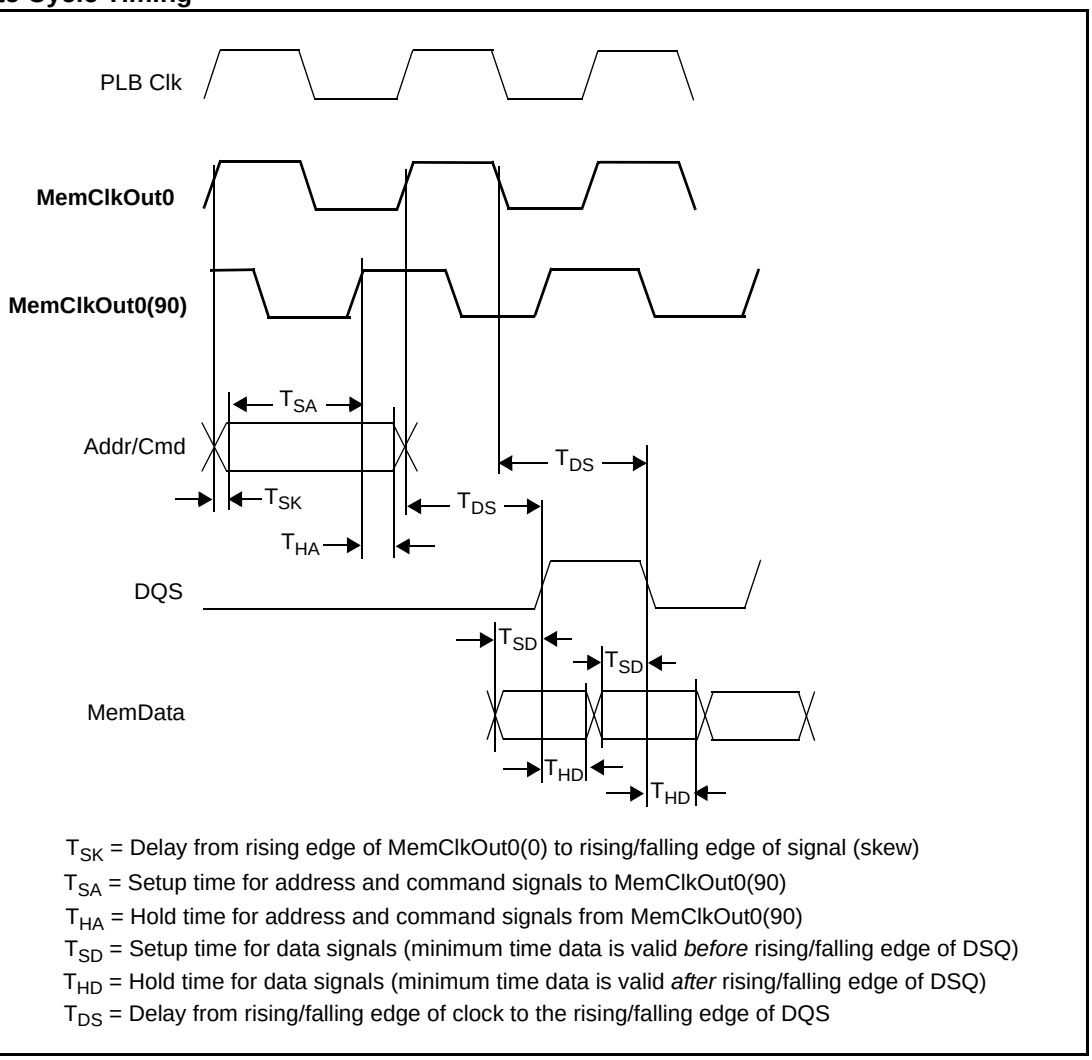
DDR SDRAM Output Driver Specifications

Signal Path	Output Current (mA)	
	I/O H (maximum)	I/O L (minimum)
Write Data		
MemData00:07	15.2	15.2
MemData08:15	15.2	15.2
MemData16:23	15.2	15.2
MemData24:31	15.2	15.2
MemData32:39	15.2	15.2
MemData40:47	15.2	15.2
MemData48:55	15.2	15.2
MemData56:63	15.2	15.2
ECC0:7	15.2	15.2
DM0:8	15.2	15.2
MemClkOut0	15.2	15.2
MemAddr00:12	15.2	15.2
BA0:1	15.2	15.2
$\overline{\text{RAS}}$	15.2	15.2
$\overline{\text{CAS}}$	15.2	15.2
$\overline{\text{WE}}$	15.2	15.2
$\overline{\text{BankSel0:3}}$	15.2	15.2
ClkEn0:3	15.2	15.2
DQS0:8	15.2	15.2

DDR SDRAM Write Operation

The following diagram illustrates the relationship among the signals involved with a DDR write operation.

DDR SDRAM Write Cycle Timing



T_{SK} = Delay from rising edge of MemClkOut0(0) to rising/falling edge of signal (skew)
T_{SA} = Setup time for address and command signals to MemClkOut0(90)
T_{HA} = Hold time for address and command signals from MemClkOut0(90)
T_{SD} = Setup time for data signals (minimum time data is valid *before* rising/falling edge of DSQ)
T_{HD} = Hold time for data signals (minimum time data is valid *after* rising/falling edge of DSQ)
T_{DS} = Delay from rising/falling edge of clock to the rising/falling edge of DQS

I/O Timing—DDR SDRAM T_{DS}

Notes:

1. All of the DQS signals are referenced to MemClkOut0(0).
2. The T_{DS} values in the table include 3/4 of a cycle at the indicated clock speed.
3. To obtain adjusted values for lower clock frequencies, subtract 4.5 ns from the 166 MHz values in the table and add 3/4 of the cycle time for the lower clock frequency (T_{DS} - 4.5 + 0.75T_{CYC}).

Clock Speed (MHz)	Signal Name	T_{DS} (ns)	
		Minimum	Maximum
166	DQS0	4.902	5.601
166	DQS1	4.872	5.535
166	DQS2	4.842	5.511
166	DQS3	4.855	5.546
166	DQS4	4.832	5.504
166	DQS5	4.867	5.525
166	DQS6	4.825	5.488
166	DQS7	4.880	5.543
166	DQS8	4.826	5.484
200	DQS0	3.660	4.295
200	DQS1	3.672	4.298
200	DQS2	3.664	4.293
200	DQS3	3.660	4.290
200	DQS4	3.671	4.294
200	DQS5	3.666	4.305
200	DQS6	3.666	4.296
200	DQS7	3.658	4.271
200	DQS8	3.662	4.291

I/O Timing—DDR SDRAM T_{SK}, T_{SA}, and T_{HA}

Notes:

1. T_{SK} is referenced to MemClkOut0(0). T_{SA} and T_{HA} are referenced to MemClkOut0(90).
2. To obtain adjusted T_{SA} values for lower clock frequencies, use 3/4 of the cycle time for the lower clock frequency and subtract T_{SK} maximum at 166 MHz ($0.75T_{CYC}$ - T_{SK}max).
3. To obtain adjusted T_{HA} values for lower clock frequencies, use 1/4 of the cycle time for the lower clock frequency and add T_{SK} minimum at 166 MHz ($0.25T_{CYC}$ + T_{SK}min).

Clock Speed (MHz)	Signal Name	T_{SK} (ns)		T_{SA} (ns)	T_{HA} (ns)
		Minimum	Maximum	Minimum	Minimum
166	MemAddr00:12	0.184	0.592	3.908	1.684
166	BA0:1	0.439	0.683	3.817	1.939
166	BankSel0:3	0.249	0.779	3.721	1.749
166	ClkEn0:3	0.344	0.724	3.776	1.844
166	$\overline{\text{CAS}}$	0.319	0.561	3.939	1.819
166	$\overline{\text{RAS}}$	0.373	0.683	3.817	1.873
166	$\overline{\text{WE}}$	0.393	0.639	3.816	1.893
200	MemAddr00:12	-0.283	0.307	3.443	0.967
200	BA0:1	-0.286	0.353	3.397	0.964
200	BankSel0:3	-0.270	0.321	3.429	0.980
200	ClkEn0:3	-0.280	0.298	3.452	0.970
200	$\overline{\text{CAS}}$	-0.270	0.294	3.456	0.980
200	$\overline{\text{RAS}}$	-0.263	0.311	3.439	0.987
200	$\overline{\text{WE}}$	-0.280	0.288	3.462	0.970

I/O Timing—DDR SDRAM T_{SD} and T_{HD}

Notes:

1. T_{SD} and T_{HD} are measured under worst case conditions.
2. The time values in the table include 1/4 of a cycle at the indicated clock speed.
3. To obtain adjusted T_{SD} and T_{HD} values for lower clock frequencies, subtract 1.5 ns from the values at 166 MHz in the table and add 1/4 of the cycle time for the lower clock frequency (e.g., T_{SD} - 1.5 + 0.25T_{CYC}).

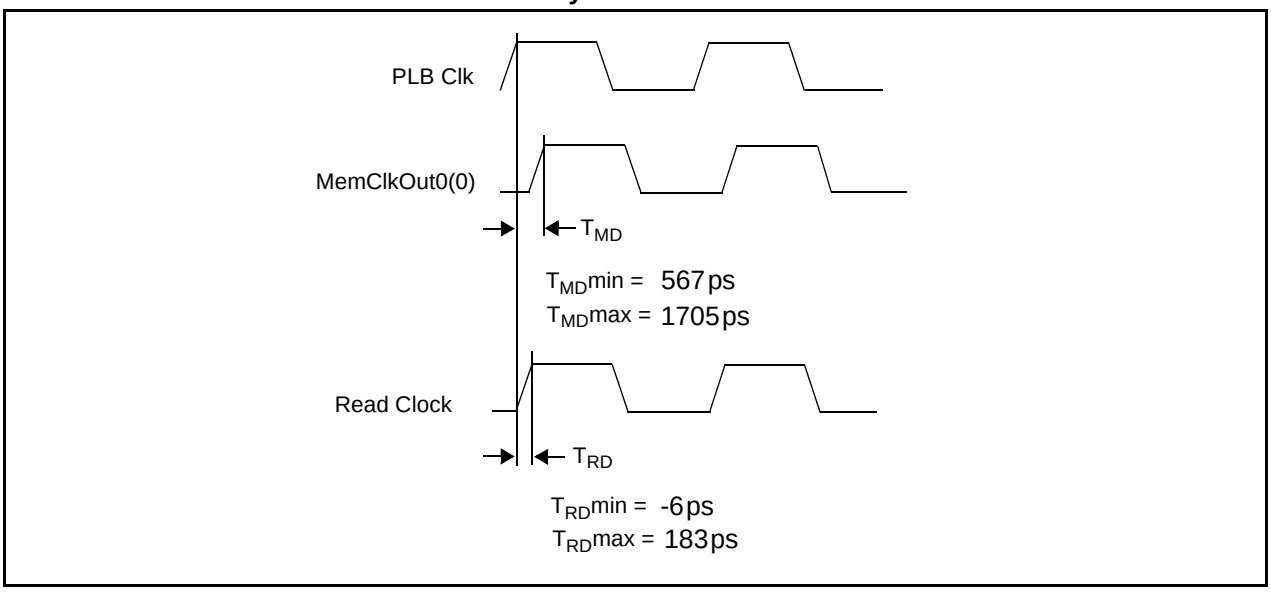
Clock Speed (MHz)	Signal Names	Reference Signal	T_{SD} (ns)	T_{HD} (ns)
166	MemData00:07, DM0	DQS0	1.240	1.224
166	MemData08:15, DM1	DQS1	1.236	1.188
166	MemData16:23, DM2	DQS2	1.223	1.224
166	MemData24:31, DM3	DQS3	1.221	1.185
166	MemData32:39, DM4	DQS4	1.238	1.230
166	MemData40:47, DM5	DQS5	1.286	1.175
166	MemData48:55, DM6	DQS6	1.234	1.214
166	MemData56:63, DM7	DQS7	1.257	1.154
166	ECC0:7, DM8	DQS8	1.237	1.243
200	MemData00:07, DM0	DQS0	0.916	0.542
200	MemData08:15, DM1	DQS1	1.018	0.522
200	MemData16:23, DM2	DQS2	1.017	0.527
200	MemData24:31, DM3	DQS3	0.951	0.532
200	MemData32:39, DM4	DQS4	1.030	0.533
200	MemData40:47, DM5	DQS5	1.014	0.536
200	MemData48:55, DM6	DQS6	0.994	0.534
200	MemData56:63, DM7	DQS7	0.994	0.546
200	ECC0:7, DM8	DQS8	1.000	0.532

DDR SDRAM Read Operation

The following examples of timing for DDR SDRAM read operations are based on the relationship between the incoming data and the PLB clock signal. Since the PLB clock cannot be directly observed, the delay of MemClkOut(0) relative to the PLB clock (T_{MD}) is provided.

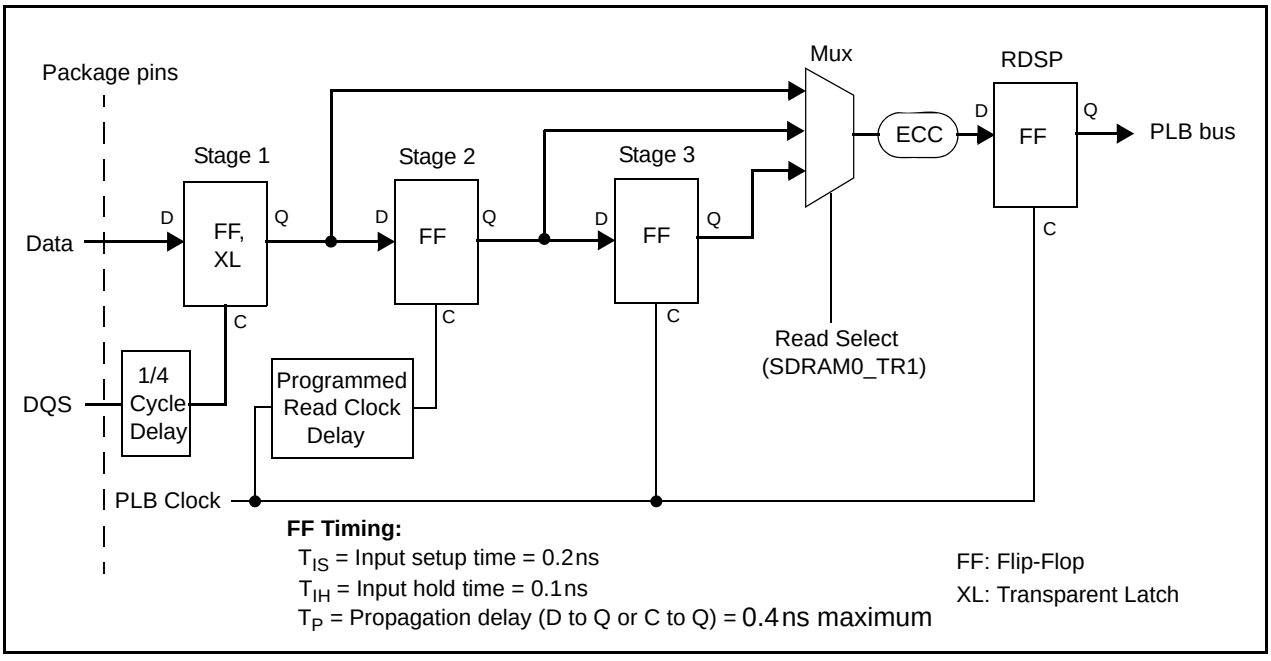
The internal Read Clock signal, like MemClkOut0, is derived from the PLB clock and can be delayed relative to the PLB clock by programming the RDCT and RDCD fields in the SDRAM0_TR1 register. The delay can be programmed from 0 to 1/2 cycle in steps using RDCT. Setting RDCD results in a 1/2 cycle delay plus the value set in RDCT. The delay of Read Clock relative to the PLB clock (T_{RD}) shown below assumes the programmable Read Clock delay is set to zero.

DDR SDRAM MemClkOut0 and Read Clock Delay



In operation, following the receipt of an address and read command from the PPC440GX, the SDRAM generates data and the DQS signals coincident with MemClkOut0. The data is latched into the PPC440GX using a DQS signal that is delayed 1/4 of a cycle. In order to accommodate timing variations introduced by the system designs using this chip, the three-stage data path shown below is used to eliminate metastability and allow data sampling to be adjusted for minimum latency. This adjustment requires programming the Read Clock delay and the selection of Stage 1, Stage 2, or Stage 3 data for sampling at RDSP.

DDR SDRAM Read Data Path



I/O Timing—DDR SDRAM T_{SIN} and T_{DIN}

Notes:

1. T_{SIN} = Delay from DQS at package pin to C on Stage 1 FF.
2. T_{DIN} = Delay from data at package pin to D on Stage 1 FF.
3. The time values for T_{SIN} include 1/4 of a cycle at the indicated clock speed.

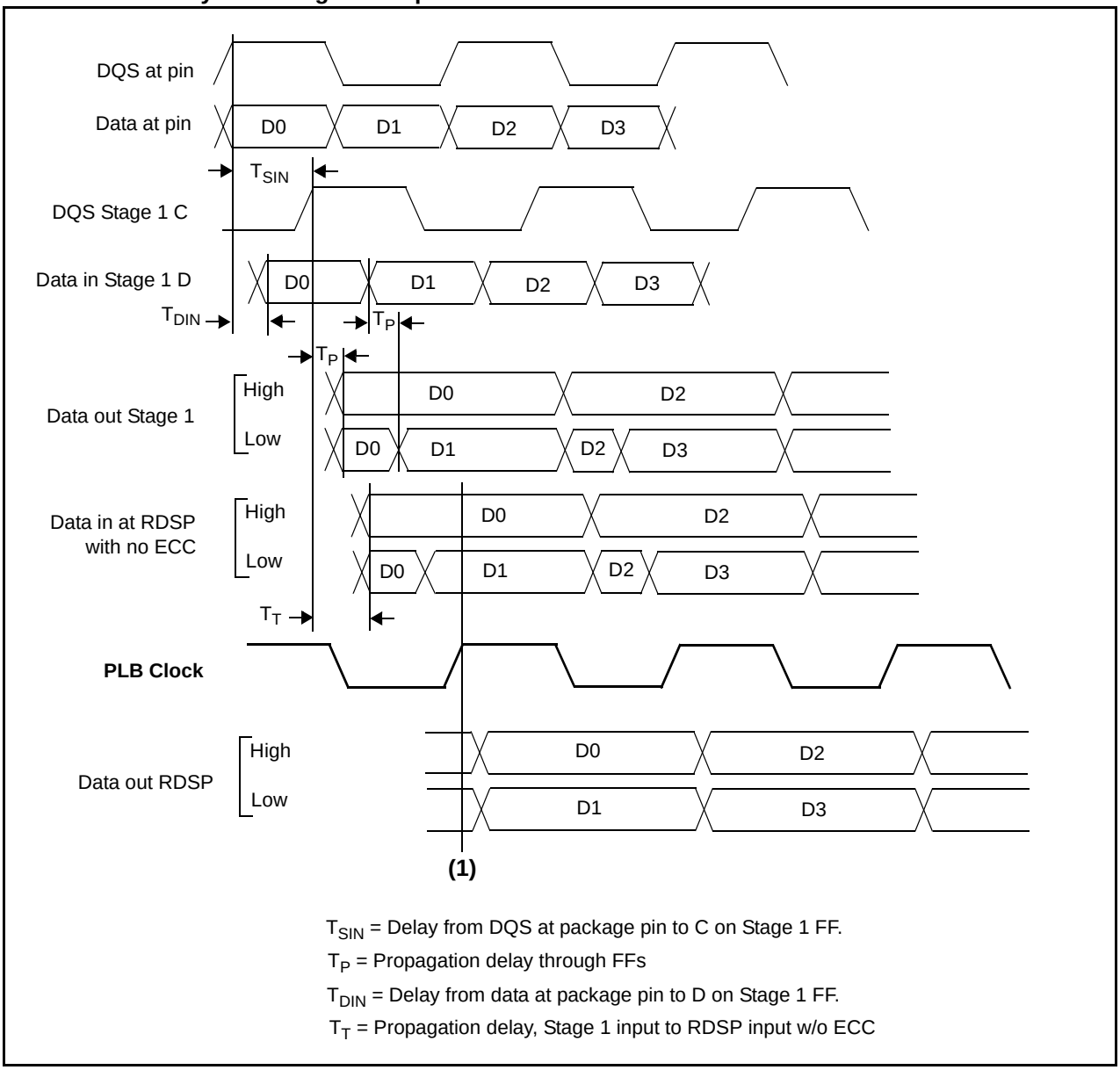
Clock Speed (MHz)	Signal Name	T_{SIN} (ns) minimum	T_{SIN} (ns) maximum	Signal Name	T_{DIN} (ns) minimum	T_{DIN} (ns) maximum
166	DQS0	2.132	2.884	MemData00:07	0.779	1.502
166	DQS1	2.132	2.867	MemData08:15	0.789	1.521
166	DQS2	2.127	2.873	MemData16:23	0.779	1.530
166	DQS3	2.116	2.851	MemData24:31	0.791	1.553
166	DQS4	2.100	2.845	MemData32:39	0.766	1.501
166	DQS5	2.103	2.844	MemData40:47	0.754	1.525
166	DQS6	2.144	2.902	MemData48:55	0.747	1.513
166	DQS7	2.110	2.864	MemData56:63	0.770	1.521
166	DQS8	2.122	2.860	ECC0:7	0.759	1.464
200	DQS0	1.942	2.365	MemData00:07	0.638	1.165
200	DQS1	1.920	2.314	MemData08:15	0.631	1.149
200	DQS2	1.938	2.361	MemData16:23	0.634	1.151
200	DQS3	1.945	2.370	MemData24:31	0.624	1.169
200	DQS4	1.932	2.332	MemData32:39	0.630	1.151
200	DQS5	1.936	2.348	MemData40:47	0.619	1.133
200	DQS6	1.938	2.356	MemData48:55	0.635	1.149
200	DQS7	1.943	2.360	MemData56:63	0.642	1.151
200	DQS8	1.952	2.381	ECC0:7	0.641	1.141

In the following examples, the data strobes (DQS) and the data are shown to be coincident. There is actually a slight skew as specified by the SDRAM specifications, and there can be additional skew due to loading and signal routing. It is recommended that the signal length for all of the eight DQS signals be matched.

Example 1:

If the data-to-PLB clock timing is as shown in the example below, then the read clock is not delayed and the Stage 1 data is sampled at **(1)**. Except for small, low frequency memory systems with the memory located physically close to the PPC440GX, it is unlikely that Stage 1 data can be sampled. When the data comes later, it is necessary to sample Stage 2 or Stage 3 data. (see Examples 2 and 3). Another way to get the desired data-to-PLB timing to allow Stage 1 sampling is to buffer MemClkOut0 and skew it enough to guarantee the timing. In this example T_T = 1.27ns at worst case conditions.

DDR SDRAM Read Cycle Timing—Example 1



T_{SIN} = Delay from DQS at package pin to C on Stage 1 FF.

T_P = Propagation delay through FFs

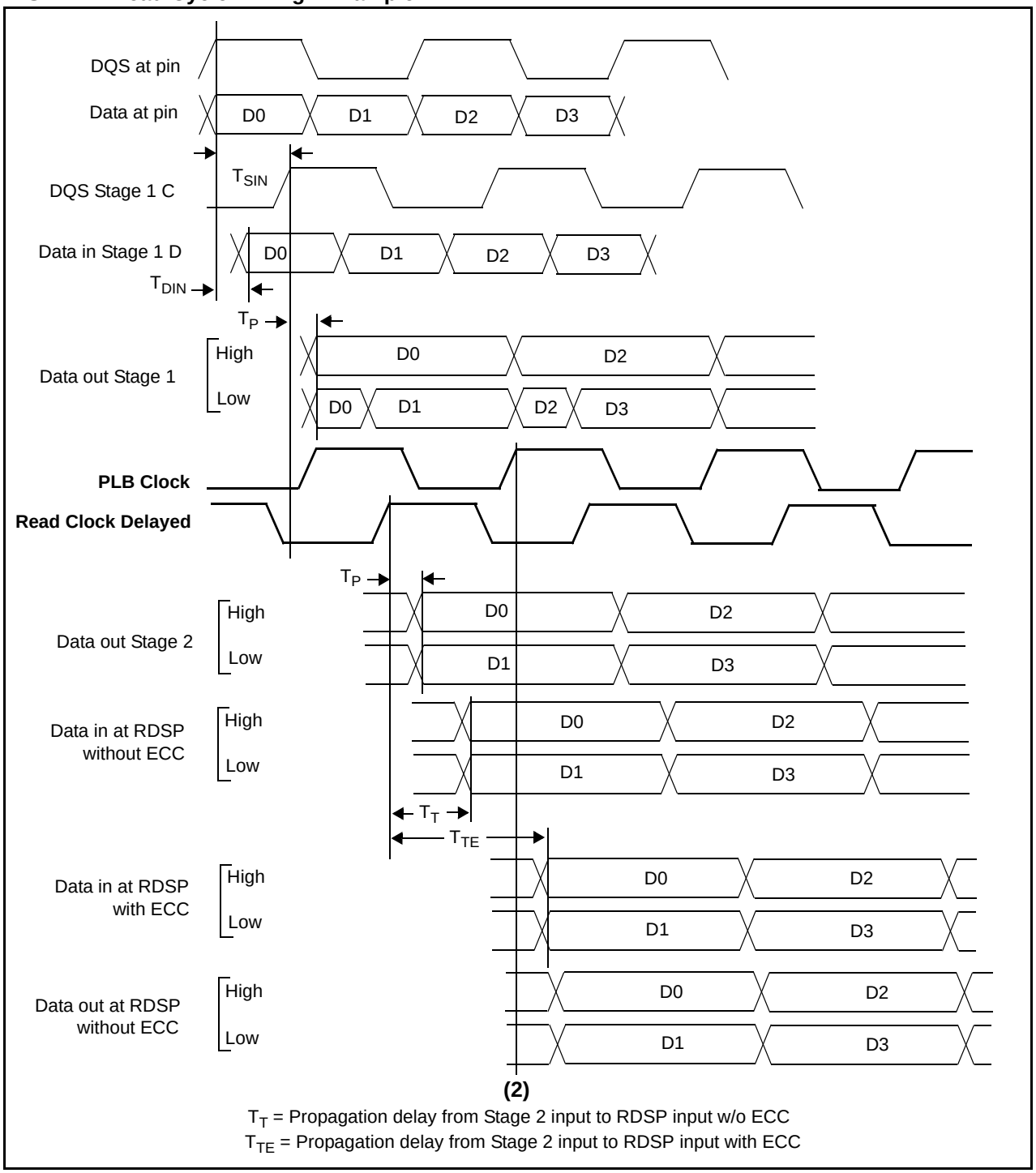
T_{DIN} = Delay from data at package pin to D on Stage 1 FF.

T_T = Propagation delay, Stage 1 input to RDSP input w/o ECC

Example 2:

In this example Read Clock is delayed almost 1/2 cycle. Without ECC, Stage 2 data can be sampled at **(2)**. If ECC is enabled, Stage 3 data must be sampled (see Example 3). In this example, T_T = 1.27ns and T_{TE} = 3.589ns at worst case conditions.

DDR SDRAM Read Cycle Timing—Example 2

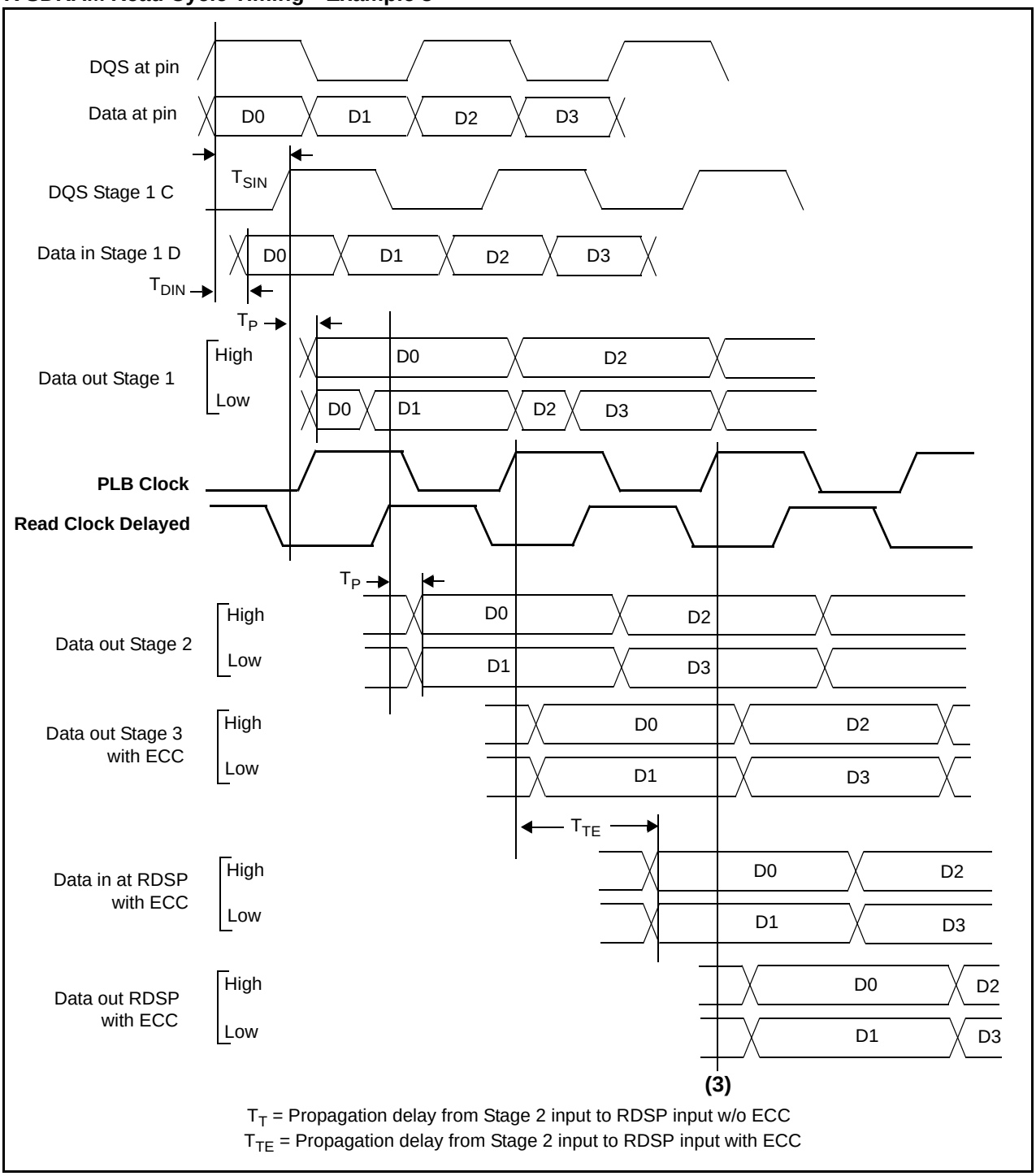


T_T = Propagation delay from Stage 2 input to RDSP input w/o ECC
T_{TE} = Propagation delay from Stage 2 input to RDSP input with ECC

Example 3:

In this example, ECC is enabled. This requires that Stage 3 data be sampled at **(3)**. If ECC is disabled, the system will still work, but there will be more latency before the data is sampled into RDSP. Again, T_T = 1.27ns and T_{TE} = 3.589ns at worst case conditions.

DDR SDRAM Read Cycle Timing—Example 3



T_T = Propagation delay from Stage 2 input to RDSP input w/o ECC
T_{TE} = Propagation delay from Stage 2 input to RDSP input with ECC

Initialization

The PPC440GX provides the option for setting initial parameters based on default values or by reading them from a slave PROM attached to the IIC0 bus (see “Serial EEPROM” below). Some of the default values can be altered by strapping on external pins (see “Strapping” below).

Strapping

While the SysReset input pin is low (system reset), the state of certain I/O pins is read to enable certain default initial conditions prior to PPC440GX start-up. The actual capture instant is the nearest SysClk edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. They are used for strap functions only during reset. Following reset they are used for normal functions.

The following table lists the strapping pins along with their functions and strapping options:

Strapping Pin Assignments

Function	Option	Ball Strapping		
		V24 (UART0_DCD)	V02 (UART0_DSR)	L07 (GMC1TxEr)
Serial device is disabled. Each of the four options (A–D) is a combination of boot source, boot-source width, and clock frequency specifications. Refer to the IIC Bootstrap Controller chapter in the *PPC440GX Embedded Processor User's Manual* for details.	A	0	0	0
	B	0	x	1
	C	0	1	0
	D	1	0	0
Serial device is enabled. The option being selected is the IIC0 slave address that will respond with strapping data.	0x54	1	0	1
	0x50	1	1	1

Serial EEPROM

During reset, initial conditions other than those obtained from the strapping pins can be read from a ROM device connected to the IIC0 port. At the de-assertion of SysReset, if the bootstrap controller is enabled, the PPC440GX sequentially reads 16 bytes from the ROM device on the IIC0 port and sets the SDR0_SDSTP0, SDR0_SDSTP1, SDR0_SDSTP2, and SDR0_SDSTP3 registers accordingly.

The initialization settings and their default values are covered in detail in the *PowerPC 440GX Embedded Processor User's Manual*.

Revision Log

Date	Contents of Modification
08/07/2002	Add revision log.
08/30/2002	Change EMC0:1TxD0:1 and EMC0:1TxEn T_{OV} from 15 to 11 ns.
09/25/2002	Update for L2 cache
10/22/2002	Add heat sink mounting information .
11/20/2002	Update I/O timing data.
01/07/2003	Update PCI-X I/O voltage specification. Correct package drawing
01/22/2003	Correct description of SysReset signal. Update for 533MHz parts and add power supply current values.
03/25/2003	Update DDR SDRAM timing. Change RTBIxTX and RX control signals to data signals.
06/16/2003	Add 667MHz part numbers, update I/O specifications, and fill in missing data points.
07/15/2003	Update information concerning higher speed parts, bus clock ratios, the duplicate trace signals, and initialization strapping pins. Update Ethernet signals with new and moved signals.
07/17/2003	Remove IBM Confidential.
12/02/2003	Revise DDR SDRAM I/O section.
01/13/2004	Correct TrcTS6 signal data (pin assignment and multiplexing).
02/12/2004	Restore V_{DD}/OV_{DD} voltage sequence restriction.
02/25/2004	Add three Revision C part numbers.
03/04/2004	Update part number list. Update dimensions on package drawing.
03/25/2004	Correct GMCTxClk signal description from input-only to I/O.
05/12/2004	Add plastic package data, new power data, and update part number list.
05/20/2004	Upgrade 533MHz ceramic part to 105°C rating.
06/15/2004	Correct dimensions on ceramic package drawing.
06/30/2004	Replace misssing 533MHz C temperature range part.
11/01/2004	Add information on minimum SysClk and $\overline{\text{TRST}}$ duration during power-on reset. Remove power sequence restrictions note from Absolute Maximum Rating table. Restate power sequencing restrictions in Recommended DC Operating Conditions table. Convert to AMCC format.
12/09/2004	Restore “Preliminary” to document classification.
06/16/2005	Add S (no L2 cache support) temperature range part numbers.
07/01/2005	Add reduced-lead ceramic and lead-free plastic part numbers.
10/17/2005	Clarify DDR SDRAM interface diagram.
11/07/2005	Remove metal-layer specification from technology description. Add logo and number nomenclature to package drawing.
12/22/2005	Update I/O timing specs for EMC0:3TxD, GMC0RxD0:3, GMC1RxD0:3, GMCRxDV, GMC1RxCtl, GMCRxD0:7, GMCRxEr, GMCCrS, GMCTxD0:7.

Date	Contents of Modification
02/08/2006	Correct timing changes made in 12/22/05 version.
04/04/2006	Add six new PNs (two 533MHz and four 677MHz). Remove two PNs (no Z shipping for 3NF533C or 3FF533C)
06/09/2006	Update clocking specs and EEPROM information.
09/11/2006	Add four posts to plastic package drawing. Reduce maximum E temperature rating for selected plastic parts.
09/26/2006	Remove five PNs (end of life) Add/change timing data (system and DDR SDRAM) for 800MHz Rev F parts Increase minimum CPU frequency from 300MHz to 333MHz. Increase SV_{DD} for DDR SDRAM parts operating a 200MHz.
02/23/2007	Add two new ceramic 400MHz PNs. One is leaded (C) and the other is reduced-lead (R).
03/05/2007	Change T_{OH} values for RGMII signals.
08/30/2007	Change the technical support telephone and fax number.
04/03/2008	Remove power supply power-up sequence requirements.
07/16/2008	Change package type to ceramic for PPC440GX-3RF400C (Doc Issue 549).

Printed in the United States of America, Wednesday, July 16, 2008

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