Dual 2 A, 1.2 V, Slew Rate Controlled Load Switch

DESCRIPTION

SiP32413 and SiP32414 are slew rate controlled load switches that is designed for 1.1 V to 5.5 V operation.

The devices guarantee low switch on-resistance at 1.2 V input. They feature a controlled soft-on slew rate of typical 150 µs that limits the inrush current for designs of capacitive load or noise sensitive loads.

The devices feature a low voltage control logic interface (On/Off interface) that can interface with low voltage digital control without extra level shifting circuit. The SiP32414 also integrates output discharge switches that enable fast shutdown load discharge. When the switches are off, they provide the reverse blocking to prevent high current flowing into the power source.

Both the SiP32413 and SiP32414 are available in TDFN8 2 mm x 2mm package. Each switch in each device can support over 2 A of continuous current.

FEATURES

- 1.1 V to 5.5 V operation voltage range
- 62 mΩ typical from 2 V to 5 V
- Low R_{ON} down to 1.2 V
- Slew rate controlled turn-on: 150 µs at 3.6 V
- Fast shutdown load discharge for SiP32414
- Low quiescent current
  - < 1 µA when disabled
  - 6.7 µA at V_{IN} = 1.2 V
- Switch off reversed blocking
- **Compliant to RoHS directive 2002/95/EC**
- **Halogen-free according to IEC 61249-2-21 definition**

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- Cellular phones
- Portable media players
- Digital camera
- GPS
- Computers
- Portable instruments and healthcare devices

TYPICAL APPLICATION CIRCUIT

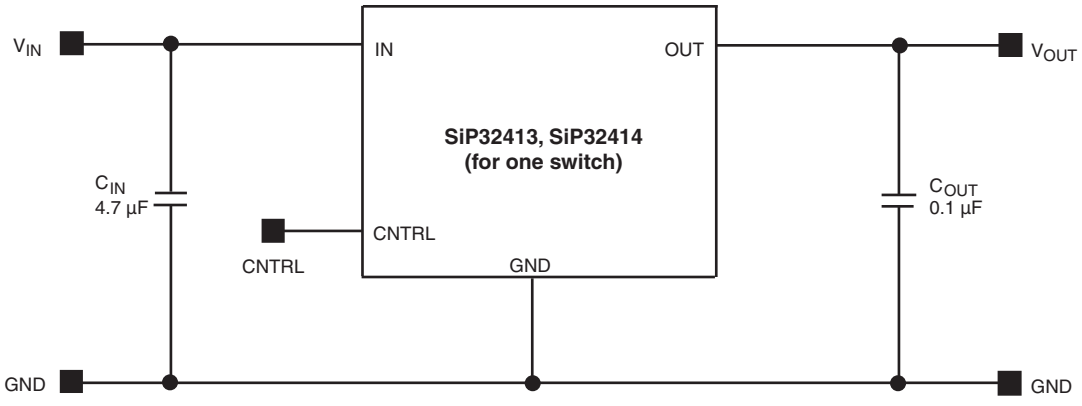


Figure 1 - SiP32413, SiP32414 Typical Application Circuit

ORDERING INFORMATION

Temperature Range	Package	Marking	Part Number
- 40 °C to 85 °C	TDFN8 2 mm x 2 mm	AA	SiP32413DNP-T1-GE4
		AB	SiP32414DNP-T1-GE4

Note:
x = Lot Code

ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit
Supply Input Voltage (V_{IN})	- 0.3 to 6	V
Enable Input Voltage (V_{EN})	- 0.3 to 6	
Output Voltage (V_{OUT})	- 0.3 to V_{IN} + 0.3	
Maximum Continuous Switch Current (I_{MAX})	2.4	A
Maximum Pulsed Current (I_{DM}) V_{IN} (Pulsed at 1 ms, 10 % Duty Cycle)	3	
ESD Rating (HBM)	4000	V
Junction Temperature (T_J)	- 40 to 125	°C
Thermal Resistance (θ_{JA})[a]	84	°C/W
Power Dissipation (P_D)[a, b]	655	mW

Notes:
a. Device mounted with all leads and power pad soldered or welded to PC board, see PCB layout.
b. Derate 11.9 mW/°C above T_A = 70 °C, see PCB layout.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
Input Voltage Range (V_{IN})	1.1 to 5.5	V
Operating Temperature Range	- 40 to 85	°C

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{IN} = 5.0 V, T_A = - 40 °C to 85 °C (Typical values are at T_A = 25 °C)	Limits - 40 °C to 85 °C Min.[a]	Typ.[b]	Max.[a]	Unit
Operating Voltage[c]	V_{IN}		1.1	-	5.5	V
Quiescent Current	I_Q	V_{IN} = 1.2 V, CNTRL = active	-	6.7	14	µA
		V_{IN} = 1.8 V, CNTRL = active	-	14	24	
		V_{IN} = 2.5 V, CNTRL = active	-	25	40	
		V_{IN} = 3.6 V, CNTRL = active	-	40	60	
		V_{IN} = 4.3 V, CNTRL = active	-	52	75	
		V_{IN} = 5.0 V, CNTRL = active	-	71	99	
Off Supply Current	$I_{Q(off)}$	CNTRL = inactive, OUT = open	-	-	1	
Off Switch Current	$I_{DS(off)}$	CNTRL = inactive, OUT = 0	-	-	1	
Reverse Blocking Current	I_{RB}	V_{OUT} = 5.5 V, V_{IN} = 1.2 V, V_{EN} = inactive	-	-	10	
On-Resistance	$R_{DS(on)}$	V_{IN} = 1.2 V, I_L = 100 mA, T_A = 25 °C	-	66	76	mΩ
		V_{IN} = 1.8 V, I_L = 100 mA, T_A = 25 °C	-	62	72	
		V_{IN} = 2.5 V, I_L = 100 mA, T_A = 25 °C	-	62	72	
		V_{IN} = 3.6 V, I_L = 100 mA, T_A = 25 °C	-	62	72	
		V_{IN} = 4.3 V, I_L = 100 mA, T_A = 25 °C	-	62	72	
		V_{IN} = 5.0 V, I_L = 100 mA, T_A = 25 °C	-	62	72	
On-Resistance Temp.-Coefficient	TC_{RDS}		-	3900	-	ppm/°C
CNTRL Input Low Voltage[c]	V_{IL}	V_{IN} = 1.2 V	-	0.5	0.3	V
		V_{IN} = 1.8 V	-	0.72	0.4[d]	
		V_{IN} = 2.5 V	-	0.87	0.5[d]	
		V_{IN} = 3.6 V	-	1.0	0.6[d]	
		V_{IN} = 4.3 V	-	1.08	0.7[d]	
		V_{IN} = 5.0 V	-	1.15	0.8[d]	
CNTRL Input High Voltage[c]	V_{IH}	V_{IN} = 1.2 V	0.9[d]	0.54	-	
		V_{IN} = 1.8 V	1.2[d]	0.78	-	
		V_{IN} = 2.5 V	1.4[d]	0.96	-	
		V_{IN} = 3.6 V	1.6[d]	1.2	-	
		V_{IN} = 4.3 V	1.7[d]	1.32	-	
		V_{IN} = 5.0 V	1.8	1.45	-	
EN Input Leakage	I_{SINK}	V_{EN} = 5.5 V	-	-	1	µA
Output Pulldown Resistance	R_{PD}	CNTRL = inactive, T_A = 25 °C (SiP32414 only)	-	217	280	Ω
Output Turn-On Delay Time	$t_{d(on)}$	V_{IN} = 3.6 V, R_{LOAD} = 10 Ω, T_A = 25 °C	-	140	210	µs
Output Turn-On Rise Time	$t_{(on)}$		80	150	220	
Output Turn-Off Delay Time	$t_{d(off)}$		-	0.27	1	

Notes:
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. For V_{IN} outside this range consult typical EN threshold curve.
d. Not tested, guarantee by design.

PIN CONFIGURATION

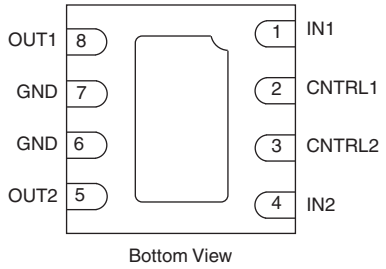


Figure 2 - TDFN8 2 mm x 2 mm Package

PIN DESCRIPTION		
Pin Number	**Name**	**Function**
1	IN1	This pin is the side 1 n-channel MOSFET drain connection. Bypass to ground through a 2.2 µF capacitor
2	CNTRL1	Side 1 control input
3	CNTRL2	Side 2 control input
4	IN2	This pin is the side 2 n-channel MOSFET drain connection. Bypass to ground through a 2.2 µF capacitor
5	OUT2	This pin is the side 2 n-channel MOSFET source connection. Bypass to ground throught a 0.1 µF capacitor
6	GND	Ground connection
7	GND	Ground connection
8	OUT1	This pin is the side 1 n-channel MOSFET source connection. Bypass to ground throught a 0.1 µF capacitor

TRUTH TABLE SiP32413			
CNTRL1	**CNTRL2**	**SW1**	**SW2**
0	0	ON	OFF
0	1	ON	ON
1	0	OFF	OFF
1	1	OFF	ON

TRUTH TABLE SiP32414			
CNTRL1	**CNTRL2**	**SW1**	**SW2**
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	ON	ON

TYPICAL CHARACTERISTICS internally regulated, 25 °C, unless otherwise noted

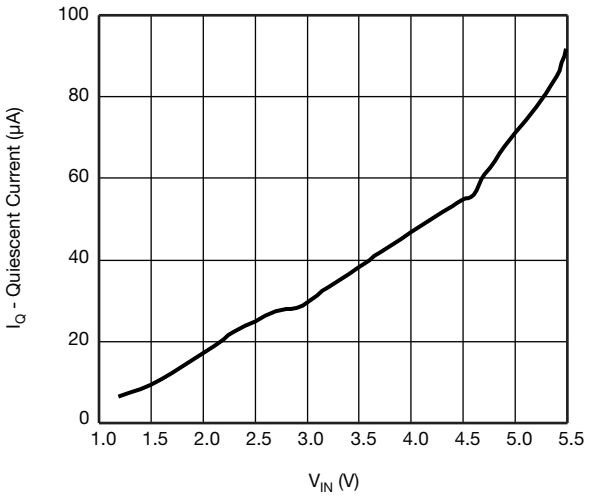


Figure 3 - Quiescent Current vs. Input Voltage

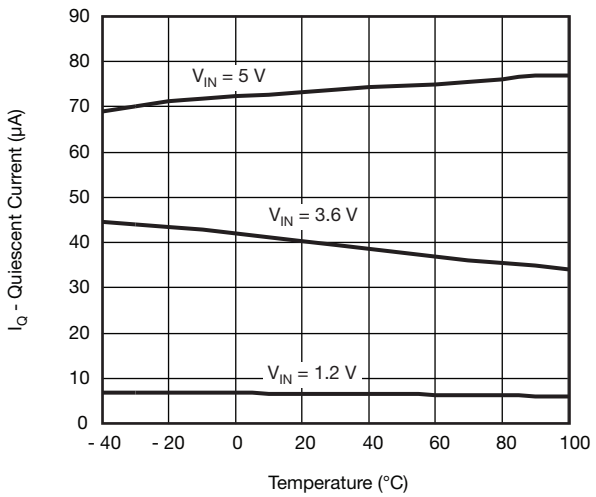


Figure 4 - Quiescent Current vs. Temperature

TYPICAL CHARACTERISTICS internally regulated, 25 °C, unless otherwise noted

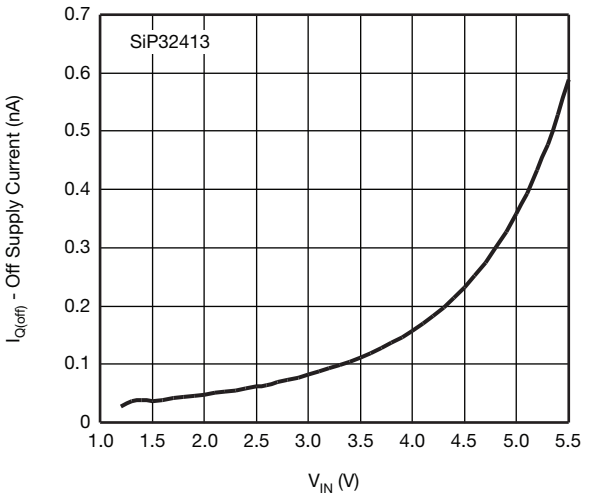


Figure 5 - SiP32413 Off Supply Current vs. V_{IN}

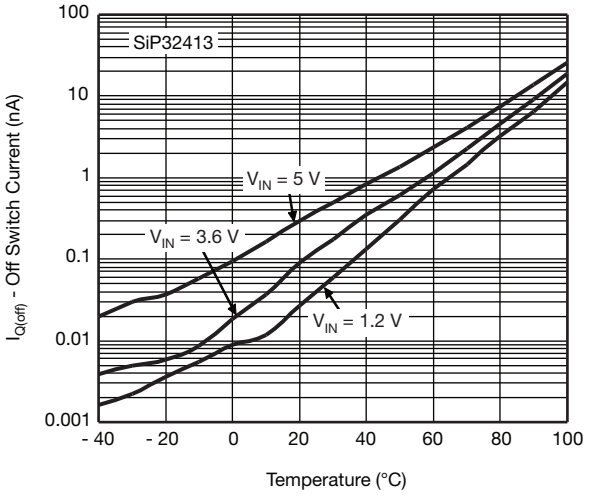


Figure 6 - SiP32414 Off Supply Current vs. Temperature

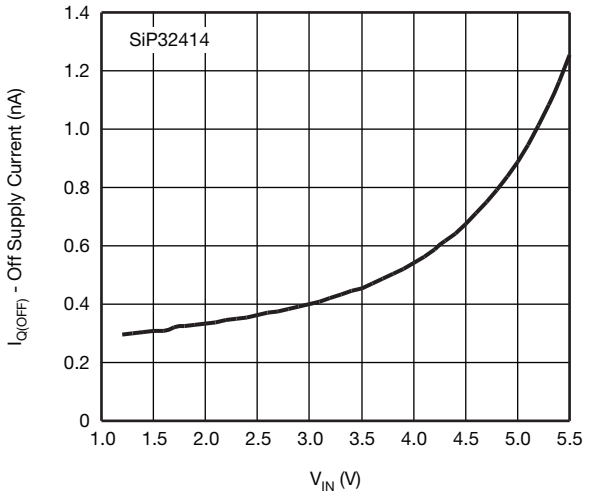


Figure 7 - SiP32414 Off Supply Current vs. V_{IN}

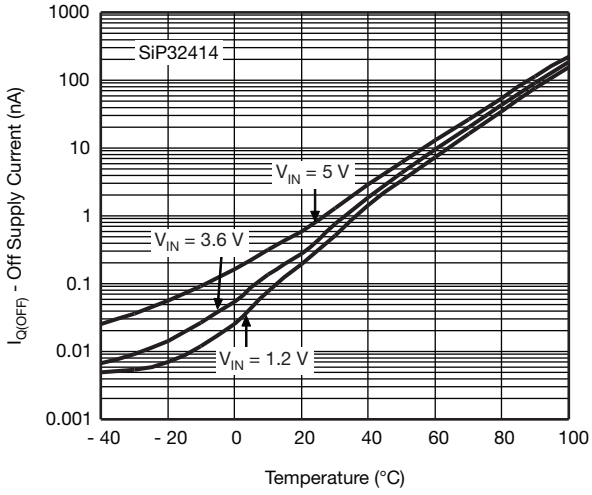


Figure 8 - SiP32414 Off Supply Current vs. Temperature

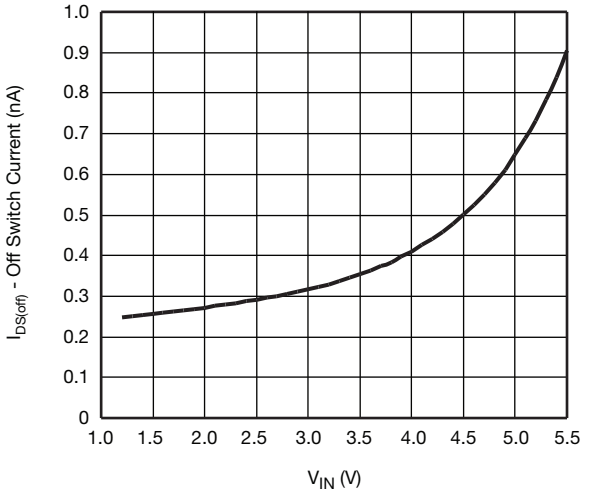


Figure 9 - Off Swith Current vs. Input Voltage

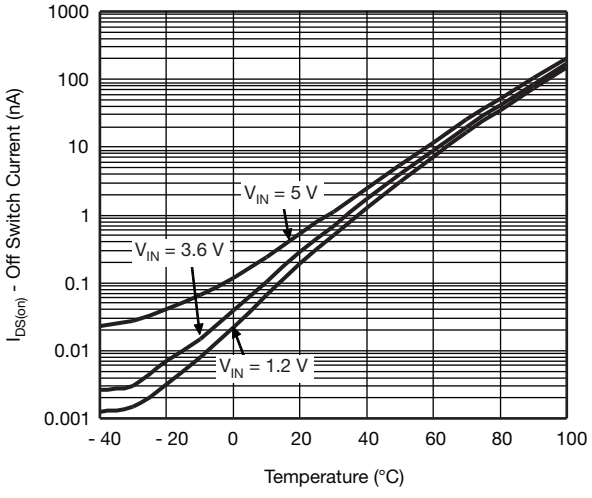


Figure 10 - Off Swith Current vs. Temperature

TYPICAL CHARACTERISTICS internally regulated, 25 °C, unless otherwise noted

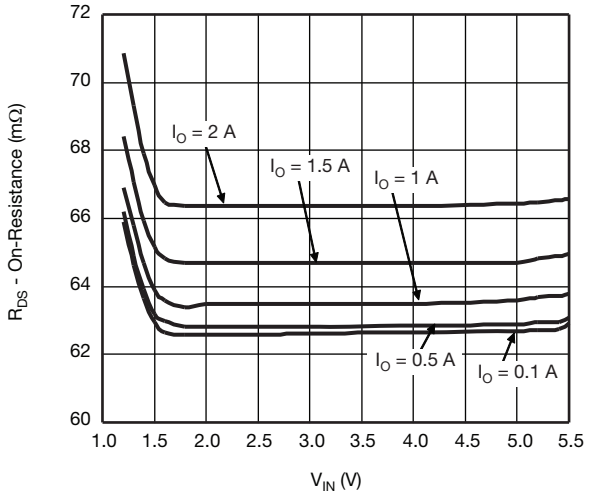


Figure 11 - $R_{DS(on)}$ vs. Input Voltage

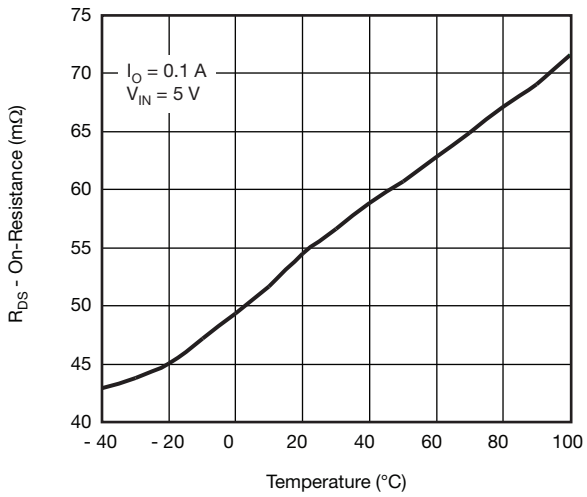


Figure 12 - $R_{DS(on)}$ vs. Temperature

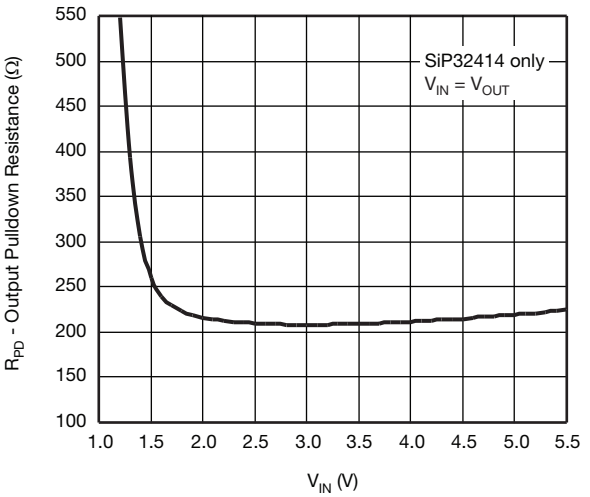


Figure 13 - SiP32414 Output Pull Down vs. Input Voltage

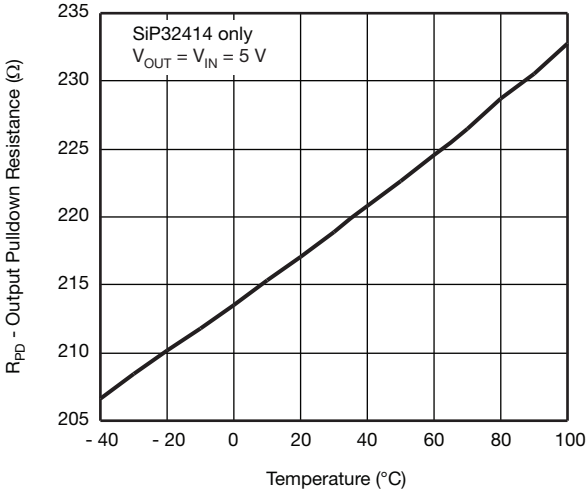


Figure 14 - SiP32414 Output Pull Down vs. Temperature

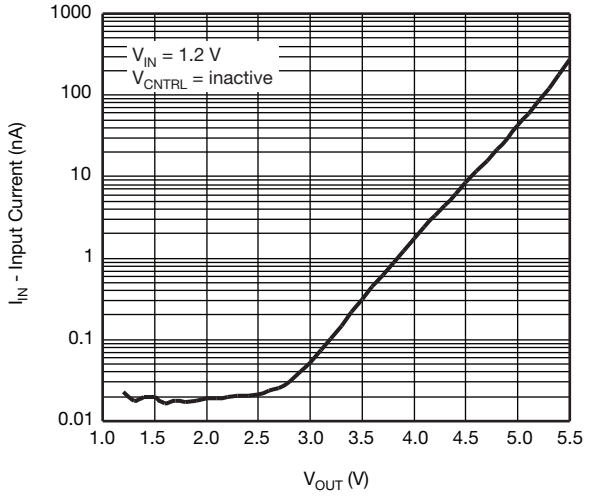


Figure 15 - Reverse Blocking Current vs. Output Voltage

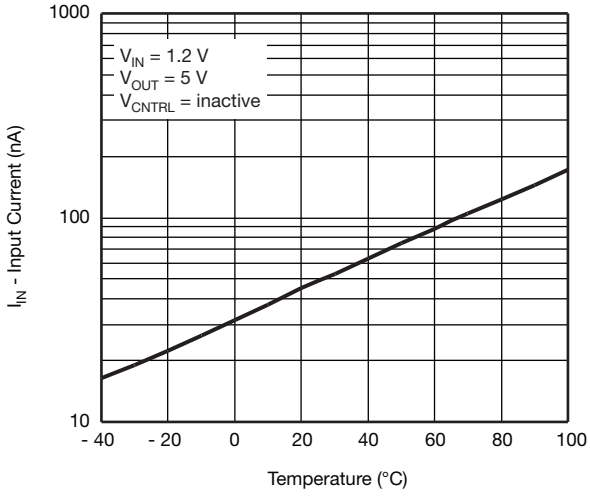


Figure 16 - Reverse Blocking Current vs. Temperature

TYPICAL CHARACTERISTICS internally regulated, 25 °C, unless otherwise noted

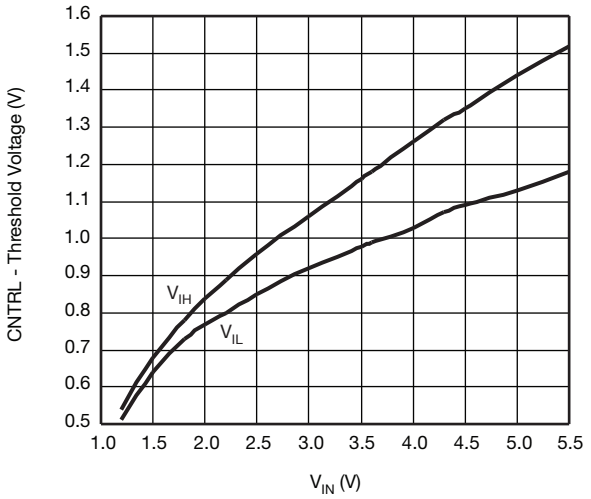


Figure 17 - CNTRL Threshold Voltage vs. Input Voltage

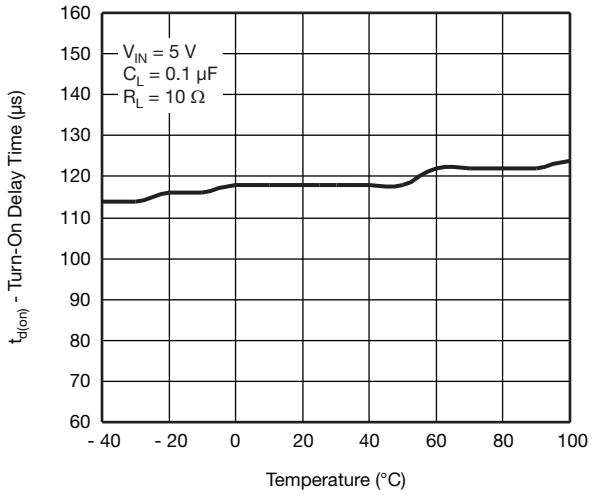


Figure 18 - Turn-On Delay Time vs. Temperature

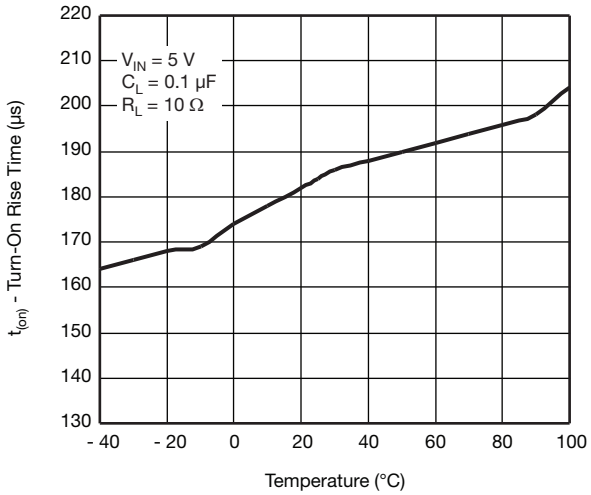


Figure 19 - Rise Time vs. Temperature

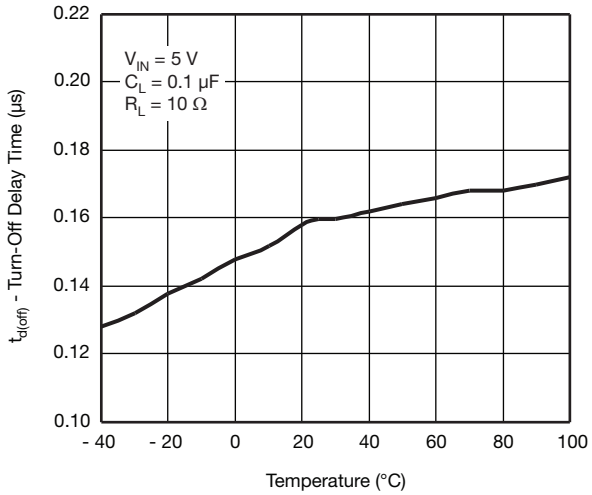


Figure 20 - Turn-Off Delay Time vs. Temperature

TYPICAL WAVEFORMS

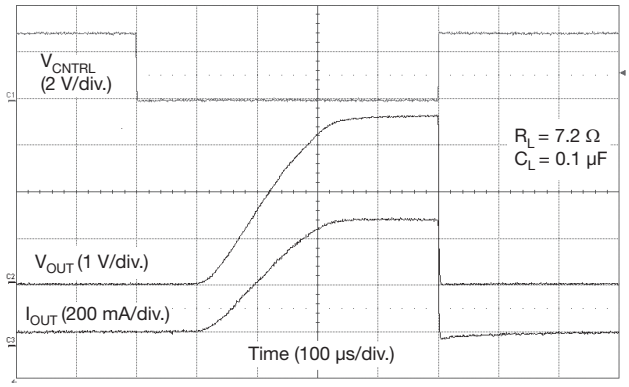


Figure 21 - SiP32413 Channel 1 Switching
(V_{IN} = 3.6 V, R_L = 7.2 Ω)

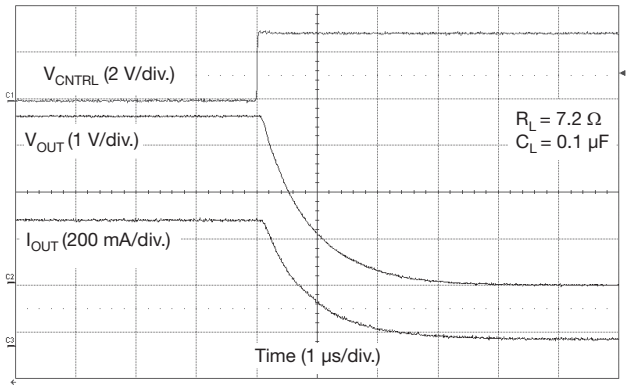


Figure 22 - SiP32413 Channel 1 Turn-Off
(V_{IN} = 3.6 V, R_L = 7.2 Ω)

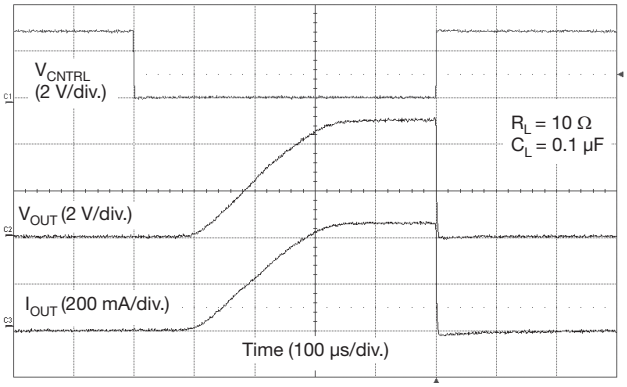


Figure 23 - SiP32413 Channel 1 Switching
(V_{IN} = 5 V, R_L = 10 Ω)

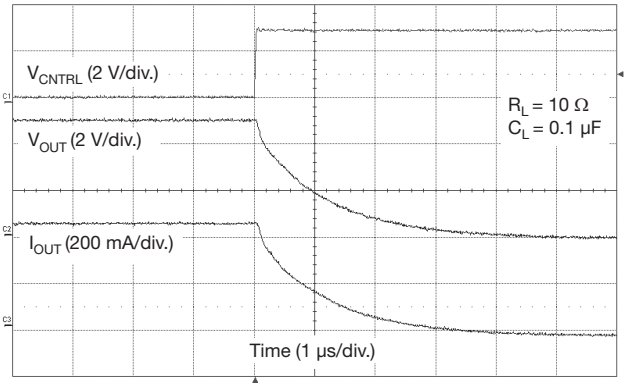


Figure 24 - SiP32413 Channel 1 Turn-Off
(V_{IN} = 5 V, R_L = 10 Ω)

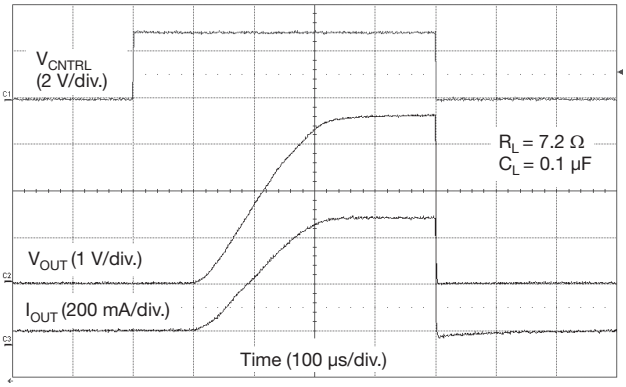


Figure 25 - SiP32413 Channel 2 and SiP32414 Switching
(V_{IN} = 3.6 V, R_L = 7.2 Ω)

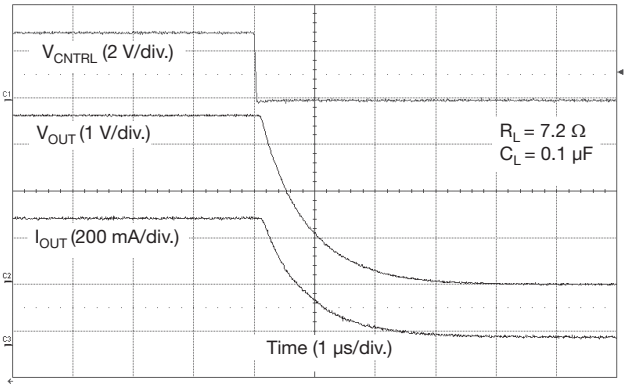


Figure 26 - SiP32413 Channel 2 and SiP32414 Turn-Off
(V_{IN} = 3.6 V, R_L = 7.2 Ω)

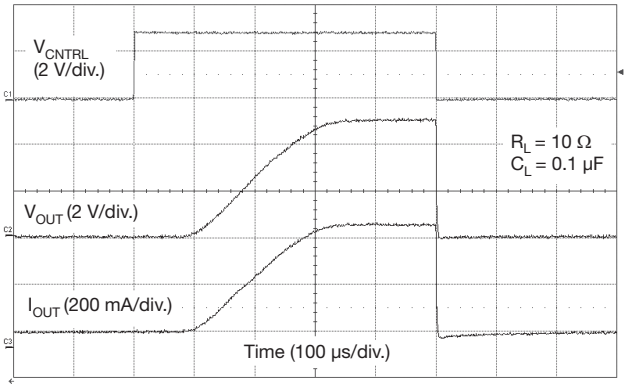


Figure 27 - SiP32413 Channel 2 and SiP32414 Switching
(V_{IN} = 5 V, R_L = 10 Ω)

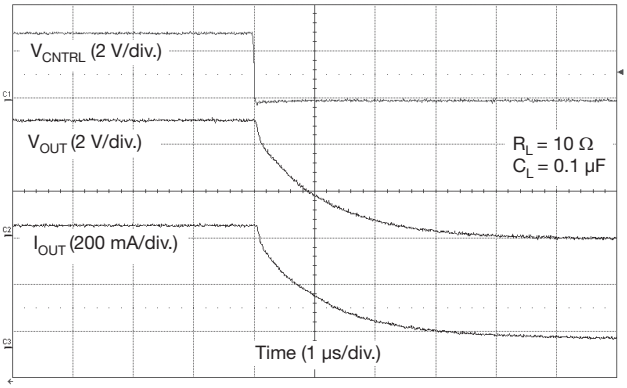


Figure 28 - SiP32413 Channel 2 and SiP32414 Turn-Off
(V_{IN} = 5 V, R_L = 10 Ω)

BLOCK DIAGRAM

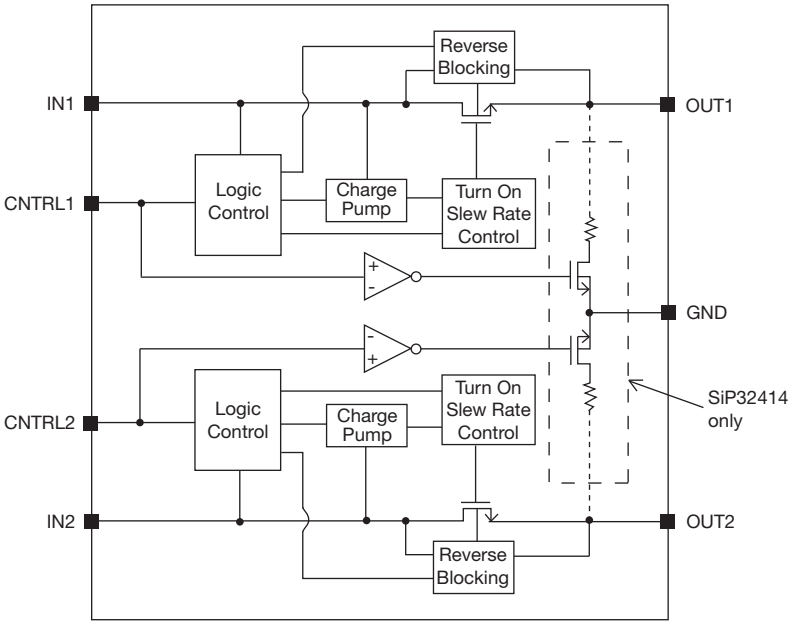
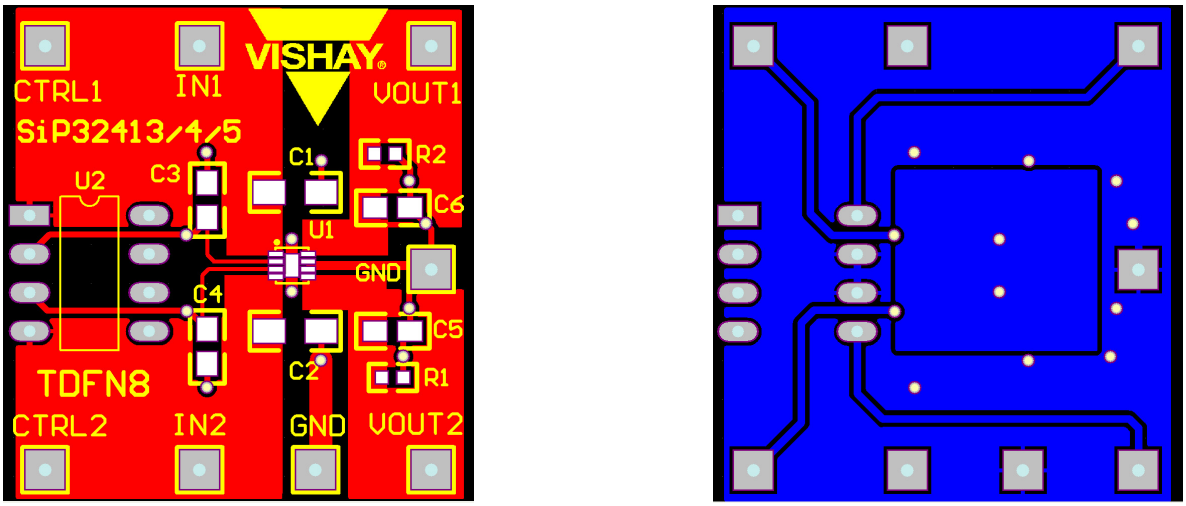


Figure 29 - Functional Block Diagram

PCB LAYOUT



Top **Bottom**

Figure 26 - PCB Layout for TDFN8 2 mm x 2 mm (board size: 1.2 inch x 1.3 inch)

DETAILED DESCRIPTION

SiP32413 and SiP32414 are dual n-channel power MOSFETs designed as high side load switch with slew rate control to prevent in-rush current. Once enable the device charge pumps the gate of the power MOSFET to 5 V gate to source voltage while controlling the slew rate of the turn on time. The mostly constant gate to source voltage keeps the on resistance low through out the input voltage range. For SiP32414, when disable the output discharge circuit turns on to help pull the output voltage to ground more quickly. For both parts, in disable mode, the reverse blocking circuit is activated to prevent current from going back to the input in case the output voltage is higher than the input voltage. Input voltage is needed for the reverse blocking circuit to work properly, it can be as low as $V_{IN(min)}$.

APPLICATION INFORMATION

Input Capacitor

While bypass capacitors on the inputs are not required, 2.2 µF or larger capacitors for C_{IN} is recommended in almost all applications. The bypass capacitors should be placed as physically close as possible to the device's input to be effective in minimizing transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 0.1 µF capacitor or larger across V_{OUT} and GND is recommended to insure proper slew operation. C_{OUT} may be increased without limit to accommodate any load transient condition with only minimal affect on the turn on slew rate time. There are no ESR or capacitor type requirement.

Control

The CNTRL pins are compatible with both TTL and CMOS logic voltage levels.

Protection Against Reverse Voltage Condition

Both SiP32413 and SiP32414 contain reverse blocking circuitries to protect the current from going to the input from the output in case where the output voltage is higher than the input voltage when the main switch is off. Supply voltages as low as the minimum required input voltage are necessary for these circuitries to work properly.

Thermal Considerations

SiP32413 and SiP32414 are designed to maintain constant output load current. Due to physical limitations of the layout and assembly of the device the maximum switch current is 2.4 A, as stated in the Absolute Maximum Ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package. To obtain the highest power dissipation (and a thermal resistance of 84) the power pad of the device should be connected to a heat sink on the printed circuit board.

The maximum power dissipation in any application is dependant on the maximum junction temperature, $T_{J(max.)}$ = 125 °C, the junction-to-ambient thermal resistance for the TDFN4 1.2 mm x 1.6 mm package, θ_{J-A} = 84 °C/W, and the ambient temperature, T_A, which may be formulaically expressed as:

$$P\ (max.) = \frac{T_J\ (max.) - T_A}{\theta_{J-A}} = \frac{125 - T_A}{84}$$

It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 655 mW.

So long as the load current is below the 2.0 A limit, the maximum continuous switch current becomes a function two things: the package power dissipation and the $R_{DS(ON)}$ at the ambient temperature.

As an example let us calculate the worst case maximum load current at T_A = 70 °C. The worst case $R_{DS(ON)}$ at 25 °C occurs at an input voltage of 1.2 V and is equal to 75 mΩ. The $R_{DS(ON)}$) at 70 °C can be extrapolated from this data using the following formula:

$R_{DS(ON)}$ (at 70 °C) = $R_{DS(ON)}$ (at 25 °C) x (1 + T_C x ΔT)

Where T_C is 3400 ppm/°C. Continuing with the calculation we have

$R_{DS(ON)}$ (at 70 °C) = 75 mΩ x (1 + 0.0034 x (70 °C - 25 °C)) = 86.5 mΩ

The maximum current limit is then determined by

$$I_{LOAD}\ (max.) < \sqrt{\frac{P\ (max.)}{R_{DS(ON)}}}$$

which in case is 2.75 A, assuming one switch turn on at a time. Under the stated input voltage condition, if the 2.75 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.

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