A5832

BiMOS II 32-Bit Serial Input Latched Driver

Discontinued Product

These parts are no longer in production The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: October 31, 2005

Recommended Substitutions:

For new customers or new applications, refer to the A6832.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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5832

BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

UCN5832A

Dwg. No. A-12,377A
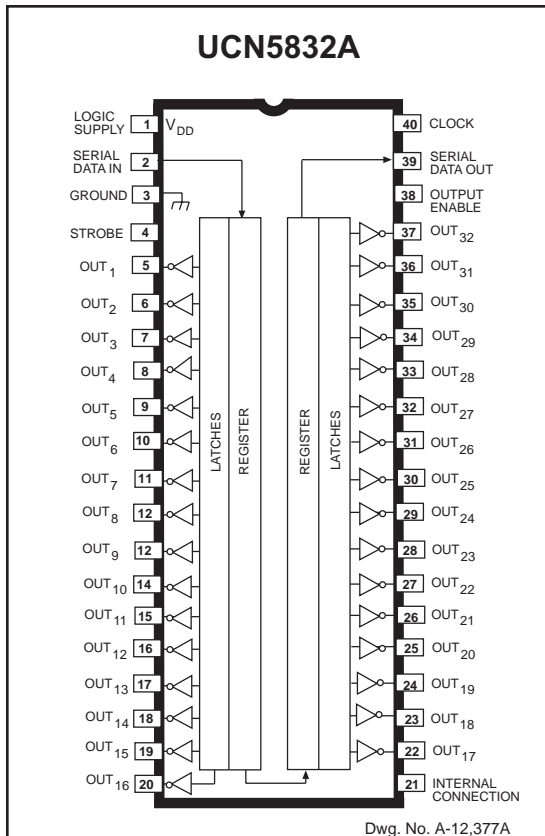
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{OUT} .... **40 V**

Logic Supply Voltage, V_{DD} .... **15 V**

Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**

Continuous Output Current,
I_{OUT} .... **150 mA**

Package Power Dissipation,
P_D .... **See Graph**

Operating Temperature Range,
T_A .... **-20°C to +85°C**

Storage Temperature Range,
T_S .... **-55°C to +150°C**

Caution: CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Intended originally to drive thermal printheads, the UCN5832A and UCN5832EP have been optimized for low output-saturation voltage, high-speed operation, and pin configurations most convenient for the tight space requirements of high-resolution printheads. These integrated circuits can also be used to drive multiplexed LED displays or incandescent lamps at up to 150 mA peak current. The combination of bipolar and MOS technologies gives BiMOS II arrays an interface flexibility beyond the reach of standard buffers and power driver circuits.

The devices each have 32 bipolar NPN open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor based systems. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high. MOS serial data outputs permit cascading for interface applications requiring additional drive lines.

The UCN5832A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. Under normal operating conditions, this device will allow all outputs to sustain 100 mA continuously without derating. The UCN5832EP is supplied in a 44-lead plastic leaded chip carrier for minimum area, surface-mount applications. Both devices are also available for operation from -40°C to +85°C. To order, change the prefix from 'UCN' to 'UCQ'.

Similar 32-bit serial-input latched source drivers are available as the UCN5818AF/EPF. Other high-voltage, high-current 8-bit devices are available as the UCN5821A, UCN5841A/LW, and UCN5842A.
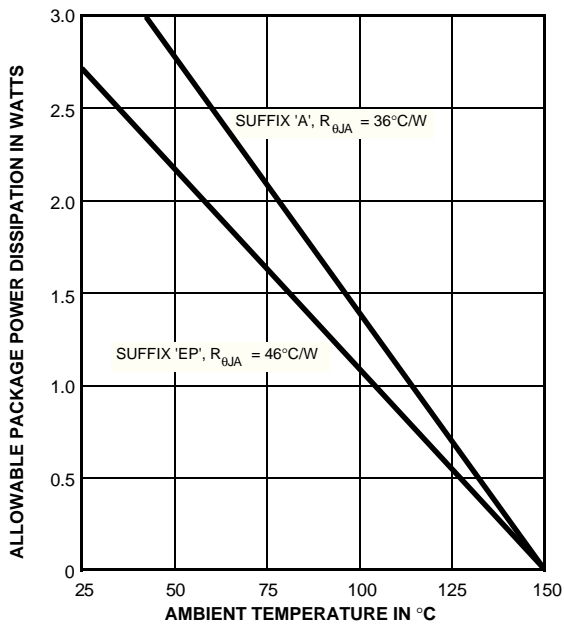
FEATURES

- ■ To 3.3 MHz Data Input Rate
- ■ Low-Power CMOS Logic and Latches
- ■ 40 V Current Sink Outputs
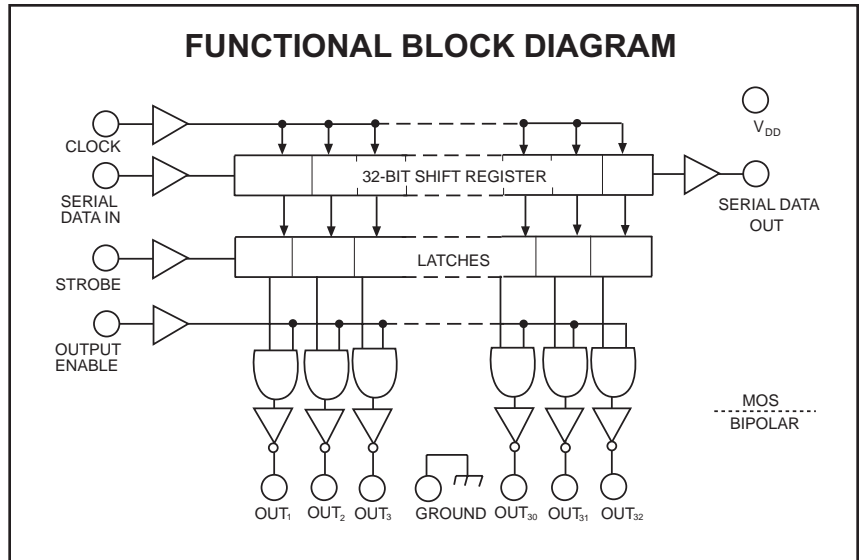- ■ Low Saturation Voltage
- ■ Automotive Capable

Always order by complete part number:

Part Number	Package
UCN5832A	40-Pin DIP
UCN5832EP	44-Lead PLCC
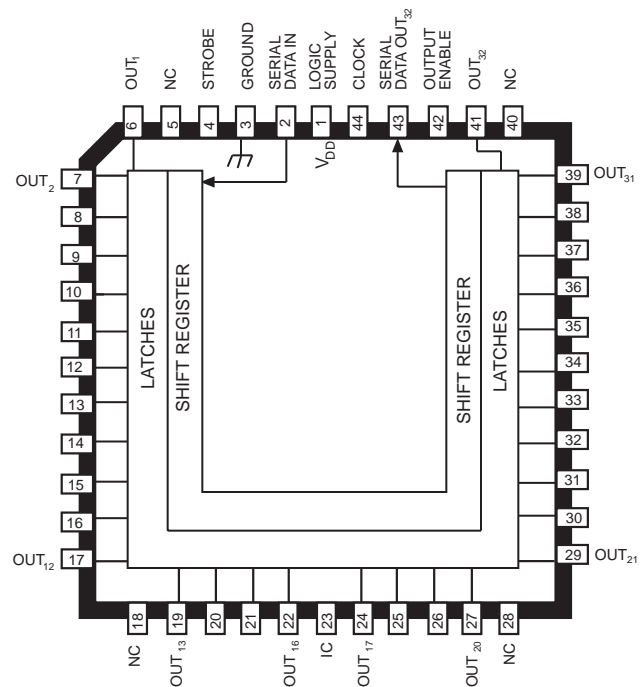
Dwg. GP-025A

SUFFIX 'A', $R_{\theta JA}$ = 36°C/W

SUFFIX 'EP', $R_{\theta JA}$ = 46°C/W

FUNCTIONAL BLOCK DIAGRAM

CLOCK

SERIAL DATA IN

32-BIT SHIFT REGISTER

V_{DD}

SERIAL DATA OUT

STROBE

LATCHES

OUTPUT ENABLE

MOS
BIPOLAR

OUT_1 OUT_2 OUT_3 GROUND OUT_{30} OUT_{31} OUT_{32}

UCN5832EP

Dwg. No. A-14,360

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted).

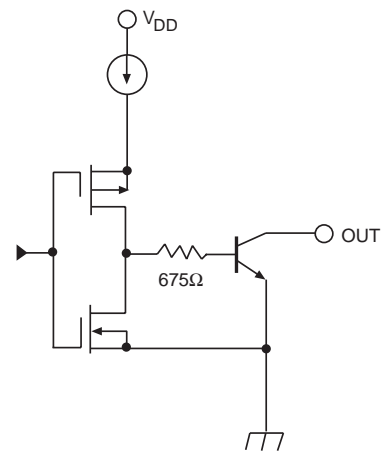| Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 40 V, T_A = 70°C	—	10	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 50 mA	—	275	mV
		I_{OUT} = 100 mA, "A" package	150	550	mV
		I_{OUT} = 100 mA, "EP" package	—	550	mV
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 3.5 V	—	1.0	μA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-1.0	μA
Input Impedance	Z_{IN}	V_{IN} = 3.5 V	3.5	—	MΩ
Serial Data Output Resistance	R_{OUT}		—	20	kΩ
Supply Current	I_{DD}	One output ON, I_{OUT} = 100 mA	—	5.0	mA
		All outputs OFF	—	50	μA
Output Rise Time	t_r	I_{OUT} = 100 mA, 10% to 90%	—	1.0	μs
Output Fall Time	t_f	I_{OUT} = 100 mA, 90% to 10%	—	1.0	μs

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

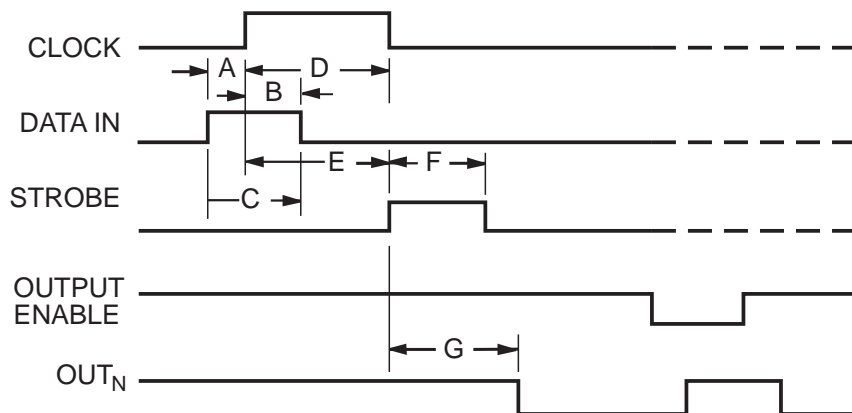## TYPICAL INPUT CIRCUIT
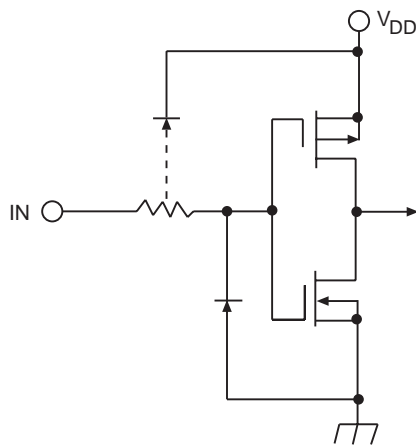
Dwg. No. A-12,379A

TYPICAL OUTPUT DRIVER

675Ω

Dwg. No. A-12,380A

Dwg. No. A-12,276A

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

TIMING CONDITIONS
(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse
(Data Set-Up Time) .... **75 ns**
B. Minimum Data Active Time After Clock Pulse
(Data Hold Time) .... **75 ns**
C. Minimum Data Pulse Width .... **150 ns**
D. Minimum Clock Pulse Width .... **150 ns**
E. Minimum Time Between Clock Activation and Strobe .... **300 ns**
F. Minimum Strobe Pulse Width .... **100 ns**
G. Typical Time Between Strobe Activation and
Output Transition .... **500 ns**

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable Input	Output Contents					
		I_1	I_2	I_3	...	I_{N-1}	I_N			I_1	I_2	I_3	...	I_{N-1}	I_N		I_1	I_2	I_3	...	I_{N-1}	I_N
H	⌐	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	⌐	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	⌐⌐	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	L	H	H	H	...	H	H

L = Low Logic Level   H = High Logic Level   X = Irrelevant   P = Present State   R = Previous State

![Allegro MicroSystems, Inc. logo]

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Worcester, Massachusetts 01615-0036 (508) 853-5000

UCN5832A

Dimensions in Inches
(controlling dimensions)

40   21

0.580
0.485

1   2   3   4   20

0.070
0.030

0.100
BSC

0.005
MIN

2.095
1.980

0.250
MAX

0.015
MIN

0.200
0.115

0.022
0.014

0.015
0.008

0.700
MAX

0.600
BSC

Dwg. MA-003-40 in

Dimensions in Millimeters
(for reference only)

40   21

14.73
12.32

1   2   3   4   20

1.77
0.77

2.54
BSC

0.13
MIN

53.2
50.3

6.35
MAX

0.39
MIN

5.08
2.93

0.558
0.356

0.381
0.204

17.78
MAX

15.24
BSC

Dwg. MA-003-40 mm
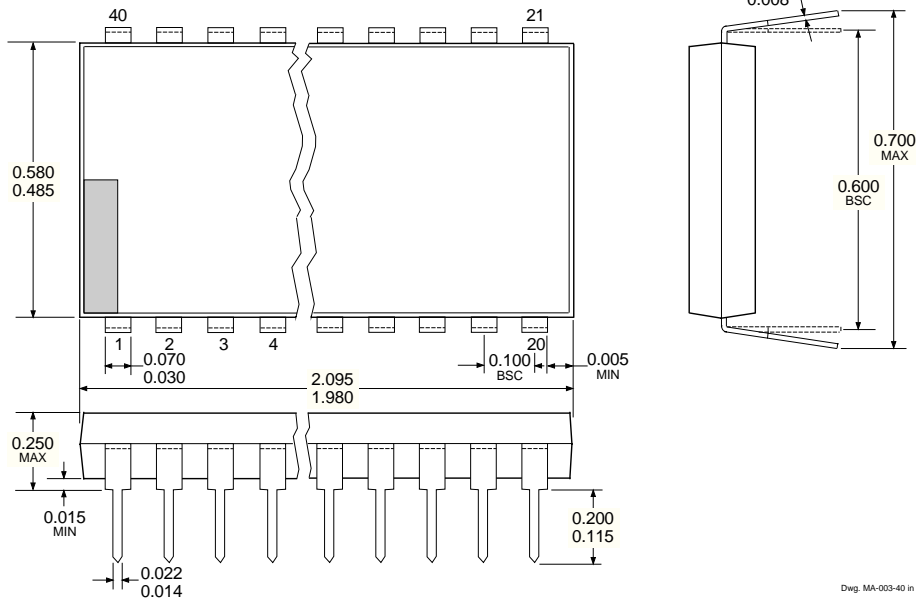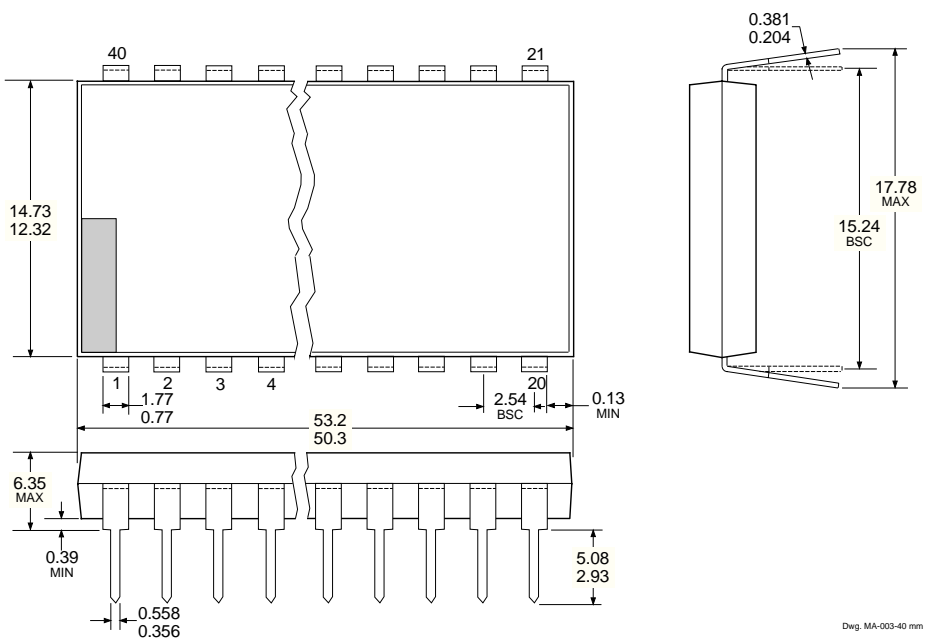
NOTES: 1. Lead thickness is measured at seating plane or below.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
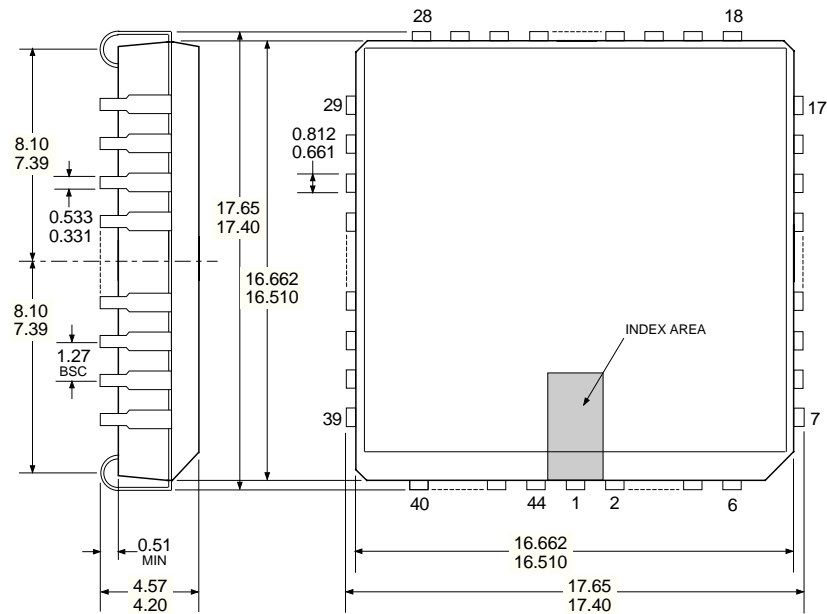
UCN5832EP
Dimensions in Inches
(controlling dimensions)

28   18

29

0.319
0.291

0.021
0.013

0.032
0.026

0.695
0.685

0.656
0.650

17

INDEX AREA

0.319
0.291

0.050
BSC

39

7

0.020
MIN

40   44 1 2   6

0.656
0.650

0.180
0.165

0.695
0.685
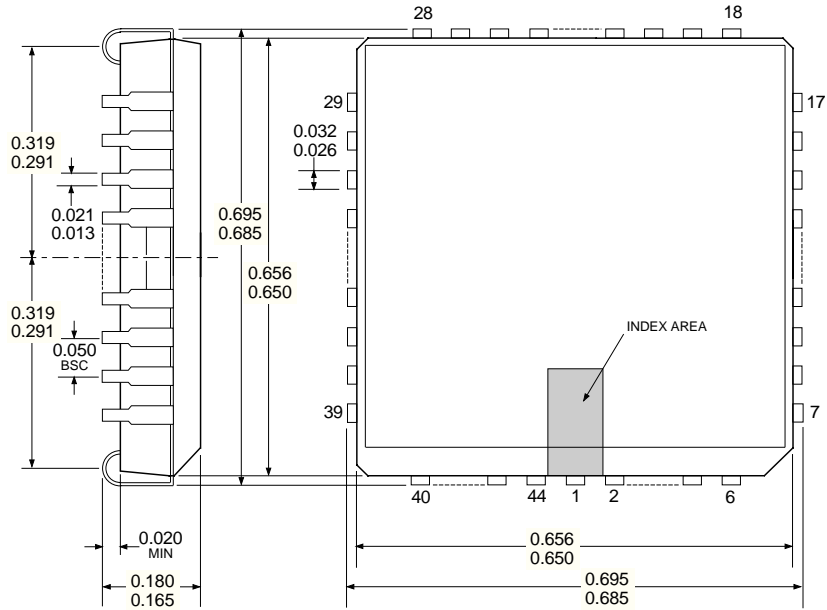
Dwg. MA-005-44A in

Dimensions in Millimeters
(for reference only)

28   18

29

8.10
7.39

0.533
0.331

0.812
0.661

17.65
17.40

16.662
16.510

17

INDEX AREA

8.10
7.39

1.27
BSC

39

7

0.51
MIN

40   44 1 2   6

16.662
16.510

4.57
4.20

17.65
17.40

Dwg. MA-005-44A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
        2. Lead spacing tolerance is non-cumulative.

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BiMOS II (Series 5800) & DABiC IV (Series 6800) INTELLIGENT POWER INTERFACE DRIVERS SELECTION GUIDE

Function	Output Ratings *		Part Number †
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
9-Bit	1.6 A	50 V	5829
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6809/10
12-Bit (active pull-downs)	-25 mA	60 V	5811 and 6811
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
SPECIAL-PURPOSE FUNCTIONS			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

*   Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits.
     Negative current is defined as coming out of (sourcing) the output.

†   Complete part number includes additional characters to indicate operating temperature range and package style.

‡   Internal transient-suppression diodes included for inductive-load protection.

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