

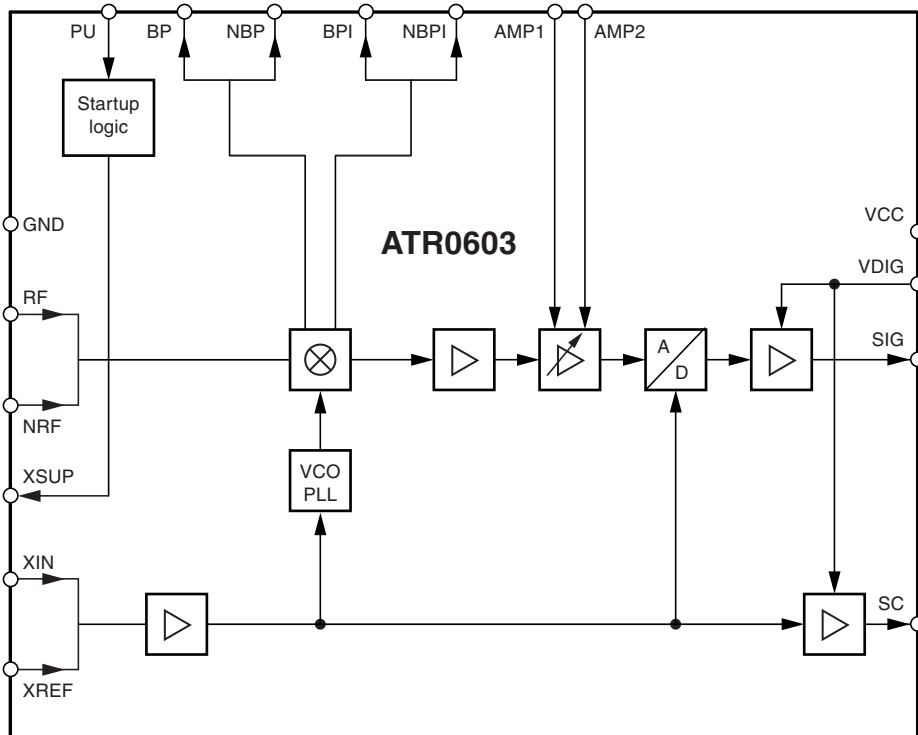
## Features

- Very Low Power Design
- Single IF Architecture
- Excellent Noise Performance
- 1-bit ADC on Chip
- Small QFN Package (4 mm × 4 mm, 24 Pins)
- Highly Integrated, Few External Components
- Advanced BiCMOS Technology (UHF6s)
- Supply Switch for External Circuitry (e.g., TCXO)
- Non-ESD-sensitive Device

## 1. Description

The ATR0603 is a single-IF GPS front-end IC, designed to meet the requirements of mobile and automotive applications. Excellent RF performance combined with high bandwidth and a low noise figure enables high-quality GPS solutions, and its very low power consumption is a perfect match for portable devices. Featuring a fully integrated balanced frequency synthesizer, only a few external components are required. The gain of the IF amplifier can be set to three different levels in order to meet the requirements for various applications. Several types of external oscillators can be connected to the robust TCXO interface. The startup logic allows significant power saving due to very low power-down current and the ability to disable the external TCXO or even other external components. CMOS output drivers deliver a 1-bit data signal and a 16.367667-MHz clock signal to the baseband interface.

Figure 1-1. Block Diagram



## GPS Front-end IC

## ATR0603

## Preliminary



## 2. Pin Configuration

Figure 2-1. Pinning QFN24 (4 mm × 4 mm)

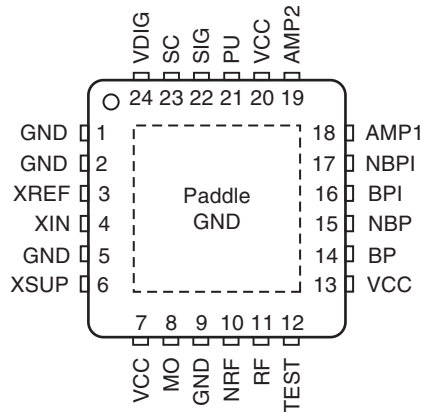


Table 2-1. Pin Description

| Pin    | Symbol | Type <sup>(1)</sup> | Function   |
|--------|--------|---------------------|--|
| Paddle | GND    | S                   | Common ground  |
| 1      | GND    | S                   | Ground   |
| 2      | GND    | S                   | Ground   |
| 3      | XREF   | A_I                 | TCXO interface ground  |
| 4      | XIN    | A_I                 | TCXO interface signal  |
| 5      | GND    | S                   | Ground   |
| 6      | XSUP   | XS                  | External circuitry supply switch                                 |
| 7      | VCC    | S                   | Analog supply  |
| 8      | MO     | A_O                 | Test buffer output ( $f_{IF}$ )                                  |
| 9      | GND    | S                   | Ground   |
| 10     | NRF    | A_I                 | Complementary RF input   |
| 11     | RF     | A_I                 | RF input   |
| 12     | TEST   | D_I                 | Enable test buffer   |
| 13     | VCC    | S                   | Analog supply  |
| 14     | BP     | A_O                 | IF filter interface (mixer output, open collector)               |
| 15     | NBP    | A_O                 | IF filter interface (complementary mixer output, open collector) |
| 16     | BPI    | A_I                 | IF filter interface (IF input)                                   |
| 17     | NBPI   | A_I                 | IF filter interface (complementary IF input)                     |
| 18     | AMP1   | D_I                 | IF gain control bit #1   |
| 19     | AMP2   | D_I                 | IF gain control bit #2   |
| 20     | VCC    | S                   | Analog supply  |
| 21     | PU     | D_I                 | Power-up signal input  |
| 22     | SIG    | D_O                 | Data output  |
| 23     | SC     | D_O                 | Sample clock   |
| 24     | VDIG   | S                   | Digital supply   |

Notes: 1. Type: A\_I = Analog input, A\_O = Analog output, D\_I = Digital input, D\_O = Digital output, S = Supply, XS = External supply

## 3. Functional Description

### 3.1 General Description

The ATR0603 GPS receiver IC has been especially designed for GPS applications in both mobile phone and automotive applications. From this system point of view, it incorporates high-level isolation between GPS and cellular bands, as well as very low power consumption.

The L1 input signal ( $f_{RF}$ ) is a direct sequence spread spectrum (DSSS) signal with a center frequency of:  $f_{RF} = 1575.42$  MHz.

The digital modulation scheme is bi-phase shift keying (BPSK) with a chip rate of 1.023 Mbps.

As the input signal power at the antenna is approximately  $-140$  dBm, the desired signal is below the thermal noise floor.

### 3.2 Startup Logic

The startup logic ensures reliable operation within the recommended operating conditions. The external power control signal PU is passed through a Schmitt trigger input to eliminate voltage ripple and prevent undesired behavior during startup and shutdown.

This block includes a switch to supply external circuits, for example, the TCXO. This switch is controlled by the power control signal PU.

### 3.3 TCXO Interface

This receiver is designed for use with an external TCXO. The TCXO output signal is fed to a balanced input buffer.

The recommended reference frequency is:  $f_{TCXO} = 16.367667$  MHz.

Connecting the supply pin of the TCXO to the XSUP pin of ATR0603 allows for a power down of the TCXO when the ATR0603 is shut off (see [Section 3.2](#)).

### 3.4 VCO/PLL

The frequency synthesizer features a balanced VCO and a fully integrated loop filter, thus no external components are required. The VCO combines very good phase noise behavior and excellent spurious suppression. The relation between the reference frequency ( $f_{TCXO}$ ) and the VCO center frequency ( $f_{VCO}$ ) is given by:

$$f_{VCO} = f_{TCXO} \times 90 = 16.367667 \text{ MHz} \times 90 = 1473.09003 \text{ MHz.}$$

### 3.5 RF Mixer/Image Filter

Combined with the antenna, an external LNA provides a first bandpass filtering of the signal. For the LNA, Atmel®'s ATR0610 is recommended, due to its low noise figure, high linearity and low power consumption. The output of the LNA drives a SAW filter, which provides image rejection for the mixer and the required isolation of all GSM bands. The output of the SAW filter is fed into a highly linear mixer with high conversion gain and excellent noise performance.

The IF frequency ( $f_{IF}$ ) is given by:

$$f_{IF} = f_{RF} - f_{VCO} = 1575.42 \text{ MHz} - 1473.09003 \text{ MHz} = 102.32997 \text{ MHz.}$$

### 3.6 IF Filter

The mixer directly drives an external LC bandpass filter via open collector outputs. In order to provide highest selectivity and conversion gain, it is recommended to design the external filter, according to the application proposal in chapter 10, as a 2-pole filter with a quality factor  $Q > 25$ .

### 3.7 IF Amplifier

The output of the IF filter drives an IF amplifier which is combined with additional low-pass filtering. The gain of this amplifier can be set to three different levels in order to optimally charge the input of the following analog-to-digital converter for each application.

The gain is internally set to high gain mode but can be adjusted by using external pull-down resistors at pin 18 (AMP1) and pin 19 (AMP2). If high gain mode is desired, pins 18 and 19 have to be left floating (see [Section 8. "Electrical Characteristics"](#) ).

### 3.8 A/D Converter

The analog-to-digital converter stage has a total resolution of 1 bit. It comprises a sub-sampling unit, clocked by the reference frequency ( $f_{TCXO}$ ). The frequency spectrum of the digital output signal ( $f_{OUT}$ ), present at the data output SIG, is then given by:  $f_{OUT} = | f_{IF} - f_{TCXO} \times n |$ . The selected sub-sampling factor ( $n = 6$ ) leads to the designated digital output signal, with a center frequency given by:

$$f_{OUT} = | f_{IF} - f_{TCXO} \times 6 | = | 102.32997 \text{ MHz} - 16.367667 \text{ MHz} \times 6 | = 4.123968 \text{ MHz}.$$

### 3.9 Clock and Data Driver

CMOS output drivers provide the output bit as well as the system clock to the baseband IC. The amplitude of this signal strongly depends on the value for the digital supply voltage (see [Section 8. "Electrical Characteristics" on page 7](#)).

## 4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters   | Symbol           | Value        | Unit |
|--|------------------|--------------|------|
| Analog supply voltage                                      | $V_{CC}$         | -0.3 to +3.7 | V    |
| Digital supply voltage                                     | $V_{DIG}$        | -0.3 to +3.7 | V    |
| Input voltage  | $V_{in}$         | -0.3 to +3.7 | V    |
| Max. supply voltage difference: $\Delta(V_{DIG} - V_{CC})$ | $V_{\Delta DIG}$ | 0.5          | V    |
| Max. supply voltage difference: $\Delta(V_{PU} - V_{CC})$  | $V_{\Delta PU}$  | 0.5          | V    |
| Operating temperature                                      | $T_{op}$         | -40 to +85   | °C   |
| Storage temperature  | $T_{stg}$        | -55 to +125  | °C   |

## 5. Thermal Resistance

| Parameters         | Symbol   | Value | Unit |
|--------------------|----------|-------|------|
| Thermal Resistance | $R_{th}$ | 45    | K/W  |

## 6. Operating Range

| Parameters             | Symbol     | Value        | Unit |
|------------------------|------------|--------------|------|
| Analog supply voltage  | $V_{CC}$   | 2.6 to 3.6   | V    |
| Digital supply voltage | $V_{DIG}$  | 1.6 to 3.6   | V    |
| Temperature range      | Temp       | -40 to +85   | °C   |
| Input frequency        | $f_{RF}$   | 1575.42      | MHz  |
| Reference frequency    | $f_{TCXO}$ | 16.3 to 16.4 | MHz  |

## 7. ESD Characteristics

| Parameters                           | Symbol    | Used Norm  | Value | Unit |
|--------------------------------------|-----------|--|-------|------|
| ESD level HBM (Human Body Model)     | $V_{HBM}$ | ESD-STM5.1-2001<br>JESD22-A114D 2006<br>AEC-Q100-002-Ref-D | 4000  | V    |
| ESD level MM (Machine Model)         | $V_{MM}$  | EIA/JESD22 A115 A  | 300   | V    |
| ESD level CDM (Charged Device Model) | $V_{CDM}$ | ESD-STM.5.3.1-1999   | 1000  | V    |

## 8. Electrical Characteristics

Temperature = +25°C

Minimum/maximum limits are at +25°C ambient temperature, unless otherwise specified.

| No.      | Parameters                            | Test Conditions                                       | Pin                                    | Symbol            | Min. | Typ.      | Max. | Unit | Type* |
|----------|---------------------------------------|---|--|-------------------|------|-----------|------|------|-------|
| <b>1</b> | <b>Common</b>                         |   |  |                   |      |           |      |      |       |
| 1.1      | Analog supply current                 | VCC = 3.6V,<br>VDIG = 1.6V,<br>V <sub>PU</sub> = 1.6V | 7, 13,<br>20                           | I <sub>S</sub>    |      | 10.5      |      | mA   | A     |
| 1.2      | Analog supply current                 | VCC = 2.6V,<br>VDIG = 1.6V,<br>V <sub>PU</sub> = 1.6V | 7, 13,<br>20                           | I <sub>S</sub>    |      | 9         |      | mA   | A     |
| 1.3      | Mixer core current                    | VCC = 3.6V,<br>VDIG = 1.6V,<br>V <sub>PU</sub> = 1.6V | 14, 15,<br>16, 17                      | I <sub>BP</sub>   |      | 1.5       |      | mA   | A     |
| 1.4      | Mixer core current                    | VCC = 2.6V,<br>VDIG = 1.6V,<br>V <sub>PU</sub> = 1.6V | 14, 15,<br>16, 17                      | I <sub>BP</sub>   |      | 1.4       |      | mA   | A     |
| 1.5      | Digital supply current <sup>(1)</sup> | VCC = 3.6V,<br>VDIG = 3.3V,<br>V <sub>PU</sub> = 1.6V | 24                                     | I <sub>DIG</sub>  |      | 1.4       |      | mA   | A     |
| 1.6      | Digital supply current <sup>(1)</sup> | VCC = 2.6V,<br>VDIG = 1.6V,<br>V <sub>PU</sub> = 1.6V | 24                                     | I <sub>DIG</sub>  |      | 1.0       |      | mA   | A     |
| 1.7      | Supply current in power-down mode     | V <sub>PU</sub> = V <sub>PU,off</sub>                 | 7, 13,<br>14, 15,<br>16, 17,<br>20, 24 | I <sub>PD</sub>   |      |           | 5    | μA   | A     |
| 1.8      | Noise figure (SSB)                    |   |  | NF <sub>tot</sub> |      | 8         |      | dB   | C     |
| <b>2</b> | <b>Mixer</b>                          |   |  |                   |      |           |      |      |       |
| 2.1      | Output frequency                      | f <sub>TCXO</sub> = 16.367667 MHz                     | 14, 15                                 | f <sub>IF</sub>   |      | 102.32997 |      | MHz  | A     |
| 2.2      | Input impedance (balanced)            | f <sub>RF</sub> = 1575.42 MHz                         | 10, 11                                 | Z <sub>11</sub>   |      | 10 - j80  |      | Ω    | C     |
| 2.3      | Conversion gain                       | Recommended IF filter                                 | 8                                      | G <sub>MIX</sub>  |      | 20        |      | dB   | B     |
| 2.4      | Noise figure (SSB)                    |   | 8                                      | NF <sub>MIX</sub> |      | 6.8       |      | dB   | C     |
| <b>3</b> | <b>IF Amplifier</b>                   |   |  |                   |      |           |      |      |       |
| 3.1      | IF gain0                              | AMP1 = AMP2 = low                                     | 18, 19                                 | G <sub>IF0</sub>  |      | 28        |      | dB   | D     |
| 3.2      | IF gain1                              | AMP1 = X <sup>(2)</sup> ,<br>AMP2 = low               | 18, 19                                 | G <sub>IF1</sub>  |      | 42        |      | dB   | D     |
| 3.3      | IF gain2                              | AMP1 = low, AMP2 = X                                  | 18, 19                                 | G <sub>IF2</sub>  |      | 42        |      | dB   | D     |
| 3.4      | IF gain3                              | AMP1 = AMP2 = X                                       | 18, 19                                 | G <sub>IF3</sub>  |      | 56        |      | dB   | D     |

\*) Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Capacitive load (C<sub>L</sub> = 10 pF) at pins 22, 23

2. X represents a pin left floating (internal pull up)

## 8. Electrical Characteristics (Continued)

Temperature = +25°C

Minimum/maximum limits are at +25°C ambient temperature, unless otherwise specified.

| No.                            | Parameters               | Test Conditions                                    | Pin  | Symbol          | Min. | Typ.                 | Max. | Unit     | Type* |
|--------------------------------|--------------------------|--|------|-----------------|------|----------------------|------|----------|-------|
| <b>4 Clock and Data Driver</b> |                          |  |      |                 |      |                      |      |          |       |
| 4.1                            | Clock driver frequency   | $f_{TCXO} = 16.367667 \text{ MHz}$                 | 23   | $f_{CLK}$       |      | 16.367667            |      | MHz      | A     |
| 4.2                            | Clock input level        | $f_{TCXO} = 16.367667 \text{ MHz}$                 | 3, 4 | $V_{TCXO}$      | 0.1  | 0.5                  |      | $V_{pp}$ | D     |
| 4.3                            | Clock output level, high | $C_{load,max} = 10 \text{ pF}$                     | 23   | $V_{CLK,high}$  |      | $0.9 \times V_{DIG}$ |      | V        | B     |
| 4.4                            | Clock output level, low  | $C_{load,max} = 10 \text{ pF}$                     | 23   | $V_{CLK,low}$   |      | $0.1 \times V_{DIG}$ |      | V        | B     |
| 4.5                            | Data output level, high  | $C_{load,max} = 10 \text{ pF}$                     | 22   | $V_{Data,high}$ |      | $0.9 \times V_{DIG}$ |      | V        | B     |
| 4.6                            | Data output level, low   | $C_{load,max} = 10 \text{ pF}$                     | 22   | $V_{Data,low}$  |      | $0.1 \times V_{DIG}$ |      | V        | B     |
| <b>5 Startup Logic</b>         |                          |  |      |                 |      |                      |      |          |       |
| 5.1                            | Voltage level power-on   |  | 21   | $V_{PU,on}$     | 1.4  |                      |      | V        | A     |
| 5.2                            | Voltage level power-off  |  | 21   | $V_{PU,off}$    |      |                      | 0.8  | V        | A     |
| 5.3                            | Voltage level at XSUP    | $I_{xsup} = 2 \text{ mA},$<br>$V_{PU} = V_{PU,on}$ | 6    | $V_{XSUP}$      |      | $(VCC - 0.1)$        |      | V        | A     |

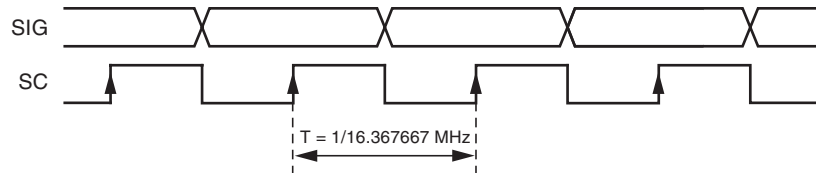
\*) Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Capacitive load ( $C_L = 10 \text{ pF}$ ) at pins 22, 23

2. X represents a pin left floating (internal pull up)

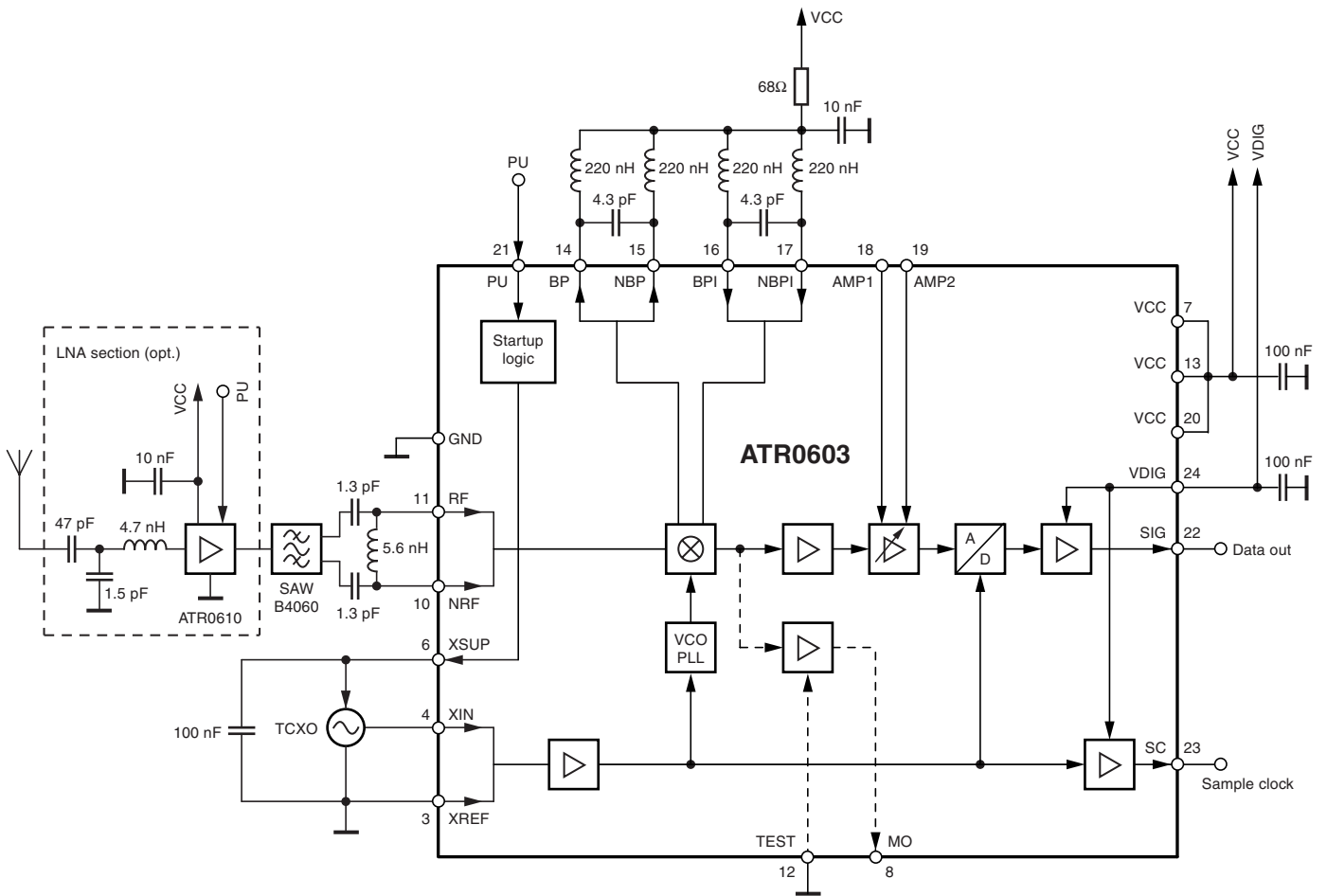
## 9. Output Interface

Figure 9-1. Data Output SIG Is Valid with Rising Edge of Sample Clock SC



# 10. Application Circuit

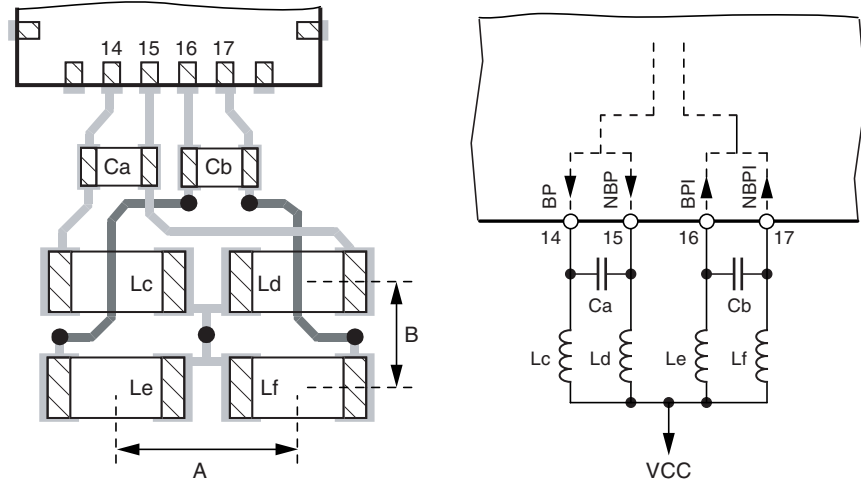
Figure 10-1. Application Example



Note: See also the recommended IF filter layout, shown in [Figure 10-2 on page 9](#).



Figure 10-2. Recommended IF Filter: Layout versus Schematic



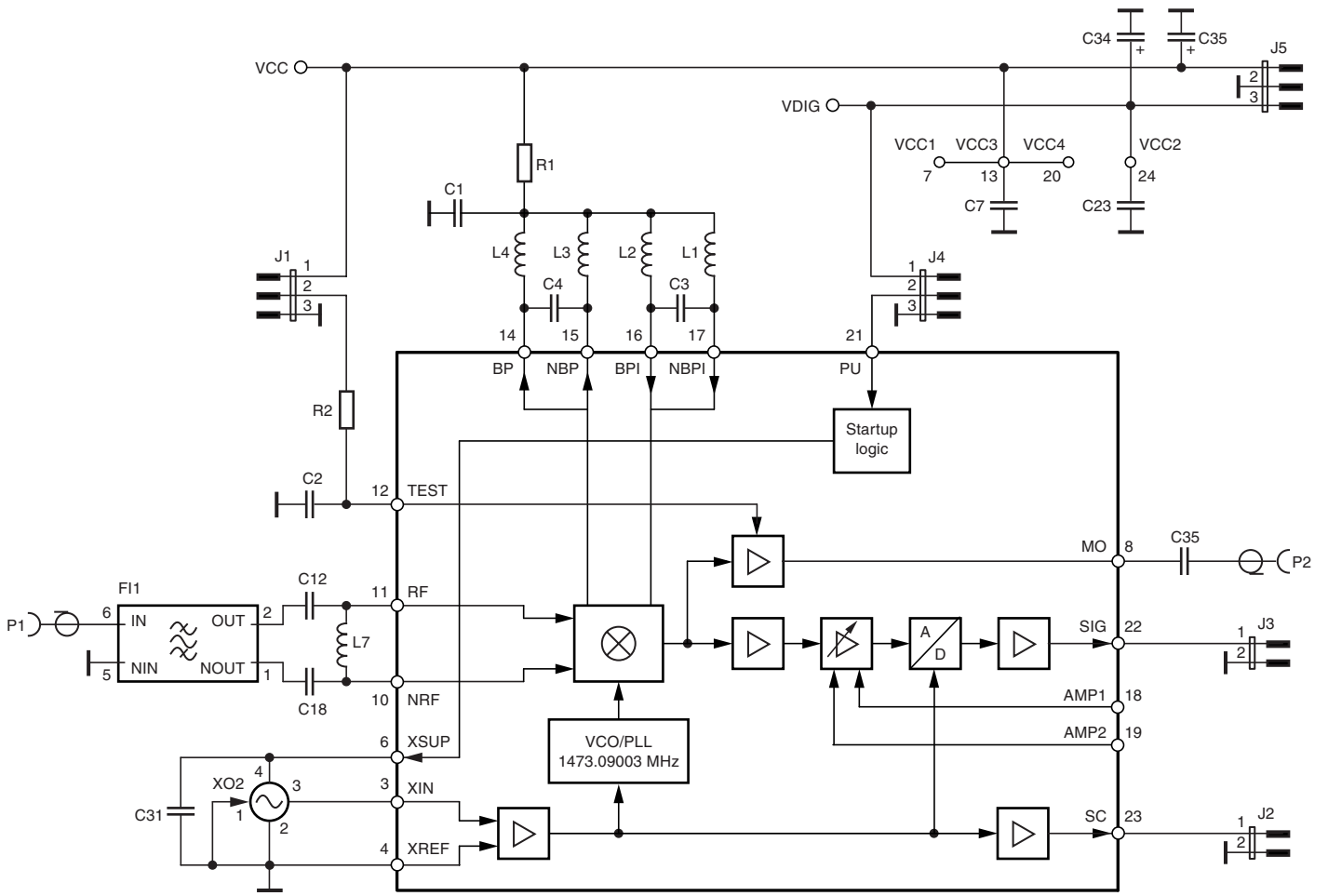
Note: Mutual inductance between the four inductors Lc to Lf plays an important role in the IF filter characteristics. In any design, the layout arrangement shown in Figure 10-2 should be followed as closely as possible. Measurements: A = 2.8 mm; B = 1.4 mm  
 Lc to Lf: Wire-wound SMD inductors, size 0603 (see Table 11-1 on page 11)

Table 10-1. Specifications of Recommended TCXO (Rakon; IT5325BE 16.367667 MHz)

| Parameter                     | Comment                              | Min. | Nominal   | Max. | Unit |
|-------------------------------|--------------------------------------|------|-----------|------|------|
| Nominal frequency             | Nominal frequency referenced to 25°C |      | 16.367667 |      | MHz  |
| Frequency deviation           | Within operating temperature range   |      |           | ±2.5 | ppm  |
| Temperature range             | Operating temperature range          | -40  |           | 85   | °C   |
| Output waveform               | DC-coupled clipped sine wave         |      |           |      |      |
| Output voltage (peak to peak) | At minimum supply voltage            | 0.8  |           |      | V    |
| Current                       | At maximum supply voltage            |      |           | 1.5  | mA   |
| Output load capacitance       | Tolerable load capacitance           | 9    |           | 11   | pF   |

# 11. Demonstration Board

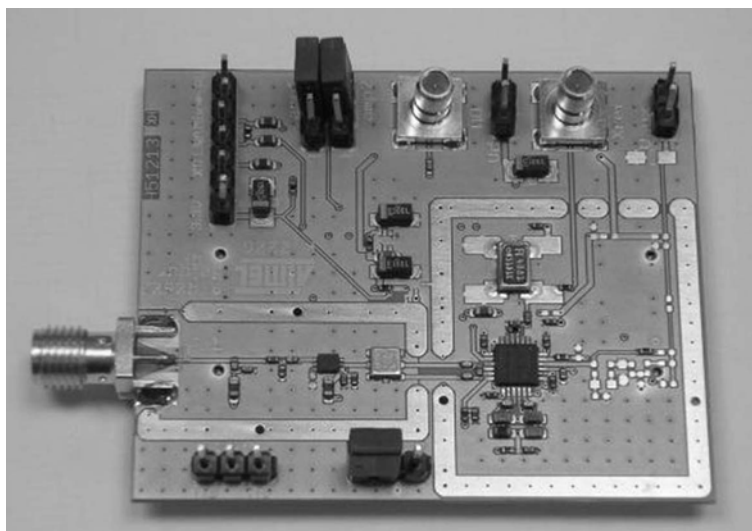
Figure 11-1. Schematic of Demonstration Board (Without LNA Section)



**Table 11-1.** Bill of Materials for the Demonstration Board (Without LNA Section)

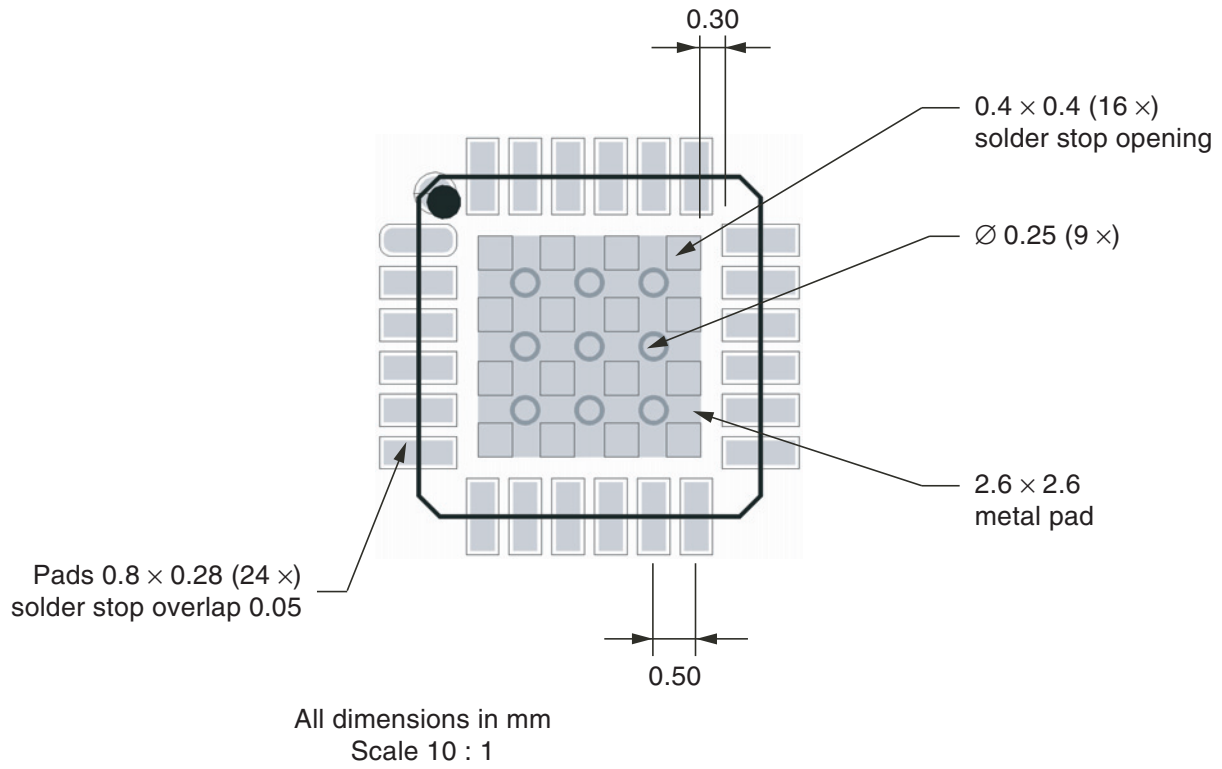
| Qty | Value                     | Parts            | Tolerance | Voltage | Material | Manufacturer                                    | Manufacturer Order Code     |
|-----|---------------------------|------------------|-----------|---------|----------|---|-----------------------------|
| 2   |                           | J2, J3           |           |         |          | Molex®  | 90120-0762                  |
| 3   |                           | J1, J4, J5       |           |         |          | Molex   | 90120-0763                  |
| 1   | 0                         | R2               |           |         |          | Vishay®   | CRCW0402000Z                |
| 2   | 1p3                       | C12, C18         | 0.1 pF    | 16V     | C0G      | Taiyo Yuden®                                    | EVK105CH1R3BW               |
| 2   | 4p3 ±0p1                  | C3, C4           | 0.1 pF    |         | C0G      | Murata®   | GRM1555C1H4R3GZ01B          |
| 1   | 5n6 2% Multilayer         | L7               | 2%        |         |          | Würth® Elektronik                               | 744784056G                  |
| 2   | 10μ                       | C5, C34          | 20%       | 16V     |          | Vishay  | 293D106X0016B2              |
| 1   | 10n                       | C1               | 5%        | 16V     | X7R      | Vishay  | VJ0402Y103JXJ               |
| 1   | 68                        | R1               | 5%        |         |          | Vishay  | CRCW0402680J                |
| 4   | 100n                      | C2, C7, C23, C31 | 20%       | 16V     | Y5V      | Vishay  | VJ0402V104MXJ               |
| 1   | 100p                      | C35              | 5%        | 25V     | C0G      | Vishay  | VJ0402A101JXXA.             |
| 1   | 142-0711-821              | P1               |           |         |          | Johnson Components™                             | 142-0711-821                |
| 4   | 220n 2%                   | L1, L2, L3, L4   | 2%        |         |          | Coilcraft®<br>alternatively<br>Würth Elektronik | 0603CS-R22XGB<br>744761222G |
| 1   | ATR0603-PFQW              | IC1              |           |         |          | Atmel   | ATR0603                     |
| 1   | B4060                     | FI1              |           |         |          | Epcos®  | B39162-B4060-U810           |
| 1   | IT5325BE<br>16.367667 MHz | XO2              | 2.0 ppm   |         |          | Rakon   | IT5325BE Ref. no. 34365     |
| 1   | R125426                   | P2               |           |         |          | Radiall®  | 125426                      |

**Figure 11-2.** Photo of Evaluation Board (Including LNA Section)



## 12. Recommended Footprint (QFN24 - 4 mm × 4 mm)

Figure 12-1. Recommended Footprint

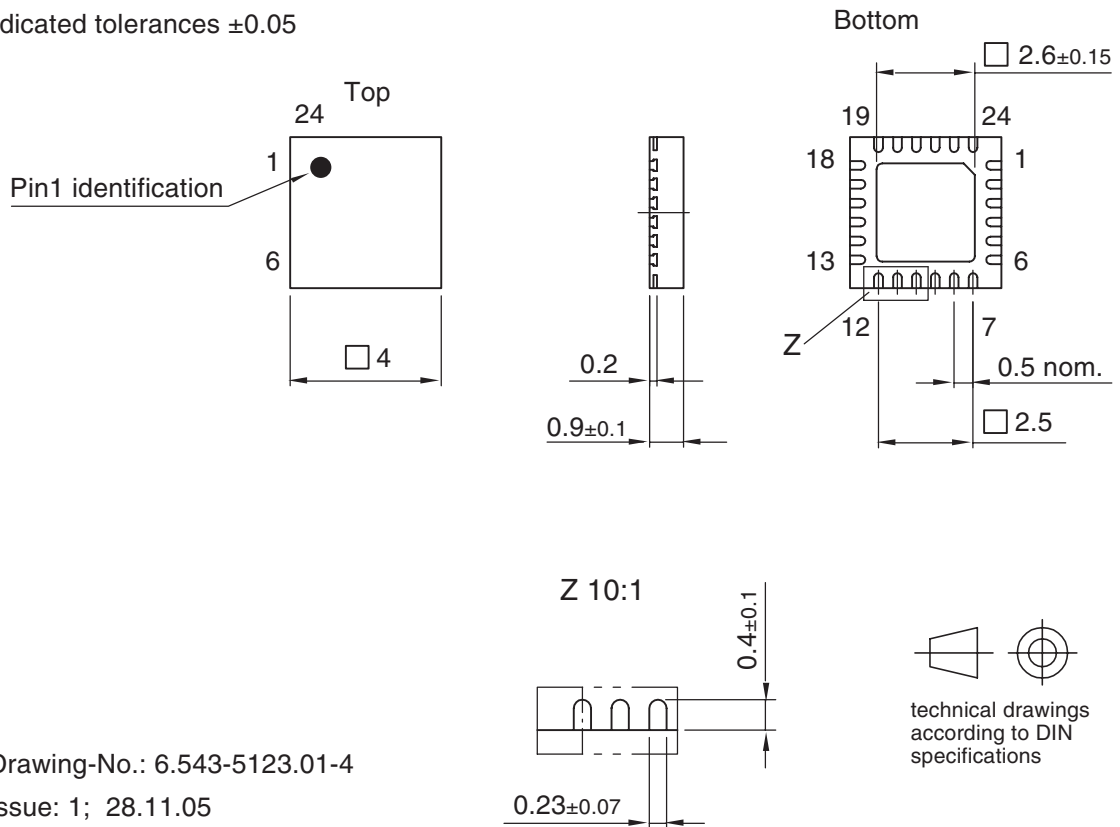


## 13. Ordering Information

| Extended Type Number | Package             | Remarks          |
|----------------------|---------------------|------------------|
| ATR0603-PFQW         | QFN24 - 4 mm × 4 mm | Taped and reeled |

## 14. Package Information

Package: QFN\_4 x 4\_24L  
 Exposed pad 2.6 x 2.6  
 Dimensions in mm  
 Not indicated tolerances  $\pm 0.05$



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