Features

- 16-channel GPS Correlator
  - 8192 Search Bins with GPS Acquisition Accelerator
  - Accuracy: 2.5m CEP (Stand-Alone, S/A off)
  - Time to First Fix: 34s (Cold Start)
  - Acquisition Sensitivity: –142 dBm (Cold Start)
  - Tracking Sensitivity: –158 dBm
- Utilizes the ARM7TDMI® ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - EmbeddedICE™ (In-circuit Emulator)
- 128 Kbyte Internal RAM
- 384 Kbyte Internal ROM, Firmware Version V5.0
- Position Technology Provided by µ-blox
- 6-channel Peripheral Data Controller (PDC)
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 2 External Interrupts
- 24 User-programmable I/O Lines
- 1 USB Device Port
  - Universal Serial Bus (USB) V2.0 Full-speed Device
  - Embedded USB V2.0 Full-speed Transceiver
  - Suspend/Resume Logic
  - Ping-pong Mode for Isochronous and Bulk Endpoints
- 2 USARTs
  - 2 Dedicated Peripheral Data Controller (PDC) Channels per USART
- Master/Slave SPI Interface
  - 2 Dedicated Peripheral Data Controller (PDC) Channels
  - 8-bit to 16-bit Programmable Data Length
  - 4 External Slave Chip Selects
- Programmable Watchdog Timer
- Advanced Power Management Controller (APMC)
  - Peripherals Can Be Deactivated Individually
  - Geared Master Clock to Reduce Power Consumption
  - Sleep State with Disabled Master Clock
  - Hibernate State with 32.768 kHz Master Clock
- Real Time Clock (RTC)
- 2.3V to 3.6V or 1.8V Core Supply Voltage
- Includes Power Supervisor
- 1.8V to 3.3V User-definable I/O Voltage for Several GPIOs with 5V Tolerance
- 4 Kbytes Battery Backup Memory
- 8 mm × 8 mm 56 Pin QFN56 Package
- RoHS-compliant, Green

GPS Baseband Processor SuperSense

ATR0625P1 Automotive

Summary

NOTE: This is a summary document. The complete document is available. For more information, please contact your local Atmel sales office.

4976AS–GPS–12/07

1. Description

The GPS baseband processor ATR0625P1 includes a 16-channel GPS correlator and is based on the ARM7TDMI processor core.

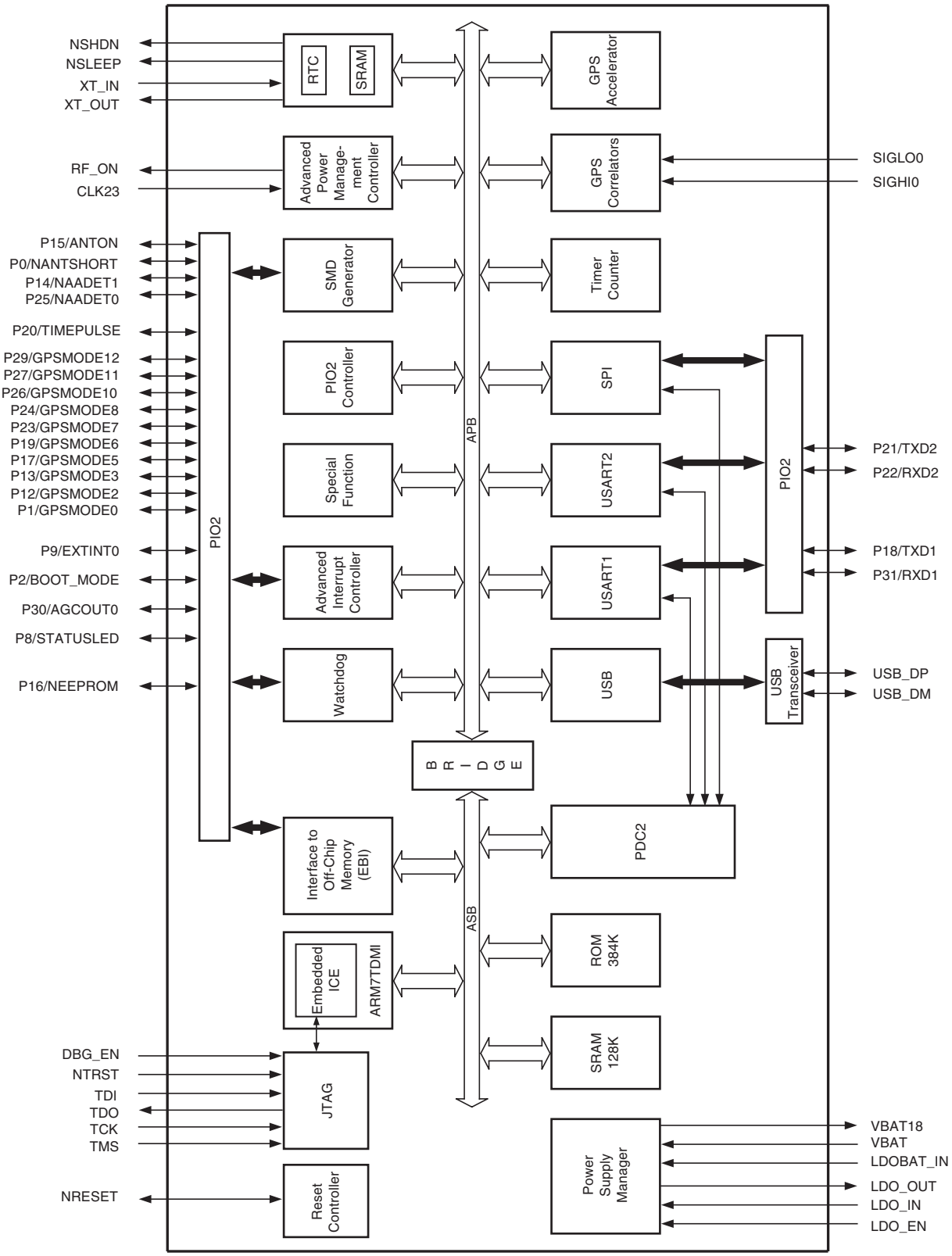
This processor has a high-performance 32-bit RISC architecture and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The ATR0625P1 has two USART and an USB device port. This port is compliant with the Universal Serial Bus (USB) V2.0 full-speed device specification.

The ATR0625P1 includes full GPS SuperSense® firmware, licensed from u-blox AG, which performs the basic GPS operation, including tracking, acquisition, navigation and position data output. For normal PVT (Position/Velocity/Time) applications, there is no need for off-chip Flash memory or ROM.

The firmware supports e.g. the NMEA® protocol (2.1 and 2.3), a binary protocol for PVT data, configuration and debugging, the RTCM protocol for DGPS, SBAS (WAAS, EGNOS and MSAS) and A-GPS (aiding). It is also possible to store the configuration settings in an optional external EEPROM.

The ATR0625P1 is manufactured using Atmel®'s high-density CMOS technology. By combining the ARM7TDMI microcontroller core with on-chip SRAM, 16-channel GPS correlator, and a wide range of peripheral functions on a monolithic chip, the ATR0625P1 provides a highly flexible and cost-effective solution for GPS applications.

Figure 1-1. ATR0625P1 Block Diagram



2. Architectural Overview

2.1 Description

The ATR0625P1 architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories. The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA™ Bridge provides an interface between the ASB and the APB.

An on-chip Peripheral Data Controller (PDC2) transfers data between the on-chip USARTs/SPI and the on-chip and off-chip memories without processor intervention. Most importantly, the PDC2 removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64K contiguous bytes without reprogramming the starting address. As a result, the performance of the microcontroller is increased and the power consumption reduced.

The ATR0625P1 peripherals are designed to be easily programmable with a minimum number of instructions. Each peripheral has a 16 Kbyte address space allocated in the upper 3 Mbyte of the 4 Gbyte address space. (Except for the interrupt controller, which has 4 Kbyte address space.) The peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status, and interrupt registers.

To maximize the efficiency of bit manipulation, frequently written registers are mapped into three memory locations. The first address is used to set the individual register bits, the second resets the bits, and the third address reads the value stored in the register. A bit can be set or reset by writing a “1” to the corresponding position at the appropriate address. Writing a “0” has no effect. Individual bits can thus be modified without having to use costly read-modify-write and complex bit-manipulation instructions.

All of the external signals of the on-chip peripherals are under the control of the Parallel I/O (PIO2) Controller. The PIO2 Controller can be programmed to insert an input filter on each pin or generate an interrupt on a signal change. After reset, the user must carefully program the PIO2 Controller in order to define which peripheral signals are connected with off-chip logic.

The ARM7TDMI processor operates in little-endian mode on the ATR0625P1 GPS Baseband. The processor's internal architecture and the ARM and Thumb instruction sets are described in the ARM7TDMI datasheet.

The ARM standard In-Circuit Emulator (ICE) debug interface is supported via the JTAG/ICE port of the ATR0625P1.

For features of the ROM firmware (SuperSense), refer to the software documentation available from u-blox AG, Switzerland.

3. Pin Configuration

3.1 Pinout

Figure 3-1. Pinout QFN56 (Top View)

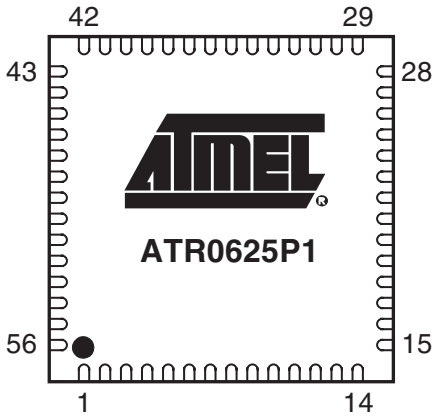


Table 3-1. ATR0625P1 Pinout

Pin Name	QFN56	Pin Type	Pull Resistor (Reset Value)[1]	Firmware Label	PIO Bank A	
					I	O
CLK23	37	OUT				
DBG_EN	8	IN	PD			
GND	[2]	IN				
LDOBAT_IN	21	IN				
LDO_EN	25	IN				
LDO_IN	20	IN				
LDO_OUT	19	OUT				
NRESET	41	I/O	Open Drain PU			
NSHDN	26	OUT				
NSLEEP	24	OUT				
NTRST	13	IN	PD			
P0	40	I/O	PD	NANTSHORT		
P1	47	I/O	Configurable (PD)	GPSMODE0		AGCOUT1
P2	46	I/O	Configurable (PD)	BOOT_MODE		“0”
P8	48	I/O	Configurable (PD)	STATUSLED		“0”
P9	29	I/O	PU to VBAT18	EXTINT0	EXTINT0	
P12	49	I/O	Configurable (PU)	GPSMODE2		NPCS2
P13	32	I/O	PU to VBAT18	GPSMODE3	EXTINT1	

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. Ground plane
3. VBAT18 represent the internal power supply of the backup power domain.
4. VDDIO is the supply voltage for the following GPIO-pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29.
5. VDD_USB is the supply voltage for following the USB-pins: USB_DM and USB_DP. For operation of the USB interface, supply of 3.0V to 3.6V is required.
6. This pin is not connected

Table 3-1. ATR0625P1 Pinout (Continued)

Pin Name	QFN56	Pin Type	Pull Resistor (Reset Value)[1]	Firmware Label	PIO Bank A	
					I	O
P14	1	I/O	Configurable (PD)	NAADET1		“0”
P15	17	I/O	PD	ANTON		
P16	6	I/O	Configurable (PU)	NEEPROM	SIGHI1	
P17	2	I/O	Configurable (PD)	GPSMODE5	SCK1	SCK1
P18	45	I/O	Configurable (PU)	TXD1		TXD1
P19	53	I/O	Configurable (PU)	GPSMODE6	SIGLO1	
P20	4	I/O	Configurable (PD)	TIMEPULSE	SCK2	SCK2
P21	52	I/O	Configurable (PU)	TXD2		TXD2
P22	30	I/O	PU to VBAT18	RXD2	RXD2	
P23	3	I/O	Configurable (PU)	GPSMODE7	SCK	SCK
P24	5	I/O	Configurable (PU)	GPSMODE8	MOSI	MOSI
P25	55	I/O	Configurable (PD)	NAADET0	MISO	MISO
P26	44	I/O	Configurable (PU)	GPSMODE10	NSS	NPCS0
P27	54	I/O	Configurable (PU)	GPSMODE11		NPCS1
P29	50	I/O	Configurable (PU)	GPSMODE12		NPCS3
P30	16	I/O	PD	AGCOUT0		AGCOUT0
P31	31	I/O	PU to VBAT18	RXD1	RXD1	
RF_ON	15	OUT	PD			
SIGHI0	38	IN				
SIGLO0	39	IN				
TCK	9	IN	PU			
TDI	10	IN	PU			
TDO	11	OUT				
TMS	12	IN	PU			
USB_DM	34	I/O				
USB_DP	35	I/O				
VBAT	22	IN				
VBAT18[3]	23	OUT				
VDD18	7, 14	IN				
VDD18	18, 36	IN				
VDD18	51	IN				
VDDIO[4]	43, 56	IN				
VDD_USB[5]	33	IN				
XT_IN	28	IN				
XT_OUT	27	OUT				
NC[6]	42					

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. Ground plane
3. VBAT18 represent the internal power supply of the backup power domain.
4. VDDIO is the supply voltage for the following GPIO-pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29.
5. VDD_USB is the supply voltage for following the USB-pins: USB_DM and USB_DP. For operation of the USB interface, supply of 3.0V to 3.6V is required.
6. This pin is not connected

3.2 Signal Description

Table 3-2. ATR0625P1 Signal Description

Module	Name	Function	Type	Active Level	Comment
EBI	BOOT_MODE	Boot Mode Input	Input	–	PIO-controlled after reset, internal pull-down resistor
USART	TXD1 to TXD2	Transmit Data Output	Output	–	PIO-controlled after reset
	RXD1 to RXD2	Receive Data Input	Input	–	PIO-controlled after reset
	SCK1 to SCK2	External Synchronous Serial Clock	I/O	–	PIO-controlled after reset
USB	USB_DP	USB Data (D+)	I/O	–	
	USB_DM	USB Data (D-)	I/O	–	
APMC	RF_ON		Output	–	Interface to ATR0601
AIC	EXTINT0-1	External Interrupt Request	Input	High/ Low/ Edge	PIO-controlled after reset
AGC	AGCOUT0-1	Automatic Gain Control	Output	–	Interface to ATR0601 PIO-controlled after reset
RTC	NSLEEP	Sleep Output	Output	Low	Interface to ATR0601
	NSHDN	Shutdown Output	Output	Low	Connect to pin LDO_EN
	XT_IN	Oscillator Input	Input	–	RTC oscillator
	XT_OUT	Oscillator Output	Output	–	RTC oscillator
SPI	SCK	SPI Clock	I/O	–	PIO-controlled after reset
	MOSI	Master Out Slave In	I/O	–	PIO-controlled after reset
	MISO	Master In Slave Out	I/O	–	PIO-controlled after reset
	NSS/NPCS0	Slave Select	I/O	Low	PIO-controlled after reset
	NPCS1 to NPCS3	Slave Select	Output	Low	PIO-controlled after reset
PIO	P0 to P31	Programmable I/O Port	I/O	–	Input after reset
GPS	SIGHI0	Digital IF	Input	–	Interface to ATR0601
	SIGLO0	Digital IF	Input	–	Interface to ATR0601
	SIGHI1	Digital IF	Input	–	PIO-controlled after reset
	SIGLO1	Digital IF	Input	–	PIO-controlled after reset
	TIMEPULSE	GPS synchronized time pulse	Output	–	PIO-controlled after reset
CONFIG	GPSMODE0-12	GPS Mode	Input	–	PIO-controlled after reset
	STATUSLED	Status LED	Output	–	PIO-controlled after reset
	NEEPROM	Enable EEPROM Support	Input	Low	PIO-controlled after reset
	ANTON	Active antenna power on Output	Output	–	PIO-controlled after reset
	NANTSHORT	Active antenna short circuit detection Input	Input	Low	PIO-controlled after reset
	NAADET0-1	Active antenna detection Input	Input	Low	PIO-controlled after reset

Note: 1. The USB transceiver is disabled if VDD_USB < 2.0V. In this case the pins USB_DM and USB_DP are connected to GND (internal pull-down resistors). The USB transceiver is enabled if VDD_USB is within 3.0V and 3.6V.

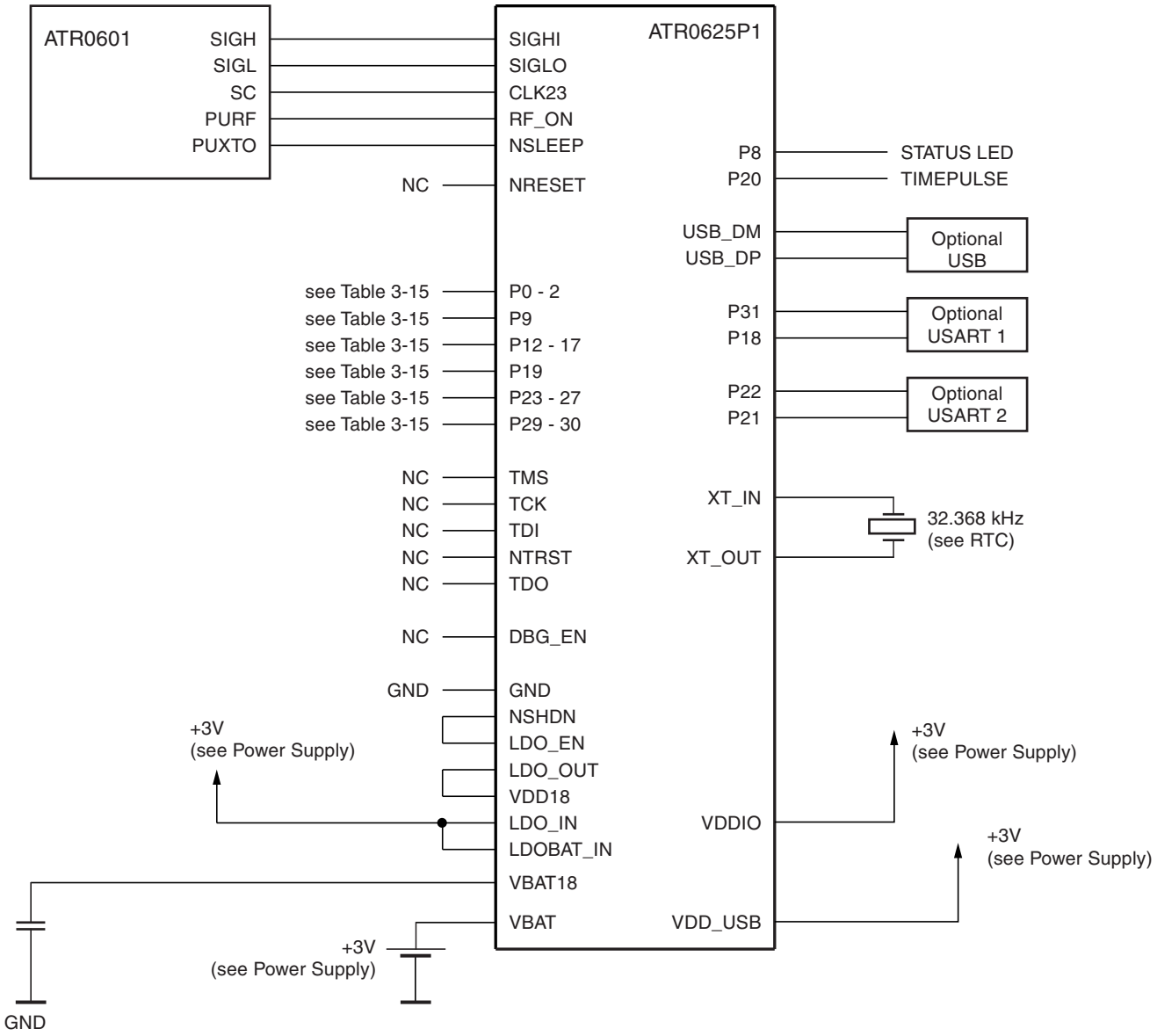
Table 3-2. ATR0625P1 Signal Description (Continued)

Module	Name	Function	Type	Active Level	Comment
JTAG/ICE	TMS	Test Mode Select	Input	–	Internal pull-up resistor
	TDI	Test Data In	Input	–	Internal pull-up resistor
	TDO	Test Data Out	Output	–	
	TCK	Test Clock	Input	–	Internal pull-up resistor
	NTRST	Test Reset Input	Input	Low	Internal pull-down resistor
	DBG_EN	Debug Enable	Input	High	Internal pull-down resistor
CLOCK	CLK23	Clock Input	Input	–	Interface to ATR0601, Schmitt trigger input
RESET	NRESET	Reset Input	I/O	Low	Open drain with internal pull-up resistor
POWER	VDD18		Power	–	Core voltage 1.8V
	VDDIO		Power	–	Variable IO voltage 1.65V to 3.6V
	VDD_USB		Power	–	USB voltage 0 to 2.0V or 3.0V to 3.6V(1)
	GND		Power	–	Ground
LDOBAT	LDOBAT_IN		Power	–	2.3V to 3.6V
	VBAT		Power	–	1.5V to 3.6V
	VBAT18		Out	–	1.8V backup voltage
LDO18	LDO_IN	LDO In	Power	–	2.3V to 3.6V
	LDO_OUT	LDO Out	Power	–	1.8V core voltage, max. 80 mA
	LDO_EN	LDO Enable	Input	–	

Note: 1. The USB transceiver is disabled if VDD_USB < 2.0V. In this case the pins USB_DM and USB_DP are connected to GND (internal pull-down resistors). The USB transceiver is enabled if VDD_USB is within 3.0V and 3.6V.

3.3 External Connections for a Working GPS System

Figure 3-2. Example of an External Connection



NC: Not connected

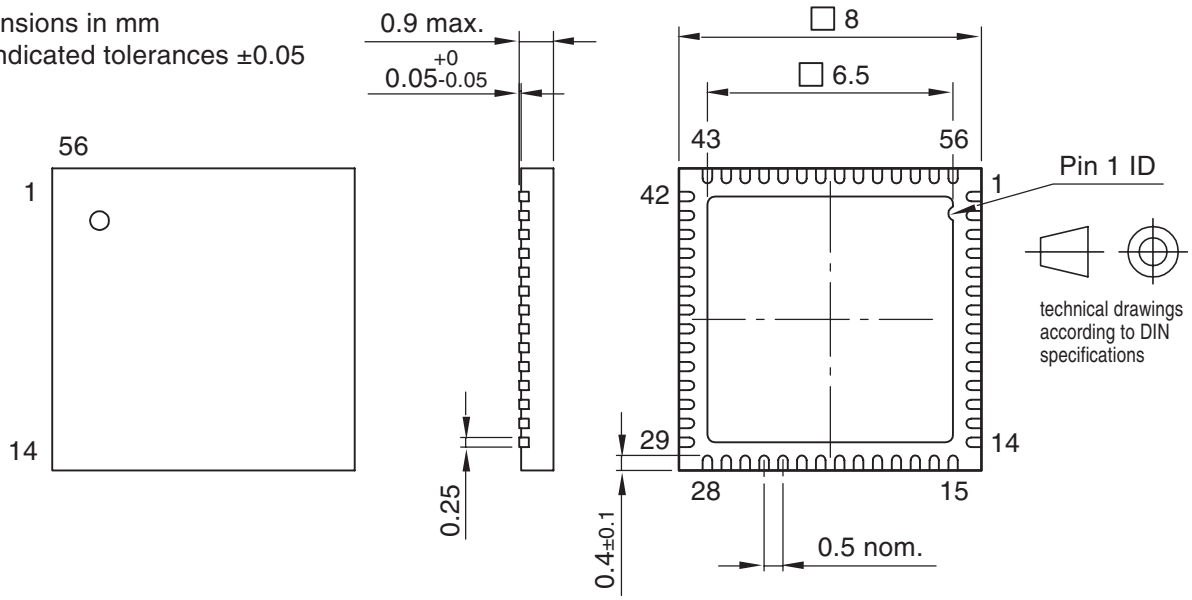
4. Ordering Information

Extended Type Number	Package	MPQ	Remarks
ATR0625P1-PYQW	QFN56	2000	8 mm × 8 mm, 0.50 mm pitch, RoHS-compliant, green, automotive type
ATR0625-EK1	-	1	Evaluation kit/Road test kit
ATR0625-DK1	-	1	Development kit including example design information

5. Package QFN56

Package: QFN56 8 x 8
Exposed pad 6.5 x 6.5

Dimensions in mm
Not indicated tolerances ±0.05



Drawing-No.: 6.543-5121.01-4

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Moisture sensitivity level (MSL) = 3

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