256Kx32 STATIC RAM CMOS, HIGH SPEED MODULE

FEATURES

- 256Kx32 bit CMOS Static RAM
  - Access Times: 15, 20, and 25ns
  - Individual Byte Selects
  - Fully Static, No Clocks
  - TTL Compatible I/O
- High Density Package with JEDEC Standard Pinouts
  - 72 Pin SIMM No. 175 (Angle)
  - 72 Pin ZIP No. 176
  - 72 Pin SIMM, No. 354 (Straight)
- Single +5V (±10%) Supply Operation

DESCRIPTION

The EDI8F32259C is a high speed 8Mb Static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256Kx4 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip enables (EØ# - E3#) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The EDI8F32259C is offered in 72 pin ZIP/SIMM package which enables eight megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

The ZIP and SIMM modules contain four PD (Presence Detect) pins which are used to identify module memory density in applications where alternate modules can be interchanged.

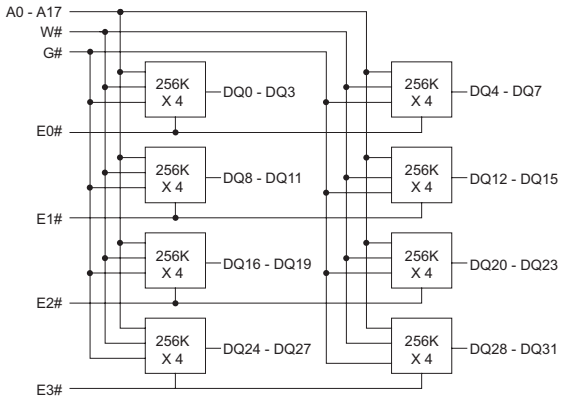
FIG. 1 PIN CONFIGURATIONS AND BLOCK DIAGRAM

NC	1	E4#	37
NC	2	E3#	38
PD3	3	A17	39
PD4	4	A16	40
V_{SS}	5	G#	41
PD1	6	V_{SS}	42
PD2	7	DQ24	43
DQ0	8	DQ16	44
DQ8	9	DQ25	45
DQ1	10	DQ17	46
DQ9	11	DQ26	47
DQ2	12	DQ18	48
DQ10	13	DQ27	49
DQ3	14	DQ19	50
DQ11	15	A3	51
V_{CC}	16	A10	52
A0	17	A4	53
A7	18	A11	54
A1	19	A5	55
A8	20	A12	56
A2	21	V_{CC}	57
A9	22	A13	58
DQ12	23	A6	59
DQ4	24	DQ20	60
DQ13	25	DQ28	61
DQ5	26	DQ21	62
DQ14	27	DQ29	63
DQ6	28	DQ22	64
DQ15	29	DQ30	65
DQ7	30	DQ23	66
V_{SS}	31	DQ31	67
W#	32	V_{SS}	68
A15	33	NC	69
A14	34	NC	70
E2#	35	NC	71
E1#	36	NC	72

PD 1,2 = V_{SS}
PD 3,4 = Open

PIN NAMES

AØ-A17	Address Inputs
EØ#-E3#	Chip Enables
W#	Write Enables
G#	Output Enable
DQØ-DQ31	Common Data Input/Output
V_{CC}	Power (+5V±10%)
V_{SS}	Ground



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature TA (Ambient) Commercial Industrial	 0°C to +70°C -40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	7.5 Watt
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	--	V_{CC}+0.3V	V
Input Low Voltage	V_{IL}	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Max 15-25	Units ns
Operating Power Supply Current	I_{CC1}	W3, E# = V_{IL}, I I/O = 0mA, Min Cycle	—	800	mA
Standby (TTL) Power Supply Current	I_{CC2}	E# ≥ V_{IH}, V_{IN} ≤ V_{IL} or V_{IN} ≥ V_{IH}	—	240	mA
Full Standby Power Supply Current CMOS	I_{CC3}	E# ≥ V_{CC}-0.2V V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V	—	40	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}	—	±80	µA
Output Leakage Current	I_{LO}	V I/O = 0V to V_{CC}	—	±20	µA
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	—	0.4	V

*Typical: T_A = 25°C, V_{CC} = 5.0V

TRUTH TABLE

E#	W#	G#	Mode	Output	Power
H	X	X	Standby	HIGH Z	I_{CC3}
L	H	L	Read	DOUT	I_{CC1}
L	L	X	Write	DIN	I_{CC1}
L	H	H	Output Deselect	HIGH Z	I_{CC1}

CAPACITANCE

(f=1.0MHz, V_{IN}=V_{CC} or V_{SS})

Parameter	Sym	Max	Unit
Address Lines	CI	60	pF
Data Lines	CD/Q	20	pF
Chip Enable Line	CC	20	pF
Write Control Line	CN	60	pF

These parameters are sampled, not 100% tested.

AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	15		20		25		ns
Address Access Time	t_{AVQV}	t_{AA}		15		20		25	ns
Chip Enable Access	t_{ELQV}	t_{ACS}		15		20		25	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		7		9		9	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		7		9		9	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		ns
Output Disable to Output in High Z (1)	t_{GHQZ}	t_{OHZ}		7		9		9	ns

Note 1: Parameter guaranteed, but not tested.

FIG. 2 READ CYCLE 1 - W# HIGH, G#, E# LOW

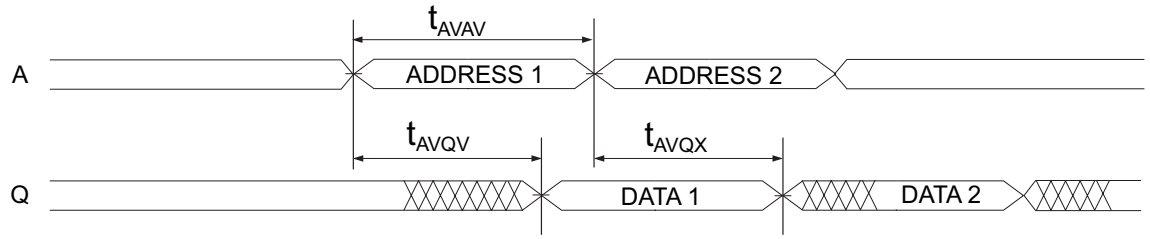
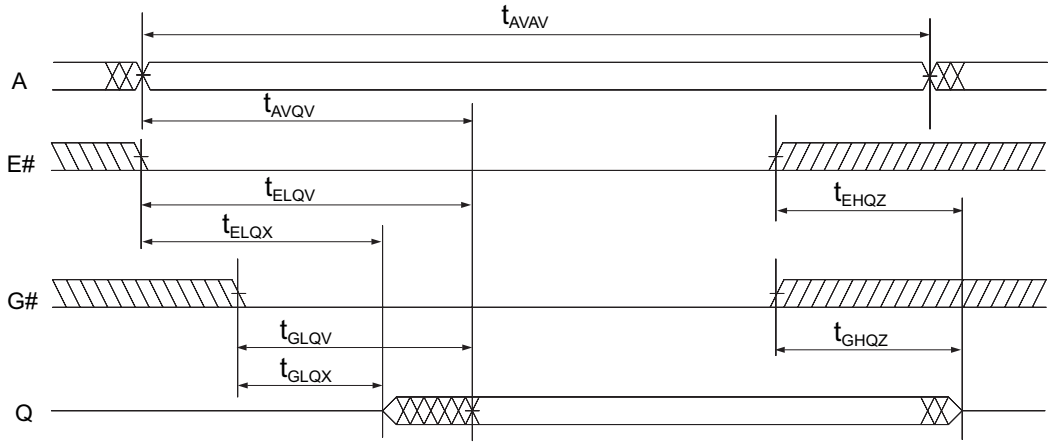


FIG. 3 READ CYCLE 2 - W# HIGH



AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	15		20		25		ns
Chip Enable to End of Write	t_{ELWH} t_{WLEH}	t_{CW} t_{CW}	12 12		14 14		14 14		ns ns
Address Setup Time	t_{AVWL} t_{AVEL}	t_{AS} t_{AS}	0 0		0 0		0 0		ns ns
Address Valid to End of Write	t_{AVWH} t_{AVEH}	t_{AW} t_{AW}	12 12		14 14		14 14		ns ns
Write Pulse Width	t_{WLWH} t_{ELEH}	t_{WP} t_{WP}	12 12		14 14		14 14		ns ns
Write Recovery Time	t_{WHAX} t_{EHAX}	t_{WR} t_{WR}	0 0		0 0		0 0		ns ns
Data Hold Time	t_{WHDX} t_{EHDX}	t_{DH} t_{DH}	3 3		3 3		3 3		ns ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	7	0	9	0	9	ns
Data to Write Time	t_{DVWH} t_{DVEH}	t_{DW} t_{DW}	7 7		8 8		8 8		ns ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

FIG. 4 WRITE CYCLE 1 - W# CONTROLLED

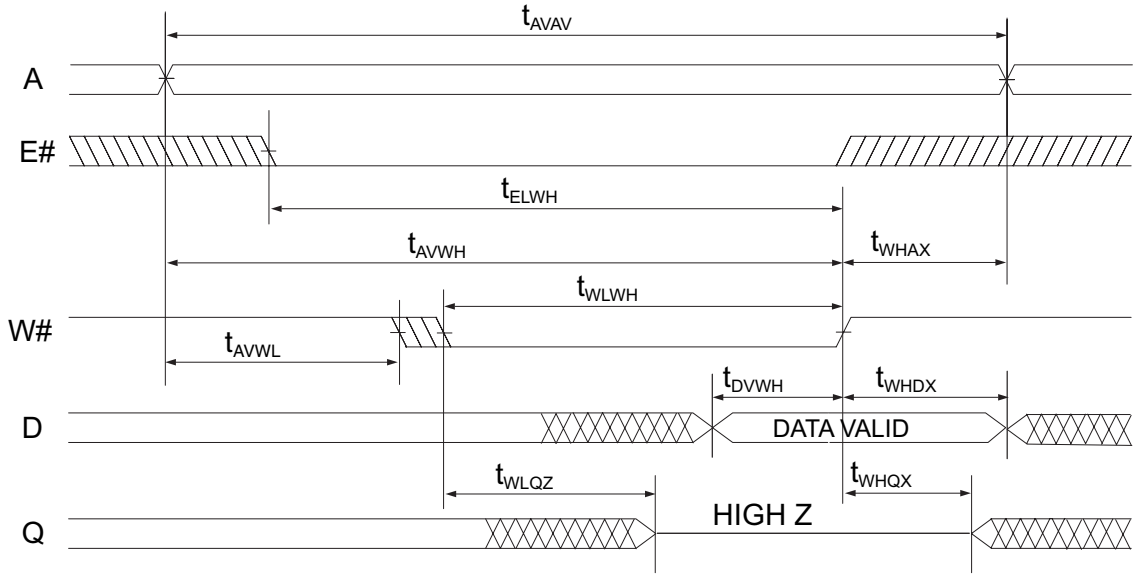
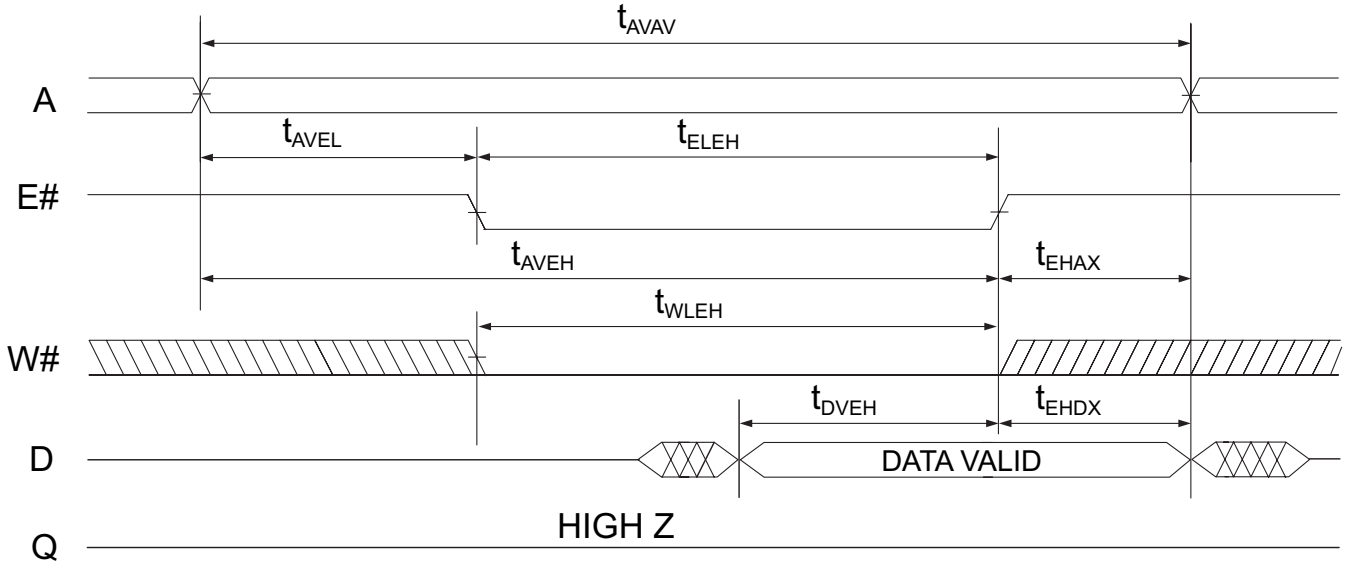


FIG. 5 WRITE CYCLE 2 - E# CONTROLLED



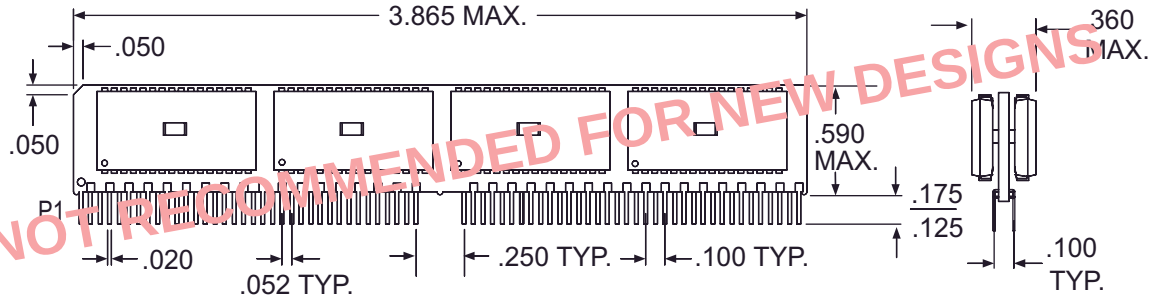
ORDERING INFORMATION

Part Number	Speed (ns)	Package No.
EDI8F32259C15MNC	15	176
EDI8F32259C20MNC	20	176
EDI8F32259C25MNC	25	176
EDI8F32259C15MMC	15	354
EDI8F32259C20MMC	20	354
EDI8F32259C25MMC	25	354
EDI8F32259C15MZC	15	175
EDI8F32259C20MZC	20	175
EDI8F32259C25MZC	25	175

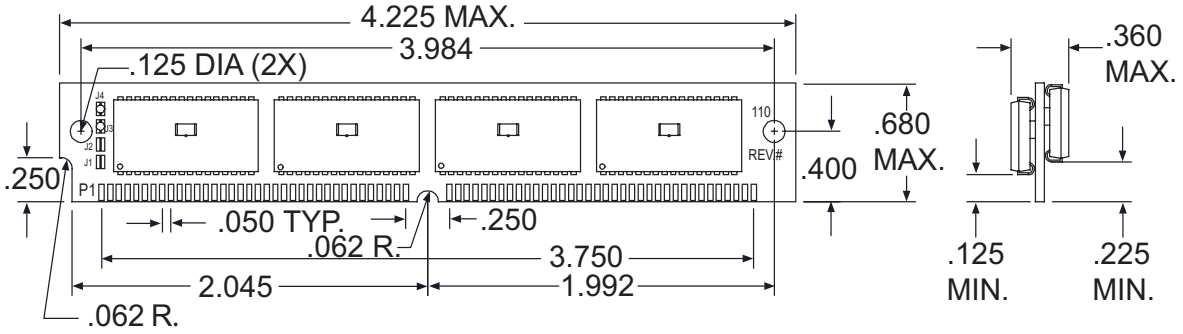
Note: For Gold SIMM, Change from EDI8F to EDI8G.

PACKAGE DESCRIPTION

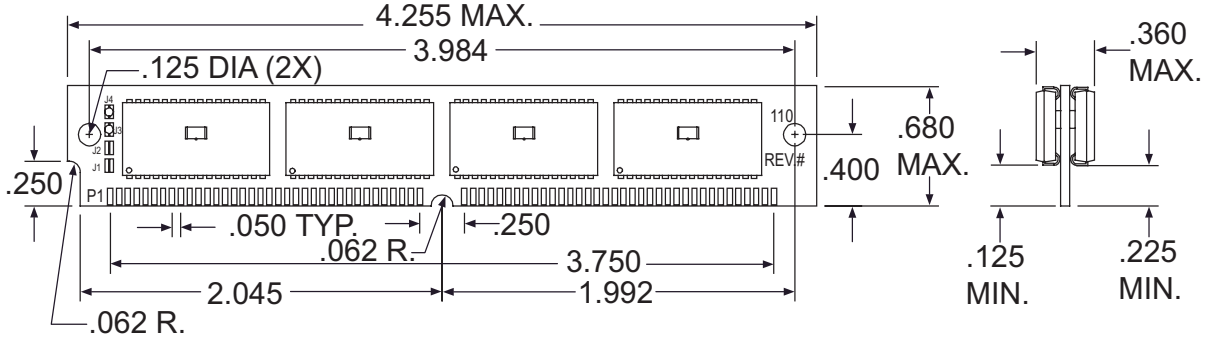
PACKAGE NO. 175: 72 PIN ZIP



PACKAGE NO. 176: 72 PIN SIMM ANGLED



PACKAGE NO. 354: 72 PIN SIMM STRAIGHT



ALL DIMENSIONS ARE IN INCHES

Document Title

256Kx32, Static RAM CMOS, High Speed Module

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	July 2006	Concept
Rev 3	3.1 Updated Access Timing Spec 3.2 Removed 12nc Option 3.3 Added new document title page	Aug. 2006	