



256Kx8 Monolithic SRAM

FEATURES

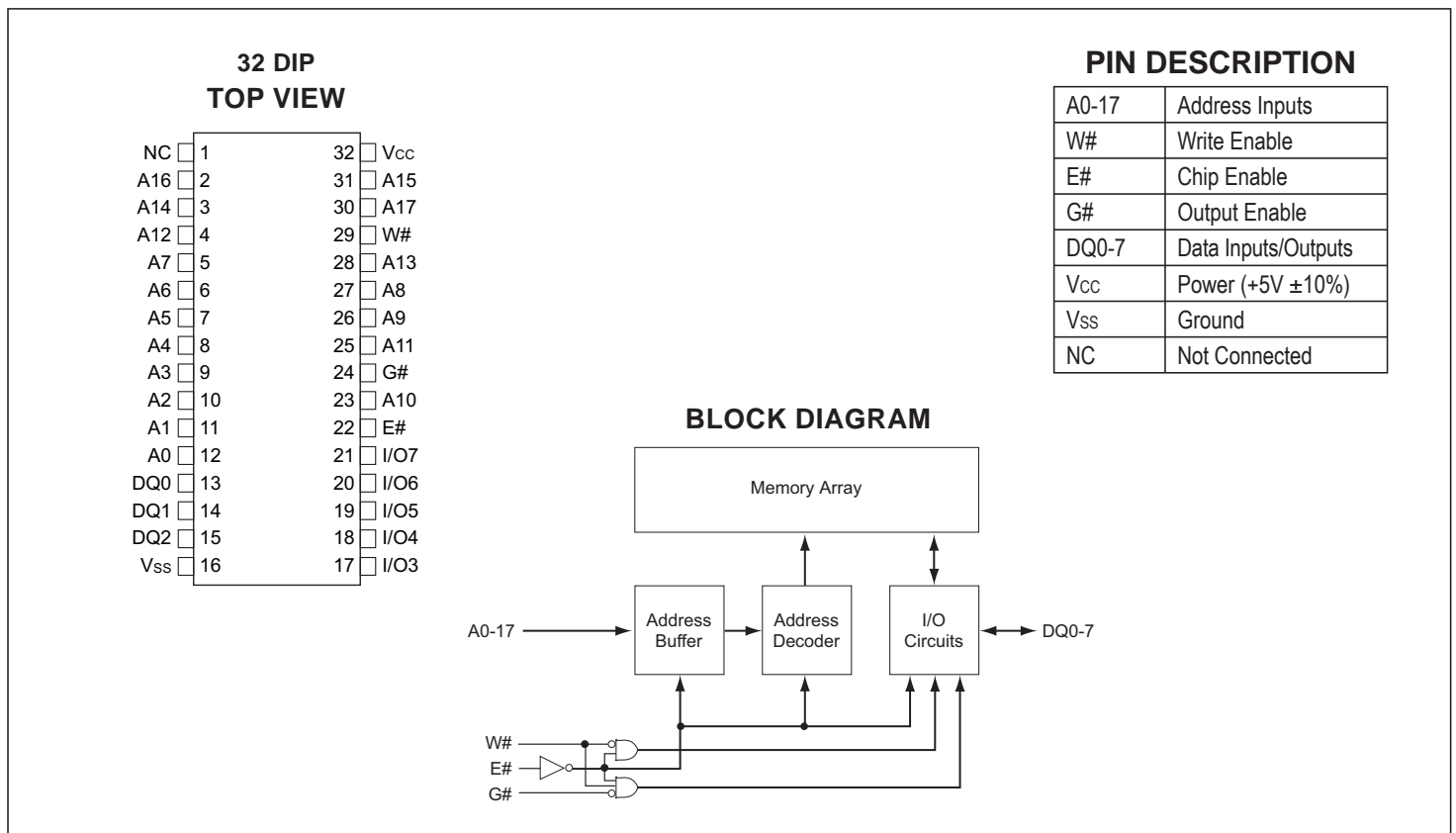
- 256Kx8 CMOS Static
- Random Access Memory
 - Access Times of 70, 85, 100ns
 - Data Retention Function (LP Versions)
 - TTL Compatible Inputs and Outputs
 - Fully Static, No Clocks
- JEDEC Approved Pinout
 - 32 pin Ceramic DIP, 0.6 mils wide (Package 9)
- Single +5V (±10%) Supply Operation

The EDI88257C is a 2 Megabit 256Kx8 bit Monolithic CMOS Static RAM.

The 32 pin DIP pinout adheres to the JEDEC standard for the two megabit device, and is a pin replacement for the 256Kx8 module, EDI88257C. The device is upgradeable to the 512Kx8 SRAM, the EDI88512C. Pin 1 becomes the higher order address.

A Low Power version, EDI88257LP, offers a data retention function for battery back-up operation. Military product is available compliant to Appendix A of MIL-PRF-38535.

FIGURE 1 – PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature TA (Ambient)	-40 to +85	°C
	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1	W
Output Current	20	mA
Junction Temperature, Tj	175	°C

NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

G#	E#	W#	Mode	Output	Power
X	H	X	Standby	High Z	Icc2, Icc3
H	L	H	Output Deselect	High Z	Icc1
L	L	H	Read	Data Out	Icc1
X	L	L	Write	Data In	Icc1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	—	VCC +0.5	V
Input Low Voltage	VIL	-0.3	—	+0.8	V

CAPACITANCE

Parameter	Symbol	Condition	Max	Unit
Address Lines	CI	VIN = VCC or VSS, f = 1.0MHz	30	pF
Data Lines	CO	VOUT = VCC or VSS, f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

VCC = 5V, TA = +25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Input Leakage Current	ILI	VIN = 0V to VCC	—	—	±10	µA	
Output Leakage Current	ILO	VIO = 0V to VCC	—	—	±10	µA	
Operating Power Supply Current	Icc1	W#, E# = VIL, IIO = 0mA, Min Cycle (70-100ns)	—	45	75	mA	
Standby (TTL) Power Supply Current	Icc2	E# ≥ VIH, VIN ≤ VIL, VIN ≥ VIH	—	3	10	mA	
Full Standby Power Supply Current	Icc3	E# ≥ VCC -0.2V	C	—	—	5	mA
		VIN ≥ VCC -0.2V or VIN ≤ 0.2V	LP	—	—	1	mA
Output Low Voltage	VOL	IOL = 2.1mA	—	—	0.4	V	
Output High Voltage	VOH	IOH = -1.0mA	2.4	—	—	V	

AC TEST CONDITIONS

Figure 1

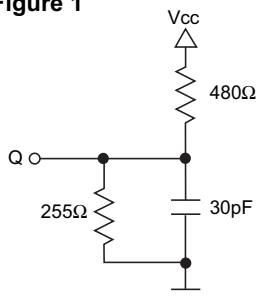
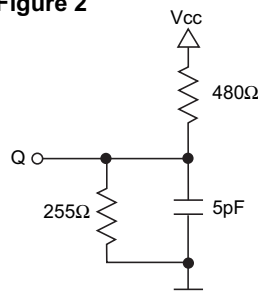


Figure 2



Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For tEHQZ, tGHQZ and tWLQZ, CL = 5pF Figure 2



AC CHARACTERISTICS – READ CYCLE

V_{CC} = 5.0V, V_{SS} = 0V, -55°C T_A +125°C

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	70		85		100		ns
Address Access Time	t _{AVQV}	t _{AA}		70		85		100	ns
Chip Enable Access Time	t _{ELQV}	t _{ACS}		70		85		100	ns
Chip Enable to Output in Low Z (1)	t _{ELQX}	t _{CLZ}	10		10		10		ns
Chip Disable to Output in High Z (1)	t _{EHQZ}	t _{CHZ}		25		30		30	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	10		10		10		ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		35		45		50	ns
Output Enable to Output in Low Z (1)	t _{GLQX}	t _{OLZ}	5		5		5		ns
Output Disable to Output in High Z(1)	t _{GHQZ}	t _{OHZ}	0	25	0	30	0	30	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE

V_{CC} = 5.0V, V_{SS} = 0V, -55°C T_A +125°C

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	70		85		100		ns
Chip Enable to End of Write	t _{ELWH}	t _{CW}	60		70		80		ns
	t _{ELEH}	t _{CW}	60		70		80		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
	t _{AVEL}	t _{AS}	0		0		0		ns
Address Valid to End of Write	t _{AVWH}	t _{AW}	65		70		80		ns
	t _{AVEH}	t _{AW}	65		70		80		ns
Write Pulse Width	t _{WLWH}	t _{WP}	50		55		60		ns
	t _{WLEH}	t _{WP}	50		55		60		ns
Write Recovery Time	t _{WHAX}	t _{WR}	0		0		0		ns
	t _{EHAX}	t _{WR}	0		0		0		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
	t _{EHDX}	t _{DH}	0		0		0		ns
Write to Output in High Z (1)	t _{WLQZ}	t _{WHZ}	0	25	0	30	0	30	ns
Data to Write Time	t _{DVWH}	t _{DW}	40		40		40		ns
	t _{DVEH}	t _{DW}	30		35		40		ns
Output Active from End of Write (1)	t _{WHQX}	t _{WLZ}	5		0		0		ns

1. This parameter is guaranteed by design but not tested.



FIGURE 2 – TIMING WAVEFORM - READ CYCLE

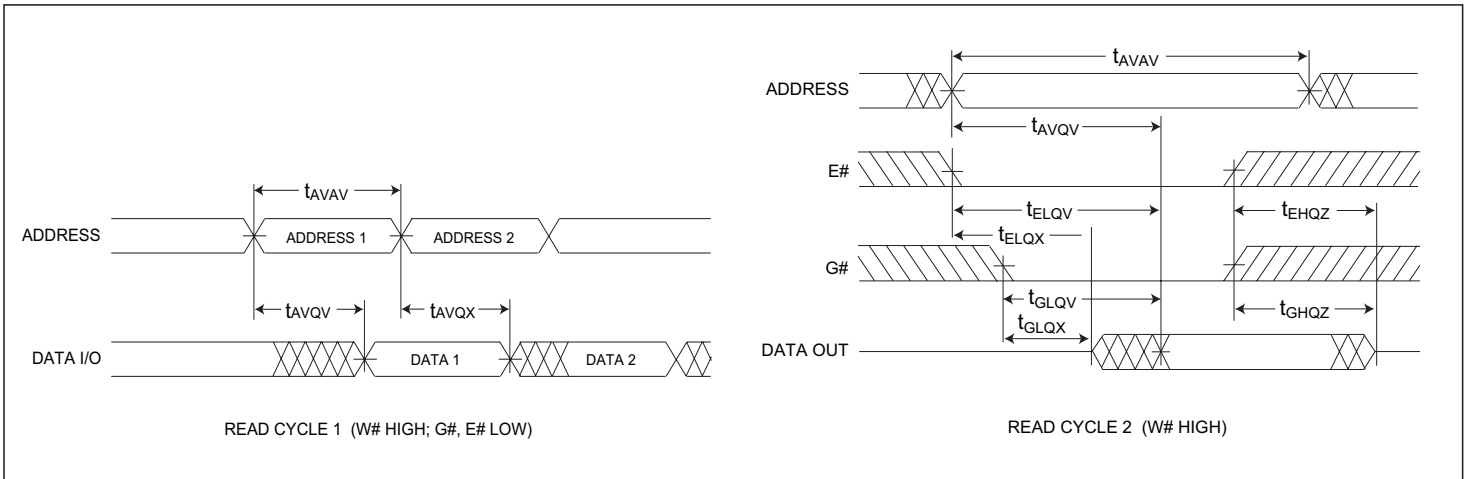


FIGURE 3 – WRITE CYCLE - W# CONTROLLED

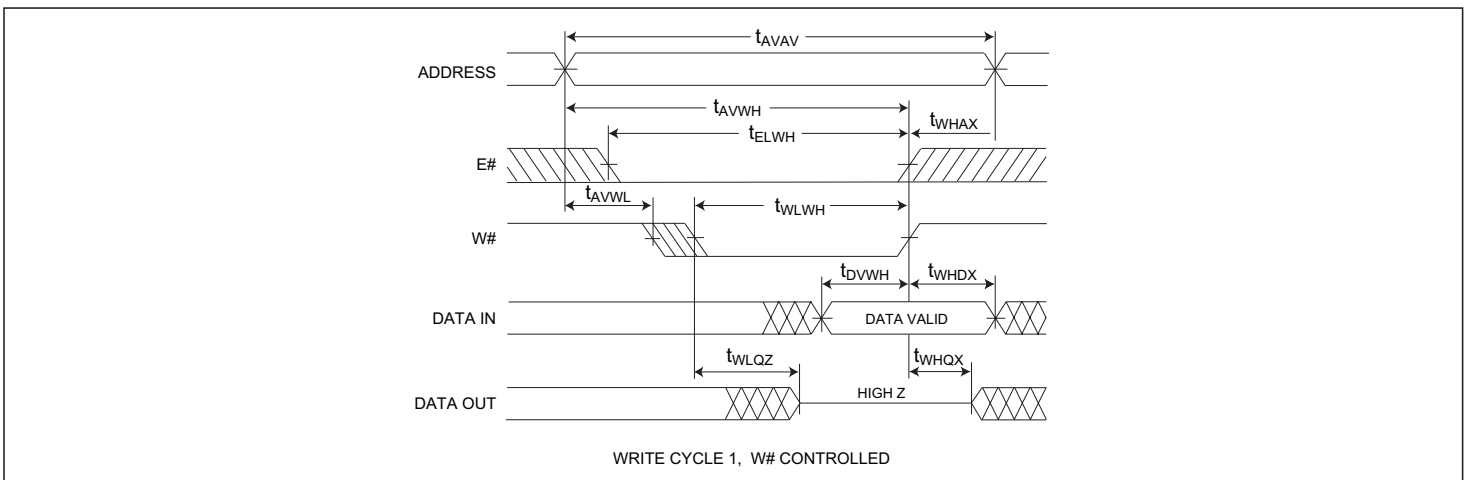
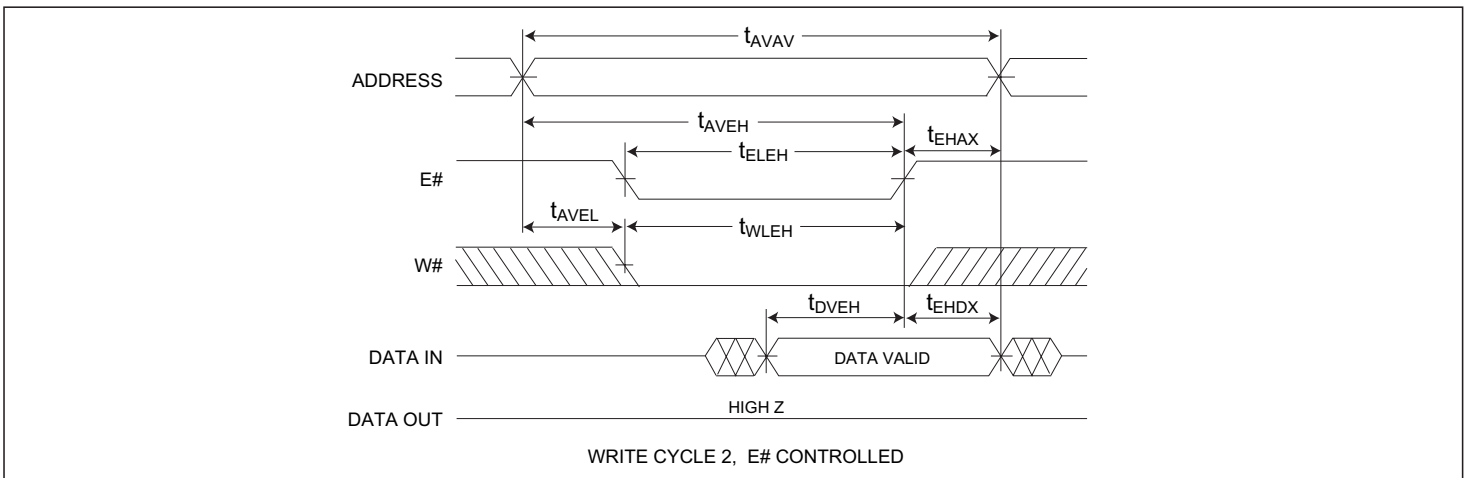


FIGURE 4 – WRITE CYCLE - E# CONTROLLED



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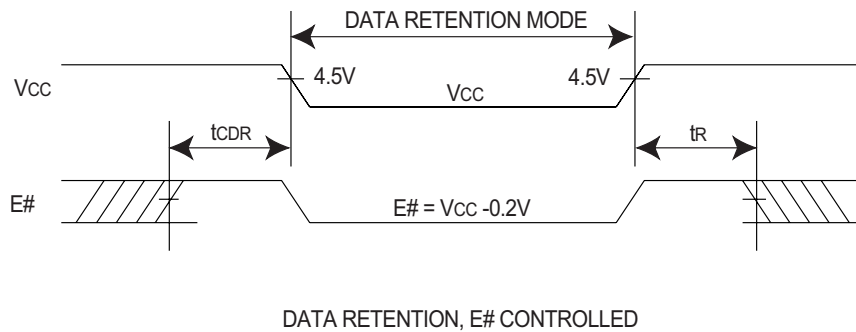


DATA RETENTION CHARACTERISTICS (EDI88257LP ONLY)

-55°C TA +125°C

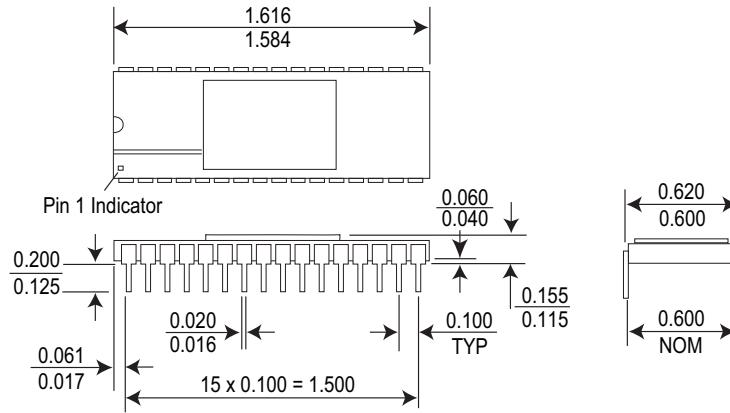
Characteristic	Sym	Conditions	Min	Typ	Max	Units
Low Power Version only						
Data Retention Voltage	V _{CC}	V _{CC} = 2.0V	2	-	-	V
Data Retention Quiescent Current	I _{CCDR}	E# ≥ V _{CC} - 0.2V	-	-	185	μA
Chip Disable to Data Retention Time	t _{CDR}	V _{IN} ≥ V _{CC} - 0.2V	0	-	-	ns
Operation Recovery Time	T _R	or V _{IN} ≤ 0.2V	t _{AVAV}	-	-	ns

FIGURE 5 – DATA RETENTION - E# CONTROLLED





PACKAGE 9: 32 PIN SIDEBRAZED CERAMIC DIP (600MILS WIDE)



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8257 C X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 256Kx8

TECHNOLOGY:

C = CMOS Standard Power

LP = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:

C = 32 lead Sidebrazed DIP, 600 mil (Package 9)

DEVICE GRADE:

B = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C