512Kx8 Plastic Monolithic SRAM CMOS

FEATURES

- 512Kx8 bit CMOS Static
- Random Access Memory
  - Access Times of 17, 20, 25ns
  - Data Retention Function (LPA version)
  - Extended Temperature Testing
  - Data Retention Functionality Testing
- 36 lead JEDEC Approved Revolutionary Pinout
  - Plastic SOJ (Package 319)
- Single +5V (±10%) Supply Operation

WEDC's ruggedized plastic 512Kx8 SRAM that allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

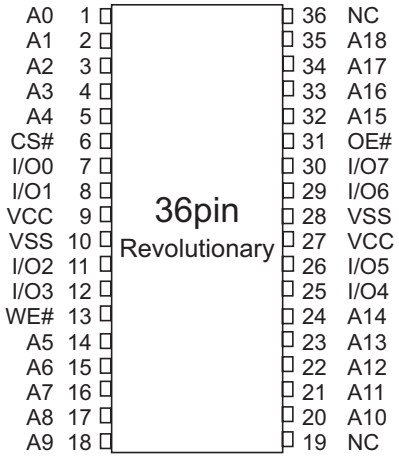
Extended temperature testing is performed with the test patterns developed for use on WEDC's fully compliant 512Kx8 SRAMs. WEDC fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of device change when it is operated beyond the commercial guarantee a device that operates reliably in the field at temperature extremes. Users of WEDC's ruggedized plastic benefit from WEDC's extensive experience in characterizing SRAMs for use in military systems.

WEDC ensures Low Power devices will retain data in Data Retention mode by characterizing the devices to determine the appropriate test conditions. This is crucial for systems operating at -40°C or below and using dense memories such as 512Kx8s.

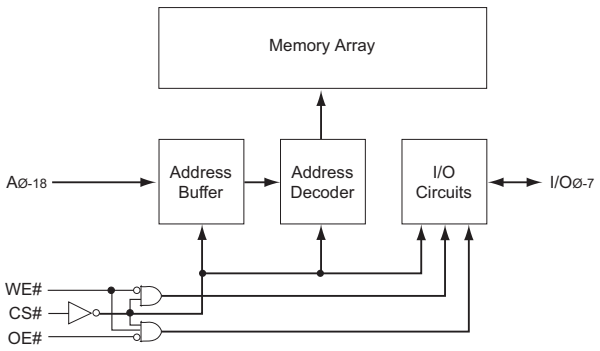
WEDC's ruggedized plastic SOJ is footprint compatible with WEDC's full military ceramic 36 pin SOJ.

FIG. 1 – PIN CONFIGURATION

TOP VIEW



BLOCK DIAGRAM



PIN Description

I/O_{0-7}	Data Inputs/Outputs
A_{0-18}	Address Inputs
WE#	Write Enables
CS#	Chip Selects
OE#	Output Enable
V_{CC}	Power (+5V ±10%)
V_{SS}	Ground
NC	Not Connected

ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature TA (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, TJ	175	°C

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE

OE#	CS#	WE#	Mode	Output	Power
X	H	X	Standby	High Z	Icc2, Icc3
H	L	H	Output Deselect	High Z	Icc1
L	L	H	Read	Data Out	Icc1
X	L	L	Write	Data In	Icc1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Condition	Max	Unit
Address Lines	CI	VIN = Vcc or Vss, f = 1.0MHz	6	pF
Data Lines	CO	VIN = Vcc or Vss, f = 1.0MHz	8	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

V_{CC} = 5V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = V_{SS} to V_{CC}		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IL}, OE# = V_{IH}, V_{OUT} = V_{SS} to V_{CC}		10	µA
Operating Supply Current	I_{CC}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		180	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		15	mA
Output High Volltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA, V_{CC} = 4.5		0.4	V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} -0.3V

AC TEST CONDITIONS

Figure 1

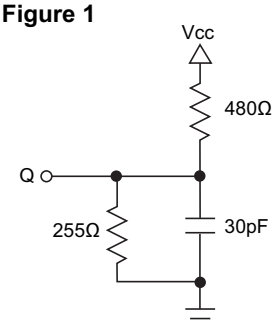
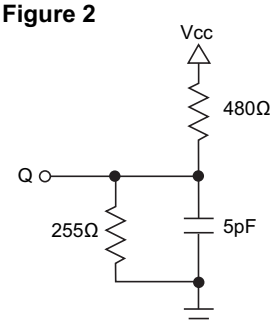


Figure 2



Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF (Figure 2)

AC CHARACTERISTICS – READ CYCLE

V_{CC} = 5.0V, V_{SS} = 0V, 0°C ≤ T_A ≤ +70°C

Parameter	Symbol JEDEC	Symbol Alt.	17ns Min	17ns Max	20ns Min	20ns Max	25ns Min	25ns Max	Units
Read Cycle Time	t_{AVAV}	t_{RC}	17		20		25		ns
Address Access Time	t_{AVQV}	t_{AA}		17		20		25	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		17		20		25	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	0		0		0		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		8		10		12	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		ns
Output Disable to Output in High Z(1)	t_{GHQZ}	t_{OHZ}	0	7	0	8	0	10	ns

1. This parameter is guaranteed by design but not tested.

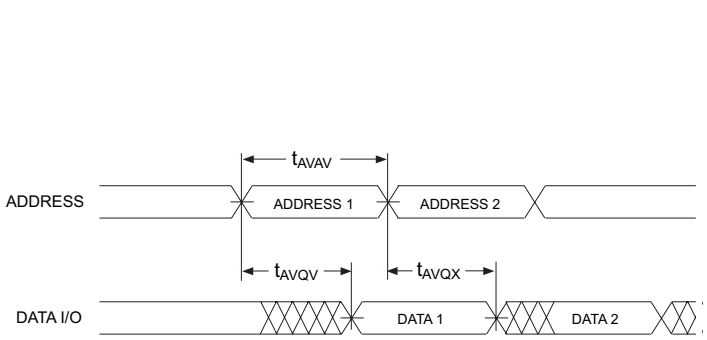
AC CHARACTERISTICS – WRITE CYCLE

V_{CC} = 5.0V, V_{SS} = 0V, 0°C ≤ T_A ≤ +70°C

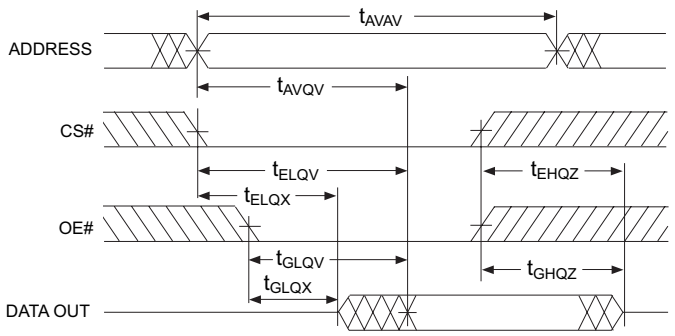
Parameter	Symbol JEDEC	Symbol Alt.	17ns Min	17ns Max	20ns Min	20ns Max	25ns Min	25ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	17		20		25		ns
Chip Enable to End of Write	t_{ELWH} t_{ELEH}	t_{CW} t_{CW}	14 14		15 15		17 17		ns ns
Address Setup Time	t_{AVWL} t_{AVEL}	t_{AS} t_{AS}	0 0		0 0		0 0		ns ns
Address Valid to End of Write	t_{AVWH} t_{AVEH}	t_{AW} t_{AW}	14 14		15 15		17 17		ns ns
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	14 14		15 15		17 17		ns ns
Write Recovery Time	t_{WHAX} t_{EHAX}	t_{WR} t_{WR}	0 0		0 0		0 0		ns ns
Data Hold Time	t_{WHDX} t_{EHDX}	t_{DH} t_{DH}	0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	8	0	8	0	10	ns
Data to Write Time	t_{DVWH} t_{DVEH}	t_{DW} t_{DW}	8 8		10 10		12 12		ns ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 2 – TIMING WAVEFORM — READ CYCLE

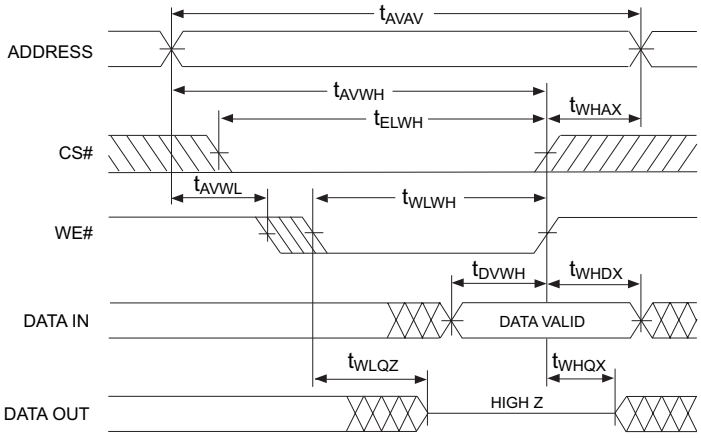


READ CYCLE 1 (WE# HIGH; OE#, CS# LOW)



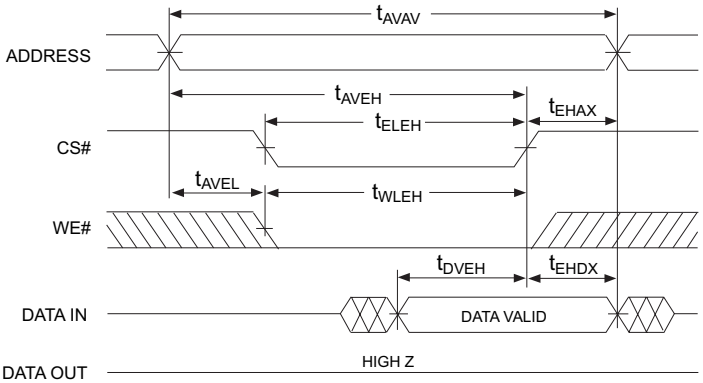
READ CYCLE 2 (WE# HIGH)

FIG. 3 – WRITE CYCLE — WE# CONTROLLED



WRITE CYCLE 1, WE# CONTROLLED

FIG. 4 – WRITE CYCLE — CS# CONTROLLED



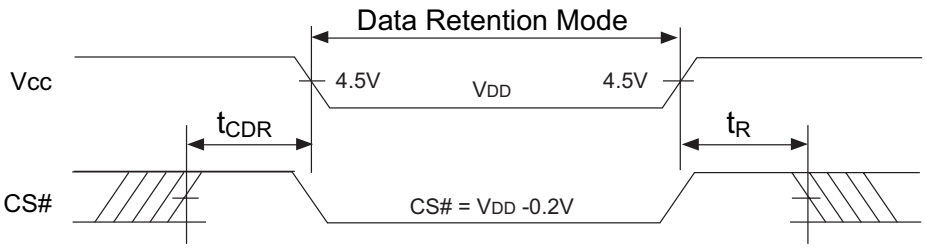
WRITE CYCLE 2, CS# CONTROLLED

DATA RETENTION CHARACTERISTICS (EDI88512LPA ONLY)

-55°C ≤ T_A ≤ +125°C

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage Data Retention Quiescent Current	V_{DD} I_{CCDR}	V_{DD} = 2.0V CS# ≥ V_{DD} -0.2V	2 –	– –	– 2	V mA
Chip Disable to Data Retention Time Operation Recovery Time	T_{CDR} T_R	V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ 0.2V	0 T_{AVAV}	–	– –	ns ns

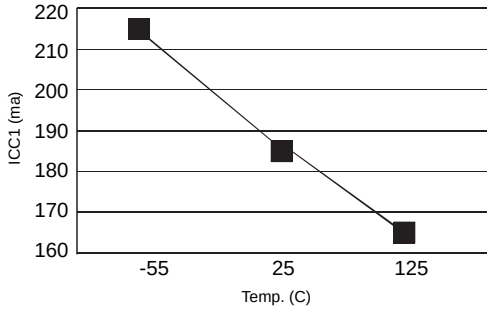
FIG. 5 – DATA RETENTION - CS# CONTROLLED



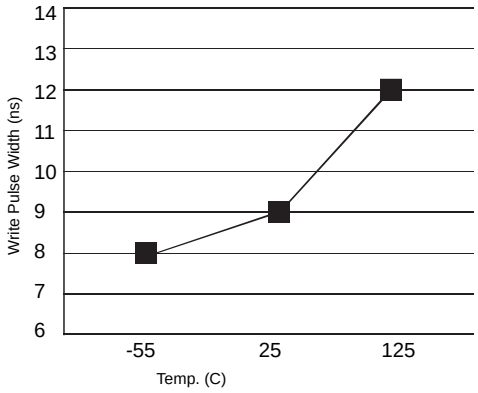
DATA RETENTION, CS# CONTROLLED

FIG. 6 – NORMALIZED OPERATING GRAPHS

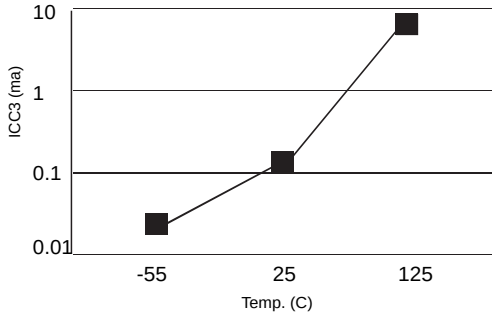
ICC1 (20ns) vs Temp



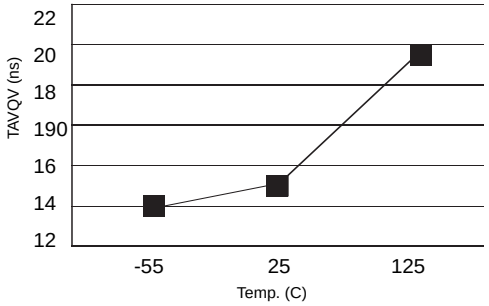
Write Pulse Width vs. Temp.



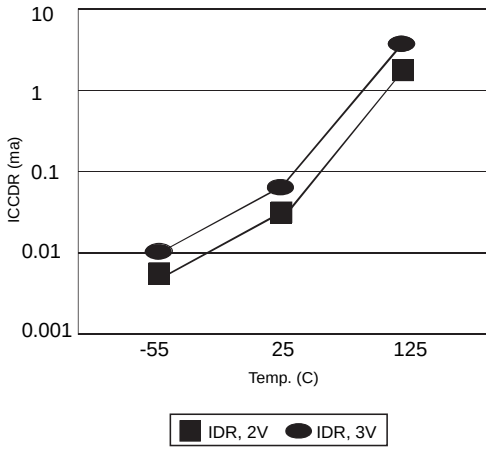
ICC3 vs. Temp



TAVQV vs. Temp



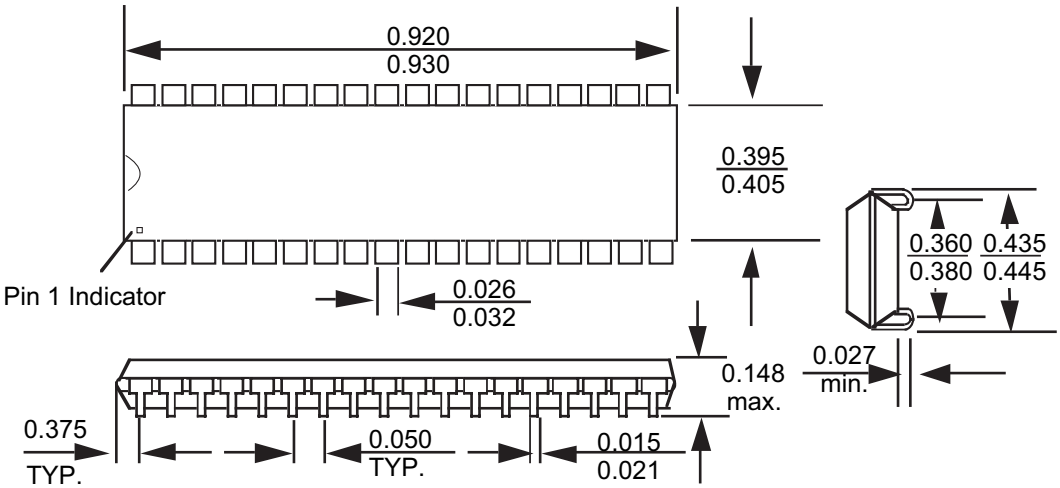
ICCDR vs. Temp



Normalized curves are offered as a service to our customers. They are not to be construed as a guarantee of operating characterics.

Characteristics of actual devices will vary.

PACKAGE 319: 36 LEAD, PLASTIC SMALL OUTLINE J-LEAD (SOJ)



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8 512 CA X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 512Kx8

TECHNOLOGY:
- CA = CMOS Standard Power
- LPA = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:
- M = 36 lead Plastic SOJ

DEVICE GRADE:

B =	MIL-STD-883 Compliant	
M =	Military Screened	-55°C to +125°C
I =	Industrial	-40°C to +85°C
C =	Commercial	0°C to +70°C