SDRAM RDIMM

MT9LSDT1672 – 128MB
MT9LSDT3272 – 256MB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 168-pin, PC133-compliant registered dual in-line memory module (RDIMM)
- Phase-lock loop (PLL) clock driver to reduce loading
- Uses 133 MHz SDRAM components
- Supports ECC error detection and correction
- 128MB (16 Meg x 72) and 256MB (32 Meg x 72)
- V_{DD} = +3.3V
- Fully synchronous; all signals are registered on the positive edge of the PLL clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/ precharge
- Programmable burst lengths (BL): 1, 2, 4, 8, or full page
- Single rank
- Auto precharge option
- Auto and self refresh modes: 15.625µs (128MB) or 7.81µs (256MB) maximum periodic refresh interval
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts

168-Pin RDIMM (MO-161 R/C A)

Figure 1: Standard Layout

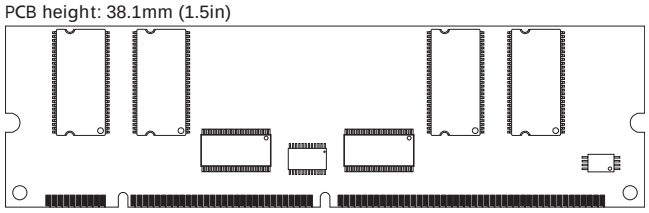
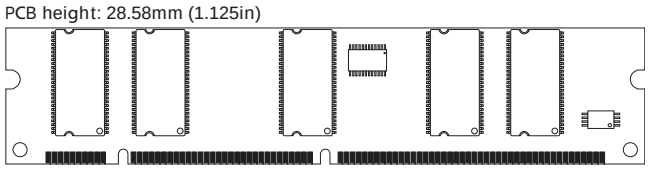


Figure 2: Low Profile Layout



Options	Marking
• Package	
– 168-pin DIMM	G
– 168-pin DIMM (Pb-free)	Y
• Frequency/CAS latency[1]	
– 133 MHz/CL = 2	-13E
– 133 MHz/CL = 3	-133

Notes: 1. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)		^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 2	CL = 3			
-13E	PC133	133	–	15	15	60
-133	PC133	–	133	20	20	66

Table 2: Addressing

Parameter	128MB	256MB
Refresh count	4K	8K
Device banks	4 (BA0, BA1)	4 (BA0, BA1)
Device configuration	128Mb (16 Meg x 8)	256Mb (32 Meg x 8)
Row address	4K (A0–A11)	8K (A0–A12)
Column address	1K (A0–A9)	1K (A0–A9)
Module ranks	1 (S0#, S2#)	1 (S0#, S2#)

Table 3: Part Numbers and Timing Parameters – 128MB Modules

Base device: MT48LC16M8A2,[1] 128Mb SDRAM

Part Number[2]	Module Density	Configuration	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9LSDT1672G-13E__[3]	128MB	16 Meg x 72	7.5ns/133 MT/s	2-2-2
MT9LSDT1672Y-13E__[3]	128MB	16 Meg x 72	7.5ns/133 MT/s	2-2-2
MT9LSDT1672G-133__	128MB	16 Meg x 72	7.5ns/133 MT/s	3-3-3
MT9LSDT1672Y-133__	128MB	16 Meg x 72	7.5ns/133 MT/s	3-3-3

Table 4: Part Numbers and Timing Parameters – 256MB Modules

Base device: MT48LC32M8A2,[1] 256Mb SDRAM

Part Number[2]	Module Density	Configuration	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9LSDT3272G-13E__	256MB	32 Meg x 72	7.5ns/133 MT/s	2-2-2
MT9LSDT3272Y-13E__	256MB	32 Meg x 72	7.5ns/133 MT/s	2-2-2
MT9LSDT3272G-133__	256MB	32 Meg x 72	7.5ns/133 MT/s	3-3-3
MT9LSDT3272Y-133__	256MB	32 Meg x 72	7.5ns/133 MT/s	3-3-3

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT9LSDT3272G-133D2.
3. End of life.

Pin Assignments and Descriptions

Figure 3: Pin Assignments

168-Pin SDRAM RDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	22	CB1	43	VSS	64	VSS
2	DQ0	23	VSS	44	NC	65	DQ21
3	DQ1	24	NC	45	S2#	66	DQ22
4	DQ2	25	NC	46	DQMB2	67	DQ23
5	DQ3	26	VDD	47	DQMB3	68	VSS
6	VDD	27	WE#	48	NC	69	DQ24
7	DQ4	28	DQMB0	49	VDD	70	DQ25
8	DQ5	29	DQMB1	50	NC	71	DQ26
9	DQ6	30	S0#	51	NC	72	DQ27
10	DQ7	31	NC	52	CB2	73	VDD
11	DQ8	32	VSS	53	CB3	74	DQ28
12	VSS	33	A0	54	VSS	75	DQ29
13	DQ9	34	A2	55	DQ16	76	DQ30
14	DQ10	35	A4	56	DQ17	77	DQ31
15	DQ11	36	A6	57	DQ18	78	VSS
16	DQ12	37	A8	58	DQ19	79	NF
17	DQ13	38	A10	59	VDD	80	NC
18	VDD	39	BA1	60	DQ20	81	NC
19	DQ14	40	VDD	61	NC	82	SDA
20	DQ15	41	VDD	62	NC	83	SCL
21	CB0	42	CK0	63	NC	84	VDD

168-Pin SDRAM RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
85	VSS	106	CB5	127	VSS	148	VSS
86	DQ32	107	VSS	128	CKE0	149	DQ53
87	DQ33	108	NC	129	NC	150	DQ54
88	DQ34	109	NC	130	DQMB6	151	DQ55
89	DQ35	110	VDD	131	DQMB7	152	VSS
90	VDD	111	CAS#	132	NC	153	DQ56
91	DQ36	112	DQMB4	133	VDD	154	DQ57
92	DQ37	113	DQMB5	134	NC	155	DQ58
93	DQ38	114	NC	135	NC	156	DQ59
94	DQ39	115	RAS#	136	CB6	157	VDD
95	DQ40	116	VSS	137	CB7	158	DQ60
96	VSS	117	A1	138	VSS	159	DQ61
97	DQ41	118	A3	139	DQ48	160	DQ62
98	DQ42	119	A5	140	DQ49	161	DQ63
99	DQ43	120	A7	141	DQ50	162	VSS
100	DQ44	121	A9	142	DQ51	163	NF
101	DQ45	122	BA0	143	VDD	164	NC
102	VDD	123	A11	144	DQ52	165	SA0
103	DQ46	124	VDD	145	NC	166	SA1
104	DQ47	125	NF	146	NC	167	SA2
105	CB4	126	NF/A12[1]	147	REGE	168	VDD

Notes: 1. Pin 126 is NF for 128MB and A12 for 256MB.

Table 5: Pin Descriptions

Symbol	Type	Description
A0–A12	Input	**Address inputs:** Sampled during the ACTIVE and READ/WRITE commands, with A10 defining auto precharge, to select one location out of the memory array in the respective device bank. A10 is sampled during a PRECHARGE command to determine whether both device banks are precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command. A0–A11 (256MB) and A0–A12 (256MB).
BA0, BA1	Input	**Bank address inputs:** BA0 and BA1 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
CK0–CK3	Input	**Clock:** CK0 is distributed through an on-board PLL to all devices. CK1–CK3 are terminated.
CKE0	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) the CK signal. Deactivating the clock provides power-down and SELF REFRESH operations (all device banks idle) or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK, are disabled during power-down and self refresh modes, providing low standby power.
DQMB0–DQMB7	Input	**Input/output mask:** DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
REGE	Input	Register enable.
S0#, S2#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
SA0–SA2	Input	**Presence-detect address inputs:** These pins are used to configure the presence-detect device.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
CB0–CB7	Input/ Output	Check bits.
DQ0–DQ63	Input/ Output	**Data input/output:** Data bus.
SDA	Input/ Output	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and data out of the EEPROM portion of the module.
V_{DD}	Supply	**Power supply:** +3.3V ±0.3V.
V_{SS}	Supply	Ground.
NC	–	**Not connected:** These pins are not connected on the module.
NF	–	**No function:** Connected within the module but provides no functionality.

Functional Block Diagrams

Figure 4: Functional Block Diagram – Standard Layout

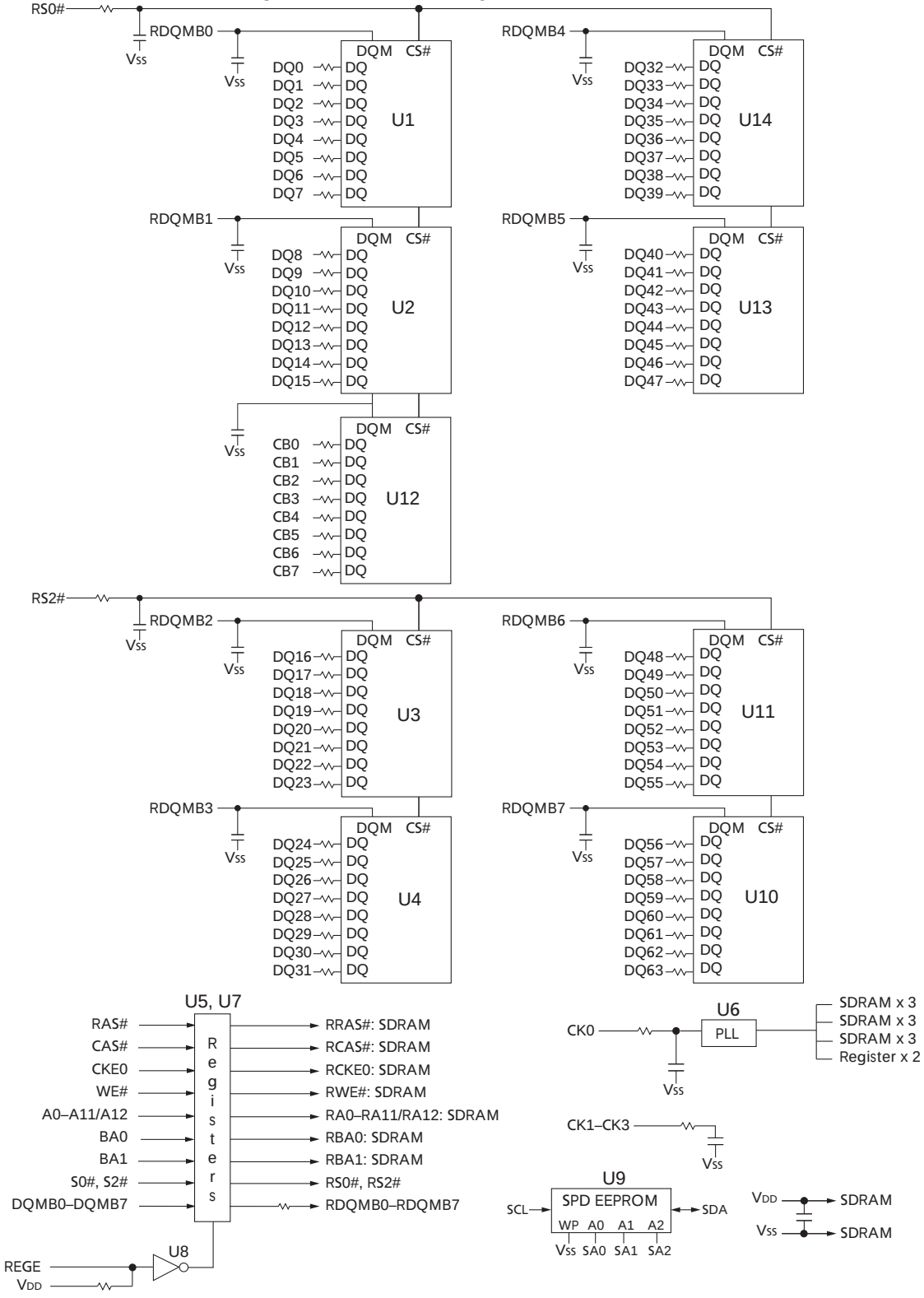
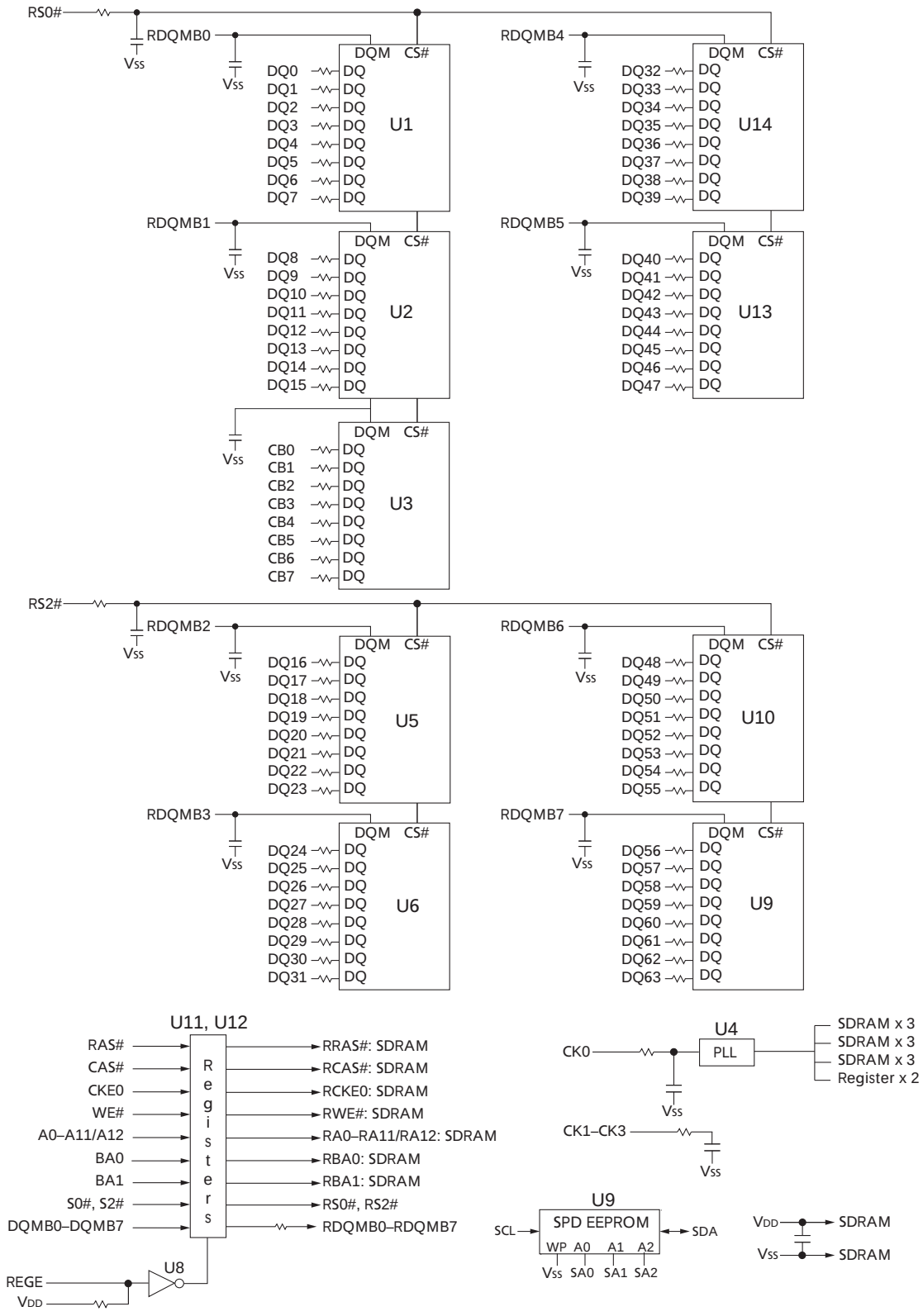


Figure 5: Functional Block Diagram – Low Profile Layout



General Description

The MT9LSDT1672 and MT9LSDT3272 are high-speed, CMOS dynamic random access 128MB and 256MB memory modules organized in a x72 ECC configuration. SDRAM modules use 4-bank SDRAM devices with a synchronous interface (all signals are registered on the positive edge of clock signal CK).

Read and write accesses to SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select the device bank; A0–A11 select the device row for the 256MB module; A0–A12 select the device row for the 512MB module). The address bits registered coincident with the READ or WRITE command are used to select the starting device column location for the burst access.

SDRAM modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed device row precharge that is initiated at the end of the burst sequence.

SDRAM modules use an internal pipelined architecture. Precharging one device bank while accessing one of the other three device banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

SDRAM modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving power-down mode. All inputs and outputs are LVTTL compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic device column-address generation, the ability to interleave between device banks to hide precharge time, and the capability to randomly change device column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 128Mb and 256Mb SDRAM component data sheets.

PLL and Register Operation

These SDRAM modules can either be operated in registered mode (REGE pin HIGH), where the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin LOW), where the input signals pass through the register/buffer to the SDRAM devices on the same clock. A phase-lock loop (PLL) on the modules is used to redrive the clock signals to the SDRAM devices to minimize system clock loading (CK0 is connected to the PLL, and CK1, CK2, and CK3 are terminated).

Serial Presence-Detect Operation

SDRAM modules incorporate serial presence-detect. The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to V_{SS} on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Units
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	–1.0	+4.6	V
V_{IN}, V_{OUT}	Voltage on inputs, NC, or I/O pins relative to V_{SS}	–1.0	+4.6	V

Table 7: Operating Conditions

Symbol	Parameter/Condition		Min	Max	Units
V_{DD}, V_{DDQ}	Supply voltage		+3.0	+3.6	V
V_{IH}	Input high voltage: Logic 1; All inputs		+2.0	V_{DD} + 0.3	V
V_{IL}	Input low voltage: Logic 0; All inputs		–0.3	0.8	V
I_I	Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA, CK, CKE, S#	–10	+10	µA
		DQMB	–5	+5	µA
I_{OZ}	Output leakage current: DQ pins are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}	DQ	–5	+5	µA
V_{OH}	Output high voltage (I_{OUT} = –4mA)		+2.4	–	V
V_{OL}	Output low voltage (I_{OUT} = 4mA)		–	0.4	V
T_{OPR}	Ambient operating temperature (commercial)		0	+55	°C

Design Considerations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the SDRAM component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

Table 8: Module and Component Speed Grades
SDRAM components meet or exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-13E	-7E
-133	-75

IDD Specifications

Table 9: IDD Specifications and Conditions – 128MB

Values are shown for the MT48LC16M8A2 SDRAM components only and are computed from values specified in the 128Mb (16 Meg x 8) component data sheet

Parameter/Condition		Symbol	-13E	-133	Units
Operating current: Active mode; BL = 2; Read or write; ^{t}RC = ^{t}RC (MIN)		IDD1	1,440	1,350	mA
Standby current: Power-down mode; All device banks idle; CKE = LOW		IDD2	18	18	mA
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All device banks active after ^{t}RCD has been met; No accesses in progress		IDD3	450	450	mA
Operating current: Burst mode; Page burst; Read or write; All device banks active		IDD4	1,485	1,350	mA
Auto refresh current: CS# = HIGH; CKE = HIGH	^{t}RFC = ^{t}RFC (MIN)	IDD5	2,970	2,790	mA
	^{t}RFC = 15.625µs	IDD6	27	27	mA
Self refresh current: CKE ≤ 0.2V		IDD7	18	18	mA

Table 10: IDD Specifications and Conditions – 256MB

Values are shown for the MT48LC32M8A2 SDRAM components only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition		Symbol	-13E	-133	Units
Operating current: Active mode; BL = 2; Read or write; ^{t}RC = ^{t}RC (MIN)		IDD1	1,215	1,125	mA
Standby current: Power-down mode; All device banks idle; CKE = LOW		IDD2	18	18	mA
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All device banks active after ^{t}RCD has been met; No accesses in progress		IDD3	360	360	mA
Operating current: Burst mode; Page burst; Read or write; All device banks active		IDD4	1,215	1,215	mA
Auto refresh current: CS# = HIGH; CKE = HIGH	^{t}RFC = ^{t}RFC (MIN)	IDD5	2,560	2,430	mA
	^{t}RFC = 7.8125µs	IDD6	32	32	mA
Self refresh current: CKE ≤ 0.2V		IDD7	23	23	mA

Register and PLL Specifications

Table 11: Register Timing Requirements and Switching Characteristics
162835A device or equivalent JESD82-2

Parameter	Symbol	Condition	Min	Max	Units
Maximum clock pulse frequency	^{f}MAX	–	150	240	MHz
Propagation delay, single rank (CK to output)	$^{t}PD1$	50pF to GND and 50Ω to VTT	1.4	3.5	ns
Propagation delay, dual rank (CK to output)	$^{t}PD2$	30pF to GND and 50Ω to VTT	0.7	2.5	ns
Pulse duration	^{t}W	CK, HIGH or LOW	3.3	–	ns
Setup time	^{t}SU	Data before CK HIGH	1.0	–	ns
Hold time	^{t}H	Data after CK HIGH	0.6	–	ns

Table 12: PLL Clock Driver Timing Requirements and Switching Characteristics
CDC2510 device or equivalent JESD82-5

Parameter	Symbol	Min	Max	Units	Notes
Operating clock frequency	^{f}CK	50	140	MHz	
Input duty cycle	^{t}DC	44	55	%	
Cycle-to-cycle jitter	$^{t}JIT_{CC}$	–75	75	ps	
Static phase offset	$^{t}\varnothing$	–150	150	ps	
SSC induced skew	^{t}SSC	–	150	ps	1, 2
Output-to-output skew	$^{t}SK_{O}$	–	150	ps	

Notes:
1. SSC = spread spectrum clock. The use of SSC synthesizers on the system motherboard will reduce EMI.
2. Skew is defined as the total clock skew between any two outputs and, therefore, is specified as a maximum only.

Serial Presence-Detect

Table 13: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3.0	µA
Standby current	I_{SB}	1.6	4.0	µA
Power supply current, read: SCL clock frequency = 100 kHz	ICC_R	0.4	1.0	mA
Power supply current, write: SCL clock frequency = 100 kHz	ICC_W	2.0	3.0	mA

Table 14: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
Clock/data fall time	^tF	–	300	ns	2
Clock/data rise time	^tR	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SCL clock frequency	^fSCL	–	400	kHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

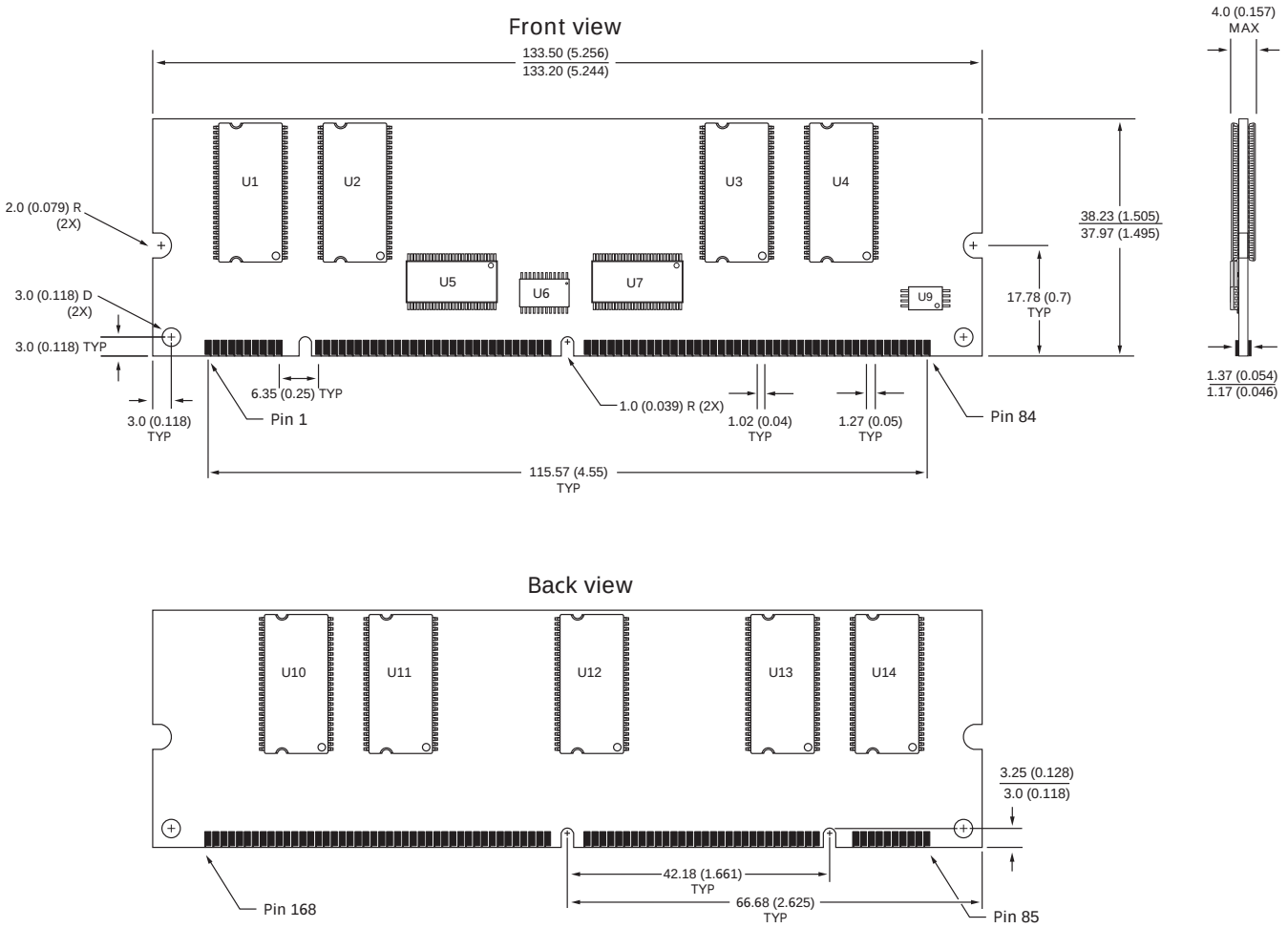
Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

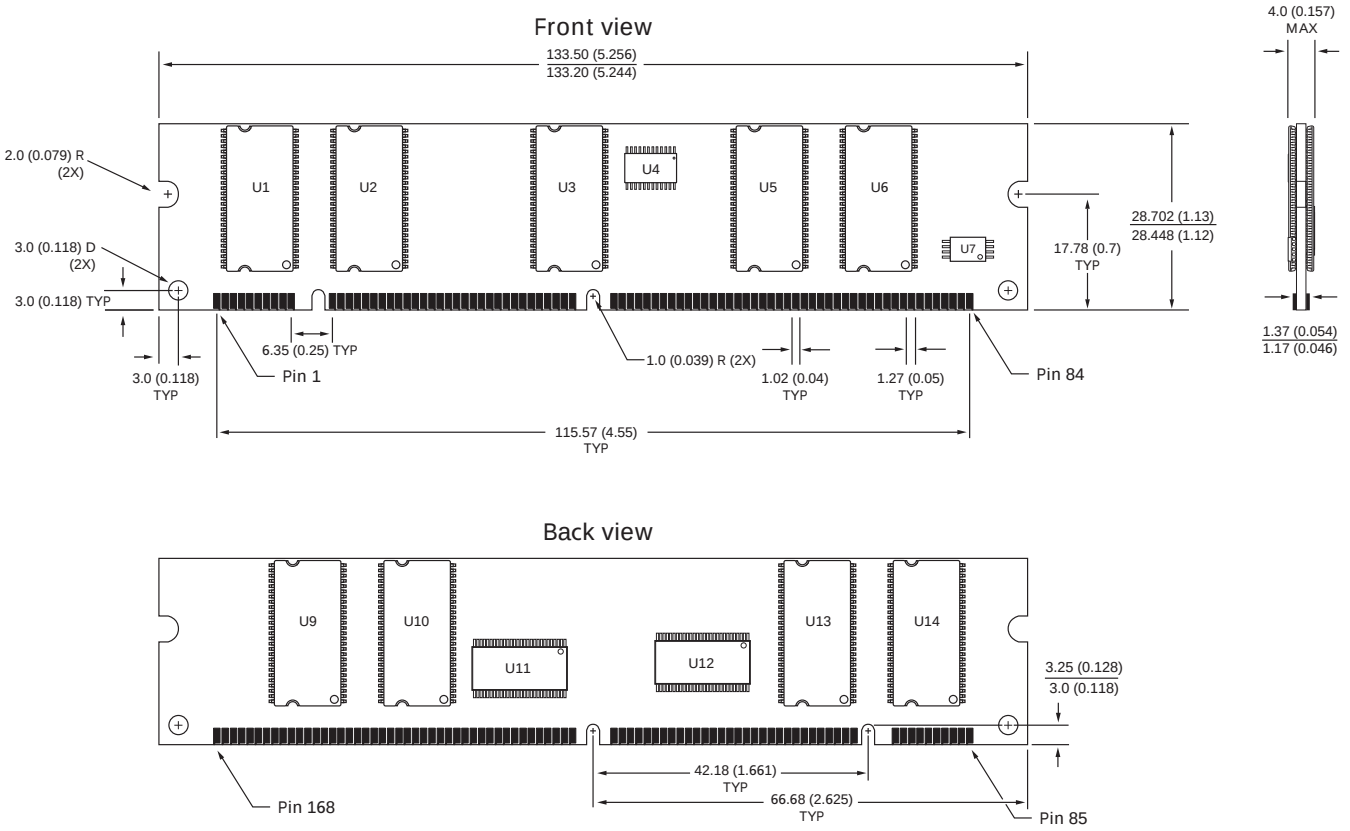
Module Dimensions

Figure 6: 168-Pin SDRAM RDIMM – Standard Layout



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

Figure 7: 168-Pin SDRAM RDIMM – Low Profile Layout



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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