32Mx64 Synchronous DRAM

FEATURES

- High Frequency = 100, 125, 133MHz
- Package:
  - 208 Plastic Ball Grid Array (PBGA), 13 x 22mm
- 3.3V ±0.3V power supply
- Fully Synchronous; all signals registered on positive edge of system clock cycle
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable Burst length 1,2,4,8 or full page
- 8192 refresh cycles
- Commercial, Industrial and Military Temperature Ranges
- Organized as 32M x 64
- Weight: W332M64V-XSBX - 1.4 grams typical

BENEFITS

- 73% SPACE SAVINGS
- Reduced part count
- Reduced trace lengths for lower parasitic capacitance
- Suitable for hi-reliability applications

* This product is to change without notice.

GENERAL DESCRIPTION

The 256MByte (2Gb) SDRAM is a high-speed CMOS, dynamic random-access, memory using 4 chips containing 536,870,912 bits. Each chip is internally configured as a quad-bank DRAM with a synchronous interface. Each of the chip's 134,217,728-bit banks is organized as 8,192 rows by 1,024 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 2Gb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

The 2Gb SDRAM is designed to operate at 3.3V. An auto refresh mode is provided, along with a power-saving, power-down mode.

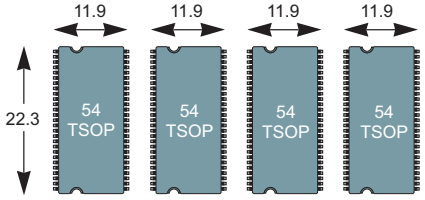
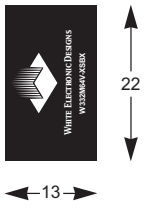
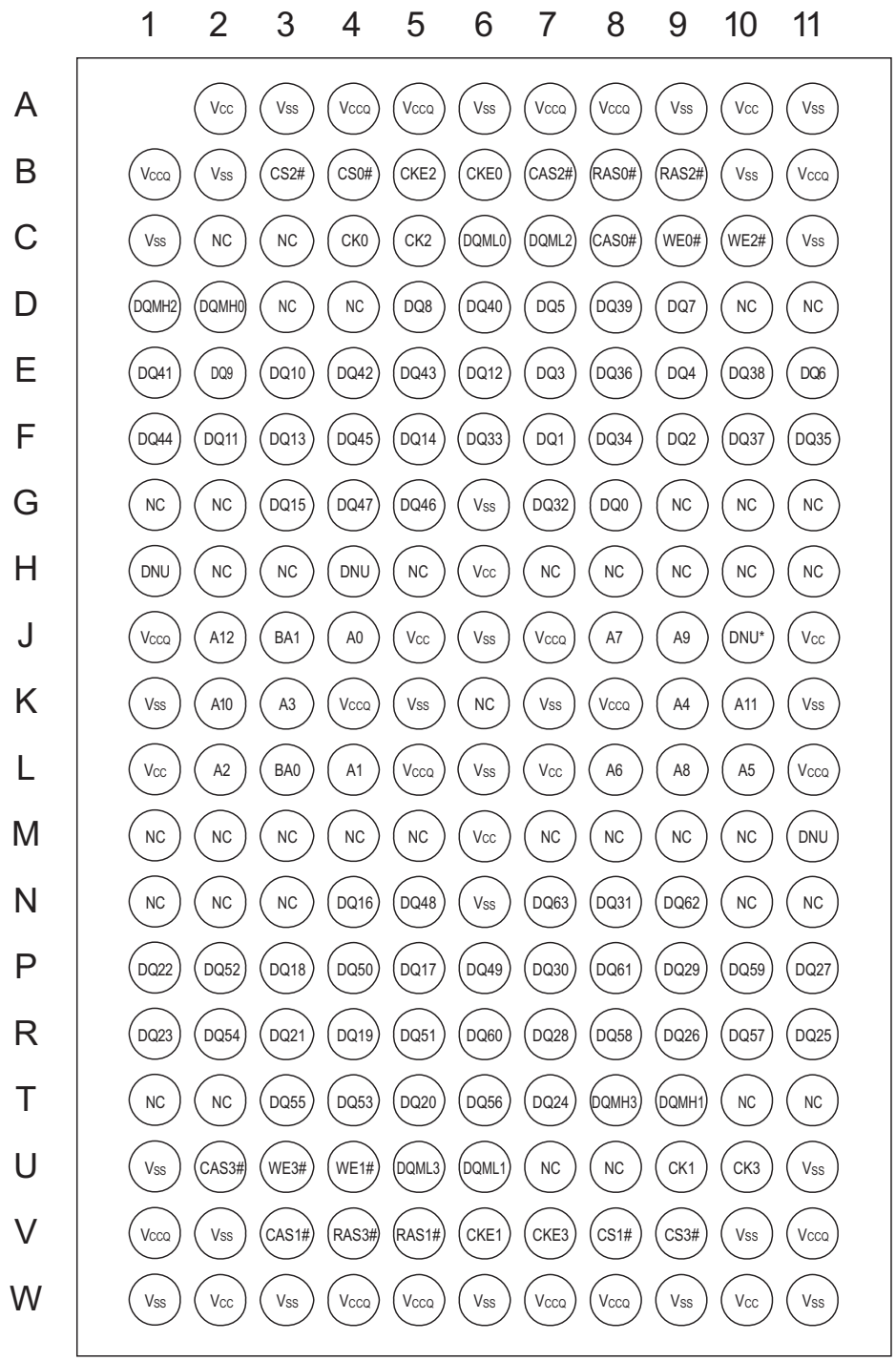
	Discrete Approach	ACTUAL SIZE	SAVINGS
			
Area	4 x 265mm^2 = 1060mm^2	286mm^2	73%

FIGURE 1 – PIN CONFIGURATION

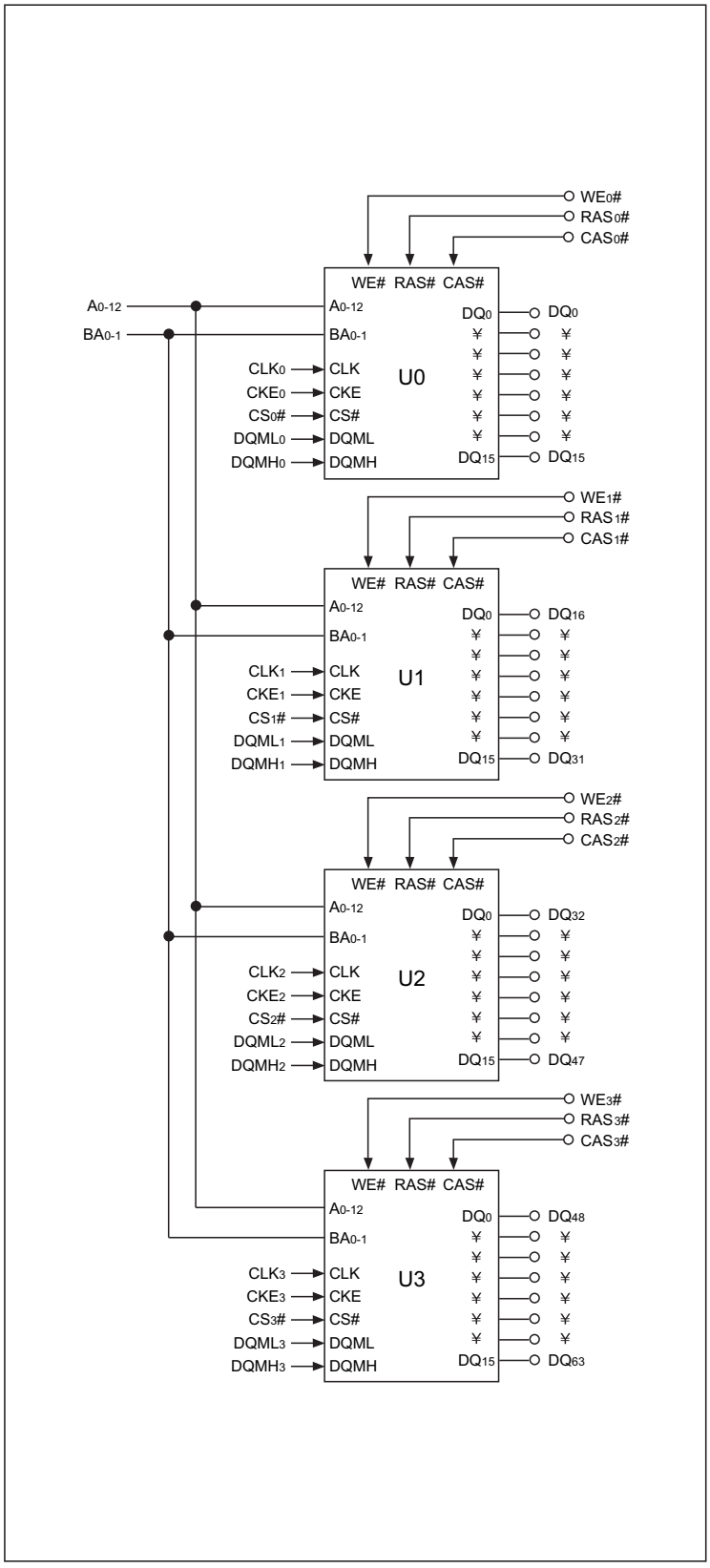
Top View



	1	2	3	4	5	6	7	8	9	10	11
A		VCC	VSS	VCCQ	VCCQ	VSS	VCCQ	VCCQ	VSS	VCC	VSS
B	VCCQ	VSS	CS2#	CS0#	CKE2	CKE0	CAS2#	RAS0#	RAS2#	VSS	VCCQ
C	VSS	NC	NC	CK0	CK2	DQML0	DQML2	CAS0#	WE0#	WE2#	VSS
D	DQMH2	DQMH0	NC	NC	DQ8	DQ40	DQ5	DQ39	DQ7	NC	NC
E	DQ41	DQ9	DQ10	DQ42	DQ43	DQ12	DQ3	DQ36	DQ4	DQ38	DQ6
F	DQ44	DQ11	DQ13	DQ45	DQ14	DQ33	DQ1	DQ34	DQ2	DQ37	DQ35
G	NC	NC	DQ15	DQ47	DQ46	VSS	DQ32	DQ0	NC	NC	NC
H	DNU	NC	NC	DNU	NC	VCC	NC	NC	NC	NC	NC
J	VCCQ	A12	BA1	A0	VCC	VSS	VCCQ	A7	A9	DNU*	VCC
K	VSS	A10	A3	VCCQ	VSS	NC	VSS	VCCQ	A4	A11	VSS
L	VCC	A2	BA0	A1	VCCQ	VSS	VCC	A6	A8	A5	VCCQ
M	NC	NC	NC	NC	NC	VCC	NC	NC	NC	NC	DNU
N	NC	NC	NC	DQ16	DQ48	VSS	DQ63	DQ31	DQ62	NC	NC
P	DQ22	DQ52	DQ18	DQ50	DQ17	DQ49	DQ30	DQ61	DQ29	DQ59	DQ27
R	DQ23	DQ54	DQ21	DQ19	DQ51	DQ60	DQ28	DQ58	DQ26	DQ57	DQ25
T	NC	NC	DQ55	DQ53	DQ20	DQ56	DQ24	DQMH3	DQMH1	NC	NC
U	VSS	CAS3#	WE3#	WE1#	DQML3	DQML1	NC	NC	CK1	CK3	VSS
V	VCCQ	VSS	CAS1#	RAS3#	RAS1#	CKE1	CKE3	CS1#	CS3#	VSS	VCCQ
W	VSS	VCC	VSS	VCCQ	VCCQ	VSS	VCCQ	VCCQ	VSS	VCC	VSS

NOTE: DNU = Do Not Use; to be left unconnected for future upgrades.
NC = Not Connected Internally.

FIGURE 2 – FUNCTIONAL BLOCK DIAGRAM



All inputs and outputs are LVTTL compatible. SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

FUNCTIONAL DESCRIPTION

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-12 select the row). The address bits (A0-9) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V_{CC} and V_{CCQ} (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or a NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All banks must be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for Mode Register programming. Because the Mode Register will power up in an unknown state, it should be loaded prior to applying any operational command.

Register Definition

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the SDRAM. This definition includes the selec-tion of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure 3. The Mode Register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the WRITE burst mode, and M10 and M11 are reserved for future use. Address A12 (M12) is undefined but should be driven LOW during loading of the mode register.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 3. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-9 when the burst length is set to two; by A2-9 when the burst length is set to four; and by A3-9 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached

FIGURE. 3 – MODE REGISTER DEFINITION

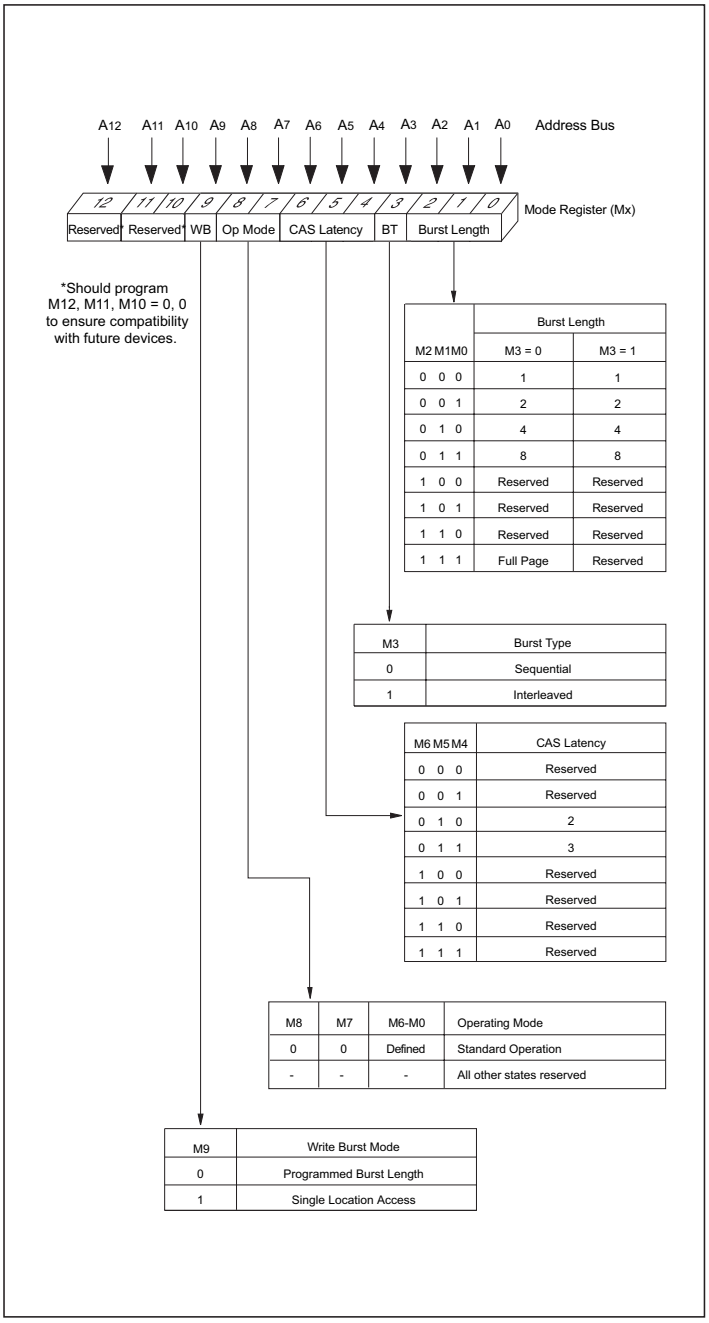
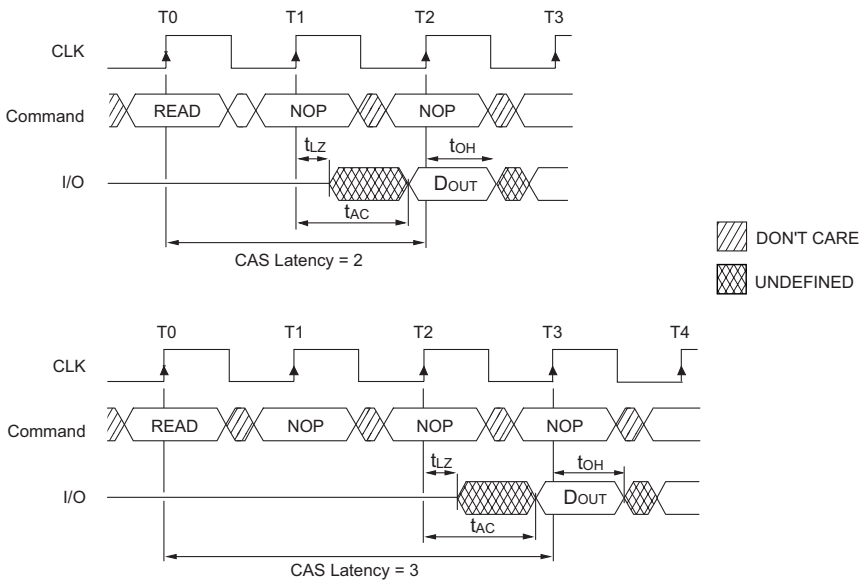


TABLE 1 – BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A 0-9 (location 0-y)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... …Cn - 1, Cn…	Not Supported

NOTES:
1. For full-page accesses: y = 1,024.
2. For a burst length of two, A1-9 select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2-9 select the block-of-four burst; A0-1 select the starting column within the block.
4. For a burst length of eight, A3-9 select the block-of-eight burst; A0-2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0-9 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0-9 select the unique column to be accessed, and Mode Register bit M3 is ignored.

FIGURE. 4 – CAS LATENCY



BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

CAS LATENCY

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge n+m. The I/Os will start driving as a result of the clock edge one cycle earlier (n + m - 1), and provided that the relevant access times are met, the data will be valid by clock edge n + m. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the I/Os will start driving after T1 and the data will be valid by T2. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

OPERATING MODE

The normal operating mode is selected by setting M7and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

TABLE 2 – CAS LATENCY

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)	
	CAS LATENCY = 2	CAS LATENCY = 3
-100	≤ 75	≤ 100
-125	≤ 100	≤ 125
-133	≤ 100	≤ 133

WRITE BURST MODE

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

TRUTH TABLE - COMMANDS AND DQM OPERATION (NOTE 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQM	ADDR	I/Os
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X
NO OPERATION (NOP)	L	H	H	H	X	X	X
ACTIVE (Select bank and activate row) (3)	L	L	H	H	X	Bank/Row	X
READ (Select bank and column, and start READ burst) (4)	L	H	L	H	L/H [8]	Bank/Col	X
WRITE (Select bank and column, and start WRITE burst) (4)	L	H	L	L	L/H [8]	Bank/Col	Valid
BURST TERMINATE	L	H	H	L	X	X	Active
PRECHARGE (Deactivate row in bank or banks) (5)	L	L	H	L	X	Code	X
AUTO REFRESH or SELF REFRESH (Enter self refresh mode) (6, 7)	L	L	L	H	X	X	X
LOAD MODE REGISTER (2)	L	L	L	L	X	Op-Code	X
Write Enable/Output Enable (8)	–	–	–	–	L	–	Active
Write Inhibit/Output High-Z (8)	–	–	–	–	H	–	High-Z

NOTES:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0-11 define the op-code written to the Mode Register and A12 should be driven low.
3. A0-12 provide row address, and BA0, BA1 determine which bank is made active.
4. A0-9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the I/Os during WRITEs (zero-clock delay) and READs (two-clock delay).

COMMANDS

The Truth Table provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear following the Operation section; these tables provide current state/ next state information.

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The Mode Register is loaded via inputs A0-11 (A12 should be driven low). See Mode Register heading in the Register Definition section. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until t_{MRD} is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-9 selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the READ burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. Read data appears on the I/Os subject to the logic level on the DQM inputs

two clocks earlier. If a given DQM signal was registered HIGH, the corresponding I/Os will be High-Z two clocks later; if the DQM signal was registered LOW, the I/Os will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-9 selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the WRITE burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. Input data appearing on the I/Os is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank PRECHARGE function described above, without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where AUTO PRECHARGE does not apply. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time.

BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analagous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. Each 512Mb SDRAM requires 8,192 AUTO REFRESH cycles every refresh period (t_{REF}). Providing a distributed AUTO REFRESH command will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (t_{RC}), once every refresh period (t_{REF}).

SELF REFRESH*

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care,” with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to tRAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints

* Self refresh available in commercial and industrial temperatures only.

specified for the clock pin) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for t_{XSR}, because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on V_{CC}, V_{CCQ} Supply relative to Vss	-1 to 4.6	V
Voltage on NC or I/O pins relative to Vss	-1 to 4.6	V
Operating Temperature TA (Mil)	-55 to +125	°C
Operating Temperature TA (Ind)	-40 to +85	°C
Storage Temperature, Plastic	-55 to +125	°C

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (NOTE 2)

Parameter	Symbol	Max	Unit
Input Capacitance: CLK	CI1	TBD	pF
Addresses, BA0-1 Input Capacitance	CA	TBD	pF
Input Capacitance: All other input-only pins	CI2	TBD	pF
Input/Output Capacitance: I/Os	CIO	TBD	pF

BGA THERMAL RESISTANCE

Description	Symbol	Max	Unit	Notes
Junction to Ambient (No Airflow)	Theta JA	20.7	C/W	1
Junction to Ball	Theta JB	18.1	C/W	1
Junction to Case (Top)	Theta JC	7.5	C/W	1

NOTE:
Refer to Application Note “PBGA Thermal Resistance Correlation” at www.wedc.com in the application notes section for modeling conditions.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS (NOTES 1, 6)

V_{CC}, V_{CCQ} = +3.3V ± 0.3V; -55°C ≤ T_A ≤ +125°C

Parameter/Condition	Symbol	Min	Max	Units
Supply Voltage	V_{CC},V_{CCQ}	3	3.6	V
Input High Voltage: Logic 1; All inputs (21)	V_{IH}	2	V_{CC} + 0.3	V
Input Low Voltage: Logic 0; All inputs (21)	V_{IL}	-0.3	0.8	V
Input Leakage Current: Any input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-5	5	µA
Input Leakage Address Current (All other pins not under test = 0V)	I_I	-20	20	µA
Output Leakage Current: I/Os are disabled; 0V V_{OUT} V_{CCQ}	I_{OZ}	-5	5	µA
Output Levels: Output High Voltage (I_{OUT} = -4mA)	V_{OH}	2.4	–	V
Output Low Voltage (I_{OUT} = 4mA)	V_{OL}	–	0.4	V

ICC SPECIFICATIONS AND CONDITIONS (NOTES 1,6,11,13)

V_{CC}, V_{CCQ} = +3.3V ± 0.3V; -55°C ≤ T_A ≤ +125°C

Parameter/Condition	Symbol	Max	Units
Operating Current: Active Mode; Burst = 2; Read or Write; t_{RC} = t_{RC} (min); CAS latency = 3 (3, 18, 19)	I_{CC1}	440	mA
Standby Current: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after t_{RCD} met; No accesses in progress (3, 12, 19)	I_{CC3}	180	mA
Operating Current: Burst Mode; Continuous burst; Read or Write; All banks active; CAS latency = 3 (3, 18, 19)	I_{CC4}	460	mA
Self Refresh Current: CKE 0.2V (Commercial and Industrial Temperature: 0°C to + 70°C) (27)	I_{CC7}	24	mA

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CHARACTERISTICS (NOTES 5, 6, 8, 9, 11)

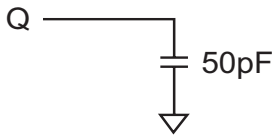
Parameter		Symbol	-100 Min	-100 Max	-125 Min	-125 Max	-133 Min	-133 Max	Unit
Access time from CLK (pos. edge)	CL = 3	t_{AC}		7		6		5.5	ns
	CL = 2	t_{AC}		7		6		6	ns
Address hold time		t_{AH}	1		1		0.8		ns
Address setup time		t_{AS}	2		2		1.5		ns
CLK high-level width		t_{CH}	3		3		2.5		ns
CLK low-level width		t_{CL}	3		3		2.5		ns
Clock cycle time (22)	CL = 3	t_{CK}	10		8		7.5		ns
	CL = 2	t_{CK}	13		10		10		ns
CKE hold time		t_{CKH}	1		1		0.8		ns
CKE setup time		t_{CKS}	2		2		1.5		ns
CS#, RAS#, CAS#, WE#, DQM hold time		t_{CMH}	1		1		0.8		ns
CS#, RAS#, CAS#, WE#, DQM setup time		t_{CMS}	2		2		1.5		ns
Data-in hold time		t_{DH}	1		1		0.8		ns
Data-in setup time		t_{DS}	2		2		1.5		ns
Data-out high-impedance time	CL = 3 (10)	t_{HZ}		7		6		5.5	ns
	CL = 2 (10)	t_{HZ}		7		6		6	ns
Data-out low-impedance time		t_{LZ}	1		1		1		ns
Data-out hold time (load)		t_{OH}	3		3		3		ns
Data-out hold time (no load) (26)		t_{OHN}	1.8		1.8		1.8		ns
ACTIVE to PRECHARGE command		t_{RAS}	50	120,000	50	120,000	50	120,00	ns
ACTIVE to ACTIVE command period		t_{RC}	70		68		68		ns
ACTIVE to READ or WRITE delay		t_{RCD}	20		20		20		ns
Refresh period (8,192 rows) – Commercial, Industrial		t_{REF}		64		64		64	ms
Refresh period (8,192 rows) – Military		t_{REF}		16		16		16	ms
AUTO REFRESH period		t_{RFC}	70		70		70		ns
PRECHARGE command period		t_{RP}	20		20		20		ns
ACTIVE bank A to ACTIVE bank B command		t_{RRD}	20		20		20		ns
Transition time (7)		t_T	0.3	1.2	0.3	1.2	0.3	1.2	ns
WRITE recovery time	(23)	t_{WR}	1 CLK + 7ns		1 CLK + 7ns		1 CLK + 7.5ns		—
	(24)		15		15		15		ns
Exit SELF REFRESH to ACTIVE command		t_{XSR}	80		80		75		ns

AC FUNCTIONAL CHARACTERISTICS (NOTES 5,6,7,8,9,11)

Parameter/Condition		Symbol	-100	-125	-133	Units
READ/WRITE command to READ/WRITE command (17)		t_{CCD}	1	1	1	t_{CK}
CKE to clock disable or power-down entry mode (14)		t_{CKED}	1	1	1	t_{CK}
CKE to clock enable or power-down exit setup mode (14)		t_{PED}	1	1	1	t_{CK}
DQM to input data delay (17)		t_{DQD}	0	0	0	t_{CK}
DQM to data mask during WRITEs		t_{DQM}	0	0	0	t_{CK}
DQM to data high-impedance during READs		t_{DQZ}	2	2	2	t_{CK}
WRITE command to input data delay (17)		t_{DWD}	0	0	0	t_{CK}
Data-in to ACTIVE command (15)		t_{DAL}	4	5	5	t_{CK}
Data-in to PRECHARGE command (16)		t_{DPL}	2	2	2	t_{CK}
Last data-in to burst STOP command (17)		t_{BDL}	1	1	1	t_{CK}
Last data-in to new READ/WRITE command (17)		t_{CDL}	1	1	1	t_{CK}
Last data-in to PRECHARGE command (16)		t_{RDL}	2	2	2	t_{CK}
LOAD MODE REGISTER command to ACTIVE or REFRESH command (25)		t_{MRD}	2	2	2	t_{CK}
Data-out to high-impedance from PRECHARGE command (17)	CL = 3	t_{ROH}	3	3	3	t_{CK}
	CL = 2	t_{ROH}	2	—	—	t_{CK}

NOTES:

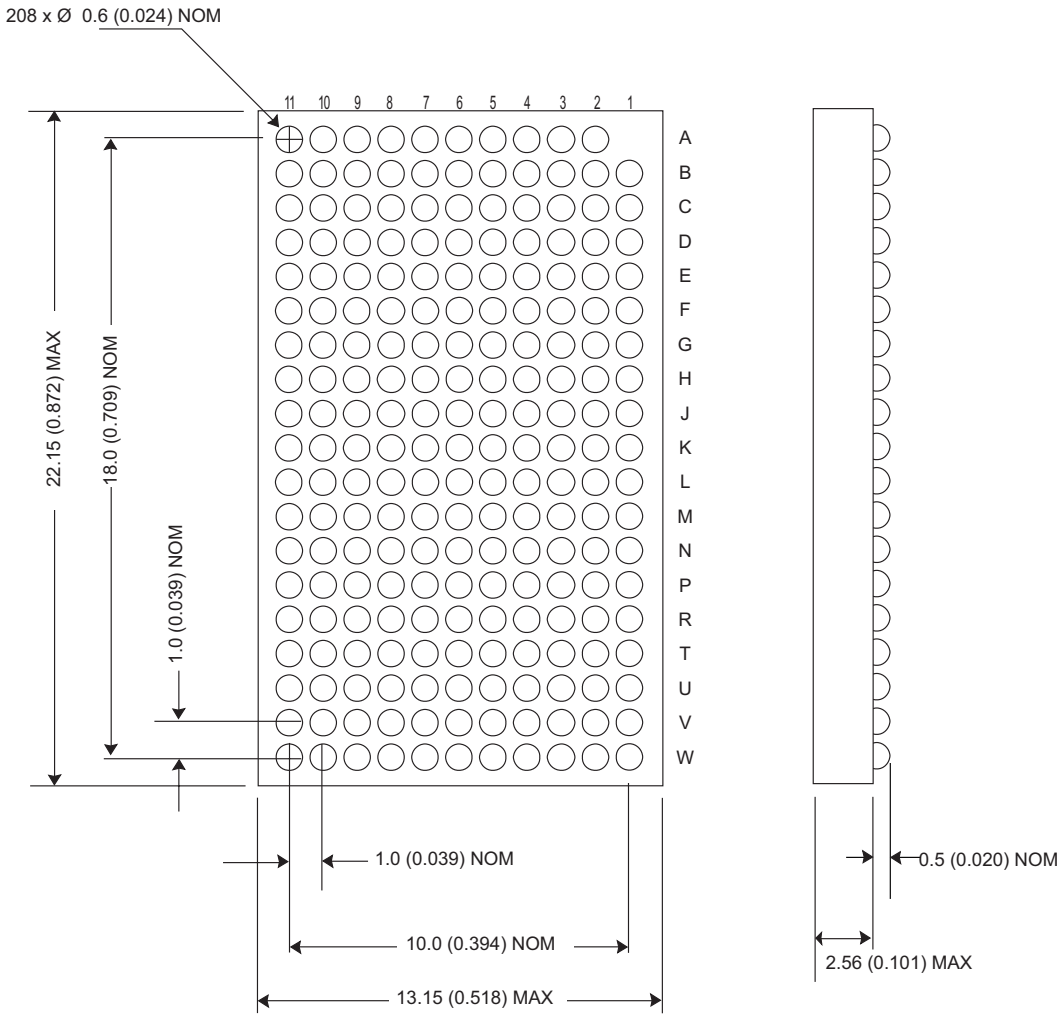
1. All voltages referenced to V_{SS}.
2. This parameter is not tested but guaranteed by design. f = 1 MHz, T_A = 25°C.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{CC} and V_{CCQ} must be powered up simultaneously.) The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume t_T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. t_{HZ} defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet t_{OH} before going High-Z.
11. AC timing and I_{CC} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{CC} specifications are tested after the device is properly initialized.
14. Timing actually specified by t_{CKS}; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by t_{WR} plus t_{RP}; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by t_{WR}.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{CC} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. V_{IH} overshoot: V_{IH} (MAX) = V_{CCQ} + 2V for a pulse width 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width 3ns.
22. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including t_{WR}, and PRECHARGE commands). CKE may be used to reduce the data rate.
23. Auto precharge mode only. The precharge timing budget (t_{RP}) begins 7.5ns/7ns after the first clock delay, after the last WRITE is executed.
24. Precharge mode only.
25. JEDEC and PC100 specify three clocks.
26. Parameter guaranteed by design.
27. Self refresh available in commercial and industrial temperatures only.

PACKAGE DIMENSION: 208 PLASTIC BALL GRID ARRAY (PBGA), 13mm x 22mm

Bottom View



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W 3 32M 64 V - XXX SB X

WHITE ELECTRONIC DESIGNS CORP.

SDRAM

CONFIGURATION, 32M x 64

3.3V Power Supply

FREQUENCY (MHz)

100 = 100MHz
125 = 125MHz
133 = 133 MHz

PACKAGE:

SB = 208 Plastic Ball Grid Array (PBGA), 13mm x 22mm

DEVICE GRADE:

M =	Military	-55°C to +125°C
I =	Industrial	-40°C to +85°C
C =	Commercial	0°C to +70°C

Document Title

32M x 64 SDRAM Multi-Chip Package, 13mm x 22mm

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	October 2004	Advanced
Rev 1	Changes (Pg. 1, 9, 13, 15) 1.1 Change status to Preliminary 1.2 PNC#04019 – Change max thickness of package body to 2.56mm 1.3 Change max storage temperature to 125°C 1.4 Change typical weight to 1.5g 1.5 Add thermal resistance values	May 2005	Preliminary
Rev. 2	Changes (Pg. 1, 10, 15) 2.1 Update input leakage address current 2.2 Update I_{CC1}, I_{CC3}, I_{CC4} and I_{CC7}	August 2005	Preliminary
Rev.3	Changes (Pg. 1-15) 3.1 Change status to Final 3.2 Add 133MHz operation charcteristics	September 2005	Final