DDR SDRAM Small-Outline DIMM

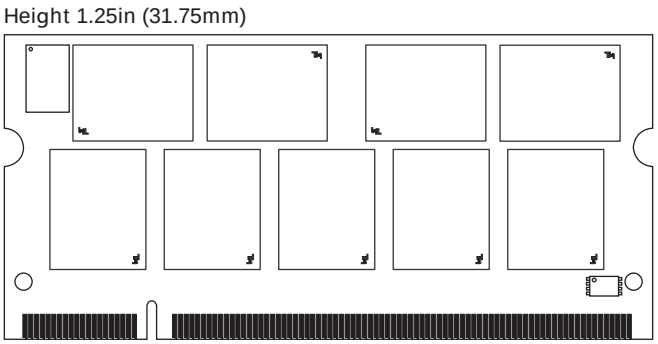
MT9VDDF3272PH(I) – 256MB,
MT9VDDF6472PH(I) – 512MB

For component specifications, refer to Micron's Web site: www.micron.com/products/ddrsdram

Features

- 200-pin, small-outline, dual in-line memory module (SODIMM)
- Supports ECC error detection and correction
- Fast data transfer rates: PC2100 and PC2700
- Utilizes 266 MT/s and 333 MT/s DDR SDRAM components
- 256MB (32 Meg x 72) and 512MB (64 Meg x 72)
- $V_{DD} = V_{DD}Q = +2.5V$
- $V_{DDSPD} = +2.3V$ to $+3.6V$
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs CK and CK#
- Programmable READ CAS latency
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 7.8125µs maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Gold edge contacts

Figure 1: 200-Pin SODIMM (MO-224)



Options — Marking

- Operating Temperature Range
  - Commercial ($0°C \le T_A \le +70°C$) — None
  - Industrial ($-40°C \le T_A \le +85°C$) — I[1]
- Package
  - 200-pin SODIMM (standard) — G
  - 200-pin SODIMM (lead-free) — Y[1]
- Clock frequency, speed, CAS latency[2]
  - 6ns (267 MHz), 333 MT/s, CL = 2.5 — -335
  - 7.5ns (133 MHz), 266 MT/s, CL = 2 — -262[1]
  - 7.5ns (133 MHz), 266 MT/s, CL = 2 — -26A[1]
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.5 — -265
- PCB Height
  - 1.25in. (31.75mm)

Notes: 1. Consult Micron for product availability.
2. CL = Device CAS (READ) latency.

Table 1: Address Table

	256MB	512MB
Refresh Count	8K	8K
Row Addressing	8K (A0–A12)	8K (A0–A12)
DeviceBankAddressing	4 (BA0, BA1)	4 (BA0, BA1)
Base Device Configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)
Column Addressing	1K (A0–A9)	1K (A0–A9, A11)
Module Rank Addressing	1 (S0#)	1 (S0#

Table 2: Part Numbers and Timing Parameters

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Latency (CL - ^{t}RCD - ^{t}RP)
MT9VDDF3272PHG-335_	256MB	32 Meg x 72	2.7 GB/s	6ns, 333 MT/s	2.5-3-3
MT9VDDF3272PHY-335_	256MB	32 Meg x 72	2.7 GB/s	6ns, 333 MT/s	2.5-3-3
MT9VDDF3272PHG-262_	256MB	32 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2-2-2
MT9VDDF3272PHY-262_	256MB	32 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2-2-2
MT9VDDF3272PHG-26A_	256MB	32 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2-3-3
MT9VDDF3272PHY-26A_	256MB	32 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2-3-3
MT9VDDF3272PH(I)G-265_	256MB	32 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2.5-3-3
MT9VDDF3272PH(I)Y-265_	256MB	32 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2.5-3-3
MT9VDDF6472PHG-335_	512MB	64 Meg x 72	2.7 GB/s	6ns, 333 MT/s	2.5-3-3
MT9VDDF6472PHY-335_	512MB	64 Meg x 72	2.7 GB/s	6ns, 333 MT/s	2.5-3-3
MT9VDDF6472PHG-262_	512MB	64 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2-2-2
MT9VDDF6472PHY-262_	512MB	64 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2-2-2
MT9VDDF6472PHG-26A_	512MB	64 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2-3-3
MT9VDDF6472PHY-26A_	512MB	64 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2-3-3
MT9VDDF6472PH(I)G-265_	512MB	64 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2.5-3-3
MT9VDDF6472PH(I)Y-265_	512MB	64 Meg x 72	2.1 GB/s	7.5ns, 266 MT/s	2.5-3-3

Note: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9VDDF3272PHG-265A1.

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Pin Assignments and Descriptions

Table 3: Pin Assignment

200-Pin SODIMM Front								200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	VSS	101	A9	151	DQ42	2	VREF	52	VSS	102	A8	152	DQ46
3	VSS	53	DQ19	103	VSS	153	DQ43	4	VSS	54	DQ23	104	VSS	154	DQ47
5	DQ0	55	DQ24	105	A7	155	VDD	6	DQ4	56	DQ28	106	A6	156	VDD
7	DQ1	57	VDD	107	A5	157	VDD	8	DQ5	58	VDD	108	A4	158	NC
9	Vdd	59	DQ25	109	A3	159	VSS	10	VDD	60	DQ29	110	A2	160	NC
11	DQS0	61	DQS3	111	A1	161	VSS	12	DM0	62	DM3	112	A0	162	VSS
13	DQ2	63	VSS	113	VDD	163	DQ48	14	DQ6	64	VSS	114	VDD	164	DQ52
15	VSS	65	DQ26	115	A10/AP	165	DQ49	16	VSS	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	VDD	18	DQ7	68	DQ31	118	RAS#	168	VDD
19	DQ8	69	VDD	119	WE#	169	DQS6	20	DQ12	70	VDD	120	CAS#	170	DM6
21	VDD	71	CB0	121	S0#	171	DQ50	22	VDD	72	CB4	122	NC	172	DQ54
23	DQ9	73	CB1	123	NC	173	VSS	24	DQ13	74	CB5	124	NC	174	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51	26	DM1	76	VSS	126	VSS	176	DQ55
27	VSS	77	DQS8	127	DQ32	177	DQ56	28	VSS	78	DM8	128	DQ36	178	DQ60
29	DQ10	79	CB2	129	DQ33	179	VDD	30	DQ14	80	CB6	130	DQ37	180	VDD
31	DQ11	81	VDD	131	VDD	181	DQ57	32	DQ15	82	VDD	132	VDD	182	DQ61
33	VDD	83	CB3	133	DQS4	183	DQS7	34	VDD	84	CB7	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	VSS	36	VDD	86	NC	136	DQ38	186	VSS
37	CK0#	87	VSS	137	VSS	187	DQ58	38	VSS	88	VSS	138	VSS	188	DQ62
39	VSS	89	NC	139	DQ35	189	DQ59	40	VSS	90	VSS	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	VDD	42	DQ20	92	VDD	142	DQ44	192	VDD
43	DQ17	93	VDD	143	VDD	193	SDA	44	DQ21	94	VDD	144	VDD	194	SA0
45	VDD	95	NC	145	DQ41	195	SCL	46	VDD	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	VDDSPD	48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	VSS	199	NC	50	DQ22	100	A11	150	VSS	200	NC

Figure 2: Module Layout

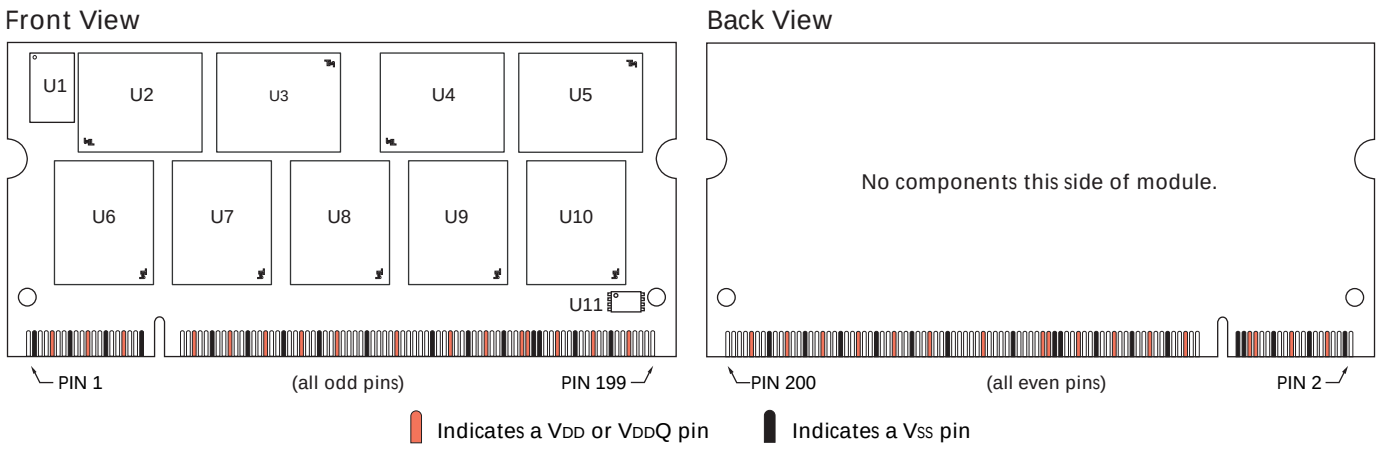


Table 4: Pin Descriptions

Refer to Pin Assignment Tables on page 6 for pin number and symbol correlation.

Pin Numbers	Symbol	Type	Description
118, 119, 120	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
35, 37	CK0, CK0#	Input	Clock: CK and CK# are differential clock inputs distributed through an on-board PLL to all devices. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
96	CKE0,	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers.and output drivers. Taking CKE LOW provides PRECHARGE POWER- DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after VDD is applied.
121	S0#	Input	Chip Select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All com- mands are masked when S# is registered HIGH. S# is considered part of the command code.
117, 116	BA0, BA1	Input	Bank Address: BA0, BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
99, 100, 101,102, 105, 106, 107, 108, 109, 110, 111, 112, 115	A0–A12 (256MB, 512MB)	Input	Address Inputs: A0-A11/A12 provide the row address for ACTIVE commands, and the column address, and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
11, 25, 47, 61, 77, 133, 147,169, 183	DQS0–DQS8	Input/ Output	Data Strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data.
12, 26, 48, 62, 78, 134, 148, 170, 184	DM0–DM8	Input	Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
71, 72, 73, 74, 79, 80, 83, 84	CB0–CB7	Input/ Output	Check Bits.

Table 4: Pin Descriptions

Refer to Pin Assignment Tables on page 6 for pin number and symbol correlation.

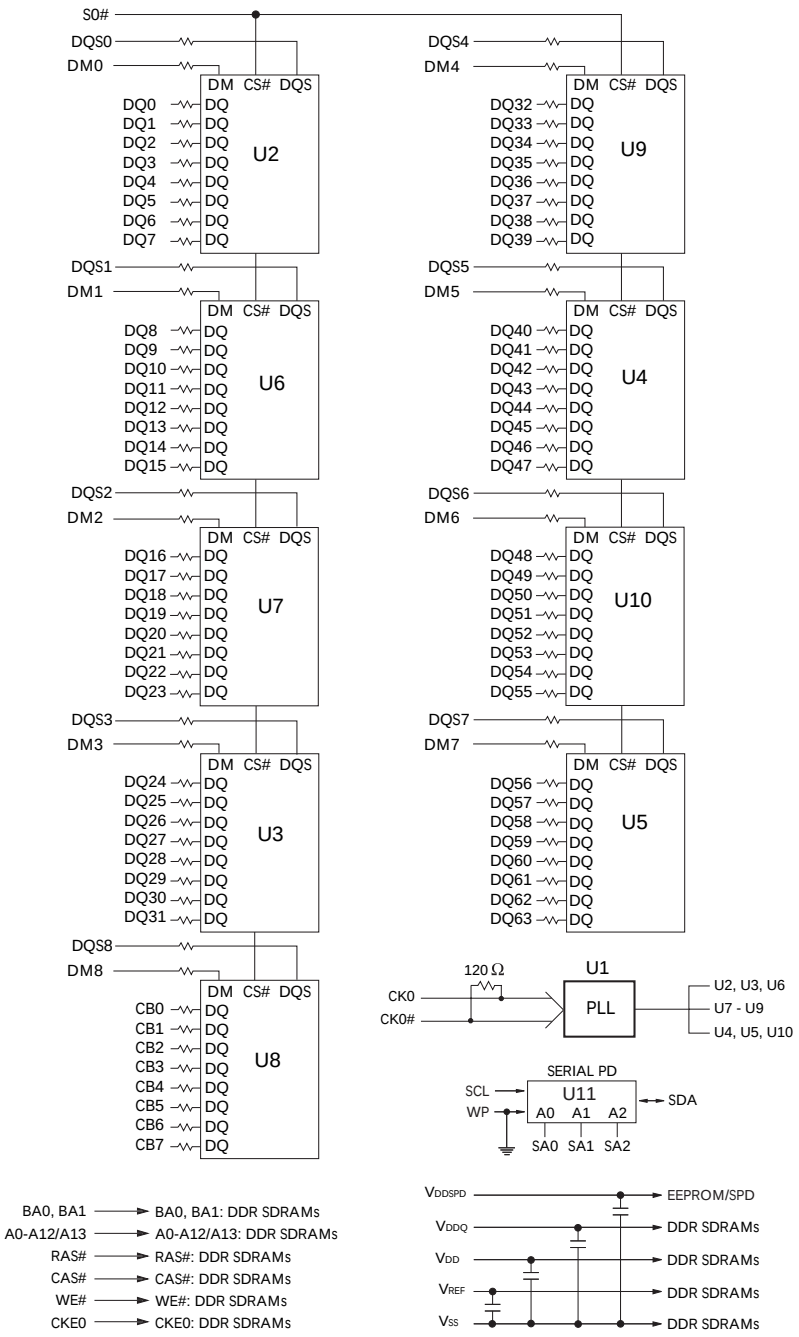
Pin Numbers	Symbol	Type	Description
5, 6, 7, 8, 13, 14, 17, 18, 19, 20, 23, 24, 29, 30, 31, 32, 41, 42, 43, 44, 49, 50, 53, 54, 55, 56, 59, 60, 61, 65, 66, 67, 68, 127, 128, 129, 130, 135, 136, 139, 140, 141, 142, 145, 146, 151, 152, 153, 154, 163, 164, 165, 166, 171, 172, 175, 176, 177, 181, 182, 187, 188, 189, 190	DQ0–DQ63	Input/ Output	Data I/Os: Data bus.
195	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
194, 196, 198	SA0–SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
193	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
1, 2	V_{REF}	Supply	SSTL_2 reference voltage.
9, 10, 21, 22, 33, 34, 36, 45, 46, 57, 58, 69, 70, 81, 82, 92, 93, 94, 113, 114, 131, 132, 143, 144, 155, 156, 157, 167, 168, 179, 180, 191, 192	V_{DD}	Supply	DQ Power Supply: +2.5V ±0.2V.
3, 4, 15, 16, 27, 28, 38, 39, 40, 51, 52, 63, 64, 75, 76, 87, 88, 90, 103, 104, 125, 126, 137, 138, 149, 150, 159, 161, 162, 173, 174, 185, 186	V_{SS}	Supply	Ground.
197	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V.
85, 86, 89, 91, 95, 97, 98, 122, 123, 124, 158, 160, 200	NC	–	No Connect: These pins should be left unconnected.

Functional Block Diagram

All resistor values are 22Ω unless otherwise specified. Per industry standard, Micron modules utilize various component speed grades, as referenced in the module part numbering guide at www.micron.com/numberguide.

Standard modules use the following DDR SDRAM devices: MT46V32M8FG (256MB); MT46V64M8FN (512MB). Lead-free modules use the following DDR SDRAM devices: MT46V32M8BG (256MB); MT46V64M8BN (512MB). For component specifications, refer to component data sheets at: www.micron.com/products/ddrsdram.

Figure 3: Functional Block Diagram



General Description

The Micron MT9VDDF3272PH and MT9VDDF6472PH are high-speed CMOS, dynamic random-access, 256MB and 512MB memory modules organized in x72 (ECC) configuration. DDR SDRAM modules use internally configured quad-bank DDR SDRAM devices.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2n-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK. A phase-lock loop (PLL) device on the module is used to redrive the differential clock signals to the DDR SDRAM devices to minimize system clock loading.

PLL Operation

A phase-lock loop (PLL) on the module is used to redrive the differential clock signals CK and CK# to the DDR SDRAM devices to minimize system clock loading.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Table 5: CAS Latency (CL) Table

Speed	Allowable Operating Clock Frequency (MHz)	
	CL = 2	CL = 2.5
-335	N/A	75 ≤ f ≤ 167
-262	75 ≤ f ≤ 133	75 ≤ f ≤ 133
-26A	75 ≤ f ≤ 133	75 ≤ f ≤ 133
-265	75 ≤ f ≤ 100	75 ≤ f ≤ 133

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Absolute Maximum Ratings Table

Parameter		Rating
V_{DD} Supply Voltage Relative to V_{SS}		-1V to +3.6V
V_{DDQ} supply voltage relative to V_{SS}		-1V to +3.6V
V_{REF} and inputs voltage relative to V_{SS}		-1V to +3.6V
I/O pins voltage relative to V_{SS}		-0.5V to V_{DDQ} + 0.5V
Operating temperature	T_A (ambient - commercial)	0°C to +70°C
	T_A (ambient - industrial)	-40°C to +85°C
Storage temperature (plastic)		-55°C to +150°C
Short circuit output current		50mA

Table 7: DC Electrical Characteristics and Operating Conditions
Notes: 1–5, 13; notes appear on pages 15–17; 0°C ≤ T_A ≤ +70°C

Parameter/Condition		Symbol	Min	Max	Units	Notes
Supply Voltage		V_{DD}	2.3	2.7	V	19, 35
I/O Supply Voltage		V_{DDQ}	2.3	2.7	V	19, 35, 36
I/O Reference Voltage		V_{REF}	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	6, 36
I/O Termination Voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	7, 36
Input High (Logic 1) Voltage		V_{IH}(DC)	V_{REF} + 0.15	V_{DD} + 0.3	V	17
Input Low (Logic 0) Voltage		V_{IL}(DC)	-0.3	V_{REF} - 0.15	V	17
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE#, CKE, S#	I_I	-18	18	µA	41
	CK, CK#	I_I	-5	5	µA	
	DM	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	DQ, DQS	I_{OZ}	-5	5	µA	41
OUTPUT LEVELS: High Current (V_{OUT} = V_{DDQ}-0.373V, minimum V_{REF}, minimum V_{TT})		I_{OH}	-16.8	–	mA	20, 34
Low Current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})		I_{OL}	16.8	–	mA	

Table 8: IDD Specifications and Conditions – 256MB

DDR SDRAM components only;
Notes: 1–5, 8, 10, 12, 42; notes appear on pages 15–17; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

			Max				
Parameter/Condition		**Symbol**	**-335**	**-262**	**-26A/ -265**	**Units**	**Notes**
OPERATING CURRENT: One device bank; Active-Precharge; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles		IDD0	1,125	1,125	960	mA	14, 37
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,530	1,440	1,305	mA	14, 37
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ^tCK = ^tCK (MIN); CKE = (LOW)		IDD2P	35	36	36	mA	15, 18, 39
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ^tCK = ^tCK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	450	405	405	mA	40
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		IDD3P	270	225	225	mA	15, 18, 39
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ^tRC = RAS (MAX); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	540	450	450	mA	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; CK = ^tCK (MIN); IOUT = 0mA		IDD4R	1,575	1,350	1,350	mA	14, 37
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,400	1,200	1,200	mA	14
AUTO REFRESH CURRENT	^tREFC = ^tRFC(MIN)	IDD5	2,295	2,115	2,115	mA	14, 39
	^tREFC = 7.8125µs	IDD5A	54	54	54	mA	16, 39
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD6	36	36	36	mA	9
OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge with, ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); Address and control inputs change only during Active READ, or WRITE commands		IDD7	3,645	3,150	3,150	mA	14, 38

Table 9: IDD Specifications and Conditions – 512MB

DDR SDRAM components only;
Notes: 1–5, 8, 10, 12, 42; notes appear on pages 15–17; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

			Max				
Parameter/Condition		**Symbol**	**-335**	**-262**	**-26A/ -265**	**Units**	**Notes**
OPERATING CURRENT: One device bank; Active-Precharge; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles		IDD0	1,040	1,040	920	mA	14, 37
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,280	1,280	1,160	mA	14, 37
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ^tCK = ^tCK (MIN); CKE = (LOW)		IDD2P	40	40	40	mA	15, 18, 39
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ^tCK = ^tCK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	360	360	320	mA	40
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		IDD3P	280	280	240	mA	15, 18, 39
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ^tRC = RAS (MAX); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	400	400	360	mA	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; CK = ^tCK (MIN); IOUT = 0mA		IDD4R	1,320	1,320	1,160	mA	14, 37
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,400	1,240	1,080	mA	14
AUTO REFRESH CURRENT	^tREFC = ^tRFC (MIN)	IDD5	2,320	2,320	2,240	mA	14, 39
	^tREFC = 7.8125µs	IDD5A	80	80	80	mA	16, 39
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD6	40	40	40	mA	9
OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge with, ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); Address and control inputs change only during Active READ, or WRITE commands		IDD7	3,240	3,200	2,800	mA	14, 38

Table 10: Capacitance)

Note: 11; notes appear on pages 15–17

Parameter	Symbol	Min	Typ	Max	Units
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	5.0	–	6.0	pF
Input Capacitance: Command and Address, S#, CKE	C_{I1}	18.0	–	27.0	pF
Input Capacitance: CK, CK#	C_{I2}	–	7.7	–	pF

Electrical Characteristics and Recommended AC Operating Conditions

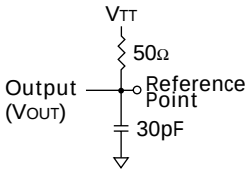
Recommended AC operating conditions are given in the DDR component data sheets, available at www.micron.com/products/ddrsdram. Module speed grades correlate with component speed grades as shown in the following table:

Table 11: Module and Component Speed Grade Table

Module Speed Grade	Component Speed Grade
-335	-6
-262	-75E
-26A	-75Z
-265	-75

Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on Vref may not exceed ±2 percent of the DC value. Thus, from V_{DDQ}/2, Vref is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 2 for -26A and -202, CL = 2.5 for -335 and -265 with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V, V_{REF} = V_{SS}, f = 100 MHz, T_A = 25°C, V_{OUT}(DC) = V_{DDQ}/2, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. For slew rates < 1 V/ns and ≥ to 0.5 Vns. If the slew rate is < 0.5V/ns, timing must be derated: ^{t}IS has an additional 50ps per each 100 mV/ns reduction in slew rate from 500 mV/ns, while ^{t}IH is unaffected. If the slew rate exceeds 4.5 V/ns, functionality is uncertain. For -335, slew rates must be ≥ 0.5 V/ns.
13. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 x V_{DDQ} is recognized as LOW.
14. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.

15. The refresh period 64ms. This equates to an average refresh rate of 7.8251µs. However, an AUTO REFRESH command must be asserted at least once every 70.3µs; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
16. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
17. To maintain a valid level, the transitioning edge of the input must:
    A. Sustain a constant slew rate from the current AC level through to the target AC level, V_{IL}(AC) or V_{IH}(AC).
    B. Reach at least the target AC level.
    C. After the AC target level is reached, continue to maintain at least the target DC level, V_{IL}(DC) or V_{IH}(DC).
18. V_{DD} must not vary more than 4 percent if CKE is not active while any bank is active.
19. Any positive glitch must be less than 1/3 of the clock and not more than +400mV or 2.9V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2V, whichever is more positive.
20. Normal Output Drive Curves:
    A. The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 4 on page 16.
    B. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 4 on page 16.
    C. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 5 on page 17
    D. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 5 on page 17.
    E. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature.
    F. The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent, for device drain-to-source voltages from 0.1V to 1.0V.

Figure 4: Pull-Down Characteristics

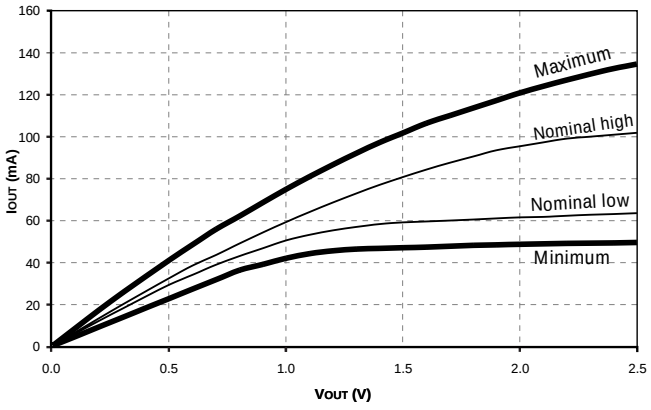
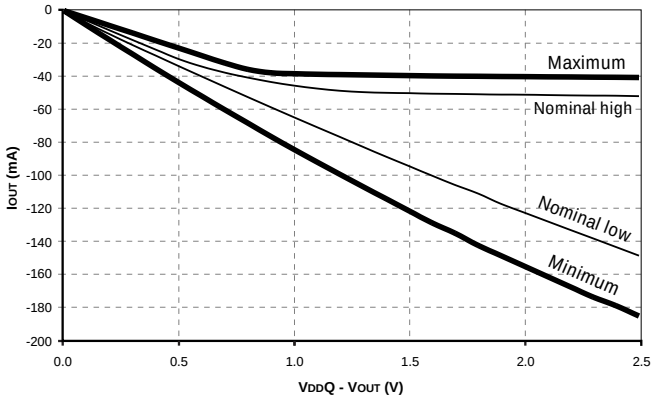


Figure 5: Pull-Up Characteristics



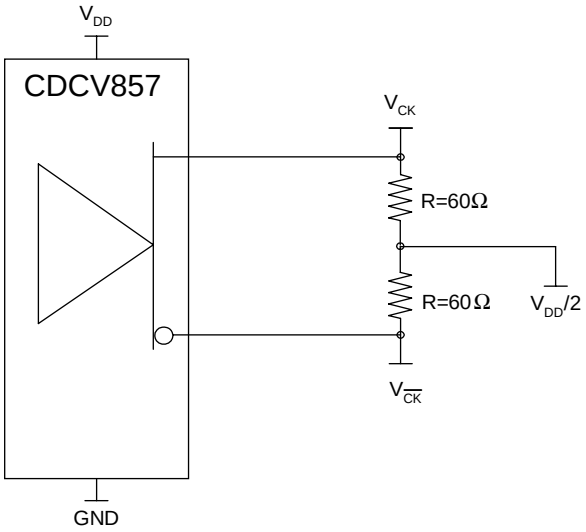
34. The voltage levels used are derived from a minimum VDD level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
35. VDD and VDDQ must track each other.
36. During initialization, VDDQ, VTT, and VREF must be equal to or less than VDD + 0.3V. Alternatively, VTT may be 1.35V maximum during power up, even if VDD/VDDQ are 0Vs, provided a minimum of 42Ω of series resistance is used between the VTT supply and the input pin.
37. Random addressing changing and 50 percent of data changing at every transfer.
38. Random addressing changing and 100 percent of data changing at every transfer.
39. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}REF later.
40. IDD2N specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is “worst case.”
41. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
42. When an input signal is HIGH or LOW, it is defined as a steady state logic HIGH or LOW.

PLL Specifications

Table 12: PLL Clock Driver Timing Requirements and Switching Characteristics
Note: 1

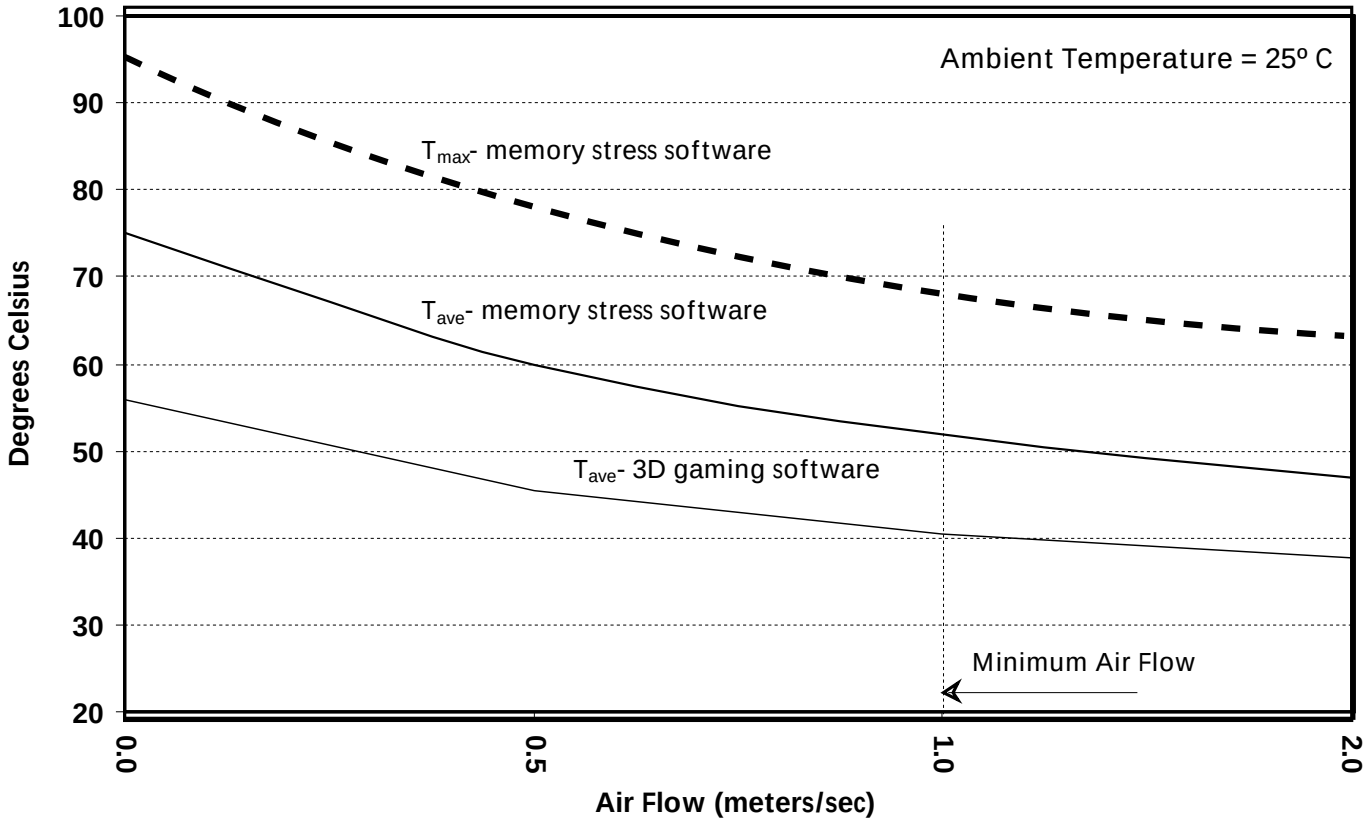
Parameter	Symbol	0°C ≤ T_A ≤ +70°C Vdd = +2.5V ±0.2V			Units	notes
		Min	Nominal	Max		
Operating Clock Frequency	^{f}CK	60	-	170	MHz	2, 3
Input Duty Cycle	^{t}DC	40	-	60	%	
Stabilization Time	$^{t}STAB$	-	-	100	ms	4
Cycle to Cycle Jitter	$^{t}JIT_{CC}$	-75	-	75	ps	
Static Phase Offset	$^{t}\varnothing$	-50	0	50	ps	5
Output Clock Skew	$^{t}SK_{O}$	-	-	100	ps	
Period Jitter	$^{t}JIT_{PER}$	-75	-	75	ps	6
Half-Period Jitter	$^{t}JIT_{HPER}$	-100	-	100	ps	6
Input Clock Slew Rate	$^{t}LS_{I}$	1.0	-	4	V/ns	
Output Clock Slew Rate	$^{t}LS_{O}$	1.0	-	2	V/ns	7

Notes:
1. The timing and switching specifications for the PLL listed above are critical for proper operation of DDR SDRAM modules. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this PLL is available in JEDEC Standard JESD82.
2. The PLL must be able to handle spread spectrum induced skew.
3. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low-speed system debug.)
4. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up.
5. Static Phase Offset does not include Jitter.
6. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
7. The output slew rate is determined from the IBIS model:



Thermal Specifications

Figure 6: Component Case Temperature vs. Air Flow



8. Micron Technology, Inc. recommends a minimum air flow of 1 meter/second (~197 LFM) across all modules.
9. The component case temperature measurements shown above were obtained experimentally. The typical system to be used for experimental purposes is a dual-processor 600 MHz work station, fully loaded, with four comparable registered memory modules. Case temperatures charted represent worst-case component locations on modules installed in the internal slots of the system.
10. Temperature versus air speed data is obtained by performing experiments with the system motherboard removed from its case and mounted in a Eiffel-type low air speed wind tunnel. Peripheral devices installed on the system motherboard for testing are the processor(s) and video card, all other peripheral devices are mounted outside of the wind tunnel test chamber.
11. The memory diagnostic software used for determining worst-case component temperatures is a memory diagnostic software application developed for internal use by Micron Technology, Inc.

Serial Presence-Detect

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 7 on page 20, and Figure 8 on page 21).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 9 on page 21).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 7: Data Validity

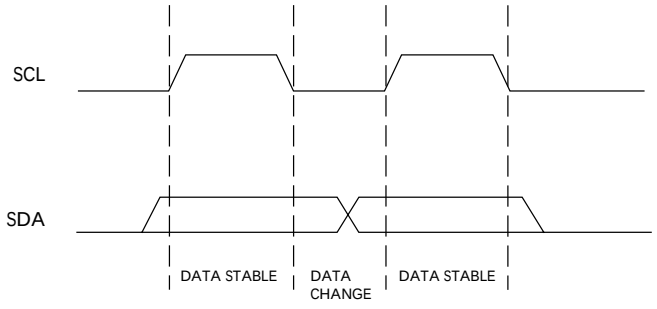


Figure 8: Definition of Start and Stop

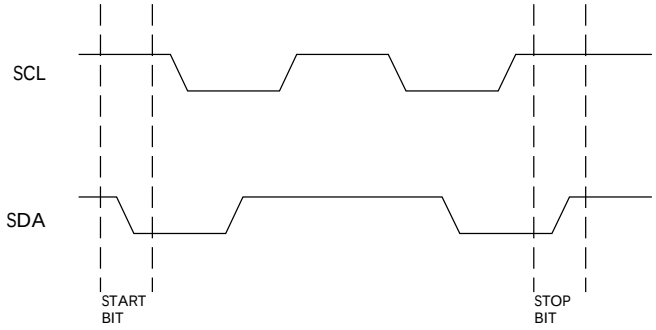


Figure 9: Acknowledge Response from Receiver

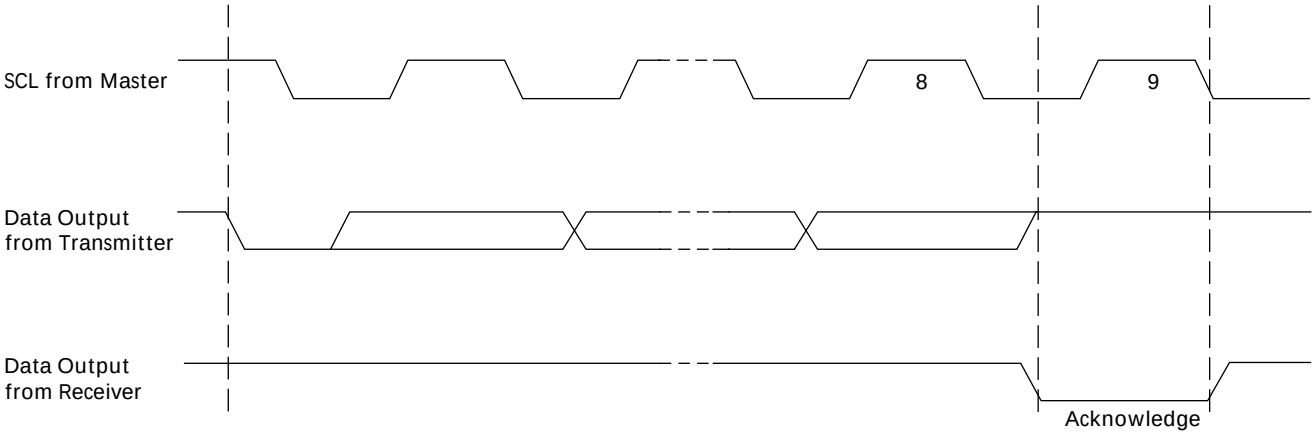


Table 13: EEPROM Device Select Code
Most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	RW

Table 14: EEPROM Operating Modes

Mode	RW Bit	WC	Bytes	Initial Sequence
Current Address Read	1	VIH or VIL	1	START, Device Select, RW = '1'
Random Address Read	0	VIH or VIL	1	START, Device Select, RW = '0', Address
	1	VIH or VIL	1	reSTART, Device Select, RW = '1'
Sequential Read	1	VIH or VIL	≥ 1	Similar to Current or Random Address Read
Byte Write	0	VIL	1	START, Device Select, RW = '0'
Page Write	0	VIL	≤ 16	START, Device Select, RW = '0'

Figure 10: SPD EEPROM Timing Diagram

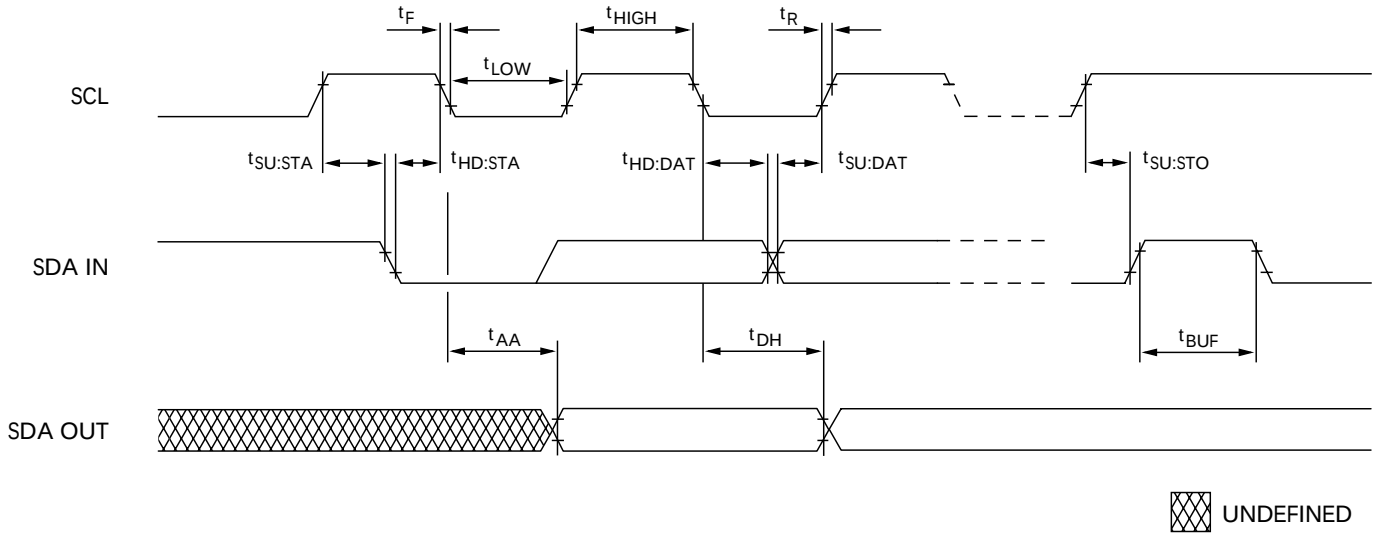


Table 15: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
SUPPLY VOLTAGE	V_{DD}	2.3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{SS} or V_{DD}	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA

Table 16: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3		µs	
Data-out hold time	^{t}DH	200		ns	
SDA and SCL fall time	^{t}F		300	ns	2
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	0.6		µs	
Clock HIGH period	$^{t}HIGH$	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		50	ns	
Clock LOW period	^{t}LOW	1.3		µs	
SDA and SCL rise time	^{t}R		0.3	µs	2
SCL clock frequency	^{f}SCL		400	KHz	
Data-in setup time	$^{t}SU:DAT$	100		ns	
Start condition setup time	$^{t}SU:STA$	0.6		µs	3
Stop condition setup time	$^{t}SU:STO$	0.6		µs	
WRITE cycle time	^{t}WRC		10	ms	4

Notes:
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 17: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT9VDDF3272PH	MT9VDDF6472PH
0	Number of SPD Bytes Used by Micron	128	80	80
1	Total Number of Bytes in SPD Device	256	08	08
2	Fundamental Memory Type	DDR SDRAM	07	07
3	Number of Row Addresses on Ass'y	13	0D	0D
4	Number of Column Addresses on Ass'y	10 or 11	0A	0B
5	Number of Physical Ranks on DIMM	1	01	01
6	Module Data Width	72	48	48
7	Module Data Width (Continued)	0	00	00
8	Module Voltage Interface Levels	SSTL 2.5V	04	04
9	SDRAM Cycle Time, ^{t}CK (CAS Latency = 2.5) (see note 2)	6ns (-335) 7ns (-262/-26A) 7.5ns (-265)	60 70 75	60 70 75
10	SDRAM Access from Clock, ^{t}AC (CAS Latency = 2.5) (see note 1)	0.7ns (-335) 0.75ns (-262/-26A/-265)	70 75	70 75
11	Module Configuration Type	ECC	02	02
12	Refresh Rate/ Type	15.6µs or 7.8µs/SELF	82	82
13	SDRAM Device Width (Primary DDR SDRAM)	8	08	08
14	Error-checking DDR SDRAM Data Width	8	08	08
15	Minimum Clock Delay, Back-to-Back Random Column Access	1 clock	01	01
16	Burst Lengths Supported	2, 4, 8	0E	0E
17	Number of Banks on DDR SDRAM Device	4	04	04
18	CAS Latencies Supported	2, 2.5	0C	0C
19	CS Latency	0	01	01
20	WE Latency	1	02	02
21	SDRAM Module Attributes	Unbuff, Diff CLK, PLL	24	24
22	SDRAM Device Attributes: General	Fast/concurrent AP	C0	C0
23	SDRAM Cycle Time, ^{t}CK (CL = 2) (See note 2)	7.5ns (-335/-262/-26A) 10ns (-265)	75 A0	75 A0
24	SDRAM Access from CK, ^{t}AC (CL = 2) (See note 2)	0.7ns (-335) 0.75ns (-265/-26A)	70 75	70 75
25	SDRAM Cycle Time, ^{t}CK (CL = 1.5)	N/A	00	00
26	SDRAM Access from CK, ^{t}AC (CL = 1.5)	N/A	00	00
27	Minimum Row Precharge Time, ^{t}RP (see note 5)	18ns (-335) 15ns (-262) 20ns (-26A/-265)	48 3C 50	48 3C 50
28	Minimum Row Active to Row Active, ^{t}RRD	12ns (-335) 15ns (-262/-26A/-265)	30 3C	30 3C
29	Minimum RAS# to CAS# Delay, ^{t}RCD (see note 5)	18ns (-335) 15ns (-262) 20ns (-26A/-265)	48 3C 50	48 3C 50
30	Minimum RAS# Pulse Width, ^{t}RAS (see note 3)	42ns (-335) 45ns (-262/-26A/-265)	2A 2D	2A 2D
31	Module Rank Density	256MB, 512MB	40	80
32	Address and Command Setup Time, ^{t}IS (see note 4)	0.8ns (-335) 1.0ns (-262/-26A/-265)	80 A0	80 A0

Table 17: Serial Presence-Detect Matrix (Continued)
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

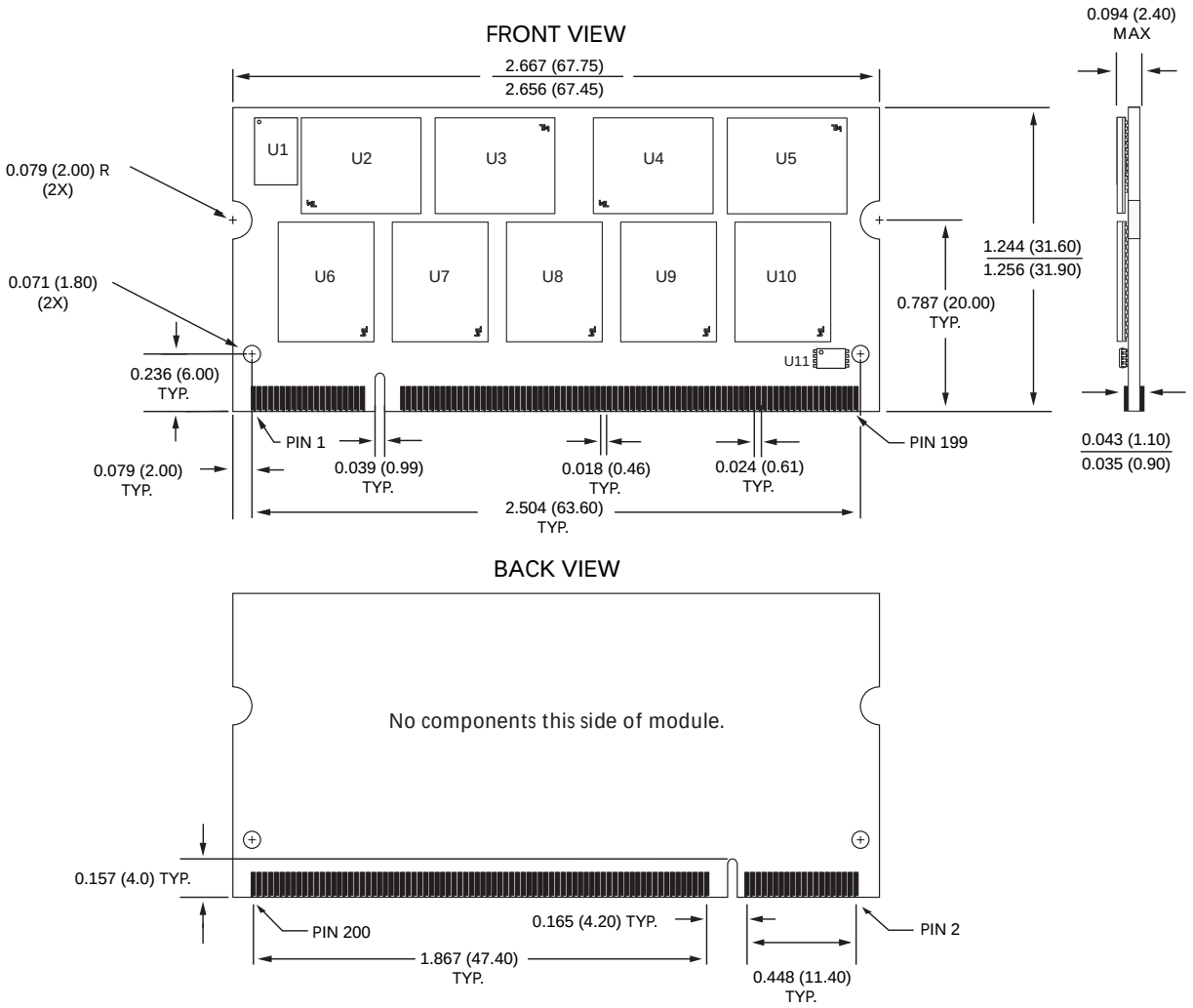
Byte	Description	Entry (Version)	MT9VDDF3272PH	MT9VDDF6472PH
33	Address and Command Hold Time, ^{t}IH (see note 4)	0.8ns (-335) 1.0ns (-262/-26A/-265)	80 A0	80 A0
34	Data/Data Mask Input Setup Time, ^{t}DS	0.45ns (-335 0.5ns (-262/-26A/-265)	45 50	45 50
35	Data/ Data Mask Input Hold Time, ^{t}DH	0.45ns (-335 0.5ns (-262/-26A/-265)	45 50	45 50
36-40	Reserved		00	00
41	Min Active Refresh Time ^{t}RC	60ns (-335/-262) 65ns (-26A/-265)	3C 41	3C 41
42	Minimum Auto Refresh to Active/Auto Refresh Command Period, ^{t}RFC	72ns (-335) 75ns (-262/-26A/-265)	48 4B	48 4B
43	SDRAM Device Max Cycle Time, $^{t}CK_{MAX}$	12ns (-335) 13ns (-262/-26A/-265)	30 34	30 34
44	SDRAM Device Max DQS–DQ Skew Time, ^{t}DQSQ	0.45ns (-335) 0.5ns (-262/-26A/-265)	2D 32	2D 32
45	SDRAM Device Max Read Data Hold Skew Factor	0.55ns (-335) 0.75ns (-262/-26A/-265)	55 75	55 75
46	Reserved		00	00
47	DIMM Height		01	01
48–61	Reserved		00	00
62	SPD Revision	Revision 1.0	10	10
63	Checksum For Bytes 0–62	-335 -262 -26A -265	33 D0 FD 2D	74 11 3E 6E
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C
65-71	Manufacturer's JEDEC ID Code (continued)		00	00
72	Manufacturing Location	01–12	01–0C	01–0C
73-90	Module Part Number (ASCII)		Variable Data	Variable Data
91	PCB Identification Code	1–9	01–09	01–09
92	Identification Code (Continued)	0	00	00
93	Year Of Manufacture in BCD		Variable Data	Variable Data
94	Week Of Manufacture in BCD		Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data
99-127	Manufacturer-Specific Data (RSVD)		–	–

Notes:
1. Device latencies used for SPD values.
2. Value for -262/-26A ^{t}CK set to 7ns (0x70) for optimum BIOS compatibility. Actual device spec. value is 7.5ns.
3. The value of ^{t}RAS used for -265 modules is calculated from ^{t}RC - ^{t}RP. Actual device spec value is 40ns.
4. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster minimum slew rate is met.
5. The value of ^{t}RP, ^{t}RCD, and ^{t}RAP for -335 modules indicated as 18ns to align with industry specifications; actual DDR SDRAM device specification is 15ns.

Package Dimensions

All dimensions are in inches (millimeters); $\frac{MAX}{MIN}$ or typical where noted.

Figure 11: 200-Pin SODIMM Dimensions



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