



144 pin SO-DIMM SDRAM Modules

HYS64V8200GDL
HYS64V16220GDL

64MB & 128 MB PC100 / PC133

- 144 Pin Eight Byte Small Outline Dual-In-Line Synchronous DRAM Modules for PC 100 and PC133 notebook applications
- one bank 8M x 64 and two bank 16M x 64 non-parity module organisation
- Performance:

		-7	-7.5	-8	
		PC133 2-2-2	PC133 3-3-3	PC100 2-2-2	Units
f _{CK}	Clock frequency (max.)	133	133	100	MHz
t _{AC}	Clock access time	5.4	5.4	6	ns

- Single +3.3V(± 0.3V) power supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTTL compatible
- Serial Presence Detect with E²PROM
- Uses 8M x 16 128Mbit SDRAM components
- 4096 refresh cycles every 64 ms
- Gold contact pad, JEDEC MO-190 outline dimensions
- This module family is fully compliant with the latest INTEL SO-DIMM layout and electrical specification
- All PC133 modules are fully backward compatible for PC100 applications.

These INFINEON modules are industry standard 144 pin 8-byte Synchronous DRAM (SDRAM) Small Outline Dual In-line Memory Modules (SO-DIMM) which are organised as 8Mx64 (64MByte) and 16x64 (128MByte) high speed memory arrays designed for use in non-parity applications. These SO-DIMMs use SDRAMs in TSOPII packages. Decoupling capacitors are mounted on the board.

The DIMMs use serial presence detects implemented via a serial E²PROM using the two pin I²C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All INFINEON 144-pin SO-DIMMs provide a high performance, flexible 8-byte interface in a 67,6 mm long footprint.

Product Spectrum:

Organisation	Partnumber	Speed	SDRAMs used	Row Addr.	Bank Select	Column Addr.	Refresh Period
8M x 64	HYS64V8200GDL-7	PC133-222	4 8Mx16	12	BA0, BA1	9	4k 64ms
	HYS64V8200GDL-7.5	PC133-333					
	HYS64V8200GDL-8	PC100-222					
16M x 64	HYS64V16220GDL-7	PC133-222	8 8Mx16				
	HYS64V16220GDL-7.5	PC133-333					
	HYS64V16220GDL-8	PC100-222					

Note: All partnumbers end with a place code (not shown), designating the die revision. Consult factory for current revision. Example: HYS64V16220GDL-8-C2, indicating Rev.C2 dies are used for SDRAM components.

Card Dimensions:

Organisation	Partnumber	PCB-Board Layout	L x H x T [mm]
8M x 64	HYS64V8200GDL	INTEL Rev. 1.0/1.2	67.60 x 25.40 x 3.80
16M x 64	HYS64V16220GDL	INTEL Rev. 1.0/1.2	67.60 x 31.75 x 3.80

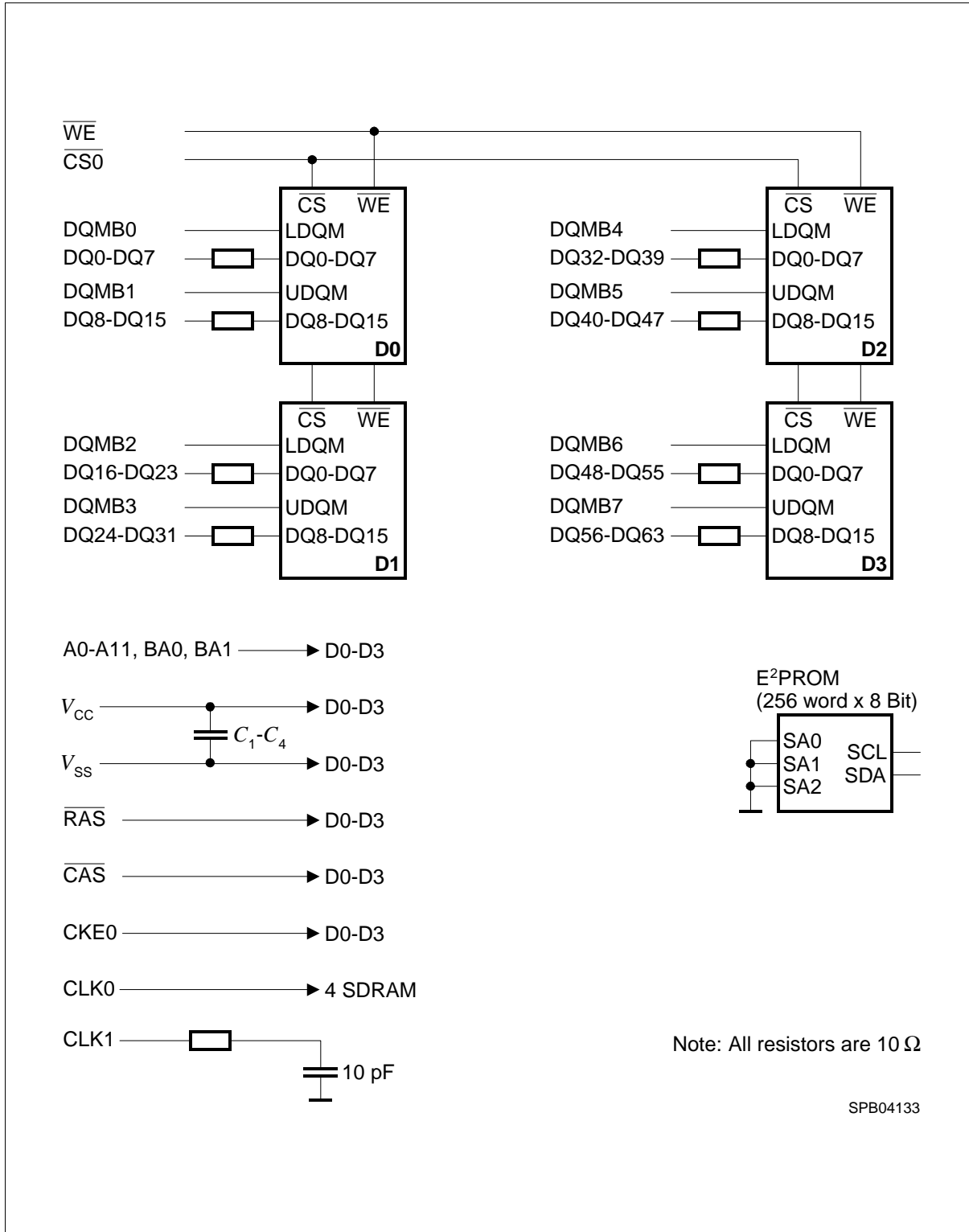
Pin Names

A0-A11	Address Inputs	DQMB0 - DQMB7	Data Mask
BA0,BA1	Bank Selects	$\overline{CS0}$, $\overline{CS1}$ *)	Chip Select
DQ0 - DQ63	Data Input/Output	Vcc	Power (+3.3 Volt)
\overline{RAS}	Row Address Strobe	Vss	Ground
\overline{CAS}	Column Address Strobe	SCL	Clock for Presence Detect
\overline{WE}	Read / Write Input	SDA	Serial Data Out for Presence Detect
CKE0, CKE1 *)	Clock Enable	N.C.	No Connection
CLK0, CLK1	Clock Input		

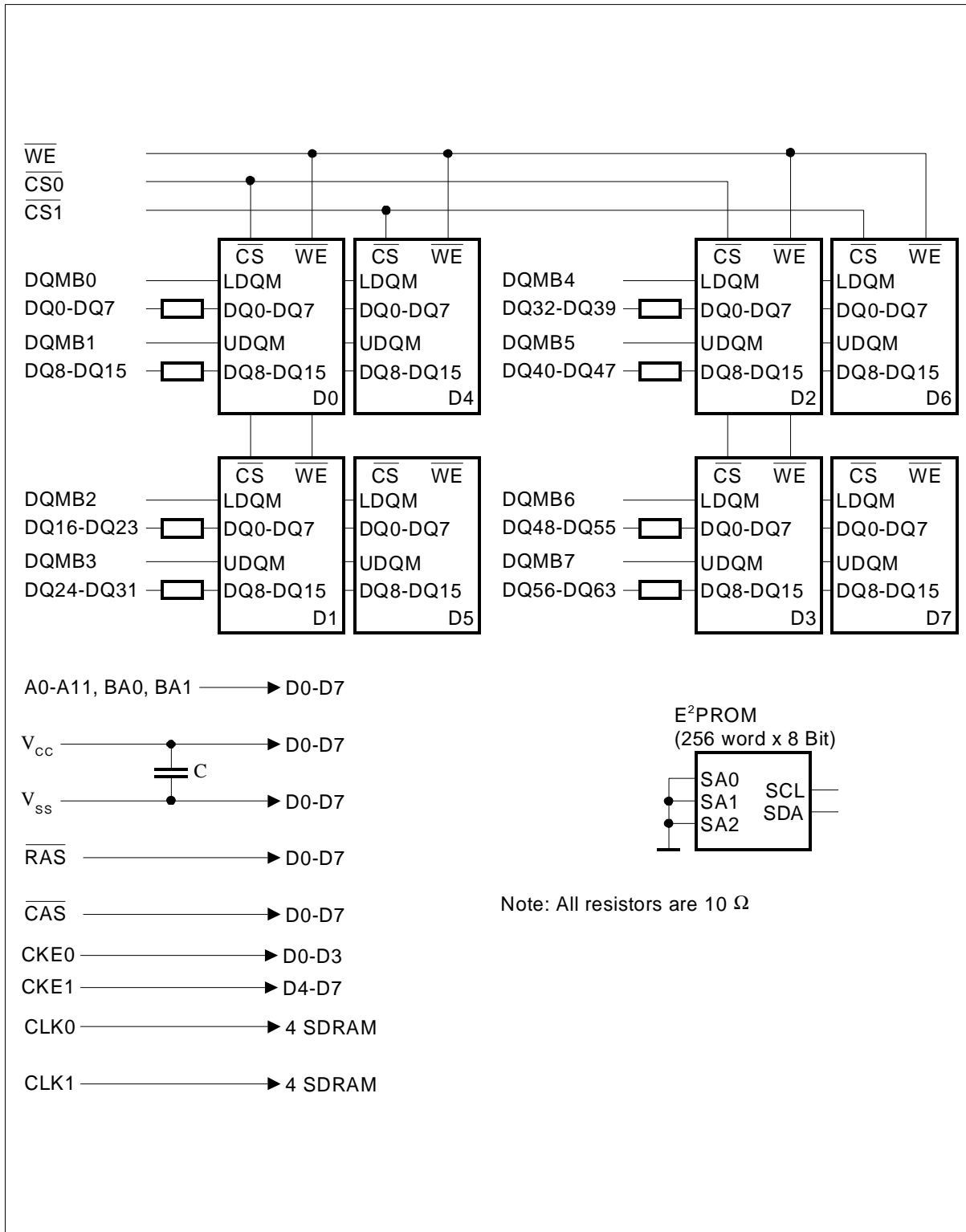
*) $\overline{CS1}$ and CKE1 on two bank modules only

Pin Configuration

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	VSS	2	VSS	73	NC	74	CLK1
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	Vcc	82	Vcc
11	VCC	12	Vcc	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	Vcc	28	Vcc	99	DQ23	100	DQ55
29	A0	30	A3	101	Vcc	102	Vcc
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	Vcc	114	Vcc
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	Vcc	46	Vcc	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	NC	58	NC	129	Vcc	130	Vcc
59	NC	60	NC	131	DQ28	132	DQ60
61	CLK0	62	CKE0	133	DQ29	134	DQ61
63	Vcc	64	Vcc	135	DQ30	136	DQ62
65	RAS	66	CAS	137	DQ31	138	DQ63
67	WE	68	CKE1	139	Vss	140	Vss
69	CS0	70	N.C.(A12)	141	SDA	142	SCL
71	CS1	72	N.C.(A13)	143	Vcc	144	Vcc



Block Diagram for one bank 8M x 64 SDRAM DIMM - Module



Block Diagram for two bank 16M x 64 SDRAM DIMM - Module

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	- 1.0	4.6	V
Power supply voltage on V_{DD}	V_{DD}	- 1.0	4.6	V
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation (per SDRAM component)	P_D	-	1	W
Data out current (short circuit)	I_{OS}	-	50	mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.
Functional operation should be restricted to recommended operation conditions.
Exposure to higher than recommended voltage for extended periods of time affect device reliability

DC Characteristics

$T_A = 0$ to 70 °C; $V_{SS} = 0$ V; $V_{DD} = 3.3$ V \pm 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	$V_{CC}+0.3$	V
Input low voltage	V_{IL}	- 0.5	0.8	V
Output high voltage ($I_{OUT} = - 4.0$ mA)	V_{OH}	2.4	-	V
Output low voltage ($I_{OUT} = 4.0$ mA)	V_{OL}	-	0.4	V
Input leakage current, any input (0 V < $V_{IN} < 3.6$ V, all other inputs = 0 V)	$I_{I(L)}$	- 20	20	μ A
Output leakage current (DQ is disabled, 0 V < $V_{OUT} < V_{DD}$)	$I_{O(L)}$	- 20	20	μ A

Capacitance

$T_A = 0$ to 70 °C; $V_{DD} = 3.3$ V \pm 0.3 V, $f = 1$ MHz

Parameter	Symbol	Limit Values		Unit
		8M x 64 max.	16M x 64 max.	
Input capacitance (A0 to A11, BA0, BA1)	C_{I1}	28	52	pF
Input capacitance (\overline{RAS} , \overline{CAS} , \overline{WE} , $\overline{CKE0}$)	C_{I2}	25	46	pF
Input Capacitance (CLK0, CLK1)	C_{I3}	35	35	pF
Input capacitance (CS0)	C_{I4}	25	30	pF
Input capacitance (DQMB0-DQMB7)	C_{I5}	10	15	pF
Input / Output capacitance (DQ0-DQ63)	C_{IO}	12	18	pF
Input Capacitance (SCL, SA0-2)	C_{sc}	8	8	pF
Input/Output Capacitance	C_{sd}	0	10	pF

Operating Currents per memory bank

($T_A = 0$ to 70°C , $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition		Symb.	-7/-7.5	-8		Note
OPERATING CURRENT						
trc=trcmin., tck=tckmin. Outputs open, Burst Length = 4, CL=3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access		ICC1	600	560	mA mA mA	1
PRECHARGE STANDBY CURRENT in Power Down Mode						
tck = min.		ICC2P	6	6	mA	1
$\overline{\text{CS}} = \text{VIH}(\text{min.}), \text{CKE} \leq \text{Vil}(\text{max})$		ICC2PS	4	4	mA	1
PRECHARGE STANDBY CURRENT in Non-Power Down Mode						
tck = min.		ICC2N	160	140	mA	1
$\overline{\text{CS}} = \text{VIH}(\text{min.}), \text{CKE} \geq \text{Vih}(\text{min})$		ICC2NS	20	20	mA	1
NO OPERATING CURRENT						
CKE \geq VIH(min.)		ICC3N	200	180	mA	1
tck = min., $\overline{\text{CS}} = \text{VIH}(\text{min})$, active state (max. 4 banks)		ICC3P	40	40	mA	1
CKE \leq VIL(max.)						
BURST OPERATING CURRENT						
tck = min., Read command cycling		ICC4	600	560	mA	1,2
AUTO REFRESH CURRENT						
tck = min., Auto Refresh command cycling		ICC5	720	680	mA	1
SELF REFRESH CURRENT						
Self Refresh Mode, CKE=0.2V		ICC6	3.2	3.2	mA	1

Notes:

1. These parameters depend on the cycle rate. These values are measured at 133 MHz for -7/ -7.5 and 100 MHz for -8 modules. Input signals are changed once during tck, excepts for ICC6 and for standby currents when tck=infinity.
2. These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the data-out current is excluded.

AC Characteristics 1)2)
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}; V_{SS} = 0 \text{ V}; V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 1 \text{ ns}$

Parameter	Symbol	Limit Values						Unit
		-7 PC133-222		-7.5 PC133-333		-8 PC100-222		
		min.	max.	min.	max.	min.	max.	

Clock and Access Time

Clock Cycle Time	t_{CK}	$\overline{\text{CAS}}$ Latency = 3	7.5	–	7.5	–	10	–	ns
		$\overline{\text{CAS}}$ Latency = 2	7.5	–	10	–	10	–	ns
Clock Frequency	t_{CK}	$\overline{\text{CAS}}$ Latency = 3	–	133	–	133	–	100	MHz
		$\overline{\text{CAS}}$ Latency = 2	–	133	–	100	–	100	MHz
Access Time from Clock	t_{AC}	$\overline{\text{CAS}}$ Latency = 3	–	5.4	–	5.4	–	6	ns
		$\overline{\text{CAS}}$ Latency = 2	–	5.4	–	6	–	6	ns
Clock High Pulse Width	t_{CH}	2.5	–	2.5	–	3	–	ns	
Clock Low Pulse Width	t_{CL}	2.5	–	2.5	–	3	–	ns	
Transition time	t_T	0.3	1.2	0.3	1.2	0.5	2	ns	

Setup and Hold Parameters

Input Setup Time	t_{IS}	1.5	–	1.5	–	2	–	ns	4
Input Hold Time	t_{IH}	0.8	–	0.8	–	1	–	ns	4
Power Down Mode Entry time	t_{SB}	–	1	–	1	–	1	CLK	4
Power Down Mode Exit Setup Time	t_{PDE}	1	–	1	–	1	–	CLK	4
Mode Register Set-up time	t_{RSC}	2	–	2	–	2	–	CLK	

Common Parameters

Row to Column Delay Time	t_{RCD}	15	–	20	–	20	–	ns	5
Row Precharge Time	t_{RP}	15	–	20	–	20	–	ns	5
Row Active Time	t_{RAS}	42	100k	45	100k	50	100k	ns	5
Row Cycle Time	t_{RC}	60	–	67	–	70	–	ns	5
Activate(a) to Activate(b) Command period	t_{RRD}	14	–	15	–	16	–	ns	5
$\overline{\text{CAS}}$ (a) to $\overline{\text{CAS}}$ (b) Command period	t_{CCD}	1	–	1	–	1	–	CLK	

Parameter	Symbol	Limit Values						Unit
		-7 PC133-222		-7.5 PC133-333		-8 PC100-222		
		min.	max.	min.	max.	min.	max.	

Refresh Cycle

Refresh Period (4096 cycles)	t_{REF}	–	64	–	64	–	64	ms	
Self Refresh Exit Time	t_{SREX}	1	–	1	–	1	–	CLK	6

Read Cycle

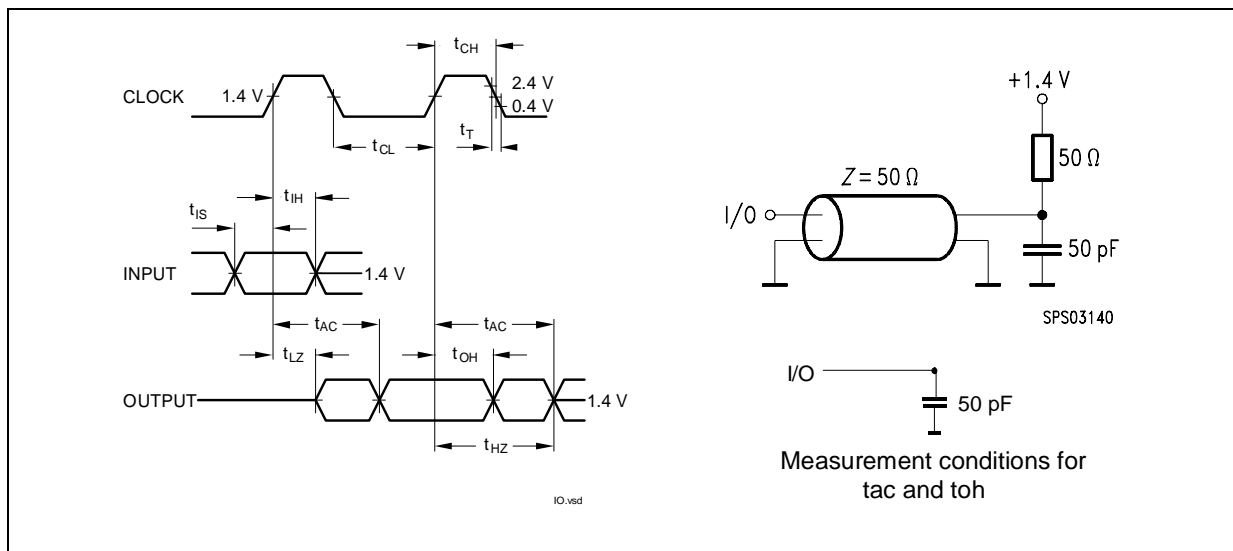
Data Out Hold Time	t_{OH}	3	–	3	–	3	–	ns	
Data Out to Low Impedance Time	t_{LZ}	0	–	0	–	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	7	3	7	3	8	ns	7
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	–	2	CLK	

Write Cycle

Data Input to Precharge (write recovery)	t_{WR}	2	–	2	–	2	–	CLK	
DQM Write Mask Latency	t_{DQW}	0	–	0	–	0	–	CLK	

Notes:

1. All AC characteristics shown are for SDRAM components.
 An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
2. AC timing tests have $V_{il} = 0.4\text{ V}$ and $V_{ih} = 2.4\text{ V}$ with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{il} . All AC measurements assume $t_T=1\text{ ns}$ with the AC output load circuit shown. Specified t_{ac} and t_{oh} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V



3. If clock rising time is longer than 1ns, a time ($t_T - 0.5$) ns has to be added to this parameter.
4. If t_T is longer than 1ns, a time ($t_T - 1$) ns has to be added to this parameter.
5. Any time that the refresh Period has been exceeded, a minimum of two Auto (CRB) Refresh commands must be given to “wake-up” the device.
6. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
7. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

Serial Presence Detects

A serial presence detect storage device - E²PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E²PROM device during module production using a serial presence detect protocol (I²C synchronous 2-wire bus)

SPD-Table:

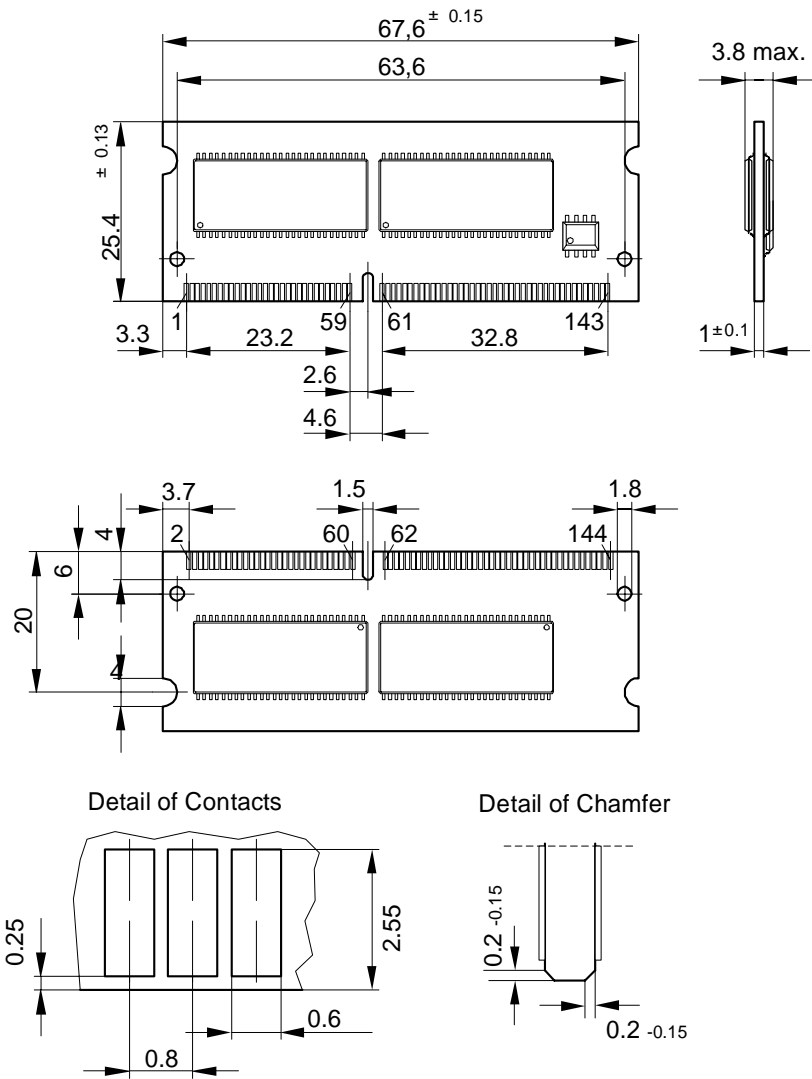
Byte#	Description	SPD Entry Value	HEX					
			8M x 64			16M x 64		
			-7	-7.5	-8	-7	-7.5	-8
0	Number of SPD bytes	128	80					
1	Total bytes in Serial PD	256	08					
2	Memory Type	SDRAM	04					
3	Number of Row Addresses	12	0C					
4	Number of Column Addresses	9	09					
5	Number of DIMM Banks	1 / 2	01			02		
6	Module Data Width	64	40					
7	Module Data Width (cont'd)	0	00					
8	Module Interface Levels	LVTTTL	01					
9	SDRAM Cycle Time at CL=3	7.5 / 10.0 ns	75	75	A0	75	75	A0
10	SDRAM Access time from Clock at CL=3	5.4 / 6.0 ns	54	54	60	54	54	60
11	Dimm Config (Error Det/Corr.)	none	00					
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80					
13	SDRAM width, Primary		10					
14	Error Checking SDRAM data width	n/a	00					
15	Minimum clock delay for back-to-back random column address	t _{ccd} = 1 CLK	01					
16	Burst Length supported	1, 2, 4 & 8	0F					
17	Number of SDRAM banks	2	04					
18	Supported CAS Latencies	2, & 3	06					
19	CS Latencies	CS latency = 0	01					
20	WE Latencies	Write latency = 0	01					
21	SDRAM DIMM module attributes	non buffered/non reg.	00					
22	SDRAM Device Attributes :General	V _{cc} tol +/- 10%	0E					
23	SDRAM Cycle Time at CL = 2	7.5 / 10.0 ns	75	A0	A0	75	A0	A0
24	SDRAM Access Time from Clock at CL=2	5.4 / 6.0 ns	54	60	60	54	60	60
25	SDRAM Cycle Time at CL = 1	not supported	00	FF	FF	00	FF	FF
26	SDRAM Access Time from Clock at CL=1	not supported	00	FF	FF	00	FF	FF
27	Minimum Row Precharge Time	15/ 20 ns	0F	14	14	0F	14	14

SPD-Table (cont'd):

Byte#	Description	SPD Entry Value	Hex					
			8Mx64			16Mx64		
			-7	-7.5	-8	-7	-7.5	-8
28	Minimum Row Active to Row Active delay	14 / 15 / 16 ns	0E	0F	10	0E	0F	10
29	Minimum RAS to CAS delay	15 / 20 ns	0F	14	14	0F	14	14
30	Minimum Ras pulse width	42 / 45 ns	2A	2D	2D	2A	2D	2D
31	Module Bank Density (per bank)	64MB	10					
32	SDRAM input setup time	1.5 / 2 ns	15	15	20	15	15	20
33	SDRAM input hold time	0.8 / 1 ns	08	08	10	08	08	10
34	SDRAM data input setup time	1.5 / 2 ns	15	15	20	15	15	20
35	SDRAM data input hold time	0.8 / 1 ns	08	08	10	08	08	10
36-61	Superset information		FF					
62	SPD Revision	Revision 1.2	12					
63	Checksum for bytes 0 - 62		E1	0A	68	E2	0B	69
64-125	Manufactures's information (optional)							
126	Frequency Specification	PC100	64					
127	Details		87			C7		
128+	Unused storage locations		FF					

Package Outlines

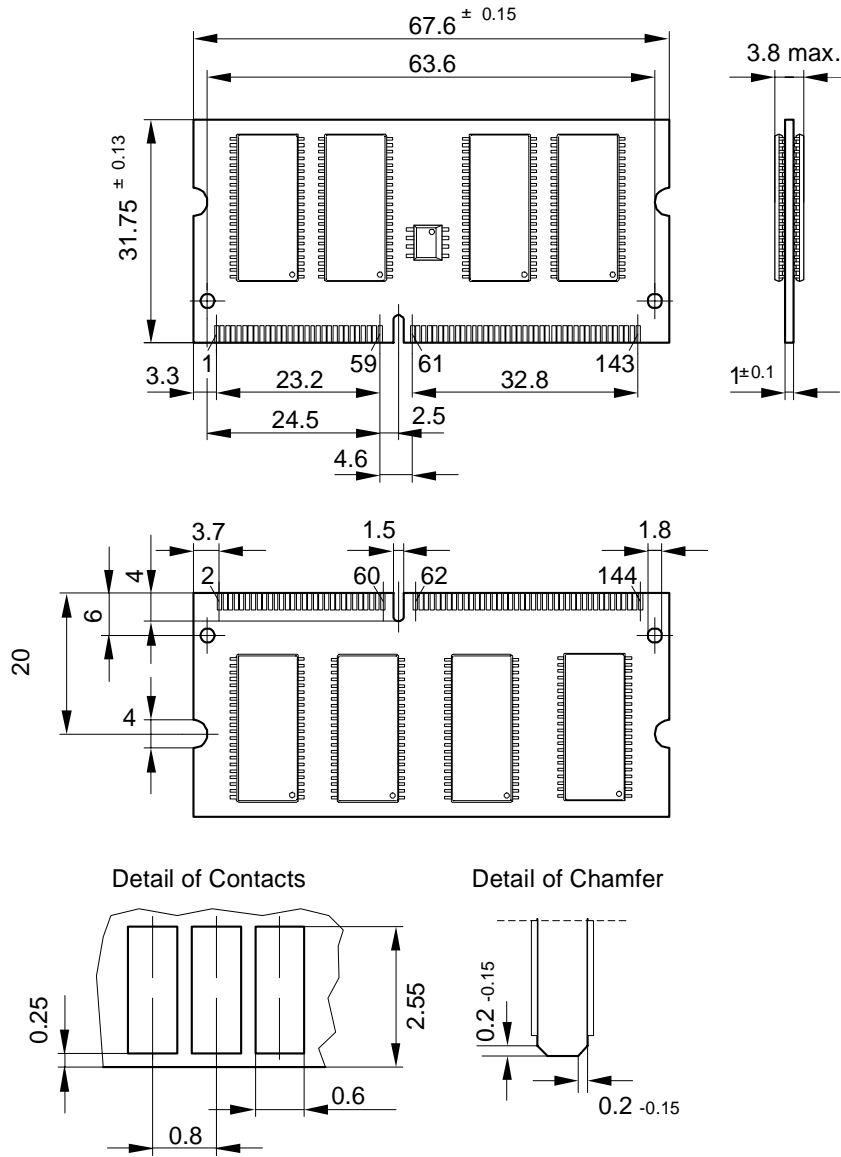
64 MByte SO-DIMM Module package (JEDEC MO-190)
HYS64V8200GDL
(144 pin, dual read-out, single in-line memory module)



L-DIM-144-10

Note: All tolerances according to JEDEC standard

128 MByte SO-DIMM Module package
HYS64V16220GDL
(144 pin, dual read-out, single in-line memory module)



L-DIM-144-9

Note: All tolerances according to JEDEC standard

Update Information:

5.6.99	First and preliminary edition
29.9.99	Checksum added
3.12.99	PC133 timing changed according to INTELs PC133 specification
17.1.2000	HYS64V8200GDL-7.5/-8 added
10.5.2000	HYS64V162221GDL-7.5/-8 version with reduced height of 1060 mil = 29,92 mm (L-DIM-144-11) added
19.7.2000	CKE1 in two bank block diagram added
8.8.2000	128Mbyte version HYS64V16221GDL removed (no plans for production)
25.9.2000	8Mx64 module height on page 2 corrected
7.03.2001	-7 speed sort added
5.09.2001	SCR: Table for Absolute Maximum Ratings added