

# HYS64D32020GDL-[5/6/7/8]-B HYS64D1600xGDL-[6/7/8]-B

200-Pin Small Outline Dual-In-Line Memory Modules  
SO-DIMM  
DDR SDRAM

Memory Products



N e v e r   s t o p   t h i n k i n g .

**Edition 2003-08**

**Published by Infineon Technologies AG,  
St.-Martin-Strasse 53,  
81669 München, Germany**

**© Infineon Technologies AG 2003.  
All Rights Reserved.**

**Attention please!**

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

**Information**

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

**Warnings**

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

# HYS64D32020GDL-[5/6/7/8]-B HYS64D1600xGDL-[6/7/8]-B

200-Pin Small Outline Dual-In-Line Memory Modules  
SO-DIMM  
DDR SDRAM

Memory Products



N e v e r   s t o p   t h i n k i n g .

<b>Revision History:</b>	<b>V1.2</b>	<b>2003-08</b>
Previous Version:	V1.1	2003-03

Page	Subjects (major changes since last revision)
all	New data sheet template
<a href="#">6,7,26,16</a>	Added Part number HYS64D32020GDL-5-B including SPD and $I_{DD}$
<a href="#">7</a>	Updated Complinance Code
<a href="#">18</a>	Added DDR400B AC characteristics added
<a href="#">16,17</a>	Corrected $I_{DD}$ 256MB for speed sort -6 & -7
<a href="#">29</a>	Updated Package Outlines
<a href="#">18</a>	Removed tbd from Table 11 for DDR400B tIPW & tDIPW

**We Listen to Your Comments**

Any information within this document that you feel is wrong, unclear or missing at all?  
Your feedback will help us to continuously improve the quality of this document.  
Please send your proposal (including a reference to this document) to:

[techdoc.mp@infineon.com](mailto:techdoc.mp@infineon.com)



## Table of Contents

<b>1</b>	<b>Overview</b> .....	<b>6</b>
1.1	Features .....	6
1.2	Description .....	6
<b>2</b>	<b>Pin Configuration</b> .....	<b>8</b>
<b>3</b>	<b>Electrical Characteristics</b> .....	<b>13</b>
3.1	Operating Conditions .....	13
3.2	Current Specification and Conditions .....	15
<b>4</b>	<b>AC Characteristics</b> .....	<b>18</b>
<b>5</b>	<b>SPD Contents</b> .....	<b>23</b>
<b>6</b>	<b>Package Outlines</b> .....	<b>29</b>

## 1 Overview

### 1.1 Features

- Non-parity 200-Pin Small Outline Dual-In-Line Memory Modules
- One rank 16M × 64 and two bank 32M × 64 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM)
- Single +2.5 V (± 0.2 V) power supply
- Built with 256 Mbit DDR SDRAMs organised as × 16 in P-TSOPII-66-1 packages
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL\_2 compatible
- Serial Presence Detect with E<sup>2</sup>PROM
- Jedec standard form factor: 67.60 mm × 31.75 mm × 3.00 / 3.80 mm
- Jedec standard reference layout Raw Cards A and C
- DDR400 speed grade supported
- Gold plated contacts

**Table 1 Performance**

Part Number Speed Code		-5	-6	-7	-8	Unit
Speed Grade	Component	DDR400B	DDR333B	DDR266A	DDR200	—
	Module	PC3200-3033	PC2700-2533	PC2100-2033	PC1600-2022	—
max. Clock Frequency	@CL3	$f_{CK3}$	200	166	—	MHz
	@CL2.5	$f_{CK2.5}$	166	166	143	MHz
	@CL2	$f_{CK2}$	133	133	133	MHz

### 1.2 Description

The HYS64D32020GDL-[5/6/7/8]-B and HYS64D1600xGDL-[6/7/8]-B are industry standard 200-Pin Small Outline Dual-In-Line Memory Modules (SO-DIMMs) organized as 32M × 64 and 16M × 64. The memory array is designed with Double Data Rate Synchronous DRAMs (DDR SDRAM). A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E<sup>2</sup>PROM device using the 2-pin I<sup>2</sup>C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

**Table 2 Ordering Information**

Type	Compliance Code	Description	SDRAM Technology
<b>PC3200 (CL=3)</b>			
HYS64D32020GDL-5-B	PC3200S-3033-0-A1	two ranks 256 MB SO-DIMM	256 Mbit (× 16)
<b>PC2700 (CL=2.5)</b>			
HYS64D16000GDL-6-B	PC2700S-2533-0-C1	one rank 128 MB SO-DIMM	256 MBit (× 16)
HYS64D16001GDL-6-B	PC2700S-2533-0-C1	one rank 128 MB SO-DIMM	256 MBit (× 16)
HYS64D32020GDL-6-B	PC2700S-2533-0-A1	two ranks 256 MB SO-DIMM	256 MBit (× 16)
<b>PC2100 (CL=2)</b>			
HYS64D16000GDL-7-B	PC2100S-2033-0-C1	one rank 128 MB SO-DIMM	256 MBit (× 16)
HYS64D16001GDL-7-B	PC2100S-2033-0-C1	one rank 128 MB SO-DIMM	256 MBit (× 16)
HYS64D32020GDL-7-B	PC2100S-2033-0-A1	two ranks 256 MB SO-DIMM	256 MBit (× 16)
<b>PC1600 (CL=2)</b>			
HYS64D16000GDL-8-B	PC1600S-2022-0-C1	one rank 128 MB SO-DIMM	256 MBit (× 16)
HYS64D32020GDL-8-B	PC1600S-2022-0-A1	two ranks 256 MB SO-DIMM	256 MBit (× 16)

**Notes**

1. All part numbers end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS64D32020GDL-6-B, indicating rev. B dies are used for SDRAM components.
2. The Compliance Code is printed on the module labels describing the speed sort (for example "PC2700"), the latencies and SPD code definition (for example "2033-0" means CAS latency of 2.0 clocks, RCD<sup>1)</sup> latency of 3 clocks, Row Precharge latency of 3 clocks, and JEDEC SPD code definition version 0), and the Raw Card used for this module.

1) RCD: Row-Column-Delay

## 2 Pin Configuration

**Table 3 Pin Definitions and Functions**

Symbol	Type <sup>1)</sup>	Function
A0 - A12	I	Address Inputs
BA0, BA1	I	Bank Address
DQ0 - DQ63	I/O	Data Input/Output
$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	I	Command Input
CKE0 - CKE1	I	Clock Enable
DQS0 - DQS7	I/O	SDRAM Data Strobe
CK0 - CK1,	I	SDRAM Clock (true signal)
$\overline{\text{CK0}}$ - $\overline{\text{CK1}}$	I	SDRAM Clock (complementary signal)
DM0 - DM8	I	Data Mask
$\overline{\text{S0}}$ , $\overline{\text{S1}}$ <sup>2)</sup>	I	Chip Select
$V_{\text{DD}}$	PWR	Power (+ 2.5 V)
$V_{\text{SS}}$	GND	Ground
$V_{\text{DDQ}}$	PWR	I/O Driver power supply
$V_{\text{DDID}}$	PWR	VDD Identification flag
$V_{\text{REF}}$	AI	I/O reference supply
$V_{\text{DDSPD}}$	PWR	Serial EEPROM power supply
SCL	I	Serial bus clock
SDA	I/O	Serial bus data line
SA0 - SA2	I	slave address select
NC	NC	Not Connected
NU	NU	Not Usable, reserved for future use

1) I: Input; O: Output; I/O: bidirectional In-/Output; AI: Analog Input; PWR: Power Supply; GND: Signal Ground; NC: Not Connected; NU: Not Usable

2) CKE1 and  $\overline{\text{S1}}$  are used on two bank modules only

**Table 4 Address Format**

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
128MB	16M × 64	1	16M × 16	4	13/2/9	8K	64 ms	7.8 μs
256MB	32M × 64	2	16M × 16	8	13/2/9	8K	64 ms	7.8 μs



Pin Configuration

Table 5 Pin Configuration

Front side		Back side		Front side		Back side		Front side		Back side	
Pin #	Symbol	Pin #	Symbol	Pin #	Symbol	Pin #	Symbol	Pin #	Symbol	Pin #	Symbol
1	V <sub>REF</sub>	2	V <sub>REF</sub>	65	DQ26	66	DQ30	133	DQS4	134	DM4
3	V <sub>SS</sub>	4	V <sub>SS</sub>	67	DQ27	68	DQ31	135	DQ34	136	DQ38
5	DQ0	6	DQ4	69	V <sub>DD</sub>	70	V <sub>DD</sub>	137	V <sub>SS</sub>	138	V <sub>SS</sub>
7	DQ1	8	DQ5	71	(CB0)	72	(CB4)	139	DQ35	140	DQ39
9	V <sub>DD</sub>	10	V <sub>DD</sub>	73	(CB1)	74	(CB5)	141	DQ40	142	DQ44
11	DQS0	12	DM0	75	V <sub>SS</sub>	76	V <sub>SS</sub>	143	V <sub>DD</sub>	144	V <sub>DD</sub>
13	DQ2	14	DQ6	77	(DQS8)	78	(DM8)	145	DQ41	146	DQ45
15	V <sub>SS</sub>	16	V <sub>SS</sub>	79	(CB2)	80	(CB6)	147	DQS5	148	DM5
17	DQ3	18	DQ7	81	V <sub>DD</sub>	82	V <sub>DD</sub>	149	V <sub>SS</sub>	150	V <sub>SS</sub>
19	DQ8	20	DQ12	83	(CB3)	84	(CB7)	151	DQ42	152	DQ46
21	V <sub>DD</sub>	22	V <sub>DD</sub>	85	DU	86	DU	153	DQ43	154	DQ47
23	DQ9	24	DQ13	87	V <sub>SS</sub>	88	V <sub>SS</sub>	155	V <sub>DD</sub>	156	V <sub>DD</sub>
25	DQS1	26	DM1	89	(CK2)	90	V <sub>SS</sub>	157	V <sub>DD</sub>	158	CK1
27	V <sub>SS</sub>	28	V <sub>SS</sub>	91	(CK2)	92	V <sub>DD</sub>	159	V <sub>SS</sub>	160	CK1
29	DQ10	30	DQ14	93	V <sub>DD</sub>	94	V <sub>DD</sub>	161	V <sub>SS</sub>	162	V <sub>SS</sub>
31	DQ11	32	DQ15	95	CKE1	96	CKE0	163	DQ48	164	DQ52
33	V <sub>DD</sub>	34	V <sub>DD</sub>	97	DU	98	DU	165	DQ49	166	DQ53
35	CK0	36	V <sub>DD</sub>	99	A12	100	A11	167	V <sub>DD</sub>	168	V <sub>DD</sub>
37	CK0	38	V <sub>SS</sub>	101	A9	102	A8	169	DQS6	170	DM6
39	V <sub>SS</sub>	40	V <sub>SS</sub>	103	V <sub>SS</sub>	104	V <sub>SS</sub>	171	DQ50	172	DQ54
<b>Key</b>				105	A7	106	A6	173	V <sub>SS</sub>	174	V <sub>SS</sub>
				107	A5	108	A4	175	DQ51	176	DQ55
41	DQ16	42	DQ20	109	A3	110	A2	177	DQ56	178	DQ60
43	DQ17	44	DQ21	111	A1	112	A0	179	V <sub>DD</sub>	180	V <sub>DD</sub>
45	V <sub>DD</sub>	46	V <sub>DD</sub>	113	V <sub>DD</sub>	114	V <sub>DD</sub>	181	DQ57	182	DQ61
47	DQS2	48	DM2	115	A10/AP	116	BA1	183	DQS7	184	DM7
49	DQ18	50	DQ22	117	BA0	118	RA <sub>S</sub>	185	V <sub>SS</sub>	186	V <sub>SS</sub>
51	V <sub>SS</sub>	52	V <sub>SS</sub>	119	WE	120	CAS	187	DQ58	188	DQ62
53	DQ19	54	DQ23	121	S0	122	S1	189	DQ59	190	DQ63
55	DQ24	56	DQ28	123	DU	124	DU	191	V <sub>DD</sub>	192	V <sub>DD</sub>
57	V <sub>DD</sub>	58	V <sub>DD</sub>	125	V <sub>SS</sub>	126	V <sub>SS</sub>	193	SDA	194	SA0
59	DQ25	60	DQ29	127	DQ32	128	DQ36	195	SCL	196	SA1
61	DQS3	62	DM3	129	DQ33	130	DQ37	197	V <sub>DDSPD</sub>	198	SA2
63	V <sub>SS</sub>	64	V <sub>SS</sub>	131	V <sub>DD</sub>	132	V <sub>DD</sub>	199	V <sub>DDID</sub>	200	DU

Pin Configuration

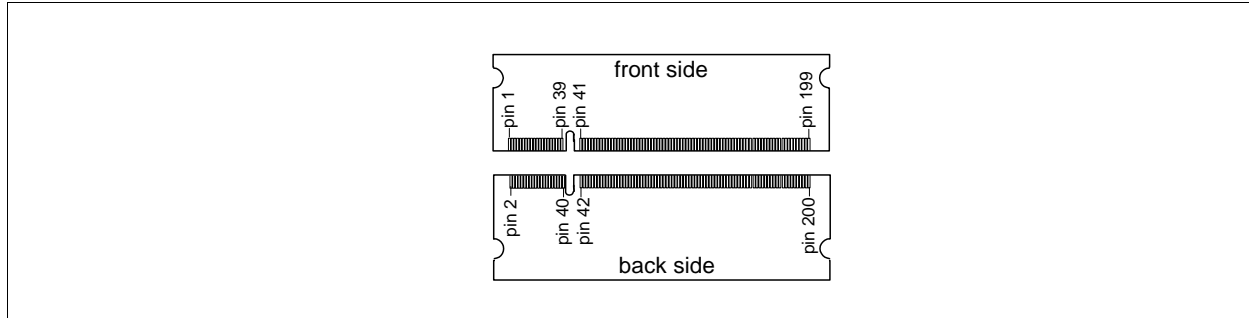


Figure 1 Pin Configuration

Pin Configuration

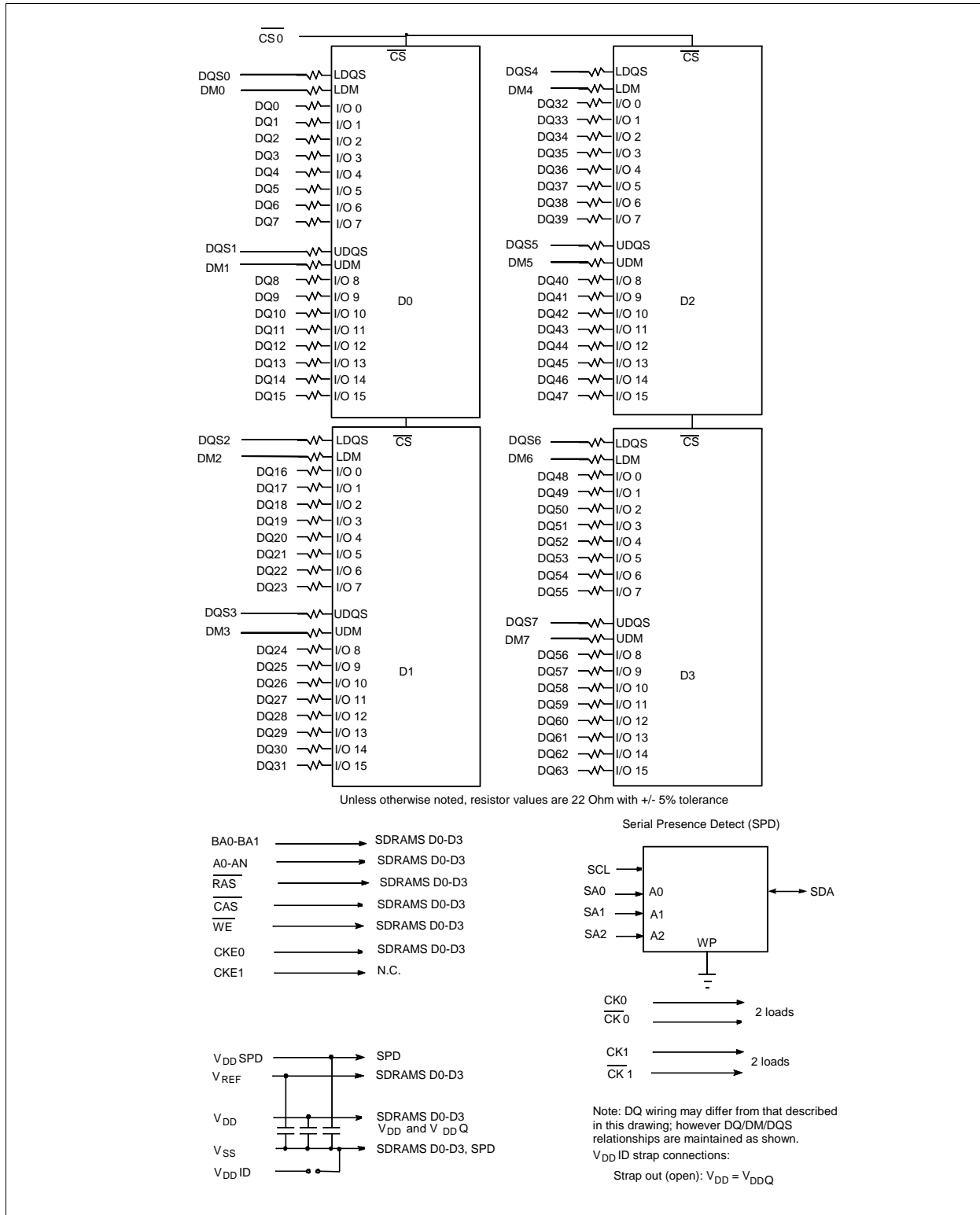


Figure 2 Block Diagram - One Rank 16M x 64 DDR SDRAM SO-DIMM HYS64D1600xGDL-[6/7/8]-B

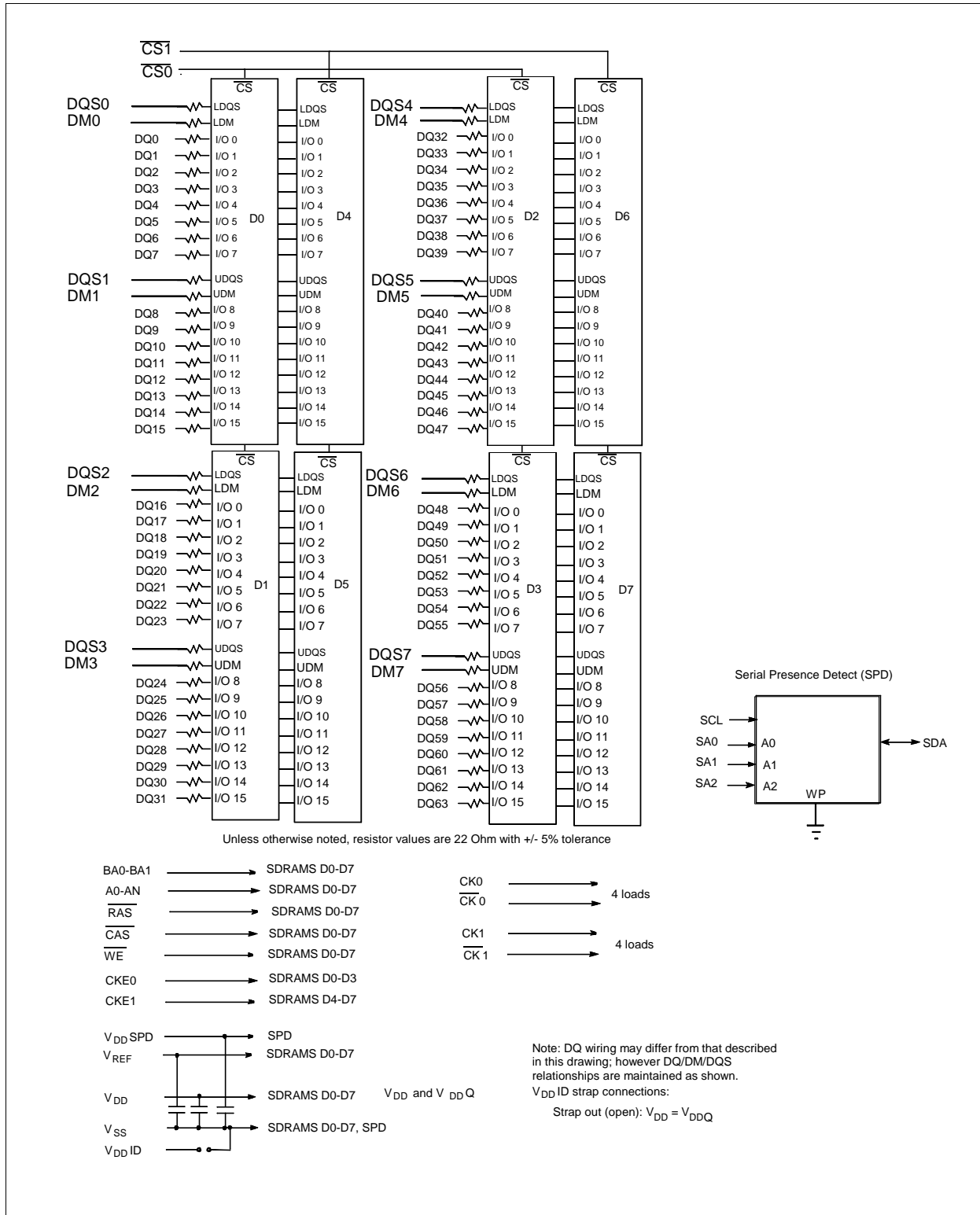


Figure 3 Block Diagram - Two Rank 32M x 64 DDR SDRAM SO-DIMM HYS64D32020GDL-[5/6/7/8]-B

### 3 Electrical Characteristics

#### 3.1 Operating Conditions

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5	-	$V_{DDQ} + 0.5$	V	-
Voltage on inputs relative to $V_{SS}$	$V_{IN}$	-1	-	+3.6	V	-
Voltage on $V_{DD}$ supply relative to $V_{SS}$	$V_{DD}$	-1	-	+3.6	V	-
Voltage on $V_{DDQ}$ supply relative to $V_{SS}$	$V_{DDQ}$	-1	-	+3.6	V	-
Operating temperature (ambient)	$T_A$	0	-	+70	°C	-
Storage temperature (plastic)	$T_{STG}$	-55	-	+150	°C	-
Power dissipation (per SDRAM component)	$P_D$	-	1	-	W	-
Short circuit output current	$I_{OUT}$	-	50	-	mA	-

**Attention:** Permanent damage to the device may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.

Table 7 Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition <sup>1)</sup>
		Min.	Typ.	Max.		
Device Supply Voltage	$V_{DD}$	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz
Device Supply Voltage	$V_{DD}$	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz <sup>2)</sup>
Output Supply Voltage	$V_{DDQ}$	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz <sup>3)</sup>
Output Supply Voltage	$V_{DDQ}$	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz <sup>2)3)</sup>
EEPROM supply voltage	$V_{DDSPD}$	2.3	2.5	3.6	V	—
Supply Voltage, I/O Supply Voltage	$V_{SS}, V_{SSQ}$	0		0	V	—
Input Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	4)
I/O Termination Voltage (System)	$V_{TT}$	$V_{REF} - 0.04$		$V_{REF} + 0.04$	V	5)
Input High (Logic1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.15$		$V_{DDQ} + 0.3$	V	8)
Input Low (Logic0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.15$	V	8)
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	-0.3		$V_{DDQ} + 0.3$	V	8)
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		$V_{DDQ} + 0.6$	V	8)6)
VI-Matching Pull-up Current to Pull-down Current	$V_{I\text{Ratio}}$	0.71		1.4	—	7)

**Electrical Characteristics**
**Table 7 Electrical Characteristics and DC Operating Conditions (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition <sup>1)</sup>
		Min.	Typ.	Max.		
Input Leakage Current	$I_I$	-2		2	$\mu\text{A}$	Any input $0\text{ V} \leq V_{IN} \leq V_{DD}$ ; All other pins not under test = 0 V <sup>8)9)</sup>
Output Leakage Current	$I_{OZ}$	-5		5	$\mu\text{A}$	DQs are disabled; $0\text{ V} \leq V_{OUT} \leq V_{DDQ}$ <sup>8)</sup>
Output High Current, Normal Strength Driver	$I_{OH}$	—		-16.2	mA	$V_{OUT} = 1.95\text{ V}$ <sup>8)</sup>
Output Low Current, Normal Strength Driver	$I_{OL}$	16.2		—	mA	$V_{OUT} = 0.35\text{ V}$ <sup>8)</sup>

1)  $0\text{ }^\circ\text{C} \leq T_A \leq 70\text{ }^\circ\text{C}$

2) DDR400 conditions apply for all clock frequencies above 166 MHz

3) Under all conditions,  $V_{DDQ}$  must be less than or equal to  $V_{DD}$ .

4) Peak to peak AC noise on  $V_{REF}$  may not exceed  $\pm 2\% V_{REF(DC)}$ .  $V_{REF}$  is also expected to track noise variations in  $V_{DDQ}$ .

5)  $V_{TT}$  is not applied directly to the device.  $V_{TT}$  is a system supply for signal termination resistors, is expected to be set equal to  $V_{REF}$ , and must track variations in the DC level of  $V_{REF}$ .

6)  $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on  $\overline{\text{CK}}$ .

7) The ration of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

8) Inputs are not recognized as valid until  $V_{REF}$  stabilizes.

9) Values are shown per DDR SDRAM component

### 3.2 Current Specification and Conditions

**Table 8**  $I_{DD}$  Conditions

Parameter	Symbol
<b>Operating Current 0</b> one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	$I_{DD0}$
<b>Operating Current 1</b> one bank; active/read/precharge; Burst Length = 4; see component data sheet.	$I_{DD1}$
<b>Precharge Power-Down Standby Current</b> all banks idle; power-down mode; $CKE \leq V_{IL,MAX}$	$I_{DD2P}$
<b>Precharge Floating Standby Current</b> $\overline{CS} \geq V_{IH,MIN}$ , all banks idle; $CKE \geq V_{IH,MIN}$ ; address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	$I_{DD2F}$
<b>Precharge Quiet Standby Current</b> $\overline{CS} \geq V_{IH,MIN}$ , all banks idle; $CKE \geq V_{IH,MIN}$ ; $V_{IN} = V_{REF}$ for DQ, DQS and DM; address and other control inputs stable at $\geq V_{IH,MIN}$ or $\leq V_{IL,MAX}$ .	$I_{DD2Q}$
<b>Active Power-Down Standby Current</b> one bank active; power-down mode; $CKE \leq V_{IL,MAX}$ ; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	$I_{DD3P}$
<b>Active Standby Current</b> one bank active; $\overline{CS} \geq V_{IH,MIN}$ ; $CKE \geq V_{IH,MIN}$ ; $t_{RC} = t_{RAS,MAX}$ ; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	$I_{DD3N}$
<b>Operating Current Read</b> one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; $I_{OUT} = 0$ mA	$I_{DD4R}$
<b>Operating Current Write</b> one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	$I_{DD4W}$
<b>Auto-Refresh Current</b> $t_{RC} = t_{RFCMIN}$ ; burst refresh	$I_{DD5}$
<b>Self-Refresh Current</b> $CKE \leq 0.2$ V; external clock on	$I_{DD6}$
<b>Operating Current 7</b> four bank interleaving with Burst Length = 4; see component data sheet.	$I_{DD7}$

Table 9 I<sub>DD</sub> Specification

Part Number & Organization	HYS64D16000GDL-6-B HYS64D16001GDL-6-B		HYS64D32020GDL-6-B		HYS64D32020GDL-5-B		Unit	Note <sup>1)2)</sup>
	128MB		256MB		256MB			
	× 64		× 64		× 64			
	1 Rank		2 Ranks		2 Ranks			
	-6		-6		-5			
Symbol	typ.	max.	typ.	max.	typ.	max.		
I <sub>DD0</sub>	352	460	604	740	640	776	mA	3)
I <sub>DD1</sub>	416	500	668	780	700	836	mA	3)4)
I <sub>DD2P</sub>	24	36	48	72	48	72	mA	5)
I <sub>DD2F</sub>	180	220	360	440	368	448	mA	5)
I <sub>DD2Q</sub>	99	112	198	224	192	272	mA	5)
I <sub>DD3P</sub>	72	84	144	168	136	192	mA	5)
I <sub>DD3N</sub>	252	280	504	560	480	592	mA	5)
I <sub>DD4R</sub>	496	640	748	920	800	996	mA	3)4)
I <sub>DD4W</sub>	564	660	816	940	840	1016	mA	3)
I <sub>DD5</sub>	574	760	826	1040	860	1076	mA	3)
I <sub>DD6</sub>	5	5	10	10	10	10	mA	5)
I <sub>DD7</sub>	872	1140	1280	1536	1280	1536	mA	3)4)

1) DRAM component currents only

2) Test condition for maximum values: V<sub>DD</sub> = 2.7 V, T<sub>A</sub> = 10 °C

3) The module I<sub>DDx</sub> values are calculated from the component I<sub>DDx</sub> data sheet values as:

$m \times I_{DDx}[\text{component}] + n \times I_{DD3N}[\text{component}]$  with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O (I<sub>DDQ</sub>) currents are not included into calculations: module I<sub>DD</sub> values will be measured differently depending on load conditions

5) The module I<sub>DDx</sub> values are calculated from the component I<sub>DDx</sub> data sheet values as:  $(m + n) \times I_{DDx}[\text{component}]$



Table 10 I<sub>DD</sub> Specification

Part Number & Organization	HYS64D16000GDL-8-B		HYS64D32020GDL-8-B		HYS64D16000GDL-7-B HYS64D16001GDL-7-B		HYS64D32020GDL-7-B		Unit	Note <sup>1)2)</sup>
	128MB		256MB		128MB		256MB			
	× 64		× 64		× 64		× 64			
	1 Rank		2 Ranks		1 Rank		2 Ranks			
	-8		-8		-7		-7			
Symbol	typ.	max.	typ.	max.	typ.	max.	typ.	max.		
I <sub>DD0</sub>	288	380	456	580	308	420	516	660	mA	5)
I <sub>DD1</sub>	332	420	500	620	376	460	584	700	mA	5)
I <sub>DD2P</sub>	20	28	40	56	22	32	44	64	mA	5)
I <sub>DD2F</sub>	120	140	240	280	140	160	280	320	mA	5)
I <sub>DD2Q</sub>	72	88	144	176	376	100	752	200	mA	5)
I <sub>DD3P</sub>	52	64	104	128	60	72	120	144	mA	3)4)
I <sub>DD3N</sub>	168	200	336	400	208	240	416	480	mA	3)
I <sub>DD4R</sub>	356	440	524	640	428	520	636	760	mA	3)
I <sub>DD4W</sub>	384	480	552	680	476	560	684	800	mA	5)
I <sub>DD5</sub>	504.8	680	672.8	880	540	720	748	960	mA	3)4)
I <sub>DD6</sub>	6	6	12	12	6	6	12	12	mA	5)
I <sub>DD7</sub>	632	880	800	1080	720	940	928	1180	mA	3)4)

1) DRAM component currents only

2) Test condition for maximum values: V<sub>DD</sub> = 2.7 V, T<sub>A</sub> = 10 °C

3) The module I<sub>DDx</sub> values are calculated from the component I<sub>DDx</sub> data sheet values as:

$m \times I_{DDx}[\text{component}] + n \times I_{DD3N}[\text{component}]$  with **m** and **n** number of components of rank 1 and 2; **n=0** for 1 rank modules

4) DQ I/O (I<sub>DDQ</sub>) currents are not included into calculations: module I<sub>DD</sub> values will be measured differently depending on load conditions

5) The module I<sub>DDx</sub> values are calculated from the component I<sub>DDx</sub> data sheet values as:  $(m + n) \times I_{DDx}[\text{component}]$

**4 AC Characteristics**
**Table 11 AC Timing - Absolute Specifications -6/-5**

Parameter	Symbol	-6		-5		Unit	Note/ Test Condition <sup>1)</sup>
		DDR333		DDR400B			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/ $\overline{\text{CK}}$	$t_{AC}$	-0.7	+0.7	-0.6	+0.6	ns	2)3)4)5)
DQS output access time from CK/ $\overline{\text{CK}}$	$t_{DQSCK}$	-0.6	+0.6	-0.5	+0.5	ns	2)3)4)5)
CK high-level width	$t_{CH}$	0.45	0.55	0.45	0.55	$t_{CK}$	2)3)4)5)
CK low-level width	$t_{CL}$	0.45	0.55	0.45	0.55	$t_{CK}$	2)3)4)5)
Clock Half Period	$t_{HP}$	min. ( $t_{CL}$ , $t_{CH}$ )		min. ( $t_{CL}$ , $t_{CH}$ )		ns	2)3)4)5)
Clock cycle time	$t_{CK}$	6	12	5	12	ns	CL = 3.0 2)3)4)5)
		6	12	6	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
DQ and DM input hold time	$t_{DH}$	0.45	—	0.4	—	ns	2)3)4)5)
DQ and DM input setup time	$t_{DS}$	0.45	—	0.4	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	$t_{IPW}$	2.2	—	2.2	—	ns	2)3)4)5)6)
DQ and DM input pulse width (each input)	$t_{DIPW}$	1.75	—	1.75	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/ $\overline{\text{CK}}$	$t_{HZ}$	-0.7	+0.7	-0.6	+0.6	ns	2)3)4)5)7)
Data-out low-impedance time from CK/ $\overline{\text{CK}}$	$t_{LZ}$	-0.7	+0.7	-0.6	+0.6	ns	2)3)4)5)7)
Write command to 1 <sup>st</sup> DQS latching transition	$t_{DQSS}$	0.75	1.25	0.75	1.25	$t_{CK}$	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	$t_{DQSQ}$	—	+0.45	—	+0.40	ns	TSOPII 2)3)4)5)
Data hold skew factor	$t_{QHS}$	—	+0.55	—	+0.50	ns	TSOPII 2)3)4)5)
DQ/DQS output hold time	$t_{QH}$	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	$t_{CK}$	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	$t_{DSS}$	0.2	—	0.2	—	$t_{CK}$	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	$t_{DSH}$	0.2	—	0.2	—	$t_{CK}$	2)3)4)5)
Mode register set command cycle time	$t_{MRD}$	2	—	2	—	$t_{CK}$	2)3)4)5)
Write preamble setup time	$t_{WPRES}$	0	—	0	—	ns	2)3)4)5)8)
Write postamble	$t_{WPST}$	0.40	0.60	0.40	0.60	$t_{CK}$	2)3)4)5)9)
Write preamble	$t_{WPPE}$	0.25	—	0.25	—	$t_{CK}$	2)3)4)5)

**Table 11 AC Timing - Absolute Specifications –6/–5 (cont'd)**

Parameter	Symbol	–6		–5		Unit	Note/ Test Condition <sup>1)</sup>
		DDR333		DDR400B			
		Min.	Max.	Min.	Max.		
Address and control input setup time	$t_{IS}$	0.75	—	0.6	—	ns	fast slew rate 3)4)5)6)10)
		0.8	—	0.7	—	ns	slow slew rate 3)4)5)6)10)
Address and control input hold time	$t_{IH}$	0.75	—	0.6	—	ns	fast slew rate 3)4)5)6)10)
		0.8	—	0.7	—	ns	slow slew rate 3)4)5)6)10)
Read preamble	$t_{RPRE}$	0.9	1.1	0.9	1.1	$t_{CK}$	2)3)4)5)
Read postamble	$t_{RPST}$	0.40	0.60	0.40	0.60	$t_{CK}$	2)3)4)5)
Active to Precharge command	$t_{RAS}$	42	70E+3	40	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	$t_{RC}$	60	—	55	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	$t_{RFC}$	72	—	65	—	ns	2)3)4)5)
Active to Read or Write delay	$t_{RCD}$	18	—	15	—	ns	2)3)4)5)
Precharge command period	$t_{RP}$	18	—	15	—	ns	2)3)4)5)
Active to Autoprecharge delay	$t_{RAP}$	18	—	15	—	ns	2)3)4)5)
Active bank A to Active bank B command	$t_{RRD}$	12	—	10	—	ns	2)3)4)5)
Write recovery time	$t_{WR}$	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	$t_{DAL}$					$t_{CK}$	2)3)4)5)11)
Internal write to read command delay	$t_{WTR}$	1	—	1	—	$t_{CK}$	2)3)4)5)
Exit self-refresh to non-read command	$t_{XSNR}$	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	$t_{XSRD}$	200	—	200	—	$t_{CK}$	2)3)4)5)
Average Periodic Refresh Interval	$t_{REFI}$	—	7.8	—	7.8	$\mu s$	2)3)4)5)12)

- 1)  $0^\circ C \leq T_A \leq 70^\circ C$ ;  $V_{DDQ} = 2.5 V \pm 0.2 V$ ,  $V_{DD} = +2.5 V \pm 0.2 V$  (DDR333);  $V_{DDQ} = 2.6 V \pm 0.1 V$ ,  $V_{DD} = +2.6 V \pm 0.1 V$  (DDR400)
- 2) Input slew rate  $\geq 1 V/ns$  for DDR400, DDR333
- 3) The CK/ $\overline{CK}$  input reference level (for timing reference to CK/ $\overline{CK}$ ) is the point at which CK and  $\overline{CK}$  cross: the input reference level for signals other than CK/ $\overline{CK}$ , is  $V_{REF}$ . CK/ $\overline{CK}$  slew rate are  $\geq 1.0 V/ns$ .
- 4) Inputs are not recognized as valid until  $V_{REF}$  stabilizes.
- 5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is  $V_{TT}$ .
- 6) These parameters guarantee device timing, but they are not necessarily tested on each device.
- 7)  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
- 8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on  $t_{DQSS}$ .

**AC Characteristics**

- 9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 10) Fast slew rate  $\geq 1.0$  V/ns, slow slew rate  $\geq 0.5$  V/ns and  $< 1$  V/ns for command/address and CK &  $\overline{\text{CK}}$  slew rate  $> 1.0$  V/ns, measured between  $V_{\text{OH(ac)}}$  and  $V_{\text{OL(ac)}}$ .
- 11) For each of the terms, if not already an integer, round to the next highest integer.  $t_{\text{CK}}$  is equal to the actual system clock cycle time.
- 12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

**Table 12 AC Timing - Absolute Specifications –8/–7**

Parameter	Symbol	–8		–7		Unit	Note/ Test Condition <sup>1)</sup>
		DDR200		DDR266A			
		Min	Max.	Min.	Max.		
DQ output access time from CK/ $\overline{\text{CK}}$	$t_{\text{AC}}$	– 0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)
DQS output access time from CK/ $\overline{\text{CK}}$	$t_{\text{DQSK}}$	– 0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)
CK high-level width	$t_{\text{CH}}$	0.4 5	0.55	0.45	0.55	$t_{\text{CK}}$	2)3)4)5)
CK low-level width	$t_{\text{CL}}$	0.4 5	0.55	0.45	0.55	$t_{\text{CK}}$	2)3)4)5)
Clock Half Period	$t_{\text{HP}}$	min. ( $t_{\text{CL}}$ , $t_{\text{CH}}$ )		min. ( $t_{\text{CL}}$ , $t_{\text{CH}}$ )		ns	2)3)4)5)
Clock cycle time	$t_{\text{CK3}}$	8	12	7	12	ns	CL = 3.0 2)3)4)5)
	$t_{\text{CK2.5}}$	8	12	7	12	ns	CL = 2.5 2)3)4)5)
	$t_{\text{CK2}}$	10	12	7.5	12	ns	CL = 2.0 2)3)4)5)
	$t_{\text{CK1.5}}$	10	12	—	—	ns	CL = 1.5 2)3)4)5)
DQ and DM input hold time	$t_{\text{DH}}$	0.6	—	0.5	—	ns	2)3)4)5)
DQ and DM input setup time	$t_{\text{DS}}$	0.6	—	0.5	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	$t_{\text{IPW}}$	2.5	—	2.2	—	ns	2)3)4)5)6)
DQ and DM input pulse width (each input)	$t_{\text{DIPW}}$	2.0	—	1.75	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/ $\overline{\text{CK}}$	$t_{\text{HZ}}$	– 0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)7)
Data-out low-impedance time from CK/ $\overline{\text{CK}}$	$t_{\text{LZ}}$	– 0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)7)
Write command to 1 <sup>st</sup> DQS latching transition	$t_{\text{DQSS}}$	0.7 5	1.25	0.75	1.25	$t_{\text{CK}}$	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	$t_{\text{DQSQ}}$	—	+0.6	—	+0.5	ns	2)3)4)5)
Data hold skew factor	$t_{\text{QHS}}$	—	1.0	—	0.75	ns	2)3)4)5)
DQ/DQS output hold time	$t_{\text{QH}}$	$t_{\text{HP}}$ – $t_{\text{QHS}}$	—	$t_{\text{HP}}$ – $t_{\text{QHS}}$	—	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{\text{DQSL,H}}$	0.3 5	—	0.35	—	$t_{\text{CK}}$	2)3)4)5)

**Table 12 AC Timing - Absolute Specifications –8/–7 (cont'd)**

Parameter	Symbol	–8		–7		Unit	Note/ Test Condition <sup>1)</sup>
		DDR200		DDR266A			
		Min	Max.	Min.	Max.		
DQS falling edge to CK setup time (write cycle)	$t_{DSS}$	0.2	—	0.2	—	$t_{CK}$	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	$t_{DSH}$	0.2	—	0.2	—	$t_{CK}$	2)3)4)5)
Mode register set command cycle time	$t_{MRD}$	2	—	2	—	$t_{CK}$	2)3)4)5)
Write preamble setup time	$t_{WPRES}$	0	—	0	—	ns	2)3)4)5)8)
Write postamble	$t_{WPST}$	0.4 0	0.60	0.40	0.60	$t_{CK}$	2)3)4)5)9)
Write preamble	$t_{WPRE}$	0.2 5	—	0.25	—	$t_{CK}$	2)3)4)5)
Address and control input setup time	$t_{IS}$	1.1	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		1.1	—	1.0	—	ns	slow slew rate 3)4)5)6)10)
Address and control input hold time	$t_{IH}$	1.1	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		1.1	—	1.0	—	ns	slow slew rate 3)4)5)6)10)
Read preamble	$t_{RPRE}$	0.9	1.1	0.9	1.1	$t_{CK}$	CL > 1.5 <sup>2)3)4)5)</sup>
		0.9	1.1	NA	NA	$t_{CK}$	CL = 1.5 <sup>2)3)4)5)11)</sup>
Read preamble setup time	$t_{RPRES}$	1.5	—	NA	NA	ns	2)3)4)5)12)
Read postamble	$t_{RPST}$	0.4 0	0.60	0.40	0.60	$t_{CK}$	2)3)4)5)
Active to Precharge command	$t_{RAS}$	50	120E+3	45	120E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	$t_{RC}$	70	—	65	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	$t_{RFC}$	80	—	75	—	ns	2)3)4)5)
Active to Read or Write delay	$t_{RCD}$	20	—	20	—	ns	2)3)4)5)
Precharge command period	$t_{RP}$	20	—	20	—	ns	2)3)4)5)
Active to Autoprecharge delay	$t_{RAP}$	20	—	20	—	ns	2)3)4)5)
Active bank A to Active bank B command	$t_{RRD}$	15	—	15	—	ns	2)3)4)5)
Write recovery time	$t_{WR}$	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	$t_{DAL}$	$(t_{wr}/t_{CK}) + (t_{rp}/t_{CK})$				$t_{CK}$	2)3)4)5)13)
Internal write to read command delay	$t_{WTR}$	1	—	1	—	$t_{CK}$	CL > 1.5 <sup>2)3)4)5)</sup>
		2	—	—	—	$t_{CK}$	CL = 1.5 <sup>2)3)4)5)</sup>
Exit self-refresh to non-read command	$t_{XSNR}$	80	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	$t_{XSRD}$	200	—	200	—	$t_{CK}$	2)3)4)5)
Average Periodic Refresh Interval	$t_{REFI}$	—	7.8	—	7.8	$\mu$ s	2)3)4)5)14)

- 1)  $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$ ;  $V_{DDQ} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{DD} = +2.5\text{ V} \pm 0.2\text{ V}$
- 2) Input slew rate  $\geq 1\text{ V/ns}$  for DDR400, DDR333, DDR266, and  $= 1\text{ V/ns}$  for DDR200
- 3) The CK/ $\overline{\text{CK}}$  input reference level (for timing reference to CK/ $\overline{\text{CK}}$ ) is the point at which CK and  $\overline{\text{CK}}$  cross: the input reference level for signals other than CK/ $\overline{\text{CK}}$ , is  $V_{REF}$ . CK/ $\overline{\text{CK}}$  slew rate are  $\geq 1.0\text{ V/ns}$ .
- 4) Inputs are not recognized as valid until  $V_{REF}$  stabilizes.
- 5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is  $V_{TT}$ .
- 6) These parameters guarantee device timing, but they are not necessarily tested on each device.
- 7)  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
- 8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on  $t_{DQSS}$ .
- 9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 10) Fast slew rate  $\geq 1.0\text{ V/ns}$ , slow slew rate  $\geq 0.5\text{ V/ns}$  and  $< 1\text{ V/ns}$  for command/address and CK &  $\overline{\text{CK}}$  slew rate  $> 1.0\text{ V/ns}$ , measured between  $V_{OH(ac)}$  and  $V_{OL(ac)}$ .
- 11) CAS Latency 1.5 operation is supported on DDR200 devices only
- 12)  $t_{RPRES}$  is defined for CL = 1.5 operation only
- 13) For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  is equal to the actual system clock cycle time.
- 14) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

## 5 SPD Contents

Table 13 SPD Codes for HYS64D1600xGDL-[6/7/8]-B

Byte#	Description	HYS64D1600GDL-6-B	HYS64D1600GDL-6-B	HYS64D1600GDL-7-B	HYS64D1600GDL-7-B	HYS64D1600GDL-8-B
		128MB	128MB	128MB	128MB	128MB
		×64	×64	×64	×64	×64
		1 Rank	1 Rank	1 Rank	1 Rank	1 Rank
		-6	-6	-7	-7	-8
HEX	HEX	HEX	HEX	HEX		
0	Programmed SPD Bytes in E2PROM	80	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08	08
2	Memory Type DDR-I = 07h	07	07	07	07	07
3	# of Row Addresses	0D	0D	0D	0D	0D
4	# Number of Column Addresses	09	09	09	09	09
5	# of DIMM Banks	01	01	01	01	01
6	Data Width (LSB)	40	40	40	40	40
7	Data Width (MSB)	00	00	00	00	00
8	Interface Voltage Levels	04	04	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	60	60	70	70	80
10	tAC SDRAM @ CLmax (Byte 18) [ns]	70	70	75	75	80
11	DIMM Configuration Type (non- / ECC)	00	00	00	00	00
12	Refresh Rate	82	82	82	82	82
13	Primary SDRAM width	10	10	10	10	10
14	Error Checking SDRAM width	00	00	00	00	00
15	tCCD [cycles]	01	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E	0E
17	Number of Banks on SDRAM	04	04	04	04	04
18	CAS Latency	0C	0C	0C	0C	0C
19	CS Latency	01	01	01	01	01
20	WE (Write) Latency	02	02	02	02	02
21	DIMM Attributes	20	20	20	20	20
22	Component Attributes	C1	C1	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	75	75	75	75	A0
24	tAC SDRAM @ CLmax -0.5 [ns]	70	70	75	75	80
25	tCK @ CLmax -1 (Byte 18) [ns]	00	00	00	00	00

Table 13 SPD Codes for HYS64D1600xGDL-[6/7/8]-B

Byte#	Part Number & Organization Description	HYS64D16000GDL-6-B	HYS64D16001GDL-6-B	HYS64D16000GDL-7-B	HYS64D16001GDL-7-B	HYS64D16000GDL-8-B
		128MB	128MB	128MB	128MB	128MB
		×64	×64	×64	×64	×64
		1 Rank	1 Rank	1 Rank	1 Rank	1 Rank
		-6	-6	-7	-7	-8
HEX	HEX	HEX	HEX	HEX	HEX	
26	tAC SDRAM @ CLmax -1 [ns]	00	00	00	00	00
27	tRPmin (ns)	48	48	50	50	50
28	tRRDmin [ns]	30	30	3C	3C	3C
29	tRCDmin [ns]	48	48	50	50	50
30	tRASmin [ns]	2A	2A	2D	2D	32
31	Module Density per Bank	20	20	20	20	20
32	tAS, tCS [ns]	75	75	90	90	B0
33	tAH, TCH [ns]	75	75	90	90	B0
34	tDS [ns]	45	45	50	50	60
35	tDH [ns]	45	45	50	50	60
36 - 40	not used	00	00	00	00	00
41	tRCmin [ns]	3C	3C	41	41	46
42	tRFCmin [ns]	48	48	4B	4B	50
43	tCKmax [ns]	30	30	30	30	30
44	tDQSQmax [ns]	2D	2D	32	32	3C
45	tQHSmax [ns]	55	55	75	75	A0
46 - 61	not used	00	00	00	00	00
62	SPD Revision	00	00	00	00	00
63	Checksum of Byte 0-62 (LSB only)	E8	E8	9A	9A	8F
64	JEDEC ID Code for Infineon	C1	C1	C1	C1	C1
65	JEDEC ID Code for Infineon	49	49	49	49	49
66	JEDEC ID Code for Infineon	4E	4E	4E	4E	4E
67	JEDEC ID Code for Infineon	46	46	46	46	46
68	JEDEC ID Code for Infineon	49	49	49	49	49
69	JEDEC ID Code for Infineon	4E	4E	4E	4E	4E
70	JEDEC ID Code for Infineon	45	45	45	45	45
71	JEDEC ID Code for Infineon	4F	4F	4F	4F	4F
72	Module Manufacturer Location	xx	09	xx	09	xx
73	Part Number, Char 1	36	36	36	36	36



Table 13 SPD Codes for HYS64D1600xGDL-[6/7/8]-B

Byte#	Part Number & Organization Description	HYS64D16000GDL-6-B	HYS64D16001GDL-6-B	HYS64D16000GDL-7-B	HYS64D16001GDL-7-B	HYS64D16000GDL-8-B
		128MB	128MB	128MB	128MB	128MB
		×64	×64	×64	×64	×64
		1 Rank	1 Rank	1 Rank	1 Rank	1 Rank
		-6	-6	-7	-7	-8
		HEX	HEX	HEX	HEX	HEX
74	Part Number, Char 2	34	34	34	34	34
75	Part Number, Char 3	44	44	44	44	44
76	Part Number, Char 4	31	31	31	31	31
77	Part Number, Char 5	36	36	36	36	36
78	Part Number, Char 6	30	30	30	30	30
79	Part Number, Char 7	30	30	30	30	30
80	Part Number, Char 8	30	31	30	31	30
81	Part Number, Char 9	47	47	47	47	47
82	Part Number, Char 10	44	44	44	44	44
83	Part Number, Char 11	4C	4C	4C	4C	4C
84	Part Number, Char 12	36	36	37	37	38
85	Part Number, Char 13	42	42	42	42	42
86	Part Number, Char 14	20	20	20	20	20
87	Part Number, Char 15	20	20	20	20	20
88	Part Number, Char 16	20	20	20	20	20
89	Part Number, Char 17	20	20	20	20	20
90	Part Number, Char 18	20	20	20	20	20
91	Module Revision Code	xx	xx	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 -127	not used	00	00	00	00	00

Table 14 SPD Codes for HYS64D32020GDL-[5/6/7/8]-B

	Part Number & Organization	HYS64D32020GDL-5-B	HYS64D32020GDL-6-B	HYS64D32020GDL-7-B	HYS64D32020GDL-8-B
		256MB	256MB	256MB	256MB
		× 64	× 64	× 64	× 64
		2 Ranks	2 Ranks	2 Ranks	2 Ranks
		-5	-6	-7	-8
Byte#	Description	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type DDR-I = 07h	07	07	07	07
3	# of Row Addresses	0D	0D	0D	0D
4	# Number of Column Addresses	09	09	09	09
5	# of DIMM Banks	02	02	02	02
6	Data Width (LSB)	40	40	40	40
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	50	60	70	80
10	tAC SDRAM @ CLmax (Byte 18) [ns]	50	70	75	80
11	DIMM Configuration Type (non- / ECC)	00	00	00	00
12	Refresh Rate	82	82	82	82
13	Primary SDRAM width	10	10	10	10
14	Error Checking SDRAM width	00	00	00	00
15	tCCD [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM	04	04	04	04
18	CAS Latency	1C	0C	0C	0C
19	CS Latency	01	01	01	01
20	WE (Write) Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	60	75	75	A0
24	tAC SDRAM @ CLmax -0.5 [ns]	50	70	75	80
25	tCK @ CLmax -1 (Byte 18) [ns]	75	00	00	00
26	tAC SDRAM @ CLmax -1 [ns]	50	00	00	00
27	tRPmin (ns)	3C	48	50	50

Table 14 SPD Codes for HYS64D32020GDL-[5/6/7/8]-B

Byte#	Description	HYS64D32020GDL-5-B	HYS64D32020GDL-6-B	HYS64D32020GDL-7-B	HYS64D32020GDL-8-B
		256MB	256MB	256MB	256MB
		×64	×64	×64	×64
		2 Ranks	2 Ranks	2 Ranks	2 Ranks
		-5	-6	-7	-8
Byte#	Description	HEX	HEX	HEX	HEX
28	tRRDmin [ns]	28	30	3C	3C
29	tRCDmin [ns]	3C	48	50	50
30	tRASmin [ns]	28	2A	2D	32
31	Module Density per Bank	20	20	20	20
32	tAS, tCS [ns]	60	75	90	B0
33	tAH, TCH [ns]	60	75	90	B0
34	tDS [ns]	40	45	50	60
35	tDH [ns]	40	45	50	60
36 - 40	not used	00	00	00	00
41	tRCmin [ns]	37	3C	41	46
42	tRFCmin [ns]	41	48	4B	50
43	tCKmax [ns]	28	30	30	30
44	tDQSQmax [ns]	28	2D	32	3C
45	tQHSmax [ns]	50	55	75	A0
46 - 61	not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62 (LSB only)	E5	E9	9B	90
64	JEDEC ID Code for Infineon	C1	C1	C1	C1
65	JEDEC ID Code for Infineon	49	49	49	49
66	JEDEC ID Code for Infineon	4E	4E	4E	4E
67	JEDEC ID Code for Infineon	46	46	46	46
68	JEDEC ID Code for Infineon	49	49	49	49
69	JEDEC ID Code for Infineon	4E	4E	4E	4E
70	JEDEC ID Code for Infineon	45	45	45	45
71	JEDEC ID Code for Infineon	4F	4F	4F	4F
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	36	36	36
74	Part Number, Char 2	34	34	34	34
75	Part Number, Char 3	44	44	44	44

Table 14 SPD Codes for HYS64D32020GDL-[5/6/7/8]-B

Byte#	Part Number & Organization	HYS64D32020GDL-5-B	HYS64D32020GDL-6-B	HYS64D32020GDL-7-B	HYS64D32020GDL-8-B
		256MB	256MB	256MB	256MB
		×64	×64	×64	×64
		2 Ranks	2 Ranks	2 Ranks	2 Ranks
		-5	-6	-7	-8
Byte#	Description	HEX	HEX	HEX	HEX
76	Part Number, Char 4	33	33	33	33
77	Part Number, Char 5	32	32	32	32
78	Part Number, Char 6	30	30	30	30
79	Part Number, Char 7	32	32	32	32
80	Part Number, Char 8	30	30	30	30
81	Part Number, Char 9	47	47	47	47
82	Part Number, Char 10	44	44	44	44
83	Part Number, Char 11	4C	4C	4C	4C
84	Part Number, Char 12	35	36	37	38
85	Part Number, Char 13	42	42	42	42
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	xx	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	not used	00	00	00	00

6 Package Outlines

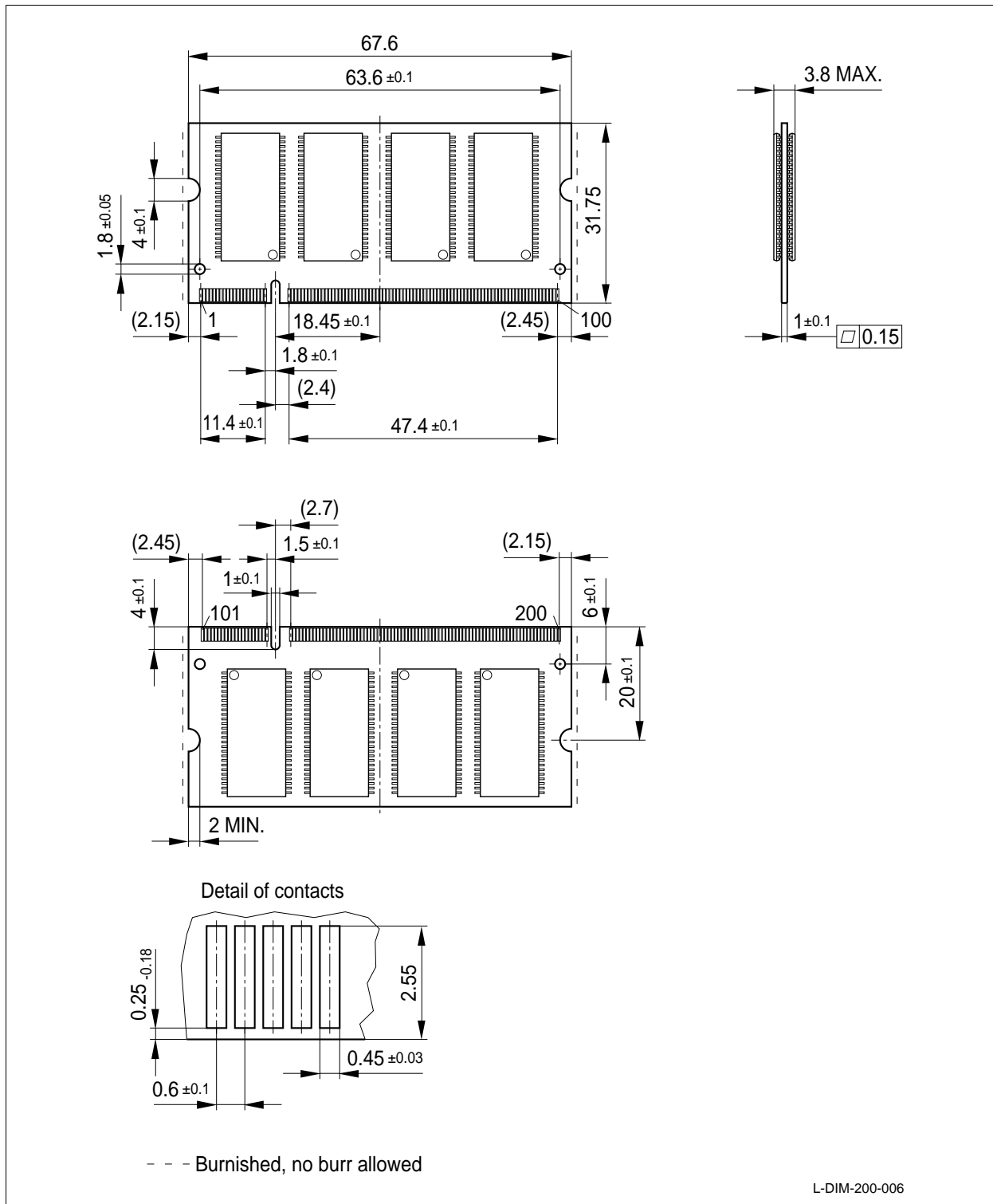


Figure 4 Package Outlines – Raw Card A DDR-SDRAM SO-DIMM Module HYS64D32020GDL-[5/6/7/8]-B

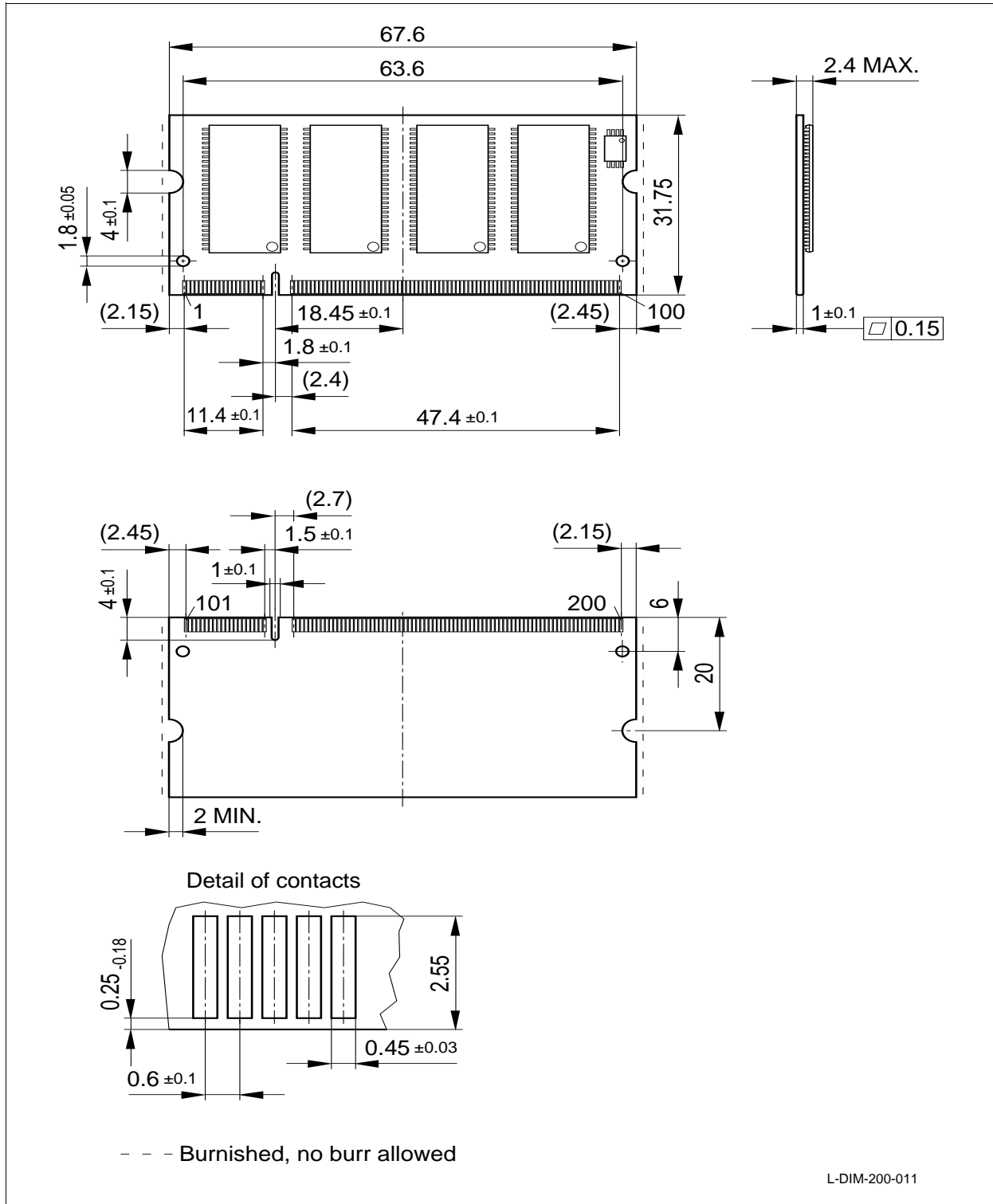


Figure 5 Package Outlines Raw Card C DDR SDRAM SO-DIMM Modules HYS64D1600xGDL-[6/7/8]-B

[www.infineon.com](http://www.infineon.com)

Published by Infineon Technologies AG