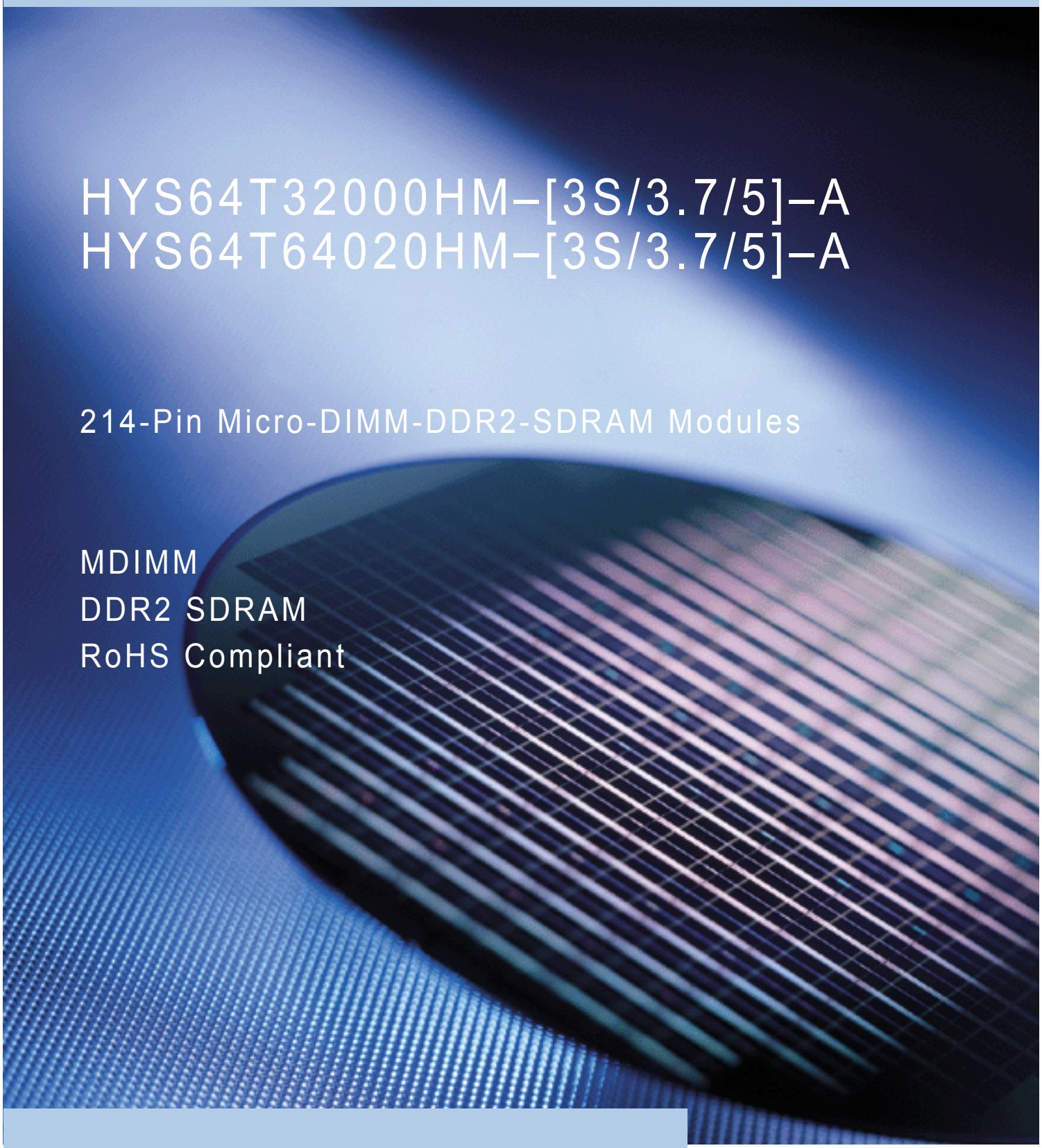
HYS64T32000HM–[3S/3.7/5]–A
HYS64T64020HM–[3S/3.7/5]–A

214-Pin Micro-DIMM-DDR2-SDRAM Modules

MDIMM
DDR2 SDRAM
RoHS Compliant



Memory Products

Infineon technologies

Never stop thinking.

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Page	Subjects (major changes since last revision)
all	Added -3S

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Table of Contents

1 Overview

This chapter gives an overview of the 1.8 V 214-Pin Micro-DIMM-DDR2-SDRAM Modules product family and describes its main characteristics.

1.1 Features

- 214-Pin PC2-5300, PC2-4200 and PC2-3200 DDR2 SDRAM memory modules for use as main memory when installed in systems such as mobile personal computers.
- 32M × 64and 64M × 64 module organization, and 32M × 16 chip organization
- JEDEC standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Built with 512Mb DDR2 SDRAMs in P-TFBGA-84 chipsize packages
- Programmable CAS Latencies (3, 4 and 5), Burst Length (8 & 4) and Burst Type
- Burst Refresh, Distributed Refresh and Self Refresh
- All inputs and outputs SSTL_1.8 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E2PROM
- MDIMM Dimensions (nominal): 30 mm high, 54.0 mm wide
- Based on JEDEC standard reference layouts Raw Card “A” & “B”
- 2-piece type Mezzanine Socket with 0,4 mm contact centers
- RoHS Compliant Products[1)]

Table 1 High Performance DDR2–667D

Product Type Speed Code			–3S	Unit
Speed Grade			**PC2–5300 5–5–5**	**—**
max. Clock Frequency	@CL5	f_{CK5}	333	MHz
	@CL4	f_{CK4}	266	MHz
	@CL3	f_{CK3}	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	ns
min. Row Precharge Time		t_{RP}	15	ns
min. Row Active Time		t_{RAS}	45	ns
min. Row Cycle Time		t_{RC}	60	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

Table 2 Performance for DDR2-533 and DDR2-400

Product Type Speed Code			–3.7	–5	Units
Speed Grade			**PC2–4200 4–4–4**	**PC2–3200 3–3–3**	**—**
Max. Clock Frequency	@CL5	f_{CK5}	266	200	MHz
	@CL4	f_{CK4}	266	200	MHz
	@CL3	f_{CK3}	200	200	MHz
Min. RAS-CAS-Delay		t_{RCD}	15	15	ns
Min. Row Precharge Time		t_{RP}	15	15	ns
Min. Row Active Time		t_{RAS}	45	40	ns
Min. Row Cycle Time		t_{RC}	60	55	ns

1.2 Description

The INFINEON HYS64T[32/64]0[0/2]0HM–[3S/3.7/5]–A module family are Unbuffered Micro-DIMM modules “MDIMMs” with 30.0-mm height based on DDR2 technology. DIMMs are available as non-ECC modules in 32M × 64 (256 MB) and 64M × 64 (512 MB) organization and density, intended for mounting into 214-pin mezzanine connector sockets.

The memory array is designed with 512-Mbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.

Table 3 Ordering Informationfor RoHS Compliant Products

Product Type[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC2-5300			
HYS64T32000HM-3S-A	256MB 1R×16 PC2–5300M–555–11–B1	1 rank, Non-ECC	512 Mbit (×16)
HYS64T64020HM-3S-A	512MB 2R×16 PC2–5300M–555–11–A1	2 ranks, Non-ECC	512 Mbit (×16)
PC2–4200			
HYS64T32000HM–3.7–A	256MB 1R×16 PC2–4200M–444–11–B1	1 rank, Non-ECC	512 Mbit (×16)
HYS64T64020HM–3.7–A	512MB 2R×16 PC2–4200M–444–11–A1	2 ranks, Non-ECC	512 Mbit (×16)
PC2–3200			
HYS64T32000HM–5–A	256MB 1R×16 PC2–3200M–333–11–B1	1 rank, Non-ECC	512 Mbit (×16)
HYS64T64020HM–5–A	512MB 2R×16 PC2–3200M–333–11–A1	2 ranks, Non-ECC	512 Mbit (×16)

1) All part numbers end with a place code, designating the silicon die revision. Example: HYS64T32000HM–3.7–A, indicating Rev. “A” dies are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see Chapter 6 of this data sheet.

2) The Compliance Code is printed on the module label and describes the speed grade, for example “PC2–4200M–444–11–B1”, where 4200M means Unbuffered Micro-DIMM modules with 4.26 GB/sec Module Bandwidth and “444-11” means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.1 and produced on the Raw Card “B”.

Table 4 Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/columns bits	Raw Card
256 MByte	32M ×64	1	Non-ECC	4	13/2/10	B
512 MByte	64M ×64	2	Non-ECC	8	13/2/10	A

Table 5 Components on Modules[1)]

Product Type[2)]	DRAM Components[2)]	DRAM Density	DRAM Organisation
HYS64T32000HM	HYB18T512160AF	512 Mbit	32M ×16
HYS64T64020HM	HYB18T512160AF	512 Mbit	32M ×16

1) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.
2) Green Product

2 Pin Configuration and Block Diagrams

2.1 Pin Configuration

The pin configuration of the DDR2 SDRAM Micro-DIMM is listed by function in **Table 6** (214 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 7** and **Table 8** respectively. The pin numbering is depicted in **Figure 1**.

Table 6 Pin Configuration of MDIMM

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
122	CK0	I	SSTL	**Clock Signal CK 1:0, Complementary Clock Signal CK 1:0**
194	CK1	I	SSTL	*Note: The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.*
123	$\overline{CK0}$	I	SSTL	
195	$\overline{CK1}$	I	SSTL	
43	CKE0	I	SSTL	**Clock Enables 1:0**
147	CKE1	I	SSTL	*Note: Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE0 initiates the Power Down Mode or the Self Refresh Mode.* *1. 2-rank module*
	NC	NC		**Not Connected** *Note: 1-rank module*
Control Signals				
165	$\overline{S0}$	I	SSTL	**Chip Select Rank 1:0**
62	$\overline{S1}$	I	SSTL	*Note: Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$. The input signals also disable all outputs (except CKE and ODT) of the register(d) on the DIMM when both inputs are high. When $\overline{S}$ is HIGH, all register outputs (except CK, ODT and Chip select) remain in the previous state.* *2. 2-rank module*
	NC	NC		**Not Connected** *Note: 1-rank module*

Table 6 Pin Configuration of MDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
163	$\overline{RAS}$	I		**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
60	$\overline{CAS}$	I	SSTL	
56	$\overline{WE}$	I	SSTL	*Note: When sampled at the cross point of the rising edge of CK,and falling edge of $\overline{CK}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.*
Address Signals				
55	BA0	I	SSTL	**Bank Address Bus 1:0**
162	BA1	I	SSTL	*Note: Select internal SDRAM memory bank*
46	BA2	I	SSTL	**Bank Address Bus 2**
				Note: Greater than 512Mb DDR2 SDRAMS
	NC	NC	–	**Not Connected**
				Note: Less than 1Gb DDR2 SDRAMS
161	A0	I	SSTL	**Address Inputs 12:0, Address Input 10/Autoprecharge**
159	A1	I	SSTL	*Note: During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA[1:0] defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA[1:0] inputs. If AP is LOW, then BA[1:0] are used to define which bank to precharge.*
52	A2	I	SSTL	
158	A3	I	SSTL	
51	A4	I	SSTL	
50	A5	I	SSTL	
157	A6	I	SSTL	
48	A7	I	SSTL	
155	A8	I	SSTL	
154	A9	I	SSTL	
54	A10	I	SSTL	
	AP	I	SSTL	
47	A11	I	SSTL	
153	A12	I	SSTL	
167	A13	I	SSTL	**Address Input 13**
				Note: Modules based on x4/x8 component
	NC	NC	–	**Not Connected**
				Note: Modules based on x16 component

Table 6 Pin Configuration of MDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Data Signals				
3	DQ0	I/O	SSTL	**Data Bus 0:38**
4	DQ1	I/O	SSTL	*Note: Data Input/Output pins*
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
109	DQ4	I/O	SSTL	
110	DQ5	I/O	SSTL	
114	DQ6	I/O	SSTL	
115	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
117	DQ12	I/O	SSTL	
118	DQ13	I/O	SSTL	
125	DQ14	I/O	SSTL	
126	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
128	DQ20	I/O	SSTL	
129	DQ21	I/O	SSTL	
133	DQ22	I/O	SSTL	
134	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
38	DQ26	I/O	SSTL	
39	DQ27	I/O	SSTL	
136	DQ28	I/O	SSTL	
137	DQ29	I/O	SSTL	
142	DQ30	I/O	SSTL	
143	DQ31	I/O	SSTL	
67	DQ32	I/O	SSTL	
68	DQ33	I/O	SSTL	
73	DQ34	I/O	SSTL	
74	DQ35	I/O	SSTL	
174	DQ36	I/O	SSTL	
175	DQ37	I/O	SSTL	
179	DQ38	I/O	SSTL	

Table 6 Pin Configuration of MDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
180	DQ39	I/O	SSTL	**Data Bus 39:57**
76	DQ40	I/O	SSTL	
77	DQ41	I/O	SSTL	
81	DQ42	I/O	SSTL	
82	DQ43	I/O	SSTL	
182	DQ44	I/O	SSTL	
183	DQ45	I/O	SSTL	
188	DQ46	I/O	SSTL	
189	DQ47	I/O	SSTL	
84	DQ48	I/O	SSTL	
85	DQ49	I/O	SSTL	
92	DQ50	I/O	SSTL	
93	DQ51	I/O	SSTL	
191	DQ52	I/O	SSTL	
192	DQ53	I/O	SSTL	
200	DQ54	I/O	SSTL	
201	DQ55	I/O	SSTL	
95	DQ56	I/O	SSTL	
96	DQ57	I/O	SSTL	
101	DQ58	I/O	SSTL	
102	DQ59	I/O	SSTL	
203	DQ60	I/O	SSTL	
204	DQ61	I/O	SSTL	
208	DQ62	I/O	SSTL	
209	DQ63	I/O	SSTL	
7	DQS0	I/O	SSTL	**Data Strobes 7:0**
6	$\overline{\text{DQS0}}$	I/O	SSTL	*Note: The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and DQS. If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to V_{SS} and DDR2 SDRAM mode registers programmed appropriately.*
19	DQS1	I/O	SSTL	
18	$\overline{\text{DQS1}}$	I/O	SSTL	
28	DQS2	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
140	DQS3	I/O	SSTL	
139	$\overline{\text{DQS3}}$	I/O	SSTL	
71	DQS4	I/O	SSTL	
70	$\overline{\text{DQS4}}$	I/O	SSTL	
186	DQS5	I/O	SSTL	*Note: See block diagram for corresponding DQ signals*
185	$\overline{\text{DQS5}}$	I/O	SSTL	
198	DQS6	I/O	SSTL	
197	$\overline{\text{DQS6}}$	I/O	SSTL	
99	DQS7	I/O	SSTL	

Table 6 Pin Configuration of MDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
98	$\overline{\text{DQS7}}$	I/O	SSTL	
112	DM0	I	SSTL	**Data Masks 7:0**
120	DM1	I	SSTL	*Note: The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect.*
131	DM2	I	SSTL	
36	DM3	I	SSTL	
177	DM4	I	SSTL	
79	DM5	I	SSTL	*Note: x8 based module*
90	DM6	I	SSTL	
206	DM7	I	SSTL	
EEPROM				
105	SCL	I	CMOS	**Serial Bus Clock** *Note: This signal is used to clock data into and out of the SPD EEPROM.*
104	SDA	I/O	OD	**Serial Bus Data** *Note: This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to V_{DDSPD} on the motherboard to act as a pull-up.*
211	SA0	I	CMOS	**Serial Address Select Bus 1:0**
213	SA1	I	CMOS	*Note: Address pins used to select the Serial Presence Detect base address.*
Power Supplies				
1	V_{REF}	AI	–	**I/O Reference Voltage** *Note: Reference voltage for the SSTL-18 inputs.*
42, 45, 49, 53, 57, 61, 64, 146, 149, 152, 156, 160, 164, 168, 171	V_{DD}	PWR	–	**Power Supply** *Note: Power and ground for the DDR SDRAM*
107	V_{DDSPD}	PWR	–	**EEPROM Power Supply** *Note: Serial EEPROM positive power supply, wired to a separate power pin at the connector which supports from 1.7 Volt to 3.6 Volt.*

Table 6 Pin Configuration of MDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 37, 40, 66, 69, 72, 75, 78, 80, 83, 86, 89, 91, 94, 97, 100, 103, 108, 111, 113, 116, 119, 121, 124, 127, 130, 132, 135, 138, 141, 144, 173, 176, 178, 181, 184, 187, 190, 193, 196, 205, 199, 202, 207, 210	V_{SS}	GND	–	**Ground Plane** *Note: Power and ground for the DDR SDRAM*
Other Pins				
166	ODT0	I	SSTL	**On-Die Termination Control 1:0** *Note: Asserts on-die termination for DQ, DM, DQS, and DQS signals if enabled via the DDR2 SDRAM mode register.* *Note: 2-rank module*
63	ODT1	I	SSTL	
	NC			**Not Connected** *Note: 1-rank module*
15, 16, 41, 44, 46, 58, 59, 65, 87, 88, 106, 145, 148, 150, 151, 167, 169, 170, 172, 212, 214	NC	NC		**Not connected** *Note: Pins not connected on Infineon MDIMMs*

Table 7 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 8 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

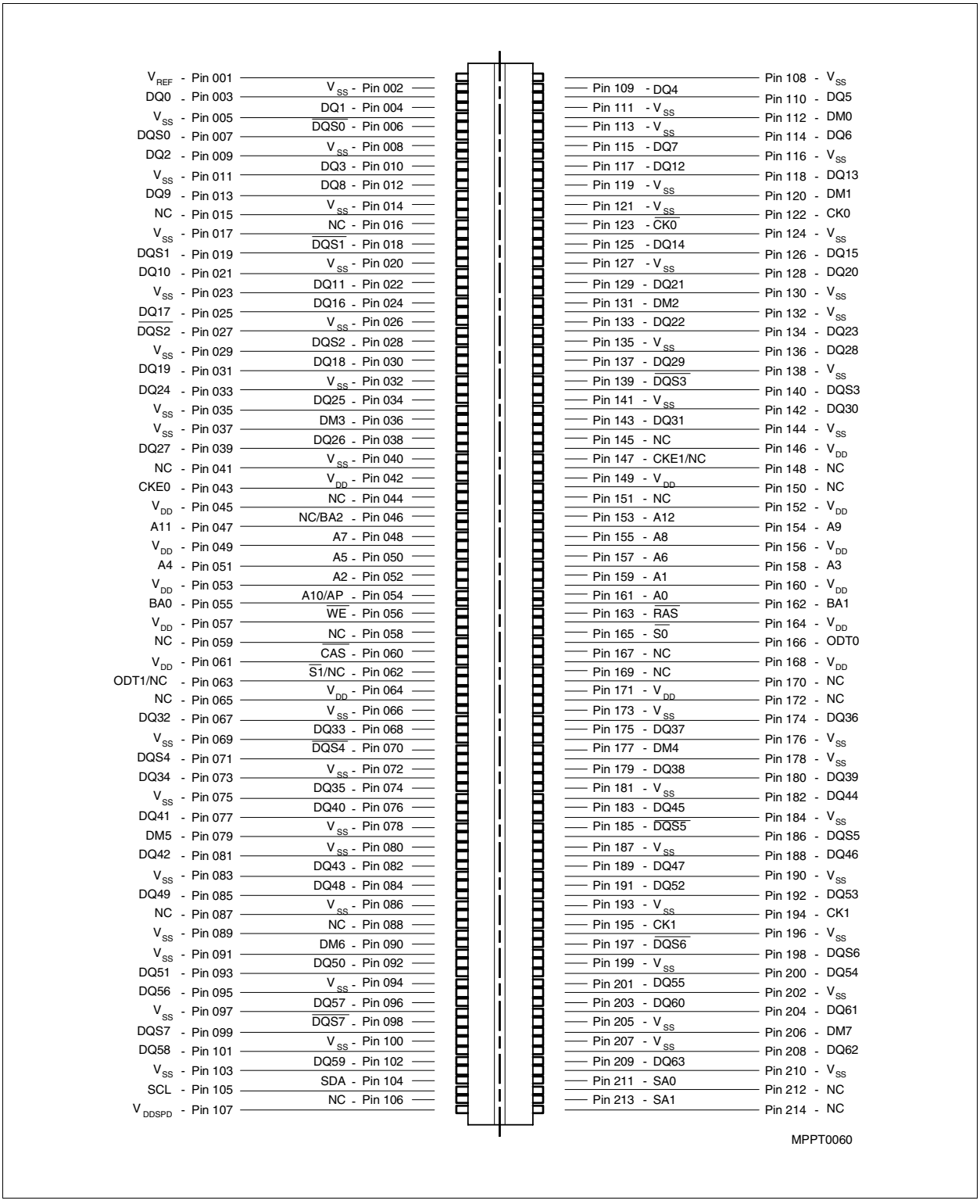

Figure 1 Pin Configuration for Two-Piece Mezzanine Socket on MDIMM (214 pins)

2.2 Block Diagrams

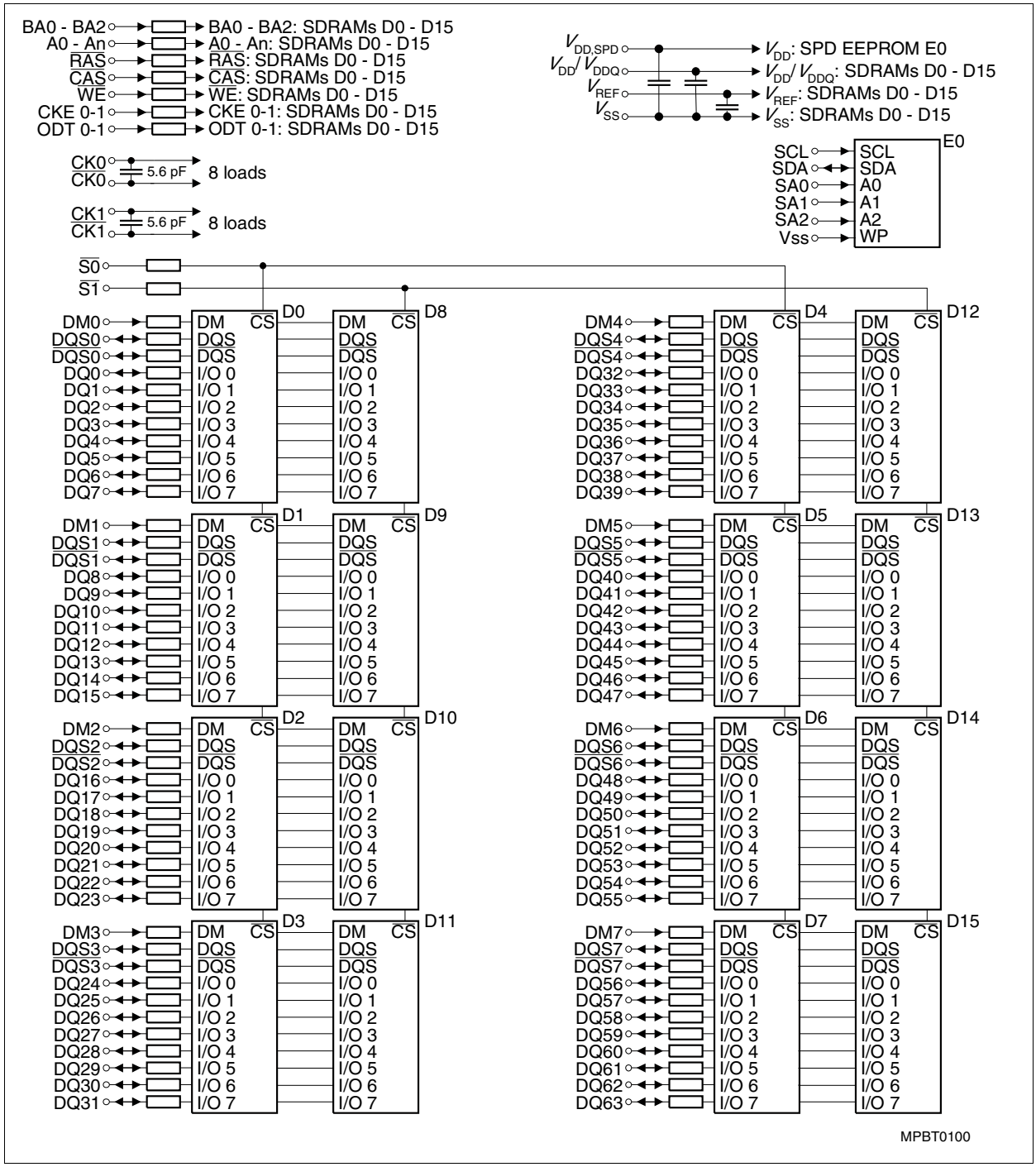

Figure 2 Block Diagram Raw Card A Micro-DIMM (×64, 2 Ranks, ×16)

Notes

1. *DQ, DQS, DM resistors are 22 Ω ±5 %*
2. *$\overline{S0}$,$\overline{S1}$, BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODTO, ODT1, CKEO, CKE1 resistors are 3 Ω ±5 %*

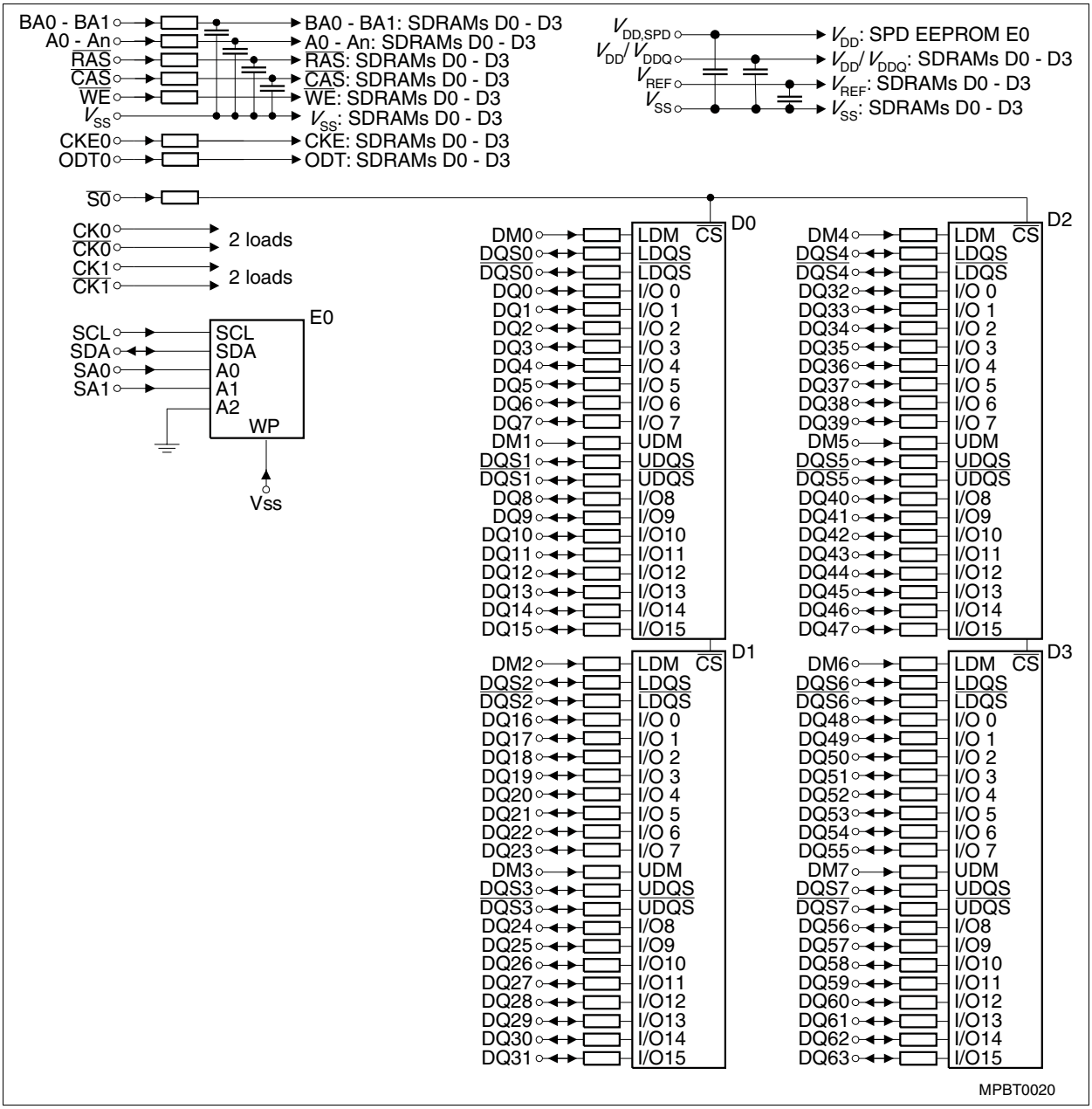

Figure 3 Block Diagram Raw Card B Micro-DIMM (x64, 1 Rank, x16)

Notes

1. *DQ, DQS, DM resistors are 22 Ω ±5 %*
2. *S0, BAn, An, RAS, CAS, WE, ODTO, CKEO resistors are 3 Ω ±5 %*
3. *Load matching Capacitors on BA0 - BA1, A0 - An, RAS, CAS, WE, with 8 pF ± 0.5pF*

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	2.3	V	
Voltage on V_{DD} relative to V_{SS}	V_{DD}	– 1.0	2.3	V	
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	– 0.5	2.3	V	
Storage Humidity (without condensation)	H_{STG}	5	95	%	

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values maycause irreversible damage to the integrated circuit.

3.2 DC Operating Conditions

Table 10 Operating Conditions

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+65	°C	
DRAM Case Temperature	T_{CASE}	0	+95	°C	1)2)3)4)
Storage Temperature	T_{STG}	– 50	+100	°C	
Barometric Pressure (operating & storage)	PBar	69	105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.

2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported

3) Above 85 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs

4) Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 °C Case Temperature before initiating Self-Refresh operation.

5) Up to 3000 m.

Table 11 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Nom.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	
DC Input Logic High	$V_{IH\ (DC)}$	V_{REF} + 0.125	—	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	—	V_{REF} – 0.125	V	
In / Output Leakage Current	I_L	– 5		5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}

2) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise in V_{DDQ}.

3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

3.3 AC Characteristics

3.3.1 Speed Grade Definitions

Table 12 Speed Grade Definition Speed Bins for DDR2-667D, DDR2–533C and DDR2–400B

Speed Grade			DDR2–667D		DDR2–533C		DDR2–400B		Unit	Notes
IFX Sort Name			–3S		–3.7		–5			
CAS-RCD-RP latencies			5–5–5		4–4–4		3–3–3		t_{CK}	
Parameter		Symbol	Min.		Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	3.75	8	5	8	ns	
	@ CL = 5	t_{CK}	3	8	3.75	8	5	8	ns	
Row Active Time		t_{RAS}	45	70000	45	70000	40	70000	ns	5)
Row Cycle Time		t_{RC}	60	—	60	—	55	—	ns	
RAS-CAS-Delay		t_{RCD}	15	—	15	—	15	—	ns	
Row Precharge Time		t_{RP}	15	—	15	—	15	—	ns	

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.

2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode

3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.

4) The output timing reference voltage level is V_{TT}.

5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

3.3.2 AC Timing Parameters

Table 13 Timing Parameter by Speed Grade - DDR2-667

Parameter	Symbol	DDR2-667		Unit	Note 1)2)3)4)5)6) 7)
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–450	+450	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	175	—	ps	
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–400	+400	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	240	—	ps	
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	ps	
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	275	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	200	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—		
Data hold skew factor	t_{QHS}	340	—	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	8)
		—	3.9	µs	9)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	

Table 13 Timing Parameter by Speed Grade - DDR2-667

Parameter	Symbol	DDR2-667		Unit	Note 1)2)3)4)5)6)7)
		Min.	Max.		
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	10)
		10	—	ns	11)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.35	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	7 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet

2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V. See notes

3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.

5) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross.
The DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode

6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.

7) The output timing reference voltage level is V_{TT}.

8) $0 \le T_{CASE} \le 85$ °C

9) 85 °C < $T_{CASE} \le 95$ °C

10) x4 & x8

11) x16

Table 14 Timing Parameter by Speed Grade - DDR2-533

Parameter	Symbol	DDR2–533		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–500	+500	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	

Table 14 Timing Parameter by Speed Grade - DDR2-533 (cont'd)

Parameter	Symbol	DDR2–533		Unit	Note[1)2) 3)4)5)6)7)]
		Min.	Max.		
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	225	—	ps	
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–450	+450	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	ps	
Write command to 1st DQS latching transition	t_{DQSS}	–0.25	+0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	ps	
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	375	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	250	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	$2 \circ t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—		
Data hold skew factor	t_{QHS}	—	400	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	8)
		—	3.9	µs	9)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	10)
		10	—	ns	11)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	$0.35 x t_{CK}$	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	

Table 14 Timing Parameter by Speed Grade - DDR2-533 (cont'd)

Parameter	Symbol	DDR2–533		Unit	Note[1)2) 3)4)5)6)7)]
		Min.	Max.		
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet

2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V. See notes

3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.

5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode

6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.

7) The output timing reference voltage level is V_{TT}.

8) $0 \le T_{CASE} \le 85$ °C

9) $85 < T_{CASE} \le 95$ °C

10) x4 & x8

11) x16

Table 15 Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2-400		Unit	Note 1)2)3)4)5)6)7)
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–600	+600	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	275	—	ps	
DQ and DM input hold time (single-ended strobe)	t_{DH1}(base)	25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–500	+500	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	

Table 15 Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2-400		Unit	Note 1)2)3)4)5)6)7)
		Min.	Max.		
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	350	ps	
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	150	—	ps	
DQ and DM input setup time (single-ended strobe)	t_{DS1}(base)	25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	475	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	350	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—		
Data hold skew factor	t_{QHS}	—	450	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	8)
		—	3.9	µs	9)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	10)
		10	—	ns	11)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.35	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet

2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V. See notes

3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross.
The DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}. See Chapter 8 for the reference load for timing measurements.
8) $0 \leq T_{CASE} \leq 85$ °C
9) 85 °C < $T_{CASE} \leq 95$ °C
10) x4 & x8
11) x16

3.3.3 ODT AC Electrical Characteristics

Table 16 ODT AC Electrical Characteristics and Operating Conditions for DDR2-667

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.

2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

Table 17 ODT AC Electrical Characteristics and Operating Conditions for DDR2-533 and DDR2-400

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 1 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.

2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

3.4 I_{DD} Specifications and Conditions

Table 18 I_{DD} Measurement Conditions [1)2)3)4)5)6)]

Parameter	Symbol
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = CL_{MIN}; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD2N}
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$
Operating Current urst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}
Burst Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}
Distributed Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}

Table 18 I_{DD} Measurement Conditions (cont'd)[1)2)3)4)5)6)]

Parameter	Symbol
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
3) Definitions for I_{DD} see **Table 19**
4) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.
5) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
6) For details and notes see the relevant INFINEON component data sheet

Table 19 Definitions for I_{DD}

Parameter	Description
LOW	$V_{IN} \le V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \ge V_{IH(ac).MIN}$
STABLE	inputs are stable at a HIGH or LOW level
FLOATING	inputs are $V_{REF} = V_{DDQ}/2$
SWITCHING	inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes

Table 20 I_{DD} Specification for HYS64T[32000/64020]HM-3S-A

Product Type	HYS64T32000HM-3S-A	HYS64T64020HM-3S-A	Unit	Notes[1)]
Organization	**256MB**	**512MB**		
	1 Rank	**2 Ranks**		
	×64	**×64**		
	–3S	**–3S**		
Symbol	**Max.**	**Max.**		
I_{DD0}	360	380	mA	2)
I_{DD1}	420	440	mA	2)
I_{DD2N}	200	400	mA	3)
I_{DD2P}	20	40	mA	3)
I_{DD2Q}	160	320	mA	3)
I_{DD3N}	200	400	mA	3)
$I_{DD3P(MRS = 0)}$	80	150	mA	3)
$I_{DD3P(MRS = 1)}$	20	50	mA	3)
I_{DD4R}	600	620	mA	2)
I_{DD4W}	680	700	mA	2)
I_{DD5B}	560	580	mA	2)
I_{DD5D}	20	50	mA	3)4)
I_{DD6}	20	40	mA	3)4)
I_{DD7}	910	930	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled

2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode

3) Both ranks are in the same I_{DD} mode

4) Values for 0 °C ≤ T_{CASE} ≤ 85 °C

Table 21 I_{DD} Specification for HYS64T[32000/64020]HM–3.7–A

Product Type	HYS64T32000HM-3.7-A	HYS64T64020HM-3.7-A	Unit	Notes[1]
Organization	**256 MB**	**512 MB**		
	1 Rank	**2 Ranks**		
	×64	**×64**		
	–3.7	**–3.7**		
Symbol	**Max.**	**Max.**		
I_{DD0}	320	340	mA	2)
I_{DD1}	360	380	mA	2)
I_{DD2N}	160	320	mA	3)
I_{DD2P}	20	30	mA	3)
I_{DD2Q}	120	240	mA	3)
I_{DD3N}	160	320	mA	3)
$I_{DD3P(MRS=0)}$	60	130	mA	3)
$I_{DD3P(MRS=1)}$	20	40	mA	3)
I_{DD4R}	400	420	mA	2)
I_{DD4W}	440	460	mA	2)
I_{DD5B}	520	540	mA	2)
I_{DD5D}	20	50	mA	3)4)
I_{DD6}	16	32	mA	3)4)
I_{DD7}	880	900	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled

2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode

3) Both ranks are in the same I_{DD} mode

4) Values for 0 °C ≤ T_{CASE} ≤ 85 °C

Table 22 I_{DD} Specification for HYS64T[32000/64020]HM–5–A

Product Type	HYS64T32000HM-5-A	HYS64T64020HM-5-A	Unit	Notes[1]
Organization	**256 MB**	**512 MB**		
	1 Rank	**2 Ranks**		
	×64	**×64**		
	–5	**–5**		
Symbol	**Max.**	**Max.**		
I_{DD0}	280	300	mA	2)
I_{DD1}	300	320	mA	2)
I_{DD2N}			mA	3)
I_{DD2P}	20	30	mA	3)
I_{DD2Q}	100	200	mA	3)
I_{DD3N}	140	280	mA	3)
$I_{DD3P(MRS=0)}$	50	100	mA	3)
$I_{DD3P(MRS=1)}$	20	40	mA	3)
I_{DD4R}	340	360	mA	2)
I_{DD4W}	360	380	mA	2)
I_{DD5B}	480	500	mA	2)
I_{DD5D}	20	50	mA	3)4)
I_{DD6}	16	32	mA	3)4)
I_{DD7}	840	860	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled

2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode

3) Both ranks are in the same I_{DD} mode

4) Values for 0 °C ≤ T_{CASE} ≤ 85 °C

3.4.1 I_{DD} Test Conditions

For testing the I_{DD} parameters, the timing parameters as in **Table 23** are used.

Table 23 I_{DD} Measurement Test Condition for DDR2–667D, DDR2–533C and DDR2–400B

Parameter	Symbol	–3S	–3.7	–5	Unit	Notes
		DDR2–667D	DDR2–533C	DDR2–400B		
CAS Latency	CL_{IDD}	5	4	3	t_{CK}	
Clock Cycle Time	t_{CKIDD}	3.75	3.75	5	ns	
Active to Read or Write delay	$t_{RCD.IDD}$	15	15	15	ns	
Active to Active / Auto-Refresh command period	$t_{RC.IDD}$	60	60	55	ns	
Active bank A to Active bank B command delay	$t_{RRD.IDD}$	7.5	7.5	7.5	ns	1)
		10	10	10	ns	2)
Active to Precharge Command	$t_{RAS.MIN.IDD}$	45	45	40	ns	
	$t_{RAS.MAX.IDD}$	70000	70000	70000	ns	
Precharge Command Period	$t_{RP.IDD}$	15	15	15	ns	
Auto-Refresh to Active / Auto-Refresh command period	$t_{RFC.IDD}$	105	105	105	ns	
Average periodic Refresh interval	t_{REFI}	7.8	7.8	7.8	µs	

1) ×4 & ×8 (1 KByte page size)

2) ×16 (2 KByte page size); not on 256M component

3.4.2 On Die Termination (ODT) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A[6,2] in the EMRS(1) a “weak” or “strong” termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tri-state or driving 0 or 1, as long a ODT is enabled during a given period of time.

Table 24 ODT current per terminated pin

Parameter	Symbol	Min.	Typ.	Max.	Unit	EMRS(1) State
Enabled ODT current per DQ ODT is HIGH; Data Bus inputs are FLOATING	I_{ODTO}	5	6	7.5	mA/DQ	A6 = 0, A2 = 1
		2.5	3	3.75	mA/DQ	A6 = 1, A2 = 0
		7.5	9	11.25	mA/DQ	A6 = 1, A2 = 1
Active ODT current per DQ ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	I_{ODTT}	10	12	15	mA/DQ	A6 = 0, A2 = 1
		5	6	7.5	mA/DQ	A6 = 1, A2 = 0
		15	18	22.5	mA/DQ	A6 = 1, A2 = 0

Note: For power consumption calculations the ODT duty cycle has to be taken into account

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

Table 25 SPD codes for PC2–5300M–555, PC2–5300M–555, PC2–4200M–444, PC2–4200M–444, PC2–3200M–333 and PC2–3200M–333

Product Type		HYS64T32000HM–3S–A	HYS64T64020HM–3S–A	HYS64T32000HM–3.7–A	HYS64T64020HM–3.7–A	HYS64T32000HM–5–A	HYS64T64020HM–5–A
Organization		**256MB**	**512MB**	**256MB**	**512MB**	**256MB**	**512MB**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**2 Ranks (×16)**	**1 Rank (×16)**	**2 Ranks (×16)**
Label Code		**PC2–5300M–555**	**PC2–5300M–555**	**PC2–4200M–444**	**PC2–4200M–444**	**PC2–3200M–333**	**PC2–3200M–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08	08
3	Number of Row Addresses	0D	0D	0D	0D	0D	0D
4	Number of Column Addresses	0A	0A	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	60	61	60	61	60	61
6	Data Width	40	40	40	40	40	40
7	Not used	00	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	3D	3D	50	50
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	50	50	60	60
11	Error Correction Support (non-ECC, ECC)	00	00	00	00	00	00
12	Refresh Rate and Type	82	82	82	82	82	82
13	Primary SDRAM Width	10	10	10	10	10	10
14	Error Checking SDRAM Width	00	00	00	00	00	00

Table 25 SPD codes for PC2–5300M–555, PC2–5300M–555, PC2–4200M–444, PC2–4200M–444, PC2–3200M–333 and PC2–3200M–333 (cont'd)

Product Type		**HYS64T32000HM–3S–A**	**HYS64T64020HM–3S–A**	**HYS64T32000HM–3.7–A**	**HYS64T64020HM–3.7–A**	**HYS64T32000HM–5–A**	**HYS64T64020HM–5–A**
Organization		**256MB**	**512MB**	**256MB**	**512MB**	**256MB**	**512MB**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**2 Ranks (×16)**	**1 Rank (×16)**	**2 Ranks (×16)**
Label Code		**PC2–5300M–555**	**PC2–5300M–555**	**PC2–4200M–444**	**PC2–4200M–444**	**PC2–3200M–333**	**PC2–3200M–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
15	Not used	00	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04	04
18	Supported CAS Latencies	38	38	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	00	00	00	00
20	DIMM Type Information	08	08	08	08	08	08
21	DIMM Attributes	00	00	00	00	00	00
22	Component Attributes	03	03	01	01	01	01
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D	3D	50	50
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50	50	60	60
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	28	28	28	28	28
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D	28	28
31	Module Density per Rank	40	40	40	40	40	40
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	25	25	35	35
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	37	37	47	47
34	$t_{DS.MIN}$ [ns]	10	10	10	10	15	15
35	$t_{DH.MIN}$ [ns]	17	17	22	22	27	27
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E	28	28

Table 25 SPD codes for PC2–5300M–555, PC2–5300M–555, PC2–4200M–444, PC2–4200M–444, PC2–3200M–333 and PC2–3200M–333 (cont'd)

Product Type		HYS64T32000HM–3S–A	HYS64T64020HM–3S–A	HYS64T32000HM–3.7–A	HYS64T64020HM–3.7–A	HYS64T32000HM–5–A	HYS64T64020HM–5–A
Organization		**256MB**	**512MB**	**256MB**	**512MB**	**256MB**	**512MB**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**2 Ranks (×16)**	**1 Rank (×16)**	**2 Ranks (×16)**
Label Code		**PC2–5300M–555**	**PC2–5300M–555**	**PC2–4200M–444**	**PC2–4200M–444**	**PC2–3200M–333**	**PC2–3200M–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C	3C	37	37
42	$t_{RFC.MIN}$ [ns]	69	69	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	1E	1E	23	23
45	$t_{QHS.MAX}$ [ns]	22	22	28	28	2D	2D
46	PLL Relock Time	00	00	00	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	55	55	53	53	51	51
48	Psi(T-A) DRAM	72	72	72	72	72	72
49	ΔT_0 (DT0)	5F	5F	53	53	43	43
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	36	36	2B	2B	23	23
51	ΔT_{2P} (DT2P)	24	24	1D	1D	1D	1D
52	ΔT_{3N} (DT3N)	24	24	1D	1D	19	19
53	$\Delta T_{3P.fast}$ (DT3P fast)	29	29	23	23	1C	1C
54	$\Delta T_{3P.slow}$ (DT3P slow)	1A	1A	16	16	16	16
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	52	52	36	36	2E	2E
56	ΔT_{5B} (DT5B)	1E	1E	1C	1C	1A	1A
57	ΔT_7 (DT7)	31	31	30	30	2D	2D
58	Psi(ca) PLL	00	00	00	00	00	00
59	Psi(ca) REG	00	00	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00	00	00

Table 25 SPD codes for PC2–5300M–555, PC2–5300M–555, PC2–4200M–444, PC2–4200M–444, PC2–3200M–333 and PC2–3200M–333 (cont'd)

Product Type		**HYS64T32000HM–3S–A**	**HYS64T64020HM–3S–A**	**HYS64T32000HM–3.7–A**	**HYS64T64020HM–3.7–A**	**HYS64T32000HM–5–A**	**HYS64T64020HM–5–A**
Organization		**256MB**	**512MB**	**256MB**	**512MB**	**256MB**	**512MB**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**2 Ranks (×16)**	**1 Rank (×16)**	**2 Ranks (×16)**
Label Code		**PC2–5300M–555**	**PC2–5300M–555**	**PC2–4200M–444**	**PC2–4200M–444**	**PC2–3200M–333**	**PC2–3200M–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00	00	00
62	SPD Revision	12	12	11	11	11	11
63	Checksum of Bytes 0-62	D0	D1	C0	C1	08	09
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx	xx
73	Product Type, Char 1	36	36	36	36	36	36
74	Product Type, Char 2	34	34	34	34	34	34
75	Product Type, Char 3	54	54	54	54	54	54
76	Product Type, Char 4	33	36	33	36	33	36
77	Product Type, Char 5	32	34	32	34	32	34
78	Product Type, Char 6	30	30	30	30	30	30
79	Product Type, Char 7	30	32	30	32	30	32
80	Product Type, Char 8	30	30	30	30	30	30
81	Product Type, Char 9	48	48	48	48	48	48
82	Product Type, Char 10	4D	4D	4D	4D	4D	4D
83	Product Type, Char 11	33	33	33	33	35	35

Table 25 SPD codes for PC2–5300M–555, PC2–5300M–555, PC2–4200M–444, PC2–4200M–444, PC2–3200M–333 and PC2–3200M–333 (cont'd)

Product Type		HYS64T32000HM–3S–A	HYS64T64020HM–3S–A	HYS64T32000HM–3.7–A	HYS64T64020HM–3.7–A	HYS64T32000HM–5–A	HYS64T64020HM–5–A
Organization		**256MB**	**512MB**	**256MB**	**512MB**	**256MB**	**512MB**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**2 Ranks (×16)**	**1 Rank (×16)**	**2 Ranks (×16)**
Label Code		**PC2–5300M–555**	**PC2–5300M–555**	**PC2–4200M–444**	**PC2–4200M–444**	**PC2–3200M–333**	**PC2–3200M–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
84	Product Type, Char 12	53	53	2E	2E	41	41
85	Product Type, Char 13	41	41	37	37	20	20
86	Product Type, Char 14	20	20	41	41	20	20
87	Product Type, Char 15	20	20	20	20	20	20
88	Product Type, Char 16	20	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20	20
91	Module Revision Code	1x	1x	3x	3x	3x	3x
92	Test Program Revision Code	xx	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00	00

5 Package Outlines

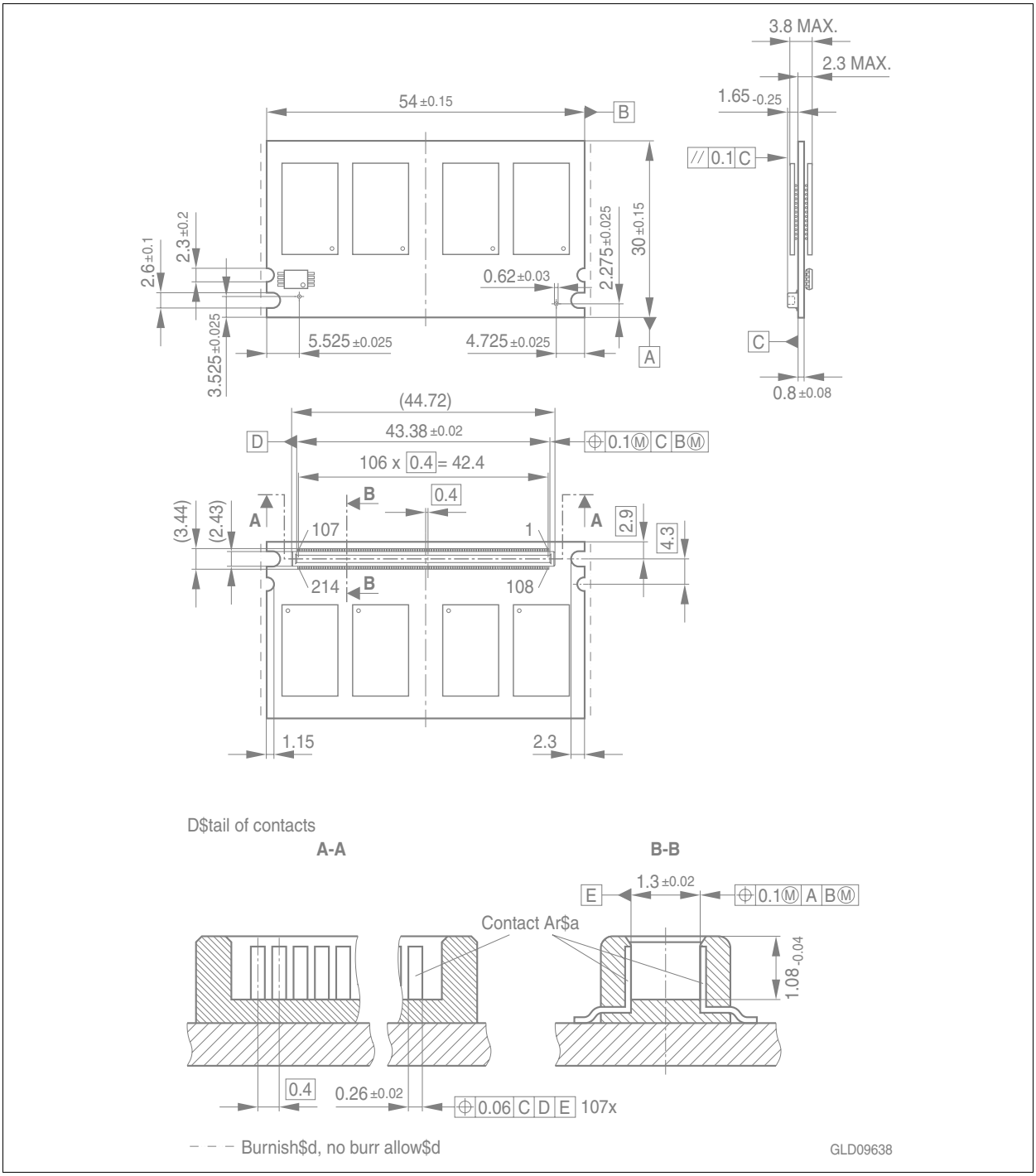

Figure 4 Package Outline Raw Card A L-DIM-214-1

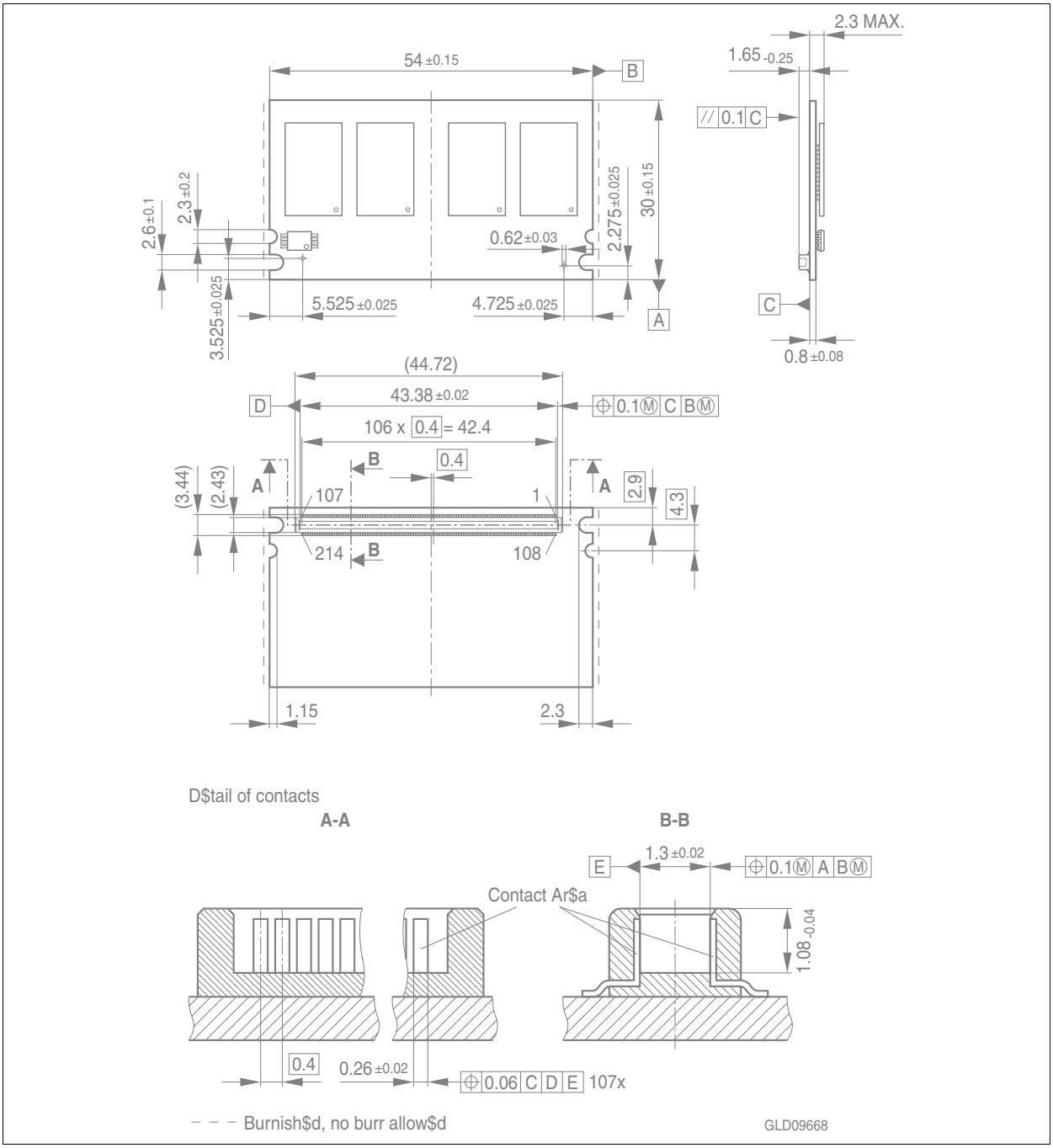

Figure 5 Package Outline Raw Card B L-DIM-214-2

6 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Infineon's nomenclature uses simple coding combined with some proprietary coding. **Table 26** provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 27** and for components in **Table 28**.

Table 26 Nomenclature Fields and Examples

Example for	Field Number										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Micro-DIMM	HYS	64	T	64	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512	16		0	A	C	–5	

Table 27 DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
10	Speed Grade	–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying "Memory Density per I/O" with "Module Data Width" and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column "Coding".

Table 28 DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL1.8
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–2.5	DDR2-800 6-6-6
		–3	DDR2-667 4-4-4
		–3S	DDR2-667 5-5-5
		–3.7	DDR2-533 4-4-4
		–5	DDR2-400 3-3-3

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