

HYS64T32000HDL-[2.5/.../5]-B  
HYS64T64020HDL-[2.5/.../5]-B  
HYS64T128021HDL-[2.5/.../5]-B

200-Pin SO-DIMM DDR2 SDRAM Modules

DDR2 SDRAM  
SO-DIMM SDRAM  
RoHS Compliant

Memory Products



Never stop thinking.

**Edition 2005-06**

**Published by Infineon Technologies AG,  
St.-Martin-Strasse 53,  
81669 München, Germany**

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Revision History: 2005-06, Rev 1.00

Previous Version:

Page	Subjects (major changes since last revision)
	Final data sheet

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## 200-Pin SO-DIMM DDR2 SDRAM Modules DDR2 SDRAM

HYS64T32000HDL-[2.5/.../5]-B  
HYS64T64020HDL-[2.5/.../5]-B  
HYS64T128021HDL-[2.5/.../5]-B

## 1 Overview

This chapter gives an overview of the 200-Pin SO-DIMM DDR2 SDRAM Modules product family and describes its main characteristics.

### 1.1 Features

- 200-Pin PC2-6400, PC2-5300, PC2-4200 and PC2-3200 DDR2 SDRAM memory modules for use as main memory when installed in systems such as mobile personal computers.
- 32M × 64, 64M × 64 and 128M × 64 module organization, and 32M × 16, 64M × 8 chip organization
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Built with 512-Mbit DDR2 SDRAMs in P-TFBGA-84 and P-TFBGA-60 chipsize packages
- Programmable CAS Latencies (3, 4 and 5), Burst Length (8 & 4) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- Programmable self refresh rate via EMRS2 setting
- Programmable partial array refresh via EMRS2 settings
- DCC enabling via EMRS2 setting
- All inputs and outputs SSTL\_1.8 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E<sup>2</sup>PROM
- UDIMM and EDIMM Dimensions (nominal): 30 mm high, 133.35 mm wide
- Based on standard reference layouts Raw Card "A", "C", "E"
- RoHS compliant products<sup>1)</sup>
- All speed grades faster than DDR400 comply with DDR400 timing specifications.

**Table 1 Performance**

Product Type Speed Code			-2.5	-3	-3S	Unit
Speed Grade			PC2-6400 6-6-6	PC2-5300 4-4-4	PC2-5300 5-5-5	—
max. Clock Frequency	@CL6	$f_{CK6}$	400	333	333	
	@CL5	$f_{CK5}$	333	333	333	MHz
	@CL4	$f_{CK4}$	266	333	266	MHz
	@CL3	$f_{CK3}$	200	200	200	MHz
min. RAS-CAS-Delay		$t_{RCD}$	15	12	15	ns
min. Row Precharge Time		$t_{RP}$	15	12	15	ns
min. Row Active Time		$t_{RAS}$	45	45	45	ns
min. Row Cycle Time		$t_{RC}$	60	57	60	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.



**Table 2 Performance**

Product Type Speed Code			-3.7	-5	Unit
Speed Grade			PC2-4200 4-4-4	PC2-3200 3-3-3	—
max. Clock Frequency	@CL5	$f_{CK5}$	266	200	MHz
	@CL4	$f_{CK4}$	266	200	MHz
	@CL3	$f_{CK3}$	200	200	MHz
min. RAS-CAS-Delay		$t_{RCD}$	15	15	ns
min. Row Precharge Time		$t_{RP}$	15	15	ns
min. Row Active Time		$t_{RAS}$	45	40	ns
min. Row Cycle Time		$t_{RC}$	60	55	ns

## 1.2 Description

The INFINEON HYS64T[32/64/128]xxxHDL-[2.5/.../5]-B module family are small outline DIMM modules “SO-DIMMs” with 30,0 mm height based on DDR2 technology. DIMMs are available as non-ECC modules in 32M × 64 (256 MB), 64M × 64 (512 MB) and 128M × 64(1 GB) organization and density, intended for mounting into 200-pin connector sockets.

The memory array is designed with 512-Mbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E<sup>2</sup>PROM device using the 2-pin I<sup>2</sup>C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.


**Table 3 Ordering Information for RoHS Compliant Products**

Product Type <sup>1)</sup>	Compliance Code <sup>2)</sup>	Description	SDRAM Technology
<b>PC2-6400</b>			
HYS64T32000HDL-2.5-B	256 MB 1R×16 PC2-6400S-666-12-C0	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64020HDL-2.5-B	512 MB 2R×16 PC2-6400S-666-12-A0	2 Rank, Non-ECC	512 Mbit (×16)
HYS64T128021HDL-2.5-B	1 GB 2Rx8 PC2-6400S-666-12-E0	2 Rank, Non-ECC	512 Mbit (×8)
<b>PC2-5300</b>			
HYS64T32000HDL-3-B	256 MB 1R×16 PC2-5300S-444-12-C0	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64020HDL-3-B	512 MB 1R×16 PC2-5300S-444-12-A0	2 Rank, Non-ECC	512 Mbit (×16)
HYS64T128021HDL-3-B	1 GB 2Rx8 PC2-5300S-444-12-E0	2 Rank, Non-ECC	512 Mbit (×8)
<b>PC2-5300</b>			
HYS64T32000HDL-3S-B	256 MB 1R×16 PC2-5300S-555-12-C0	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64020HDL-3S-B	512 MB 1R×16 PC2-5300S-555-12-A0	2 Rank, Non-ECC	512 Mbit (×16)
HYS64T128021HDL-3S-B	1 GB 2Rx8 PC2-5300S-555-12-E0	2 Rank, Non-ECC	512 Mbit (×8)
<b>PC2-4200</b>			
HYS64T32000HDL-3.7-B	256 MB 1R×16 PC2-4200S-444-12-C0	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64020HDL-3.7-B	512 MB 1R×16 PC2-4200S-444-12-A0	2 Rank, Non-ECC	512 Mbit (×16)
HYS64T128021HDL-3.7-B	1 GB 2Rx8 PC2-4200S-444-12-E0	2 Rank, Non-ECC	512 Mbit (×8)
<b>PC2-3200</b>			
HYS64T32000HDL-5-B	256 MB 1R×16 PC2-3200S-333-12-C0	1 Rank, Non-ECC	512 Mbit (×16)

**Table 3 Ordering Information for RoHS Compliant Products (cont'd)**

Product Type <sup>1)</sup>	Compliance Code <sup>2)</sup>	Description	SDRAM Technology
HYS64T64020HDL-5-B	512 MB 1R×16 PC2-3200S-333-12-A0	2 Rank, Non-ECC	512 Mbit (×16)
HYS64T128021HDL-5-B	1 GB 2Rx8 PC2-3200S-333-12-E0	2 Rank, Non-ECC	512 Mbit (×8)

- 1) All part numbers end with a place code, designating the silicon die revision. Example: HYS64T16000HU-5-A, indicating Rev. "B" dies are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see [Chapter 6](#) of this data sheet.
- 2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC2-4200U-444-11-A0", where 4200U means Unbuffered DIMM modules with 4.26 GB/sec Module Bandwidth and "444-11" means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.1 and produced on the Raw Card "C".

**Table 4 Address Format**

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits	Raw Card
256 MByte	32M × 64	1	Non-ECC	4	13/2/10	C
512 MByte	64M × 64	2	Non-ECC	8	13/2/10	A
1 GByte	128M × 64	2	Non-ECC	16	14/2/10	E

**Table 5 Components on Modules <sup>1)</sup>**

Product Type <sup>2)</sup>	DRAM Components <sup>2)</sup>	DRAM Density	DRAM Organisation
HYS64T32000HU	HYB18T512160BF	512 Mbit	32M × 16
HYS64T64020HU	HYB18T512160BF	512 Mbit	64M × 16
HYS64T128021HU	HYB18T512800BF	512 Mbit	64M × 8

- 1) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.
- 2) Green Product

## 2 Pin Configurations and Block Diagrams

### 2.1 Pin Configuration

The pin configuration of the Small Outline DDR2 SDRAM DIMM is listed by function in [Table 6](#) (200 pins). The abbreviations used in columns Pin and Buffer Type are explained in [Table 7](#) and [Table 8](#) respectively. The pin numbering is depicted in [Figure 1](#)

**Table 6 Pin Configuration of SO-DIMM**

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
<b>Clock Signals</b>				
30	CK0	I	SSTL	<b>Clock Signals 2:0, Complement Clock Signals 2:0</b> The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
164	CK1	I	SSTL	
32	CK0	I	SSTL	
166	CK1	I	SSTL	
79	CKE0	I	SSTL	<b>Clock Enable Rank 1:0</b> Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE LOW initiates the Power Down Mode or the Self Refresh Mode. <i>Note: 2 Ranks module</i>
80	CKE1	I	SSTL	
	NC	NC	—	
<b>Control Signals</b>				
110	S0	I	SSTL	<b>Chip Select Rank 1:0</b> Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by S0; Rank 1 is selected by S1. Ranks are also called "Physical banks".2 Ranks module
115	S1	I	SSTL	
	NC	NC	—	
108	RAS	I	SSTL	<b>Row Address Strobe</b> When sampled at the cross point of the rising edge of CK, and falling edge of CK, RAS, CAS and WE define the operation to be executed by the SDRAM.
113	CAS	I	SSTL	<b>Column Address Strobe</b>
109	WE	I	SSTL	<b>Write Enable</b>



Table 6 Pin Configuration of SO-DIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
<b>Address Signals</b>				
107	BA0	I	SSTL	<b>Bank Address Bus 2:0</b> Selects which DDR2 SDRAM internal bank of four or eight is activated.
106	BA1	I	SSTL	
85	BA2	I	SSTL	<b>Bank Address Bus 2</b> Greater than 512Mb DDR2 SDRAMs
	NC	NC	SSTL	<b>Less than 1Gb DDR2 SDRAMs</b>
102	A0	I	SSTL	<b>Address Bus 12:0</b> During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{CK}$ . During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$ . In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is LOW, then BA0-BAn are used to define which bank to precharge.
101	A1	I	SSTL	
100	A2	I	SSTL	
99	A3	I	SSTL	
98	A4	I	SSTL	
97	A5	I	SSTL	
94	A6	I	SSTL	
92	A7	I	SSTL	
93	A8	I	SSTL	
91	A9	I	SSTL	
105	A10	I	SSTL	
	AP	I	SSTL	
90	A11	I	SSTL	
89	A12	I	SSTL	<b>Address Signal 12</b> <i>Note: Module based on 256 Mbit or larger dies</i>
116	A13	I	SSTL	<b>Address Signal 13</b> <i>Note: 1 Gbit based module</i>
	NC	NC	—	<b>Not Connected</b> <i>Note: Module based on 512 Mbit or smaller dies</i>
<b>Data Signals</b>				
5	DQ0	I/O	SSTL	<b>Data Bus 63:0</b> <i>Note: Data Input/Output pins</i>
7	DQ1	I/O	SSTL	
17	DQ2	I/O	SSTL	
19	DQ3	I/O	SSTL	
4	DQ4	I/O	SSTL	
6	DQ5	I/O	SSTL	
14	DQ6	I/O	SSTL	
16	DQ7	I/O	SSTL	
23	DQ8	I/O	SSTL	
25	DQ9	I/O	SSTL	
35	DQ10	I/O	SSTL	
37	DQ11	I/O	SSTL	

**Table 6 Pin Configuration of SO-DIMM (cont'd)**

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
20	DQ12	I/O	SSTL	<b>Data Bus 63:0</b> Data Input/Output pins
22	DQ13	I/O	SSTL	
36	DQ14	I/O	SSTL	
38	DQ15	I/O	SSTL	
43	DQ16	I/O	SSTL	
45	DQ17	I/O	SSTL	
55	DQ18	I/O	SSTL	
57	DQ19	I/O	SSTL	
44	DQ20	I/O	SSTL	
46	DQ21	I/O	SSTL	
56	DQ22	I/O	SSTL	
58	DQ23	I/O	SSTL	
61	DQ24	I/O	SSTL	
63	DQ25	I/O	SSTL	
73	DQ26	I/O	SSTL	
75	DQ27	I/O	SSTL	
62	DQ28	I/O	SSTL	
64	DQ29	I/O	SSTL	
74	DQ30	I/O	SSTL	
76	DQ31	I/O	SSTL	
123	DQ32	I/O	SSTL	
125	DQ33	I/O	SSTL	
135	DQ34	I/O	SSTL	
137	DQ35	I/O	SSTL	
124	DQ36	I/O	SSTL	
126	DQ37	I/O	SSTL	
134	DQ38	I/O	SSTL	
136	DQ39	I/O	SSTL	
141	DQ40	I/O	SSTL	
143	DQ41	I/O	SSTL	
151	DQ42	I/O	SSTL	
153	DQ43	I/O	SSTL	
140	DQ44	I/O	SSTL	
142	DQ45	I/O	SSTL	
152	DQ46	I/O	SSTL	
154	DQ47	I/O	SSTL	
157	DQ48	I/O	SSTL	
159	DQ49	I/O	SSTL	
173	DQ50	I/O	SSTL	
175	DQ51	I/O	SSTL	

**Table 6 Pin Configuration of SO-DIMM (cont'd)**

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
158	DQ52	I/O	SSTL	<b>Data Bus 63:0</b>
160	DQ53	I/O	SSTL	
174	DQ54	I/O	SSTL	
176	DQ55	I/O	SSTL	
179	DQ56	I/O	SSTL	
181	DQ57	I/O	SSTL	
189	DQ58	I/O	SSTL	
191	DQ59	I/O	SSTL	
180	DQ60	I/O	SSTL	
182	DQ61	I/O	SSTL	
192	DQ62	I/O	SSTL	
194	DQ63	I/O	SSTL	

**Data Strobe Signals**

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
13	DQS0	I/O	SSTL	<b>Data Strobe Bus 7:0</b> The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$ . If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to $V_{SS}$ and DDR2 SDRAM mode registers programmed appropriately.
11	$\overline{DQS0}$	I/O	SSTL	
31	DQS1	I/O	SSTL	
29	$\overline{DQS1}$	I/O	SSTL	
51	DQS2	I/O	SSTL	
49	$\overline{DQS2}$	I/O	SSTL	
70	DQS3	I/O	SSTL	
68	$\overline{DQS3}$	I/O	SSTL	
131	DQS4	I/O	SSTL	
129	$\overline{DQS4}$	I/O	SSTL	
148	DQS5	I/O	SSTL	
146	$\overline{DQS5}$	I/O	SSTL	
169	DQS6	I/O	SSTL	
167	$\overline{DQS6}$	I/O	SSTL	
188	DQS7	I/O	SSTL	
186	$\overline{DQS7}$	I/O	SSTL	

**Data Mask Signals**

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
10	DM0	I	SSTL	<b>Data Mask Bus 7:0</b> The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect.
26	DM1	I	SSTL	
52	DM2	I	SSTL	
67	DM3	I	SSTL	
130	DM4	I	SSTL	
147	DM5	I	SSTL	
170	DM6	I	SSTL	
185	DM7	I	SSTL	

**EEPROM**

Pin Configurations and Block Diagrams

**Table 6 Pin Configuration of SO-DIMM (cont'd)**

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
197	SCL	I	CMOS	<b>Serial Bus Clock</b> This signal is used to clock data into and out of the SPD EEPROM.
195	SDA	I/O	OD	<b>Serial Bus Data</b> This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to $V_{DDSPD}$ on the motherboard to act as a pull-up.
198	SA0	I	CMOS	<b>Serial Address Select Bus 2:0</b> Address pins used to select the Serial Presence Detect base address.
200	SA1	I	CMOS	
<b>Power Supplies</b>				
1	$V_{REF}$	AI	—	<b>I/O Reference Voltage</b> Reference voltage for the SSTL-18 inputs.
199	$V_{DDSPD}$	PWR	—	<b>EEPROM Power Supply</b> Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
81,82,87,88,95,96,103,104,111,112,117,118	$V_{DD}$	PWR	—	<b>Power Supply</b> Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
2,3,8,9,12,15,18,21,24,27,28,33,34,39,40,41,42,47,48,53,54,59,60,65,66,71,72,77,78,121,122,127,128,132,133,138,139,144,145,149,150,155,156,161,162,165,171,172,177,178,183,184,187,190,193,196	$V_{SS}$	GND	—	<b>Ground Plane</b> Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
<b>Other Pins</b>				
114	ODT0	I	SSTL	<b>On-Die Termination Control 1:0</b>
119	ODT1	I	SSTL	<b>On-Die Termination Control 1</b> Asserts on-die termination for DQ, DM, DQS, and DQS signals if enabled via the DDR2 SDRAM mode register. <i>Note: 2 Rank modules</i>
	NC	NC	—	<b>Not Connected</b> <i>Note: 1 Rank modules</i>
50,69,83,84,120,163,168	NC	NC	—	<b>Not connected</b> Pins not connected on Infineon SO-DIMMs

**Table 7 Abbreviations for Pin Type**

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.

**Table 7 Abbreviations for Pin Type (cont'd)**

Abbreviation	Description
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

**Table 8 Abbreviations for Buffer Type**

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

Pin Configurations and Block Diagrams

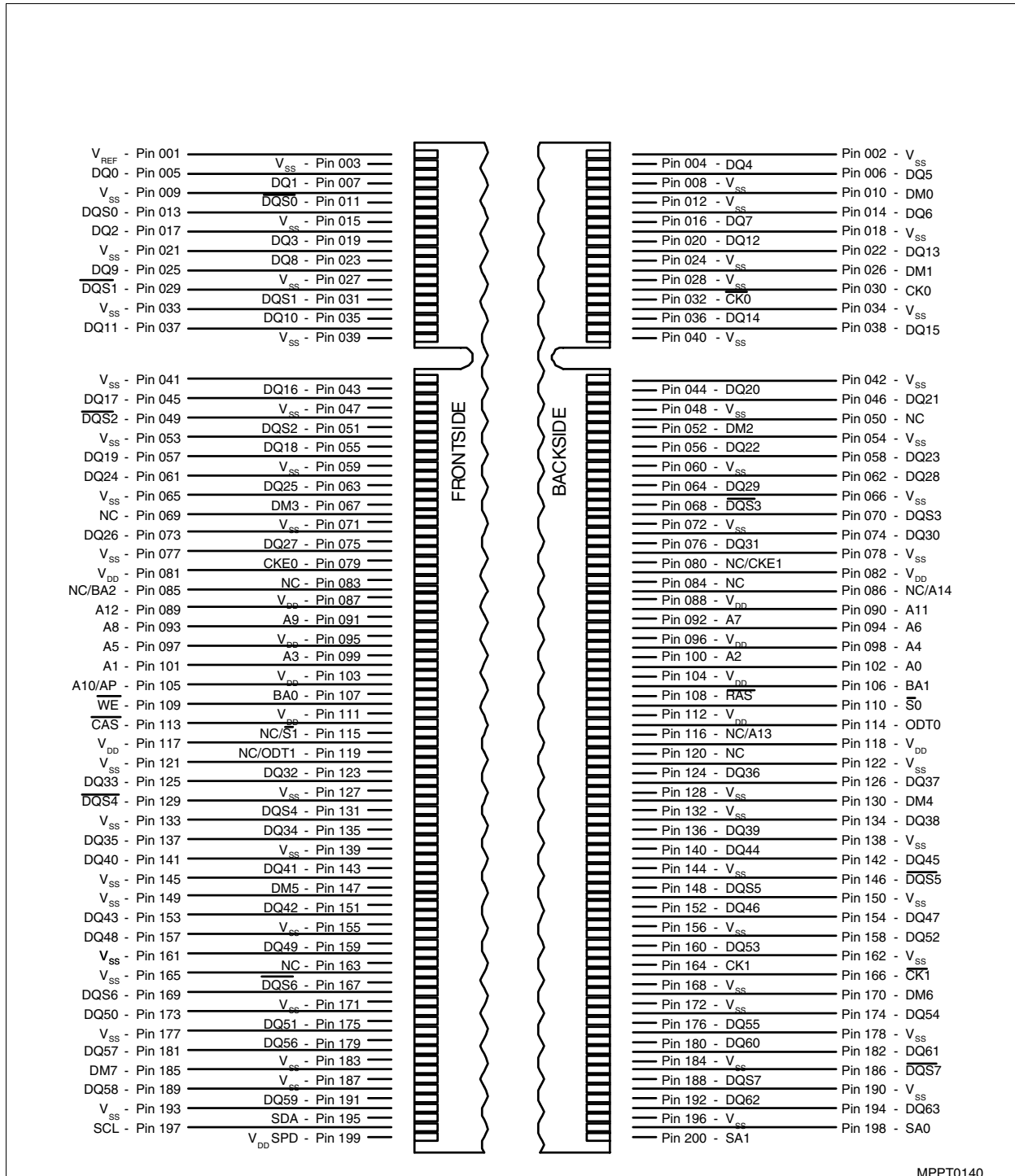


Figure 1 Pin Configuration SO-DIMM (200 Pin)

MPPT0140



## 2.2 Block Diagrams

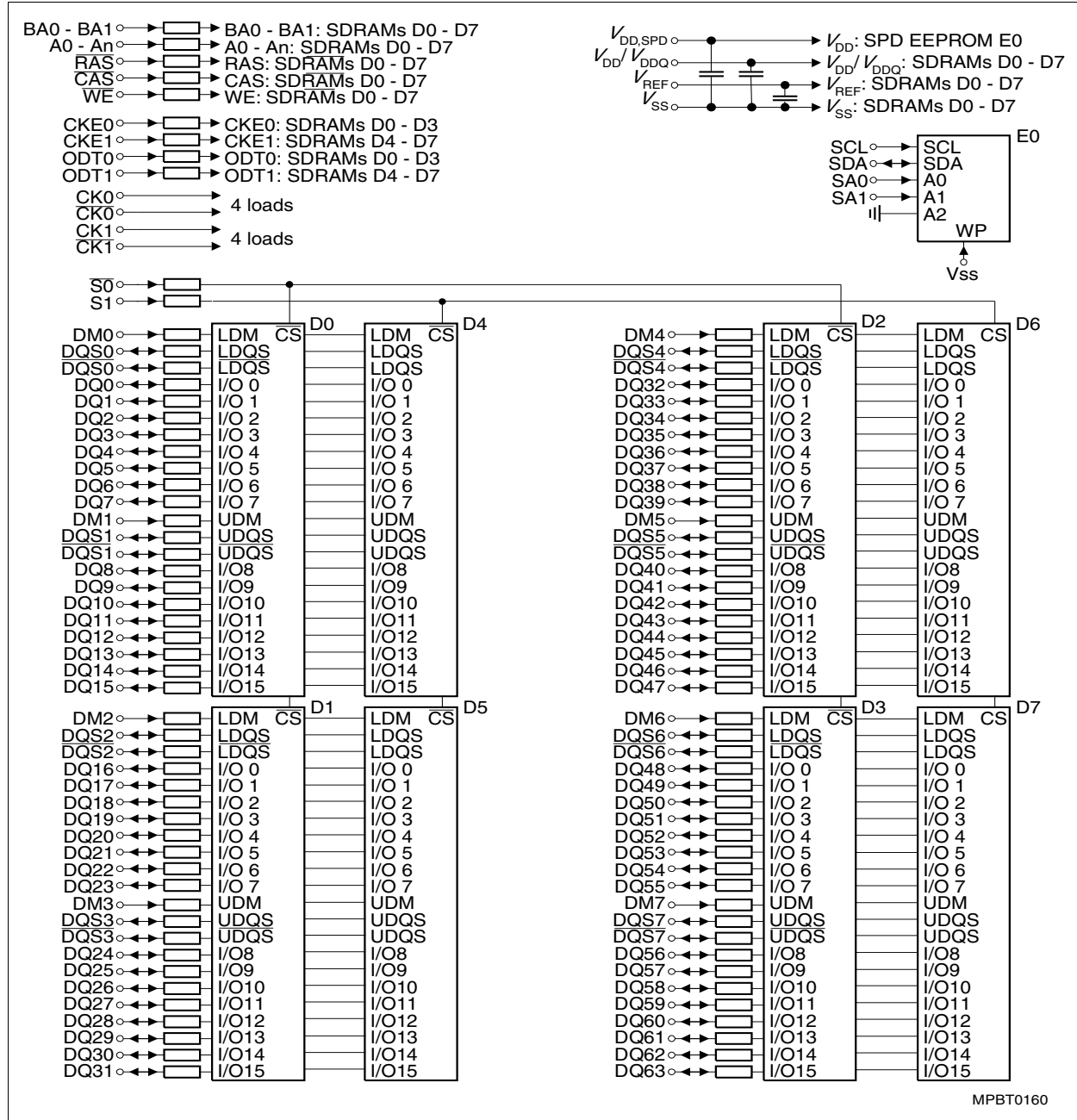


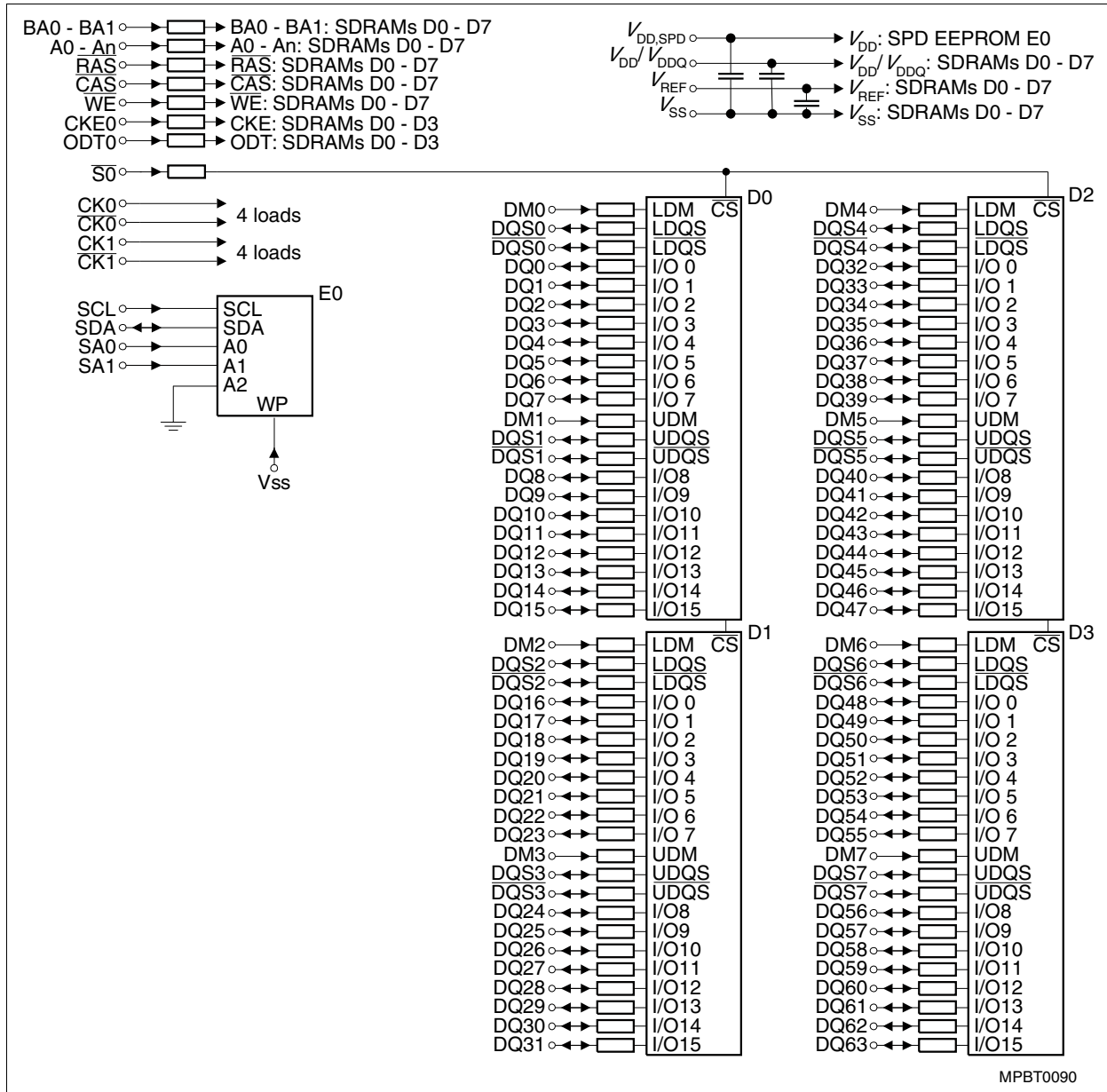
Figure 2 Block Diagram Raw Card A SO-DIMM (x64, 2 Ranks, x16)

### Notes

1. DQ, DQS, DM resistors are  $22 \Omega \pm 5\%$

2.  $\overline{S0}$ ,  $\overline{S1}$ ,  $\overline{BA_n}$ ,  $\overline{A_n}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{ODT0}$ ,  $\overline{ODT1}$ ,  $\overline{CKE0}$ ,  $\overline{CKE1}$  resistors are  $3 \Omega \pm 5\%$

**Pin Configurations and Block Diagrams**



**Figure 3 Block Diagram Raw Card C SO-DIMM (x64, 1Rank, x16)**

Note:

1. DQ, DQS, DM resistors are  $22 \Omega \pm 5 \%$
2.  $\overline{S0}$ ,  $\overline{S1}$ ,  $\overline{BA_n}$ ,  $\overline{An}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , ODT0, ODT1, CKE0, CKE1 resistors are  $3 \Omega \pm 5 \%$

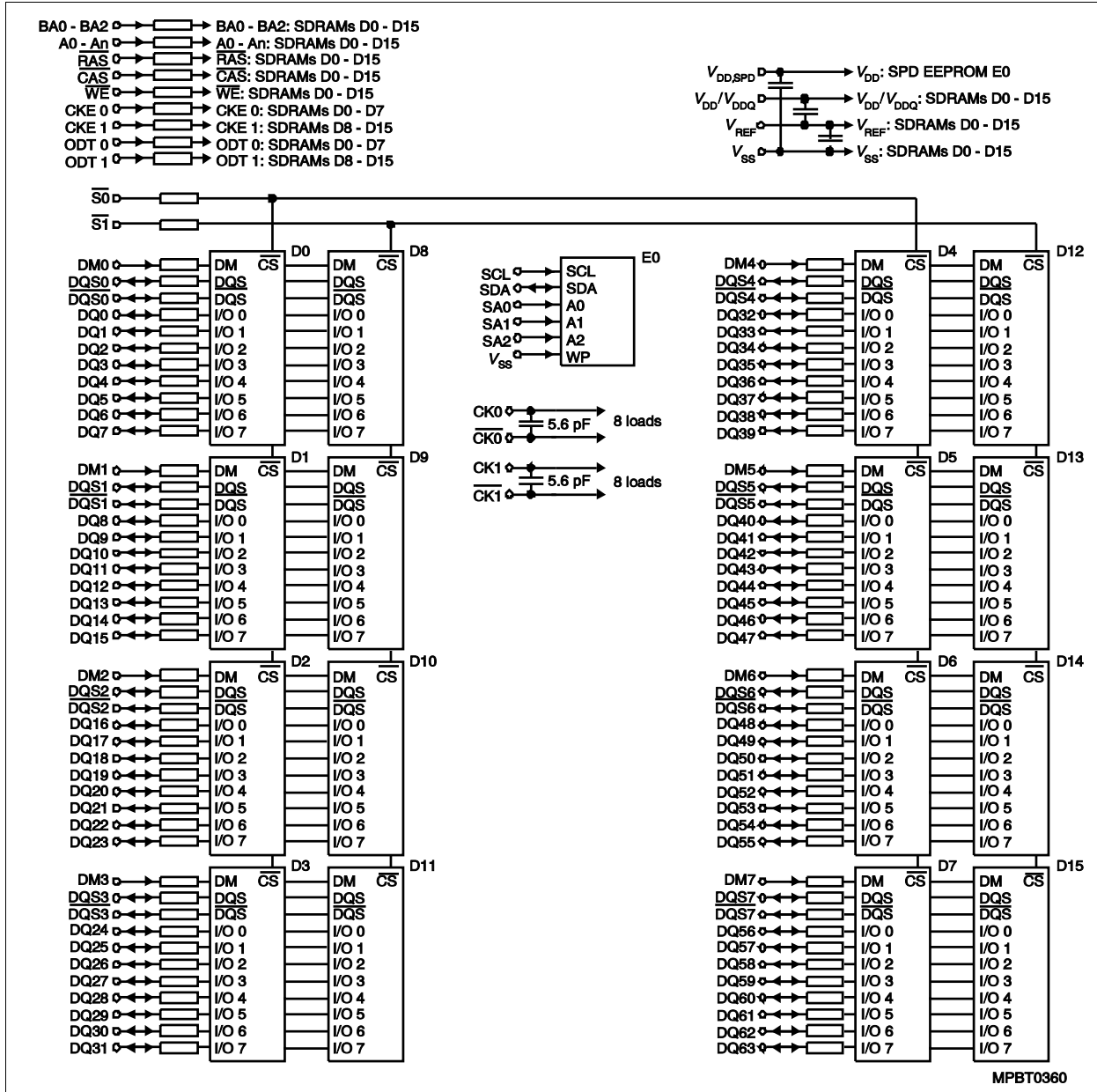


Figure 4 Block Diagram Raw Card E SO-DIMM (x64, 2 Ranks, x8)

Notes

1. DQ, DQS, DM resistors are  $22 \Omega \pm 5 \%$

2.  $\overline{S0}$ ,  $\overline{S1}$ ,  $\overline{BA}n$ ,  $\overline{A}n$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{ODT0}$ ,  $\overline{ODT1}$ ,  $\overline{CKE0}$ ,  $\overline{CKE1}$  resistors are  $3 \Omega \pm 5 \%$

### 3 Electrical Characteristics

#### 3.1 Absolute Maximum Ratings

**Table 9 Absolute Maximum Ratings**

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Voltage on any pins relative to $V_{SS}$	$V_{IN}, V_{OUT}$	- 0.5	2.3	V	1)
Voltage on $V_{DD}$ relative to $V_{SS}$	$V_{DD}$	- 1.0	2.3	V	1)
Voltage on $V_{DDQ}$ relative to $V_{SS}$	$V_{DDQ}$	- 0.5	2.3	V	1)
Storage Humidity (without condensation)	$H_{STG}$	5	95	%	1)

- 1) Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### 3.2 DC Operating Conditions

**Table 10 Operating Conditions**

Parameter	Symbol	Values		Unit	Notes
		Min.	Max.		
Operating temperature (ambient)	$T_{OPR}$	0	+65	°C	
DRAM Case Temperature	$T_{CASE}$	0	+95	°C	1)2)3)4)
Storage Temperature	$T_{STG}$	- 50	+100	°C	
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	5)
Operating Humidity (relative)	$H_{OPR}$	10	90	%	

- 1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.  
 2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported  
 3) Above 85 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to  $t_{REFI} = 3.9 \mu s$   
 4) For Self Refresh Operation above 85°C it is necessary to set extended mode register 2 (EMR(2)) Bit A7 to "1" to enable the High Temperature Self Refresh option.  
 5) Up to 3000 m.

**Table 11 Recommended DC Operating Conditions (SSTL\_18)**

Symbol	Parameter	Rating			Unit	Notes
		Min.	Typ.	Max.		
$V_{DD}$	Supply Voltage	1.7	1.8	1.9	V	1)
$V_{DDDL}$	Supply Voltage for DLL	1.7	1.8	1.9	V	1)
$V_{DDQ}$	Supply Voltage for Output	1.7	1.8	1.9	V	1)
$V_{REF}$	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)3)
$V_{TT}$	Termination Voltage	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V	4)

- 1)  $V_{DDQ}$  tracks with  $V_{DD}$ ,  $V_{DDDL}$  tracks with  $V_{DD}$ . AC parameters are measured with  $V_{DD}$ ,  $V_{DDQ}$  and  $V_{DDDL}$  tied together.
- 2) The value of  $V_{REF}$  may be selected by the user to provide optimum noise margin in the system. Typically the value of  $V_{REF}$  is expected to be about  $0.5 \times V_{DDQ}$  of the transmitting device and  $V_{REF}$  is expected to track variations in  $V_{DDQ}$ .
- 3) Peak to peak ac noise on  $V_{REF}$  may not exceed  $\pm 2\% V_{REF}$  (dc)
- 4)  $V_{TT}$  is not applied directly to the device.  $V_{TT}$  is a system supply for signal termination resistors, is expected to be set equal to  $V_{REF}$ , and must track variations in die dc level of  $V_{REF}$ .

### 3.3 AC Characteristics

#### 3.3.1 Speed Grade Definitions

All Speed grades faster than DDR2-DDR400B comply with DDR2-DDR400B timing specifications ( $t_{CK} = 5ns$  with  $t_{RAS} = 40ns$ ).

List of Speed Grade Definition tables:

- [Table 12 “Speed Grade Definition Speed Bins DDR2-800E” on Page 19](#)
- [Table 13 “Speed Grade Definition Speed Bins for DDR2-667” on Page 20](#)
- [Table 14 “Speed Grade Definition Speed Bins for DDR2-533 and DDR2-400” on Page 20](#)

**Table 12 Speed Grade Definition Speed Bins DDR2-800E**

Speed Grade		DDR2-800E			Unit	Note
IFX Sort Name		-2.5				
CAS-RCD-RP latencies		6-6-6			$t_{CK}$	
Parameter	Symbol	Min.	Max.	—		
Clock Frequency	@ CL = 3	$t_{CK}$	5	8	ns	1)2)3)4)
	@ CL = 4	$t_{CK}$	3.75	8	ns	1)2)3)4)
	@ CL = 5	$t_{CK}$	3	8	ns	1)2)3)4)
	@ CL = 6	$t_{CK}$	2.5	8	ns	1)2)3)4)
Row Active Time	$t_{RAS}$	45	70000	ns	1)2)3)4)5)	
Row Cycle Time	$t_{RC}$	60	—	ns	1)2)3)4)	
RAS-CAS-Delay	$t_{RCD}$	15	—	ns	1)2)3)4)	
Row Precharge Time	$t_{RP}$	15	—	ns	1)2)3)4)	

- 1) Timings are guaranteed with CK/CK differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
- 2) The CK/ $\overline{CK}$  input reference level (for timing reference to CK/ $\overline{CK}$ ) is the point at which CK and  $\overline{CK}$  cross. The DQS /  $\overline{DQS}$ , RDQS /  $\overline{RDQS}$ , input reference level is the crosspoint when in differential strobe mode

Electrical Characteristics

- 3) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $CKE = 0.2 \times V_{DDQ}$  is recognized as low.
- 4) The output timing reference voltage level is  $V_{TT}$ .
- 5)  $t_{RAS,MAX}$  is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to  $9 \times t_{REFI}$ .

**Table 13 Speed Grade Definition Speed Bins for DDR2-667**

Speed Grade			DDR2-667C		DDR2-667D		Unit	Note
IFX Sort Name			-3		-3S			
CAS-RCD-RP latencies			4-4-4		5-5-5		$t_{CK}$	
Parameter		Symbol	Min.	Max.	Min.	Max.		—
Clock Frequency	@ CL = 3	$t_{CK}$	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	$t_{CK}$	3	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	$t_{CK}$	3	8	3	8	ns	1)2)3)4)
Row Active Time		$t_{RAS}$	45	70000	45	70000	ns	1)2)3)4)5)
Row Cycle Time		$t_{RC}$	57	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		$t_{RCD}$	12	—	15	—	ns	1)2)3)4)
Row Precharge Time		$t_{RP}$	12	—	15	—	ns	1)2)3)4)

- 1) Timings are guaranteed with CK/CK differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
- 2) The CK/ $\overline{CK}$  input reference level (for timing reference to CK/ $\overline{CK}$ ) is the point at which CK and  $\overline{CK}$  cross. The DQS/ $\overline{DQS}$ , RDQS/ $\overline{RDQS}$ , input reference level is the crosspoint when in differential strobe mode
- 3) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $CKE = 0.2 \times V_{DDQ}$  is recognized as low.
- 4) The output timing reference voltage level is  $V_{TT}$ .
- 5)  $t_{RAS,MAX}$  is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to  $9 \times t_{REFI}$ .

**Table 14 Speed Grade Definition Speed Bins for DDR2-533 and DDR2-400**

Speed Grade			DDR2-533C		DDR2-400B		Unit	Note
IFX Sort Name			-3.7		-5			
CAS-RCD-RP latencies			4-4-4		3-3-3		$t_{CK}$	
Parameter		Symbol	Min.	Max.	Min.	Max.		—
Clock Frequency	@ CL = 3	$t_{CK}$	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	$t_{CK}$	3.75	8	5	8	ns	1)2)3)4)
	@ CL = 5	$t_{CK}$	3.75	8	5	8	ns	1)2)3)4)
Row Active Time		$t_{RAS}$	45	70000	40	70000	ns	1)2)3)4)5)
Row Cycle Time		$t_{RC}$	60	—	55	—	ns	1)2)3)4)
RAS-CAS-Delay		$t_{RCD}$	15	—	15	—	ns	1)2)3)4)
Row Precharge Time		$t_{RP}$	15	—	15	—	ns	1)2)3)4)

- 1) Timings are guaranteed with CK/CK differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
- 2) The CK/ $\overline{CK}$  input reference level (for timing reference to CK/ $\overline{CK}$ ) is the point at which CK and  $\overline{CK}$  cross. The DQS /  $\overline{DQS}$ , RDQS /  $\overline{RDQS}$ , input reference level is the crosspoint when in differential strobe mode



- 3) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $CKE = 0.2 \times V_{DDQ}$  is recognized as low.
- 4) The output timing reference voltage level is  $V_{TT}$ .
- 5)  $t_{RAS,MAX}$  is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to  $9 \times t_{REFI}$ .

### 3.3.2 AC Timing Parameters

List of Timing Parameters for DDR2-800, DDR2-667([Table 15](#)), and DDR2-533, DDR2-400([Table 16](#))

**Table 15 Timing Parameter by Speed Grade - DDR2-800 & DDR2-667**

Parameter	Symbol	DDR2-800		DDR2-667		Unit	Notes <sup>1)</sup>
		Min.	Max.	Min.	Max.		
DQ output access time from CK / CK	$t_{AC}$	-400	+400	-450	+450	ps	
CAS A to CAS B command period	$t_{CCD}$	2	—	2	—	$t_{CK}$	
CK, CK high-level width	$t_{CH}$	0.45	0.55	0.45	0.55	$t_{CK}$	
CKE minimum high and low pulse width	$t_{CKE}$	3	—	3	—	$t_{CK}$	
CK, CK low-level width	$t_{CL}$	0.45	0.55	0.45	0.55	$t_{CK}$	
Auto-Precharge write recovery + precharge time	$t_{DAL}$	WR + $t_{RP}$	—	WR + $t_{RP}$	—	$t_{CK}$	
Minimum time clocks remain ON after CKE asynchronously drops LOW	$t_{DELAY}$	$t_{IS} + t_{CK} + t_{IH}$	—	$t_{IS} + t_{CK} + t_{IH}$	—	ns	
DQ and DM input hold time (differential data strobe)	$t_{DH}(\text{base})$	125	—	175	—	ps	
DQ and DM input hold time (single ended data strobe)	$t_{DH1}(\text{base})$	—	—	—	—	ps	
DQ and DM input pulse width (each input)	$t_{DIPW}$	0.35	—	0.35	—	$t_{CK}$	
DQS output access time from CK / CK	$t_{DQSCK}$	-350	+350	-400	+400	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	$t_{CK}$	
DQS-DQ skew (for DQS & associated DQ signals)	$t_{DQSQ}$	—	200	—	240	ps	
Write command to 1st DQS latching transition	$t_{DQSS}$	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	$t_{CK}$	
DQ and DM input setup time (differential data strobe)	$t_{DS}(\text{base})$	50	—	100	—	ps	
DQ and DM input setup time (single ended data strobe)	$t_{DS1}(\text{base})$	—	—	—	—	ps	
DQS falling edge hold time from CK (write cycle)	$t_{DSH}$	0.2	—	0.2	—	$t_{CK}$	
DQS falling edge to CK setup time (write cycle)	$t_{DSS}$	0.2	—	0.2	—	$t_{CK}$	
Clock half period	$t_{HP}$	MIN. ( $t_{CL}, t_{CH}$ )		MIN. ( $t_{CL}, t_{CH}$ )			

**Table 15 Timing Parameter by Speed Grade - DDR2-800 & DDR2-667 (cont'd)**

Parameter	Symbol	DDR2-800		DDR2-667		Unit	Notes <sup>1)</sup>
		Min.	Max.	Min.	Max.		
Data-out high-impedance time from CK / $\overline{\text{CK}}$	$t_{\text{HZ}}$	—	$t_{\text{AC.MAX}}$	—	$t_{\text{AC.MAX}}$	ps	
Address and control input hold time	$t_{\text{IH}}(\text{base})$	250	—	275	—	ps	
Address and control input pulse width (each input)	$t_{\text{IPW}}$	0.6	—	0.6	—	$t_{\text{CK}}$	
Address and control input setup time	$t_{\text{IS}}(\text{base})$	175	—	200	—	ps	
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{\text{LZ}}(\text{DQ})$	$2 \times t_{\text{AC.MIN}}$	$t_{\text{AC.MAX}}$	$2 \times t_{\text{AC.MIN}}$	$t_{\text{AC.MAX}}$	ps	
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{\text{LZ}}(\text{DQS})$	$t_{\text{AC.MIN}}$	$t_{\text{AC.MAX}}$	$t_{\text{AC.MIN}}$	$t_{\text{AC.MAX}}$	ps	
Mode register set command cycle time	$t_{\text{MRD}}$	2	—	2	—	$t_{\text{CK}}$	
OCD drive mode output delay	$t_{\text{OIT}}$	0	12	0	12	ns	
Data output hold time from DQS	$t_{\text{QH}}$	$t_{\text{HP}} - t_{\text{QHS}}$	—	$t_{\text{HPQ}} - t_{\text{QHS}}$	—		
Data hold skew factor	$t_{\text{QHS}}$	—	300	—	340	ps	
Average periodic refresh Interval	$t_{\text{REFI}}$	—	7.8	—	7.8	$\mu\text{s}$	<sup>2)</sup>
		—	3.9	—	3.9	$\mu\text{s}$	<sup>3)</sup>
Auto-Refresh to Active/Auto-Refresh command period	$t_{\text{RFC}}$	105	—	105	—	ns	
Precharge-All (4 banks) command period	$t_{\text{RP}}$	$t_{\text{RP}} + 1t_{\text{CK}}$	—	$t_{\text{RP}} + 1t_{\text{CK}}$	—	ns	
Read preamble	$t_{\text{RPRE}}$	0.9	1.1	0.9	1.1	$t_{\text{CK}}$	
Read postamble	$t_{\text{RPST}}$	0.40	0.60	0.40	0.60	$t_{\text{CK}}$	
Active bank A to Active bank B command period	$t_{\text{RRD}}$	7.5	—	7.5	—	ns	
		10	—	10	—	ns	
Internal Read to Precharge command delay	$t_{\text{RTP}}$	7.5	—	7.5	—	ns	
Write preamble	$t_{\text{WPRE}}$	$0.35 \times t_{\text{CK}}$	—	$0.35 \times t_{\text{CK}}$	—	$t_{\text{CK}}$	
Write postamble	$t_{\text{WPST}}$	0.40	0.60	0.40	0.60	$t_{\text{CK}}$	
Write recovery time for write without Auto-Precharge	$t_{\text{WR}}$	15	—	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	$t_{\text{WR}}/t_{\text{CK}}$	—	$t_{\text{WR}}/t_{\text{CK}}$	—	$t_{\text{CK}}$	<sup>4)</sup>
Internal Write to Read command delay	$t_{\text{WTR}}$	7.5	—	7.5	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	$t_{\text{XARD}}$	2	—	2	—	$t_{\text{CK}}$	
Exit active power-down mode to Read command (slow exit, lower power)	$t_{\text{XARDS}}$	8 – AL	—	7 – AL	—	$t_{\text{CK}}$	

**Table 15 Timing Parameter by Speed Grade - DDR2-800 & DDR2-667 (cont'd)**

Parameter	Symbol	DDR2-800		DDR2-667		Unit	Notes <sup>1)</sup>
		Min.	Max.	Min.	Max.		
Exit precharge power-down to any valid command (other than NOP or Deselect)	$t_{XP}$	2	—	2	—	$t_{CK}$	
Exit Self-Refresh to non-Read command	$t_{XSNR}$	$t_{RFC} + 10$	—	$t_{RFC} + 10$	—	ns	
Exit Self-Refresh to Read command	$t_{XSRD}$	200	—	200	—	$t_{CK}$	

- 1) For details and notes see the relevant INFINEON component data sheet
- 2)  $0 \leq T_{CASE} \leq 85 \text{ }^\circ\text{C}$
- 3)  $85 \text{ }^\circ\text{C} < T_{CASE} \leq 95 \text{ }^\circ\text{C}$
- 4) WR must be programmed to fulfill the minimum requirement for the  $t_{WR}$  timing parameter, where  $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$  rounded up to the next integer value.  $t_{DAL} = WR + (t_{RP}/t_{CK})$ . For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  refers to the application clock period. WR refers to the WR parameter stored in the MRS.

**Table 16 Timing Parameter by Speed Grade - DDR2-400 & DDR2-533**

Parameter	Symbol	DDR2-533		DDR2-400		Unit	Notes <sup>1)</sup>
		Min.	Max.	Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	$t_{AC}$	-500	+500	-600	+600	ps	
$\overline{\text{CAS A}}$ to $\overline{\text{CAS B}}$ command period	$t_{CCD}$	2	—	2	—	$t_{CK}$	
CK, $\overline{\text{CK}}$ high-level width	$t_{CH}$	0.45	0.55	0.45	0.55	$t_{CK}$	
CKE minimum high and low pulse width	$t_{CKE}$	3	—	3	—	$t_{CK}$	
CK, $\overline{\text{CK}}$ low-level width	$t_{CL}$	0.45	0.55	0.45	0.55	$t_{CK}$	
Auto-Precharge write recovery + precharge time	$t_{DAL}$	WR + $t_{RP}$	—	WR + $t_{RP}$	—	$t_{CK}$	
Minimum time clocks remain ON after CKE asynchronously drops LOW	$t_{DELAY}$	$t_{IS} + t_{CK} + t_{IH}$	—	$t_{IS} + t_{CK} + t_{IH}$	—	ns	
DQ and DM input hold time (differential data strobe)	$t_{DH}(\text{base})$	225	—	275	—	ps	
DQ and DM input hold time (single ended data strobe)	$t_{DH1}(\text{base})$	-25	—	-25	—	ps	
DQ and DM input pulse width (each input)	$t_{DIPW}$	0.35	—	0.35	—	$t_{CK}$	
DQS output access time from CK / $\overline{\text{CK}}$	$t_{DQSCK}$	-450	+450	-500	+500	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	$t_{CK}$	
DQS-DQ skew (for DQS & associated DQ signals)	$t_{DQSQ}$	—	300	—	350	ps	
Write command to 1st DQS latching transition	$t_{DQSS}$	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	$t_{CK}$	
DQ and DM input setup time (differential data strobe)	$t_{DS}(\text{base})$	100	—	150	—	ps	
DQ and DM input setup time (single ended data strobe)	$t_{DS1}(\text{base})$	-25	—	-25	—	ps	
DQS falling edge hold time from CK (write cycle)	$t_{DSH}$	0.2	—	0.2	—	$t_{CK}$	
DQS falling edge to CK setup time (write cycle)	$t_{DSS}$	0.2	—	0.2	—	$t_{CK}$	
Clock half period	$t_{HP}$	MIN. ( $t_{CL}, t_{CH}$ )		MIN. ( $t_{CL}, t_{CH}$ )			
Data-out high-impedance time from CK / $\overline{\text{CK}}$	$t_{HZ}$	—	$t_{AC,MAX}$	—	$t_{AC,MAX}$	ps	
Address and control input hold time	$t_{IH}(\text{base})$	375	—	475	—	ps	
Address and control input pulse width (each input)	$t_{IPW}$	0.6	—	0.6	—	$t_{CK}$	

**Table 16 Timing Parameter by Speed Grade - DDR2-400 & DDR2-533 (cont'd)**

Parameter	Symbol	DDR2-533		DDR2-400		Unit	Notes <sup>1)</sup>
		Min.	Max.	Min.	Max.		
Address and control input setup time	$t_{IS}(\text{base})$	250	—	350	—	ps	
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	$t_{MRD}$	2	—	2	—	$t_{CK}$	
OCD drive mode output delay	$t_{OIT}$	0	12	0	12	ns	
Data output hold time from DQS	$t_{QH}$	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—		
Data hold skew factor	$t_{QHS}$	—	400	—	450	ps	
Average periodic refresh Interval	$t_{REFI}$	—	7.8	—	7.8	$\mu\text{s}$	2)
		—	3.9	—	3.9	$\mu\text{s}$	3)
Auto-Refresh to Active/Auto-Refresh command period	$t_{RFC}$	105	—	105	—	ns	
Precharge-All (4 banks) command period	$t_{RP}$	$t_{RP} + 1t_{CK}$	—	$t_{RP} + 1t_{CK}$	—	ns	
Read preamble	$t_{RPRE}$	0.9	1.1	0.9	1.1	$t_{CK}$	
Read postamble	$t_{RPST}$	0.40	0.60	0.40	0.60	$t_{CK}$	
Active bank A to Active bank B command period	$t_{RRD}$	7.5	—	7.5	—	ns	
		10	—	10	—	ns	
Internal Read to Precharge command delay	$t_{RTP}$	7.5	—	7.5	—	ns	
Write preamble	$t_{WPRE}$	$0.25 \times t_{CK}$	—	$0.25 \times t_{CK}$	—	$t_{CK}$	
Write postamble	$t_{WPST}$	0.40	0.60	0.40	0.60	$t_{CK}$	
Write recovery time for write without Auto-Precharge	$t_{WR}$	15	—	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	$t_{WR}/t_{CK}$		$t_{WR}/t_{CK}$		$t_{CK}$	4)
Internal Write to Read command delay	$t_{WTR}$	7.5	—	10	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	$t_{XARD}$	2	—	2	—	$t_{CK}$	
Exit active power-down mode to Read command (slow exit, lower power)	$t_{XARDS}$	6 – AL	—	6 – AL	—	$t_{CK}$	
Exit precharge power-down to any valid command (other than NOP or Deselect)	$t_{XP}$	2	—	2	—	$t_{CK}$	

**Table 16 Timing Parameter by Speed Grade - DDR2-400 & DDR2-533 (cont'd)**

Parameter	Symbol	DDR2-533		DDR2-400		Unit	Notes <sup>1)</sup>
		Min.	Max.	Min.	Max.		
Exit Self-Refresh to non-Read command	$t_{XSNR}$	$t_{RFC} + 10$	—	$t_{RFC} + 10$	—	ns	
Exit Self-Refresh to Read command	$t_{XSRD}$	200	—	200	—	$t_{CK}$	

- 1) For details and notes see the relevant INFINEON component data sheet
- 2)  $0 \leq T_{CASE} \leq 85 \text{ }^\circ\text{C}$
- 3)  $85 \text{ }^\circ\text{C} < T_{CASE} \leq 95 \text{ }^\circ\text{C}$
- 4) WR must be programmed to fulfill the minimum requirement for the  $t_{WR}$  timing parameter, where  $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$  rounded up to the next integer value.  $t_{DAL} = WR + (t_{RP}/t_{CK})$ . For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  refers to the application clock period. WR refers to the WR parameter stored in the MRS.

### 3.3.3 ODT AC Electrical Characteristics

List of ODT tables.

- [Table 17 “ODT AC Electrical Characteristics and Operating Conditions for DDR2-667 and DDR2-800” on Page 26](#)
- [Table 18 “ODT AC Characteristics and Operating Conditions for DDR2-533 and DDR2-400” on Page 26](#)

**Table 17 ODT AC Electrical Characteristics and Operating Conditions for DDR2-667 and DDR2-800**

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
$t_{AOND}$	ODT turn-on delay	2	2	$t_{CK}$	
$t_{AON}$	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX} + 0.7 \text{ ns}$	ns	<sup>1)</sup>
$t_{AONPD}$	ODT turn-on (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
$t_{AOFD}$	ODT turn-off delay	2.5	2.5	$t_{CK}$	
$t_{AOF}$	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX} + 0.6 \text{ ns}$	ns	<sup>2)</sup>
$t_{AOFPD}$	ODT turn-off (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
$t_{ANPD}$	ODT to Power Down Mode Entry Latency	3	—	$t_{CK}$	
$t_{AXPD}$	ODT Power Down Exit Latency	8	—	$t_{CK}$	

- 1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from  $t_{AOND}$ .
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from  $t_{AOFD}$ .

**Table 18 ODT AC Characteristics and Operating Conditions for DDR2-533 and DDR2-400**

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
$t_{AOND}$	ODT turn-on delay	2	2	$t_{CK}$	
$t_{AON}$	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX} + 1 \text{ ns}$	ns	<sup>1)</sup>
$t_{AONPD}$	ODT turn-on (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
$t_{AOFD}$	ODT turn-off delay	2.5	2.5	$t_{CK}$	
$t_{AOF}$	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX} + 0.6 \text{ ns}$	ns	<sup>2)</sup>
$t_{AOFPD}$	ODT turn-off (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	



**Table 18 ODT AC Characteristics and Operating Conditions for DDR2-533 and DDR2-400 (cont'd)**

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
$t_{ANPD}$	ODT to Power Down Mode Entry Latency	3	—	$t_{CK}$	
$t_{AXPD}$	ODT Power Down Exit Latency	8	—	$t_{CK}$	

- 1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from  $t_{AOND}$ .
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from  $t_{AOFD}$ .

### 3.4 $I_{DD}$ Specifications and Conditions

List of tables defining  $I_{DD}$  Specifications and Conditions.

- [Table 19 “IDD Measurement Conditions” on Page 27](#)
- [Table 21 “IDD Specification for HYS64T\[32/64/128\]xxxHDL-2.5-B” on Page 30](#)
- [Table 22 “IDD Specification for HYS64T\[32/64/128\]xxxHDL-3-B” on Page 31](#)
- [Table 23 “IDD Specification for HYS64T\[32/64/128\]xxxHDL-3S-B” on Page 32](#)
- [Table 24 “IDD Specification for HYS64T\[32/64/128\]xxxHDL-3.7-B” on Page 33](#)
- [Table 25 “IDD Specification for HYS64T\[32/64/128\]xxxHDL-5-B” on Page 34](#)

**Table 19  $I_{DD}$  Measurement Conditions** <sup>1)2)3)4)5)6)</sup>

Parameter	Symbol
<b>Operating Current 0</b> One bank Active - Precharge; $t_{CK} = t_{CK,MIN}$ , $t_{RC} = t_{RC,MIN}$ , $t_{RAS} = t_{RAS,MIN}$ , CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	$I_{DD0}$
<b>Operating Current 1</b> One bank Active - Read - Precharge; $I_{OUT} = 0$ mA, BL = 4, $t_{CK} = t_{CK,MIN}$ , $t_{RC} = t_{RC,MIN}$ , $t_{RAS} = t_{RAS,MIN}$ , $t_{RCD} = t_{RCD,MIN}$ , AL = 0, CL = CL <sub>MIN</sub> ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	$I_{DD1}$
<b>Precharge Standby Current</b> All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK,MIN}$ ; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	$I_{DD2N}$
<b>Precharge Power-Down Current</b> Other control and address inputs are STABLE, Data bus inputs are FLOATING.	$I_{DD2P}$
<b>Precharge Quiet Standby Current</b> All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK,MIN}$ ; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	$I_{DD2Q}$
<b>Active Standby Current</b> Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL <sub>MIN</sub> ; $t_{CK} = t_{CK,MIN}$ ; $t_{RAS} = t_{RAS,MAX}$ , $t_{RP} = t_{RP,MIN}$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; $I_{OUT} = 0$ mA.	$I_{DD3N}$
<b>Active Power-Down Current</b> All banks open; $t_{CK} = t_{CK,MIN}$ , CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$
<b>Active Power-Down Current</b> All banks open; $t_{CK} = t_{CK,MIN}$ , CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$

**Table 19**  $I_{DD}$  Measurement Conditions (cont'd)<sup>1)2)3)4)5)6)</sup>

Parameter	Symbol
<p><b>Operating Current</b>           urst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL<sub>MIN</sub>; <math>t_{CK} = t_{CK.MIN}</math>;  <math>t_{RAS} = t_{RAS.MAX}</math>, <math>t_{RP} = t_{RP.MAX}</math>; CKE is HIGH, <math>\overline{CS}</math> is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;</p>	$I_{DD4W}$
<p><b>Burst Refresh Current</b>  <math>t_{CK} = t_{CK.MIN}</math>, Refresh command every <math>t_{RFC} = t_{RFC.MIN}</math> interval, CKE is HIGH, <math>\overline{CS}</math> is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.</p>	$I_{DD5B}$
<p><b>Distributed Refresh Current</b>  <math>t_{CK} = t_{CK.MIN}</math>, Refresh command every <math>t_{RFC} = t_{REFI}</math> interval, CKE is LOW and <math>\overline{CS}</math> is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.</p>	$I_{DD5D}$

**Table 19**  $I_{DD}$  Measurement Conditions (cont'd)<sup>1)2)3)4)5)6)</sup>

Parameter	Symbol
<b>Self-Refresh Current</b> CKE $\leq$ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. $I_{DD6}$ current values are guaranteed up to $T_{CASE}$ of 85 °C max.	$I_{DD6}$
<b>All Bank Interleave Read Current</b> All banks are being interleaved at minimum $t_{RC}$ without violating $t_{RRD}$ using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. $I_{out} = 0$ mA.	$I_{DD7}$
1) $V_{DDQ} = 1.8\text{ V} \pm 0.1\text{ V}$ ; $V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$ 2) $I_{DD}$ specifications are tested after the device is properly initialized and $I_{DD}$ parameter are specified with ODT disabled. 3) Definitions for $I_{DD}$ see <a href="#">Table 20</a> 4) $I_{DD1}$ , $I_{DD4R}$ and $I_{DD7}$ current measurements are defined with the outputs disabled ( $I_{OUT} = 0$ mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH. 5) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode $I_{DD2P}$ 6) For details and notes see the relevant INFINEON component data sheet	

**Table 20** Definitions for  $I_{DD}$

Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac).MAX}$ , HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	inputs are stable at a HIGH or LOW level
FLOATING	inputs are $V_{REF} = V_{DDQ}/2$
SWITCHING	inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes

Table 21  $I_{DD}$  Specification for HYS64T[32/64/128]xxxHDL-2.5-B

Product Type	HYS64T32000HDL-2.5-B	HYS64T64020HDL-2.5-B	HYS64T128021HDL-2.5-B	Unit	Note <sup>1)</sup>
<b>Organization</b>	<b>256 MB</b>	<b>512 MB</b>	<b>1 GB</b>		
	<b>1 Rank</b>	<b>2 Ranks</b>	<b>2 Ranks</b>		
	<b>×64</b>	<b>×64</b>	<b>×64</b>		
	<b>-2.5</b>	<b>-2.5</b>	<b>-2.5</b>		
<b>Symbol</b>	<b>Max.</b>	<b>Max.</b>	<b>Max.</b>		
$I_{DD0}$	400	430	700	mA	2)
$I_{DD1}$	460	490	820	mA	2)
$I_{DD2P}$	30	60	110	mA	3)
$I_{DD2N}$	200	410	820	mA	3)
$I_{DD2Q}$	180	360	720	mA	3)
$I_{DD3P}$ ( MRS = 0)	160	310	620	mA	3)
$I_{DD3P}$ ( MRS = 1)	40	70	140	mA	3)
$I_{DD3N}$	240	480	960	mA	3)
$I_{DD4R}$	720	750	1300	mA	2)
$I_{DD4W}$	800	830	1300	mA	2)
$I_{DD5B}$	580	610	1220	mA	2)
$I_{DD5D}$	40	70	140	mA	3)4)
$I_{DD6}$	20	40	80	mA	3)4)
$I_{DD7}$	1020	1050	1340	mA	2)

1) Calculated values from component data. ODT disabled.  $I_{DD1}$ ,  $I_{DD4R}$ , and  $I_{DD7}$ , are defined with the outputs disabled.

2) The other rank is in  $I_{DD2P}$  Precharge Power-Down Current mode

3) Both ranks are in the same  $I_{DD}$  current mode

4) These values are for  $0^{\circ}\text{C} \leq T_{\text{Case}} \leq 85^{\circ}\text{C}$

Table 22  $I_{DD}$  Specification for HYS64T[32/64/128]xxxHDL-3-B

Product Type	HYS64T32000HDL-3-B	HYS64T64020HDL-3-B	HYS64T128021HDL-3-B	Unit	Note <sup>1)</sup>
<b>Organization</b>	<b>256 MB</b>	<b>512 MB</b>	<b>1 GB</b>		
	<b>1 Rank</b>	<b>2 Ranks</b>	<b>2 Ranks</b>		
	<b>×64</b>	<b>×64</b>	<b>×64</b>		
	<b>-3</b>	<b>-3</b>	<b>-33</b>		
<b>Symbol</b>	<b>Max.</b>	<b>Max.</b>	<b>Max.</b>		
$I_{DD0}$	380	410	660	mA	2)
$I_{DD1}$	420	450	780	mA	2)
$I_{DD2P}$	30	60	110	mA	3)
$I_{DD2N}$	180	360	720	mA	3)
$I_{DD2Q}$	160	320	640	mA	3)
$I_{DD3P}$ ( MRS = 0)	130	260	530	mA	3)
$I_{DD3P}$ ( MRS = 1)	40	70	140	mA	3)
$I_{DD3N}$	200	400	800	mA	3)
$I_{DD4R}$	620	650	1100	mA	2)
$I_{DD4W}$	680	710	1100	mA	2)
$I_{DD5B}$	560	590	1180	mA	2)
$I_{DD5D}$	40	70	140	mA	3)4)
$I_{DD6}$	20	40	80	mA	3)4)
$I_{DD7}$	1010	1040	1340	mA	2)

1) Calculated values from component data. ODT disabled.  $I_{DD1}$ ,  $I_{DD4R}$ , and  $I_{DD7}$ , are defined with the outputs disabled.

2) The other rank is in  $I_{DD2P}$  Precharge Power-Down Current mode

3) Both ranks are in the same  $I_{DD}$  current mode

4) These values are for  $0\text{ °C} \leq T_{Case} \leq 85\text{ °C}$ .

Table 23  $I_{DD}$  Specification for HYS64T[32/64/128]xxxHDL-3S-B

Product Type	HYS64T32000HDL-3S-B	HYS64T64020HDL-3S-B	HYS64T128021HDL-3S-B	Unit	Note <sup>1)</sup>
<b>Organization</b>	<b>256 MB</b>	<b>512 MB</b>	<b>1 GB</b>		
	<b>1 Rank</b>	<b>2 Ranks</b>	<b>2 Ranks</b>		
	<b>×64</b>	<b>×64</b>	<b>×64</b>		
	<b>-3S</b>	<b>-3S</b>	<b>-3S</b>		
<b>Symbol</b>	<b>Max.</b>	<b>Max.</b>	<b>Max.</b>		
$I_{DD0}$	360	390	620	mA	2)
$I_{DD1}$	400	430	740	mA	2)
$I_{DD2P}$	30	60	110	mA	3)
$I_{DD2N}$	180	360	720	mA	3)
$I_{DD2Q}$	160	320	640	mA	3)
$I_{DD3P}$ ( MRS = 0)	130	260	530	mA	3)
$I_{DD3P}$ ( MRS = 1)	40	70	140	mA	3)
$I_{DD3N}$	200	400	800	mA	3)
$I_{DD4R}$	620	650	1100	mA	2)
$I_{DD4W}$	680	710	1100	mA	2)
$I_{DD5B}$	560	590	1180	mA	2)
$I_{DD5D}$	40	70	140	mA	3)4)
$I_{DD6}$	20	40	80	mA	3)4)
$I_{DD7}$	960	990	1270	mA	2)

1) Calculated values from component data. ODT disabled.  $I_{DD1}$ ,  $I_{DD4R}$ , and  $I_{DD7}$ , are defined with the outputs disabled.

2) The other rank is in  $I_{DD2P}$  Precharge Power-Down Current mode

3) Both ranks are in the same  $I_{DD}$  current mode

4) These values are for  $0\text{ °C} \leq T_{\text{Case}} \leq 85\text{ °C}$ .



Table 24  $I_{DD}$  Specification for HYS64T[32/64/128]xxxHDL-3.7-B

Product Type	HYS64T32000HDL-3.7-B	HYS64T64020HDL-3.7-B	HYS64T128021HDL-3.7-B	Unit	Note <sup>1)</sup>
<b>Organization</b>	<b>256 MB</b>	<b>512 MB</b>	<b>1 GB</b>		
	<b>1 Rank</b>	<b>2 Ranks</b>	<b>2 Ranks</b>		
	<b>×64</b>	<b>×64</b>	<b>×64</b>		
	<b>-3.7</b>	<b>-3.7</b>	<b>-3.7</b>		
<b>Symbol</b>	<b>Max.</b>	<b>Max.</b>	<b>Max.</b>		
$I_{DD0}$	320	350	580	mA	2)
$I_{DD1}$	360	390	660	mA	2)
$I_{DD2P}$	30	60	110	mA	3)
$I_{DD2N}$	150	300	610	mA	3)
$I_{DD2Q}$	140	280	560	mA	3)
$I_{DD3P}$ ( MRS = 0)	110	220	450	mA	3)
$I_{DD3P}$ ( MRS = 1)	40	70	140	mA	3)
$I_{DD3N}$	170	340	690	mA	3)
$I_{DD4R}$	520	550	940	mA	2)
$I_{DD4W}$	580	610	940	mA	2)
$I_{DD5B}$	520	550	1100	mA	2)
$I_{DD5D}$	40	70	140	mA	3)4)
$I_{DD6}$	20	40	80	mA	3)4)
$I_{DD7}$	920	950	1220	mA	2)

1) Calculated values from component data. ODT disabled.  $I_{DD1}$ ,  $I_{DD4R}$ , and  $I_{DD7}$ , are defined with the outputs disabled.

2)The other rank is in  $I_{DD2P}$  Precharge Power-Down Current mode

3) Both ranks are in the same  $I_{DD}$  current mode

4) These values are for  $0\text{ °C} \leq T_{Case} \leq 85\text{ °C}$

Table 25  $I_{DD}$  Specification for HYS64T[32/64/128]xxxHDL-5-B

Product Type	HYS64T32000HDL-5-B	HYS64T64020HDL-5-B	HYS64T128021HDL-5-B	Unit	Note <sup>1)</sup>
<b>Organization</b>	<b>256 MB</b>	<b>512 MB</b>	<b>1 GB</b>		
	<b>1 Rank</b>	<b>2 Ranks</b>	<b>2 Ranks</b>		
	<b>×64</b>	<b>×64</b>	<b>×64</b>		
	<b>-5</b>	<b>-5</b>	<b>-5</b>		
<b>Symbol</b>	<b>Max.</b>	<b>Max.</b>	<b>Max.</b>		
$I_{DD0}$	300	330	540	mA	2)
$I_{DD1}$	330	360	620	mA	2)
$I_{DD2P}$	30	60	110	mA	3)
$I_{DD2N}$	140	270	540	mA	3)
$I_{DD2Q}$	130	260	510	mA	3)
$I_{DD3P}(MRS = 0)$	100	190	380	mA	3)
$I_{DD3P}(MRS = 1)$	40	70	140	mA	3)
$I_{DD3N}$	160	310	620	mA	3)
$I_{DD4R}$	460	490	820	mA	2)
$I_{DD4W}$	520	550	820	mA	2)
$I_{DD5B}$	500	530	1060	mA	2)
$I_{DD5D}$	40	70	140	mA	3)4)
$I_{DD6}$	20	40	80	mA	3)
$I_{DD7}$	880	910	1180	mA	2)

1) Calculated values from component data. ODT disabled.  $I_{DD1}$ ,  $I_{DD4R}$ , and  $I_{DD7}$ , are defined with the outputs disabled.

2) The other rank is in  $I_{DD2P}$  Precharge Power-Down Current mode

3) Both ranks are in the same  $I_{DD}$  current mode

4) These values are for  $0\text{ °C} \leq T_{Case} \leq 85\text{ °C}$ .

### 3.4.1 $I_{DD}$ Test Conditions

For testing the  $I_{DD}$  parameters, the timing parameters as shown in the tables below are used.

- [Table 26 “IDD Measurement Test Condition for DDR2–800E” on Page 35](#)
- [Table 27 “IDD Measurement Test Condition for DDR2–667C” on Page 35](#)
- [Table 28 “IDD Measurement Test Condition for DDR2–667D” on Page 36](#)
- [Table 29 “IDD Measurement Test Condition for DDR2–533C” on Page 36](#)
- [Table 30 “IDD Measurement Test Condition for DDR2–400B” on Page 36](#)

**Table 26  $I_{DD}$  Measurement Test Condition for DDR2–800E**

Parameter	Symbol	–2.5	Unit	Notes
		DDR2–800E		
CAS Latency	$CL_{IDD}$	6	$t_{CK}$	
Clock Cycle Time	$t_{CK.IDD}$	2.5	ns	
Active to Read or Write delay	$t_{RCD.IDD}$	15	ns	
Active to Active / Auto-Refresh command period	$t_{RC.IDD}$	60	ns	
Active bank A to Active bank B command delay	$t_{RRD.IDD}$	7.5	ns	1)
		10	ns	2)
Active to Precharge Command	$t_{RAS.MIN.IDD}$	45	ns	
	$t_{RAS.MAX.IDD}$	70000	ns	
Precharge Command Period	$t_{RP.IDD}$	15	ns	
Auto-Refresh to Active / Auto-Refresh command period	$t_{RFC.IDD}$	105	ns	
Average periodic Refresh interval	$0^{\circ}C \leq T_{CASE} \leq 85^{\circ}C$	$t_{REFI}$	$\mu s$	
	$85^{\circ}C \leq T_{CASE} \leq 95^{\circ}C$	$t_{REFI}$	$\mu s$	

1)  $\times 4$  &  $\times 8$  (1 kB page size)

2)  $\times 16$  (2 kB page size)

**Table 27  $I_{DD}$  Measurement Test Condition for DDR2–667C**

Parameter	Symbol	–3	Unit	Notes
		DDR2–667C		
CAS Latency	$CL_{IDD}$	4	$t_{CK}$	
Clock Cycle Time	$t_{CK.IDD}$	3	ns	
Active to Read or Write delay	$t_{RCD.IDD}$	12	ns	
Active to Active / Auto-Refresh command period	$t_{RC.IDD}$	57	ns	
Active bank A to Active bank B command delay	$t_{RRD.IDD}$	7.5	ns	1)
		10	ns	2)
Active to Precharge Command	$t_{RAS.MIN.IDD}$	45	ns	
	$t_{RAS.MAX.IDD}$	70000	ns	
Precharge Command Period	$t_{RP.IDD}$	12	ns	
Auto-Refresh to Active / Auto-Refresh command period	$t_{RFC.IDD}$	105	ns	
Average periodic Refresh interval	$0^{\circ}C \leq T_{CASE} \leq 85^{\circ}C$	$t_{REFI}$	$\mu s$	
	$85^{\circ}C \leq T_{CASE} \leq 95^{\circ}C$	$t_{REFI}$	$\mu s$	

1)  $\times 4$  &  $\times 8$  (1 kB page size)

2)  $\times 16$  (2 kB page size)

**Table 28  $I_{DD}$  Measurement Test Condition for DDR2–667D**

Parameter	Symbol	–3S	Unit	Notes
		DDR2–667D		
CAS Latency	$CL_{IDD}$	5	$t_{CK}$	
Clock Cycle Time	$t_{CK,IDD}$	3	ns	
Active to Read or Write delay	$t_{RCD,IDD}$	15	ns	
Active to Active / Auto-Refresh command period	$t_{RC,IDD}$	60	ns	
Active bank A to Active bank B command delay	$t_{RRD,IDD}$	7.5	ns	1)
		10	ns	2)
Active to Precharge Command	$t_{RAS,MIN,IDD}$	45	ns	
	$t_{RAS,MAX,IDD}$	70000	ns	
Precharge Command Period	$t_{RP,IDD}$	15	ns	
Auto-Refresh to Active / Auto-Refresh command period	$t_{RFC,IDD}$	105	ns	
Average periodic Refresh interval	$0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$	$t_{REFI}$	7.8	$\mu\text{s}$
	$85^{\circ}\text{C} \leq T_{CASE} \leq 95^{\circ}\text{C}$	$t_{REFI}$	3.9	$\mu\text{s}$

 1)  $\times 4$  &  $\times 8$  (1 kB page size)

 2)  $\times 16$  (2 kB page size)

**Table 29  $I_{DD}$  Measurement Test Condition for DDR2–533C**

Parameter	Symbol	–3.7	Unit	Notes
		DDR2–533C		
CAS Latency	$CL_{IDD}$	4	$t_{CK}$	
Clock Cycle Time	$t_{CK,IDD}$	3.75	ns	
Active to Read or Write delay	$t_{RCD,IDD}$	15	ns	
Active to Active / Auto-Refresh command period	$t_{RC,IDD}$	60	ns	
Active bank A to Active bank B command delay	$t_{RRD,IDD}$	7.5	ns	1)
		10	ns	2)
Active to Precharge Command	$t_{RAS,MIN,IDD}$	45	ns	
	$t_{RAS,MAX,IDD}$	7000	ns	
Precharge Command Period	$t_{RP,IDD}$	15	ns	
Auto-Refresh to Active / Auto-Refresh command period	$t_{RFC,IDD}$	105	ns	
Average periodic Refresh interval	$0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$	$t_{REFI}$	7.8	$\mu\text{s}$
	$85^{\circ}\text{C} \leq T_{CASE} \leq 95^{\circ}\text{C}$	$t_{REFI}$	3.9	$\mu\text{s}$

 1)  $\times 4$  &  $\times 8$  (1 kB page size)

 2)  $\times 16$  (2 kB page size)

**Table 30  $I_{DD}$  Measurement Test Condition for DDR2–400B**

Parameter	Symbol	–5	Unit	Notes
		DDR2–400B		
CAS Latency	$CL_{IDD}$	3	$t_{CK}$	
Clock Cycle Time	$t_{CK,IDD}$	5	ns	
Active to Read or Write delay	$t_{RCD,IDD}$	15	ns	

**Table 30**  $I_{DD}$  Measurement Test Condition for DDR2-400B

Parameter	Symbol	-5	Unit	Notes	
		DDR2-400B			
Active to Active / Auto-Refresh command period	$t_{RC.IDD}$	55	ns		
Active bank A to Active bank B command delay	$t_{RRD.IDD}$	7.5	ns	1)	
		10	ns	2)	
Active to Precharge Command	$t_{RAS.MIN.IDD}$	40	ns		
	$t_{RAS.MAX.IDD}$	7000	ns		
Precharge Command Period	$t_{RP.IDD}$	15	ns		
Auto-Refresh to Active / Auto-Refresh command period	$t_{RFC.IDD}$	105	ns		
Average periodic Refresh interval	$0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$	$t_{REFI}$	7.8	$\mu\text{s}$	
	$85^{\circ}\text{C} \leq T_{CASE} \leq 95^{\circ}\text{C}$	$t_{REFI}$	3.9	$\mu\text{s}$	

1)  $\times 4$  &  $\times 8$  (1 kB page size)

2)  $\times 16$  (2 kB page size)

### 3.4.2 On Die Termination (ODT) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A[6,2] in the EMRS(1) a “weak” or “strong” termination can be selected. The

current consumption for any terminated input pin, depends on the input pin is in tri-state or driving 0 or 1, as long a ODT is enabled during a given period of time.

**Table 31** ODT current per terminated pin

Parameter	Symbol	Min.	Typ.	Max.	Unit	EMRS(1) State
<b>Enabled ODT current per DQ</b> ODT is HIGH; Data Bus inputs are FLOATING	$I_{ODTO}$	5	6	7.5	mA/DQ	A6 = 0, A2 = 1
		2.5	3	3.75	mA/DQ	A6 = 1, A2 = 0
<b>Active ODT current per DQ</b> ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	$I_{ODTT}$	10	12	15	mA/DQ	A6 = 0, A2 = 1
		5	6	7.5	mA/DQ	A6 = 1, A2 = 0

Note: For power consumption calculations the ODT duty cycle has to be taken into account

## 4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

### List of SPD Code Tables

- [Table 32 “SPD Codes for HYS64T\[32/64/128\]xxxHDL-2.5-B” on Page 38](#)
- [Table 33 “SPD Codes for HYS64T\[32/64/128\]xxxHDL-3-B” on Page 42](#)
- [Table 34 “SPD Codes for HYS64T\[32/64/128\]xxxHDL-3S-B” on Page 46](#)
- [Table 35 “SPD Codes for HYS64T\[32/64/128\]xxxHDL-3.7-B” on Page 50](#)
- [Table 36 “SPD Codes for HYS64T\[32/64/128\]xxxHDL-5-B” on Page 54](#)

**Table 32 SPD Codes for HYS64T[32/64/128]xxxHDL-2.5-B**

Product Type		HYS64T32000HDL-2.5-B	HYS64T64020HDL-2.5-B	HYS64T128021HDL-2.5-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-6400S-666</b>	<b>PC2-6400S-666</b>	<b>PC2-6400S-666</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
Byte#	Description	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	61	61
6	Data Width	40	40	40
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	25	25	25
10	$t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns]	40	40	40
11	Error Correction Support (non-ECC, ECC)	00	00	00
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	10	08
14	Error Checking SDRAM Width	00	00	00
15	Not used	00	00	00

Table 32 SPD Codes for HYS64T[32/64/128]xxxHDL-2.5-B (cont'd)

Product Type		HYS64T32000HDL-2.5-B	HYS64T64020HDL-2.5-B	HYS64T128021HDL-2.5-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-6400S-666</b>	<b>PC2-6400S-666</b>	<b>PC2-6400S-666</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
Byte#	Description	HEX	HEX	HEX
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	70	70	70
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	04	04	04
21	DIMM Attributes	00	00	00
22	Component Attributes	07	07	07
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	30	30	30
24	$t_{AC}$ SDRAM @ $CL_{MAX} -1$ [ns]	45	45	45
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	3D	3D	3D
26	$t_{AC}$ SDRAM @ $CL_{MAX} -2$ [ns]	50	50	50
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	28	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	40	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	15	15	15
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	22	22	22
34	$t_{DS.MIN}$ [ns]	05	05	05
35	$t_{DH.MIN}$ [ns]	12	12	12
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	$t_{RC}$ and $t_{RFC}$ Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69



Table 32 SPD Codes for HYS64T[32/64/128]xxxHDL-2.5-B (cont'd)

Product Type		HYS64T32000HDL-2.5-B	HYS64T64020HDL-2.5-B	HYS64T128021HDL-2.5-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-6400S-666</b>	<b>PC2-6400S-666</b>	<b>PC2-6400S-666</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
Byte#	Description	HEX	HEX	HEX
43	$t_{CK,MAX}$ [ns]	80	80	80
44	$t_{DQSQ,MAX}$ [ns]	14	14	14
45	$t_{QHS,MAX}$ [ns]	1E	1E	1E
46	PLL Relock Time	00	00	00
47	$T_{CASE,MAX}$ Delta / $\Delta T_{4R4W}$ Delta	55	55	50
48	Psi(T-A) DRAM	72	72	7A
49	$\Delta T_0$ (DT0)	6F	6F	5B
50	$\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM)	37	37	3B
51	$\Delta T_{2P}$ (DT2P)	33	33	36
52	$\Delta T_{3N}$ (DT3N)	2B	2B	2E
53	$\Delta T_{3P,fast}$ (DT3P fast)	54	54	5A
54	$\Delta T_{3P,slow}$ (DT3P slow)	27	27	2A
55	$\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W)	62	62	5A
56	$\Delta T_{5B}$ (DT5B)	1F	1F	22
57	$\Delta T_7$ (DT7)	37	37	25
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	$\Delta T_{PLL}$ (DTPLL)	00	00	00
61	$\Delta T_{REG}$ (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	0B	0C	26
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00

Table 32 SPD Codes for HYS64T[32/64/128]xxxHDL-2.5-B (cont'd)

Product Type		HYS64T32000HDL-2.5-B	HYS64T64020HDL-2.5-B	HYS64T128021HDL-2.5-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-6400S-666</b>	<b>PC2-6400S-666</b>	<b>PC2-6400S-666</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
70	JEDEC ID Code of Infineon (7)	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	36
74	Product Type, Char 2	34	34	34
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	31
77	Product Type, Char 5	32	34	32
78	Product Type, Char 6	30	30	38
79	Product Type, Char 7	30	32	30
80	Product Type, Char 8	30	30	32
81	Product Type, Char 9	48	48	31
82	Product Type, Char 10	44	44	48
83	Product Type, Char 11	4C	4C	44
84	Product Type, Char 12	32	32	4C
85	Product Type, Char 13	2E	2E	32
86	Product Type, Char 14	35	35	2E
87	Product Type, Char 15	42	42	35
88	Product Type, Char 16	20	20	42
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00

Table 33 SPD Codes for HYS64T[32/64/128]xxxHDL-3-B

Product Type		HYS64T3200HDL-3-B	HYS64T64020HDL-3-B	HYS64T128021HDL-3-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-5300S-444</b>	<b>PC2-5300S-444</b>	<b>PC2-5300S-444</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	61	61
6	Data Width	40	40	40
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	30	30	30
10	$t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns]	45	45	45
11	Error Correction Support (non-ECC, ECC)	00	00	00
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	10	08
14	Error Checking SDRAM Width	00	00	00
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	04	04	04
21	DIMM Attributes	00	00	00
22	Component Attributes	07	07	07
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	30	30	30
24	$t_{AC}$ SDRAM @ $CL_{MAX} -1$ [ns]	45	45	45
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50	50
26	$t_{AC}$ SDRAM @ $CL_{MAX} -2$ [ns]	60	60	60

Table 33 SPD Codes for HYS64T[32/64/128]xxxHDL-3-B (cont'd)

Product Type		HYS64T32000HDL-3-B	HYS64T64020HDL-3-B	HYS64T128021HDL-3-B
<b>Organization</b>		256 MB	512 MB	1 GByte
		×64	×64	×64
		1 Rank (×16)	2 Ranks (×16)	2 Ranks (×8)
<b>Label Code</b>		PC2-5300S-444	PC2-5300S-444	PC2-5300S-444
<b>JEDEC SPD Revision</b>		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
27	$t_{RP.MIN}$ [ns]	30	30	30
28	$t_{RRD.MIN}$ [ns]	28	28	1E
29	$t_{RCD.MIN}$ [ns]	30	30	30
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	40	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	$t_{RC}$ and $t_{RFC}$ Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	39	39	39
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22
46	PLL Relock Time	00	00	00
47	$T_{CASE.MAX}$ Delta / $\Delta T_{4R4W}$ Delta	54	54	50
48	Psi(T-A) DRAM	72	72	7A
49	$\Delta T_0$ (DT0)	67	67	53
50	$\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM)	31	31	34
51	$\Delta T_{2P}$ (DT2P)	33	33	36
52	$\Delta T_{3N}$ (DT3N)	24	24	27
53	$\Delta T_{3P.fast}$ (DT3P fast)	47	47	4C

Table 33 SPD Codes for HYS64T[32/64/128]xxxHDL-3-B (cont'd)

Product Type		HYS64T32000HDL-3-B	HYS64T64020HDL-3-B	HYS64T128021HDL-3-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		×64	×64	×64
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-5300S-444</b>	<b>PC2-5300S-444</b>	<b>PC2-5300S-444</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
54	$\Delta T_{3P,slow}$ (DT3P slow)	27	27	2A
55	$\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W)	54	54	4C
56	$\Delta T_{5B}$ (DT5B)	1E	1E	20
57	$\Delta T_7$ (DT7)	37	37	25
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	$\Delta T_{PLL}$ (DTPLL)	00	00	00
61	$\Delta T_{REG}$ (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	E1	E2	FA
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	36
74	Product Type, Char 2	34	34	34
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	31
77	Product Type, Char 5	32	34	32
78	Product Type, Char 6	30	30	38
79	Product Type, Char 7	30	32	30
80	Product Type, Char 8	30	30	32

Table 33 SPD Codes for HYS64T[32/64/128]xxxHDL-3-B (cont'd)

Product Type		HYS64T32000HDL-3-B	HYS64T64020HDL-3-B	HYS64T128021HDL-3-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		×64	×64	×64
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-5300S-444</b>	<b>PC2-5300S-444</b>	<b>PC2-5300S-444</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
81	Product Type, Char 9	48	48	31
82	Product Type, Char 10	44	44	48
83	Product Type, Char 11	4C	4C	44
84	Product Type, Char 12	33	33	4C
85	Product Type, Char 13	42	42	33
86	Product Type, Char 14	20	20	42
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	1x	1x	2x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00

Table 34 SPD Codes for HYS64T[32/64/128]xxxHDL-3S-B

Product Type		HYS64T32000HDL-3S-B	HYS64T64020HDL-3S-B	HYS64T128021HDL-3S-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-5300S-555</b>	<b>PC2-5300S-555</b>	<b>PC2-5300S-555</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	61	61
6	Data Width	40	40	40
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	30	30	30
10	$t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns]	45	45	45
11	Error Correction Support (non-ECC, ECC)	00	00	00
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	10	08
14	Error Checking SDRAM Width	00	00	00
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	04	04	04
21	DIMM Attributes	00	00	00
22	Component Attributes	07	07	07
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	3D	3D	3D
24	$t_{AC}$ SDRAM @ $CL_{MAX} -1$ [ns]	50	50	50
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50	50

Table 34 SPD Codes for HYS64T[32/64/128]xxxHDL-3S-B (cont'd)

Product Type		HYS64T32000HDL-3S-B	HYS64T64020HDL-3S-B	HYS64T128021HDL-3S-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-5300S-555</b>	<b>PC2-5300S-555</b>	<b>PC2-5300S-555</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
26	$t_{AC}$ SDRAM @ $CL_{MAX} - 2$ [ns]	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	28	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	40	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	$t_{RC}$ and $t_{RFC}$ Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22
46	PLL Relock Time	00	00	00
47	$T_{CASE.MAX}$ Delta / $\Delta T_{4R4W}$ Delta	54	54	50
48	Psi(T-A) DRAM	72	72	7A
49	$\Delta T_0$ (DT0)	5F	5F	4B
50	$\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM)	31	31	34
51	$\Delta T_{2P}$ (DT2P)	33	33	36
52	$\Delta T_{3N}$ (DT3N)	24	24	27



Table 34 SPD Codes for HYS64T[32/64/128]xxxHDL-3S-B (cont'd)

Product Type		HYS64T32000HDL-3S-B	HYS64T64020HDL-3S-B	HYS64T128021HDL-3S-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-5300S-555</b>	<b>PC2-5300S-555</b>	<b>PC2-5300S-555</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
53	$\Delta T_{3P.fast}$ (DT3P fast)	47	47	4C
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	27	2A
55	$\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W)	54	54	4C
56	$\Delta T_{5B}$ (DT5B)	1E	1E	20
57	$\Delta T_7$ (DT7)	34	34	23
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	$\Delta T_{PLL}$ (DTPLL)	00	00	00
61	$\Delta T_{REG}$ (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	09	0A	23
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	36
74	Product Type, Char 2	34	34	34
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	31
77	Product Type, Char 5	32	34	32
78	Product Type, Char 6	30	30	38
79	Product Type, Char 7	30	32	30

Table 34 SPD Codes for HYS64T[32/64/128]xxxHDL-3S-B (cont'd)

Product Type		HYS64T32000HDL-3S-B	HYS64T64020HDL-3S-B	HYS64T128021HDL-3S-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-5300S-555</b>	<b>PC2-5300S-555</b>	<b>PC2-5300S-555</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
Byte#	Description	HEX	HEX	HEX
80	Product Type, Char 8	30	30	32
81	Product Type, Char 9	48	48	31
82	Product Type, Char 10	44	44	48
83	Product Type, Char 11	4C	4C	44
84	Product Type, Char 12	33	33	4C
85	Product Type, Char 13	53	53	33
86	Product Type, Char 14	42	42	53
87	Product Type, Char 15	20	20	42
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 89	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00

Table 35 SPD Codes for HYS64T[32/64/128]xxxHDL-3.7-B

Product Type		HYS64T32000HDL-3.7-B	HYS64T64020HDL-3.7-B	HYS64T128021HDL-3.7-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-4200S-444</b>	<b>PC2-4200S-444</b>	<b>PC2-4200S-444</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
Byte#	Description	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	61	61
6	Data Width	40	40	40
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	3D	3D	3D
10	$t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns]	50	50	50
11	Error Correction Support (non-ECC, ECC)	00	00	00
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	10	08
14	Error Checking SDRAM Width	00	00	00
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	04	04	04
21	DIMM Attributes	00	00	00
22	Component Attributes	07	07	07
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	3D	3D	3D
24	$t_{AC}$ SDRAM @ $CL_{MAX} -1$ [ns]	50	50	50
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50	50

Table 35 SPD Codes for HYS64T[32/64/128]xxxHDL-3.7-B (cont'd)

Product Type		HYS64T32000HDL-3.7-B	HYS64T64020HDL-3.7-B	HYS64T128021HDL-3.7-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-4200S-444</b>	<b>PC2-4200S-444</b>	<b>PC2-4200S-444</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
Byte#	Description	HEX	HEX	HEX
26	$t_{AC}$ SDRAM @ $CL_{MAX} - 2$ [ns]	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	28	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	40	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	25	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	37	37
34	$t_{DS.MIN}$ [ns]	10	10	10
35	$t_{DH.MIN}$ [ns]	22	22	22
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	$t_{RC}$ and $t_{RFC}$ Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	1E	1E	1E
45	$t_{QHS.MAX}$ [ns]	28	28	28
46	PLL Relock Time	00	00	00
47	$T_{CASE.MAX}$ Delta / $\Delta T_{4R4W}$ Delta	54	54	50
48	Psi(T-A) DRAM	72	72	7A
49	$\Delta T_0$ (DT0)	53	53	43
50	$\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM)	29	29	2C
51	$\Delta T_{2P}$ (DT2P)	33	33	36
52	$\Delta T_{3N}$ (DT3N)	1F	1F	21

Table 35 SPD Codes for HYS64T[32/64/128]xxxHDL-3.7-B (cont'd)

Product Type		HYS64T32000HDL-3.7-B	HYS64T64020HDL-3.7-B	HYS64T128021HDL-3.7-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-4200S-444</b>	<b>PC2-4200S-444</b>	<b>PC2-4200S-444</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
53	$\Delta T_{3P.fast}$ (DT3P fast)	3D	3D	41
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	27	2A
55	$\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W)	46	46	40
56	$\Delta T_{5B}$ (DT5B)	1C	1C	1E
57	$\Delta T_7$ (DT7)	32	32	22
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	$\Delta T_{PLL}$ (DTPLL)	00	00	00
61	$\Delta T_{REG}$ (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	18	19	37
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	36
74	Product Type, Char 2	34	34	34
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	31
77	Product Type, Char 5	32	34	32
78	Product Type, Char 6	30	30	38
79	Product Type, Char 7	30	32	30

Table 35 SPD Codes for HYS64T[32/64/128]xxxHDL-3.7-B (cont'd)

Product Type		HYS64T32000HDL-3.7-B	HYS64T64020HDL-3.7-B	HYS64T128021HDL-3.7-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-4200S-444</b>	<b>PC2-4200S-444</b>	<b>PC2-4200S-444</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
80	Product Type, Char 8	30	30	32
81	Product Type, Char 9	48	48	31
82	Product Type, Char 10	44	44	48
83	Product Type, Char 11	4C	4C	44
84	Product Type, Char 12	33	33	4C
85	Product Type, Char 13	2E	2E	33
86	Product Type, Char 14	37	37	2E
87	Product Type, Char 15	42	42	37
88	Product Type, Char 16	20	20	42
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00

Table 36 SPD Codes for HYS64T[32/64/128]xxxHDL-5-B

Product Type		HYS64T32000HDL-5-B	HYS64T64020HDL-5-B	HYS64T128021HDL-5-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-3200S-333</b>	<b>PC2-3200S-333</b>	<b>PC2-3200S-333</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	61	61
6	Data Width	40	40	40
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	50	50	50
10	$t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns]	60	60	60
11	Error Correction Support (non-ECC, ECC)	00	00	00
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	10	08
14	Error Checking SDRAM Width	00	00	00
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	04	04	04
21	DIMM Attributes	00	00	00
22	Component Attributes	07	07	07
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	50	50	50
24	$t_{AC}$ SDRAM @ $CL_{MAX} -1$ [ns]	60	60	60
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50	50
26	$t_{AC}$ SDRAM @ $CL_{MAX} -2$ [ns]	60	60	60

**Table 36 SPD Codes for HYS64T[32/64/128]xxxHDL-5-B (cont'd)**

Product Type		HYS64T32000HDL-5-B	HYS64T64020HDL-5-B	HYS64T128021HDL-5-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-3200S-333</b>	<b>PC2-3200S-333</b>	<b>PC2-3200S-333</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
Byte#	Description	HEX	HEX	HEX
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	28	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	28	28	28
31	Module Density per Rank	40	40	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	35	35	35
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	47	47	47
34	$t_{DS.MIN}$ [ns]	15	15	15
35	$t_{DH.MIN}$ [ns]	27	27	27
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	28	28	28
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	$t_{RC}$ and $t_{RFC}$ Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	37	37	37
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	23	23	23
45	$t_{QHS.MAX}$ [ns]	2D	2D	2D
46	PLL Relock Time	00	00	00
47	$T_{CASE.MAX}$ Delta / $\Delta T_{4R4W}$ Delta	54	54	50
48	Psi(T-A) DRAM	72	72	7A
49	$\Delta T_0$ (DT0)	4B	4B	3B
50	$\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM)	25	25	27
51	$\Delta T_{2P}$ (DT2P)	33	33	36
52	$\Delta T_{3N}$ (DT3N)	1C	1C	1E
53	$\Delta T_{3P.fast}$ (DT3P fast)	34	34	38



Table 36 SPD Codes for HYS64T[32/64/128]xxxHDL-5-B (cont'd)

Product Type		HYS64T32000HDL-5-B	HYS64T64020HDL-5-B	HYS64T128021HDL-5-B
<b>Organization</b>		256 MB	512 MB	1 GByte
		×64	×64	×64
		1 Rank (×16)	2 Ranks (×16)	2 Ranks (×8)
<b>Label Code</b>		PC2-3200S-333	PC2-3200S-333	PC2-3200S-333
<b>JEDEC SPD Revision</b>		Rev. 1.2	Rev. 1.2	Rev. 1.2
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
54	$\Delta T_{3P,slow}$ (DT3P slow)	27	27	2A
55	$\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W)	3E	3E	38
56	$\Delta T_{5B}$ (DT5B)	1B	1B	1D
57	$\Delta T_7$ (DT7)	30	30	21
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	$\Delta T_{PLL}$ (DTPLL)	00	00	00
61	$\Delta T_{REG}$ (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	6F	70	8E
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	36
74	Product Type, Char 2	34	34	34
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	31
77	Product Type, Char 5	32	34	32
78	Product Type, Char 6	30	30	38
79	Product Type, Char 7	30	32	30
80	Product Type, Char 8	30	30	32

Table 36 SPD Codes for HYS64T[32/64/128]xxxHDL-5-B (cont'd)

Product Type		HYS64T32000HDL-5-B	HYS64T64020HDL-5-B	HYS64T128021HDL-5-B
<b>Organization</b>		<b>256 MB</b>	<b>512 MB</b>	<b>1 GByte</b>
		<b>×64</b>	<b>×64</b>	<b>×64</b>
		<b>1 Rank (×16)</b>	<b>2 Ranks (×16)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-3200S-333</b>	<b>PC2-3200S-333</b>	<b>PC2-3200S-333</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
81	Product Type, Char 9	48	48	31
82	Product Type, Char 10	44	44	48
83	Product Type, Char 11	4C	4C	44
84	Product Type, Char 12	35	35	4C
85	Product Type, Char 13	42	42	35
86	Product Type, Char 14	20	20	42
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00

## 5 Package Outlines

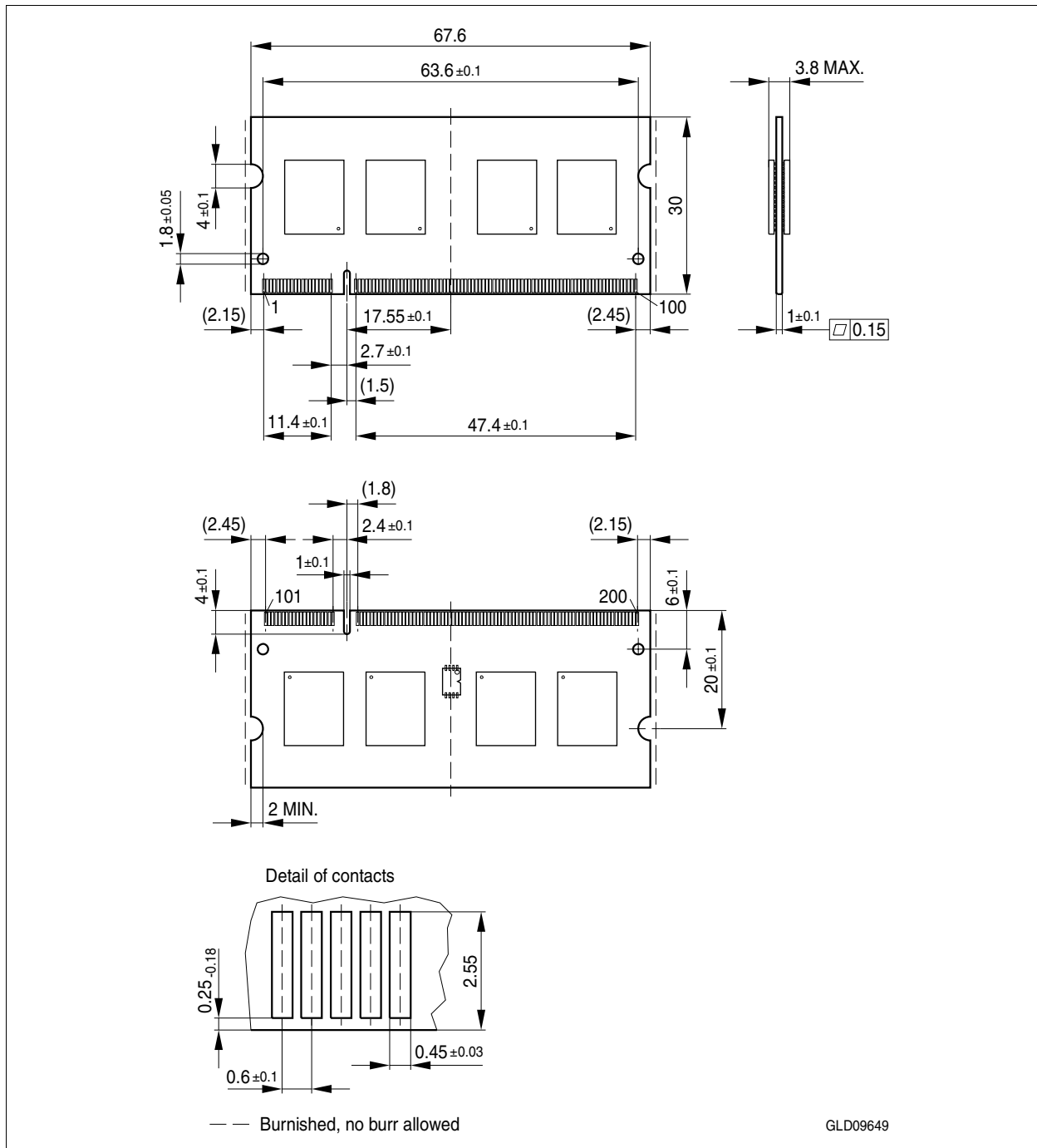


Figure 5 Package Outline Raw Card A L-DIM-200-31



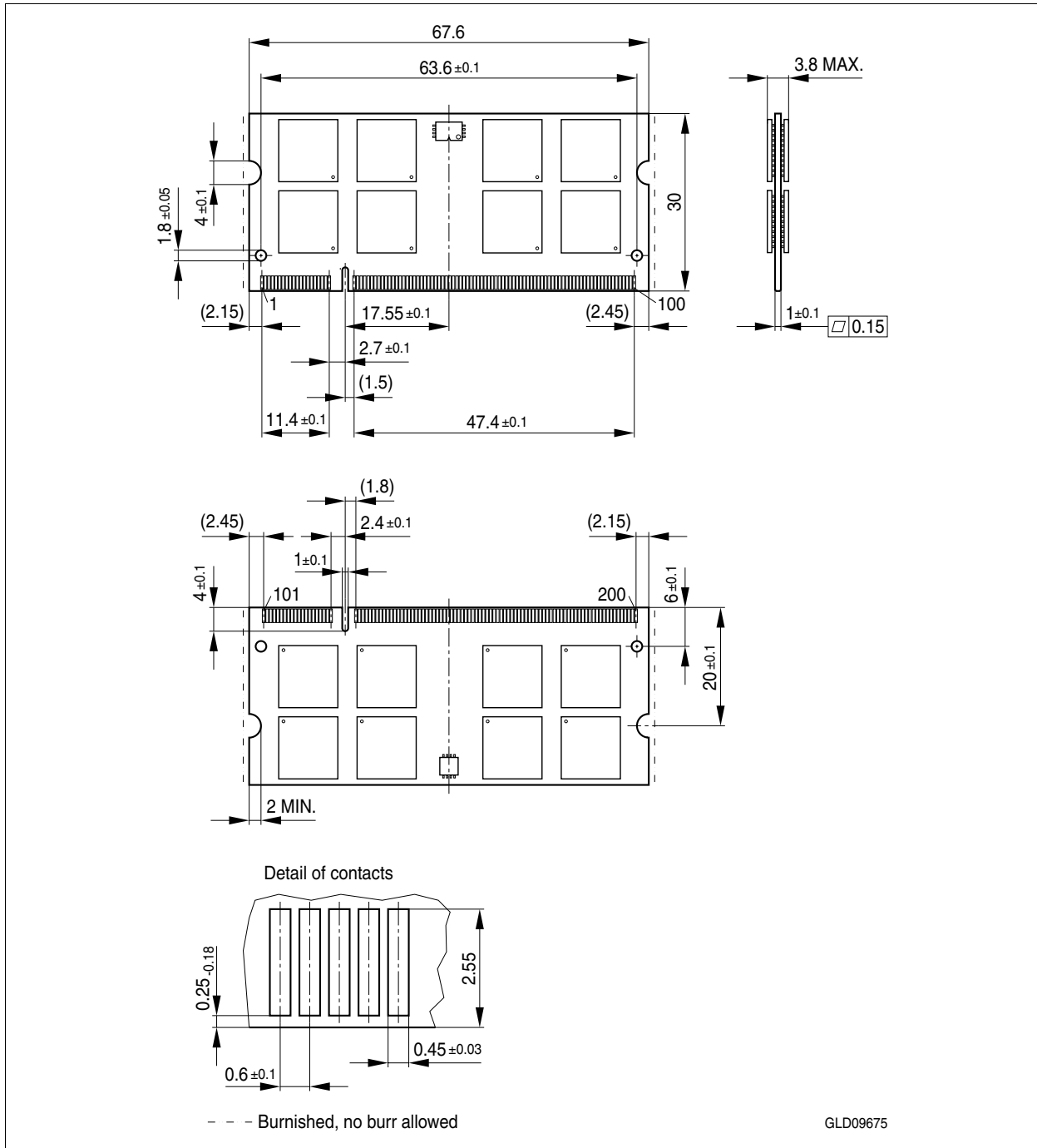


Figure 7 Package Outline Raw Card E L-DIM-200-36

## 6 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Infineon's nomenclature uses simple coding combined with some proprietary coding. [Table 37](#) provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in [Table 38](#) and for components in [Table 39](#).

**Table 37 Nomenclature Fields and Examples**

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
Micro-DIMM	HYS	64	T	64	0	2	0	K	M	-5	-A
DDR2 DRAM	HYB	18	T	512	16		0	A	C	-5	

**Table 38 DDR2 DIMM Nomenclature**

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density <sup>1)</sup>	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-DIMM
		M	Micro-DIMM
		R	Registered
		U	Unbuffered
10	Speed Grade	-3.7	PC2-4200 4-4-4
		-5	PC2-3200 3-3-3
11	Die Revision	-A	First
		-B	Second

1) Multiplying "Memory Density per I/O" with "Module Data Width" and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column "Coding".

**Table 39 DDR2 DRAM Nomenclature**

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL1.8
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
5+6	Number of I/Os	2G	2 Gbit
		40	×4
		80	×8
7	Product Variations	16	×16
		0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	-3.7	DDR2-533C
		-5	DDR2-400B
11	N/A for Components		

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