

HYS64T128020HM-3.7-A HYS64T128020HM-5-A

214-Pin Micro-DIMM-DDR2-SDRAM Modules

MDIMM
DDR2 SDRAM
RoHS Compliant

Memory Products



N e v e r s t o p t h i n k i n g .

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1 Overview

This chapter gives an overview of the 214-Pin Micro-DIMM-DDR2-SDRAM Modules product family and describes its main characteristics.

1.1 Features

List of Micro-DIMM features

- 214-Pin PC2-4200 and PC2-3200 DDR2 SDRAM memory modules for use as main memory when installed in systems such as mobile personal computers.
- 128M × 64 module organisation and 64M × 16 chip organisation
- JEDEC standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Built with 1 Gb DDR2 SDRAMs in P-TFBGA-92 chipsize packages
- Programmable CAS Latencies (3, 4 and 5), Burst Length (8 & 4) and Burst Type
- Burst Refresh, Distributed Refresh and Self Refresh
- All inputs and outputs SSTL_18 compatible
- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- Serial Presence Detect with E²PROM
- Micro-DIMM Dimensions (nominal): 30 mm high, 54.0 mm wide
- Based on JEDEC standard reference layouts Raw Card “B”
- RoHS compliant product¹⁾

Table 1 Performance for DDR2-533 and DDR2-400

Product Type Speed Code			-3.7	-5	Units
Speed Grade			PC2-4200 4-4-4	PC2-3200 3-3-3	—
max. Clock Frequency	@CL5	f_{CK5}	266	200	MHz
	@CL4	f_{CK4}	266	200	MHz
	@CL3	f_{CK3}	200	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	15	ns
min. Row Precharge Time		t_{RP}	15	15	ns
min. Row Active Time		t_{RAS}	45	40	ns
min. Row Cycle Time		t_{RC}	60	55	ns

1.2 Description

The INFINEON HYS64T128020HM-[3.7/5]-A module family are low profile Unbuffered Micro-DIMM modules “MDIMMs” with 30,0 mm height based on DDR2 technology. DIMMs are available as 128M × 64 organisation and density, intended for mounting into 214-pin mezzanine connector sockets. are write protected; the second 128 bytes are available

The memory array is designed with 1 Gb Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E²PROM device using the 2-pin I²C protocol. The first 128 bytes are programmed with configuration data and to the customer.

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.



Table 2 Ordering Information

Product Type ¹⁾	Compliance Code ²⁾	Description	SDRAM Technology
HYS64T128020HM-3.7-A	1GB 2R×16 PC2-4200M-444-11-A0	two ranks 1 GByte DIMM	1 Gbit (×16)
HYS64T128020HM-5-A	1GB 2R×16 PC2-4200M-444-11-A0	two ranks 1 GByte DIMM	1 Gbit (×16)

1) All part numbers end with a place code, designating the silicon die revision. Example: HYS64T128020HM-3.7-A, indicating Rev. "A" dies are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see [Chapter 6](#) of this data sheet.

2) The Compliance Code is printed on the module label and describes the speed grade, e.g. "PC2-4200M-444-11-A0", where 4200M means Micro-DIMM modules with 4.26 GB/sec Module Bandwidth and "444-11" means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.1 and produced on the Raw Card "A".

Table 3 Address Format

DIMM Density	Module Organization	Memory Ranks	# of SDRAMs	# of row/bank/column bits	Raw Card
1 GByte	128M × 64	2	8	13/3/10	A

Table 4 Components on Modules¹⁾

Product Type ²⁾	DRAM Components ²⁾	DRAM Density	DRAM Organisation
HYS64T128020HM-3.7-A	HYB18T1G160AF	1 Gbit	64M × 16
HYS64T128020HM-5-A	HYB18T1G160AF	1 Gbit	64M × 16

1) For a detailed description of all functions of the DRAM components on these modules see the component data sheet.

2) Green Product

2 Pin Configuration and Block Diagrams

2.1 Pin Configuration

The pin configuration of the DDR2 SDRAM Micro-DIMM is listed by function in [Table 5](#) (214 pins). The abbreviations used in columns Pin and Buffer Type are explained in [Table 6](#) and [Table 7](#) respectively. The pin numbering is depicted in [Figure 1](#).

Table 5 Pin Configuration of MDIMM

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
122	CK0	I	SSTL	Clock Signal CK 1:0, Complementary Clock Signal CK 1:0 <i>Note: The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of \overline{CK}. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.</i>
194	CK1	I	SSTL	
123	$\overline{CK0}$	I	SSTL	
195	$\overline{CK1}$	I	SSTL	
Clock Enables 1:0				
43	CKE0	I	SSTL	<i>Note: Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE0 initiates the Power Down Mode or the Self Refresh Mode.</i> 1. 2-rank module
147	CKE1	I	SSTL	
	NC	NC		Not Connected <i>Note: 1-rank module</i>
Control Signals				
Chip Select Rank 1:0				
165	$\overline{S0}$	I	SSTL	<i>Note: Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$. The input signals also disable all outputs (except CKE and ODT) of the register(d) on the DIMM when both inputs are high. When \overline{S} is HIGH, all register outputs (except CK, ODT and Chip select) remain in the previous state.</i> 2. 2-rank module
62	$\overline{S1}$	I	SSTL	
	NC	NC		Not Connected <i>Note: 1-rank module</i>

Table 5 Pin Configuration of MDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
163	$\overline{\text{RAS}}$	I		Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE) <i>Note: When sampled at the cross point of the rising edge of $\overline{\text{CK}}$, and falling edge of $\overline{\text{CK}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.</i>
60	$\overline{\text{CAS}}$	I	SSTL	
56	$\overline{\text{WE}}$	I	SSTL	
Address Signals				
55	BA0	I	SSTL	Bank Address Bus 1:0
162	BA1	I	SSTL	<i>Note: Select internal SDRAM memory bank</i>
46	BA2	I	SSTL	Bank Address Bus 2 <i>Note: Greater than 512Mb DDR2 SDRAMs</i>
	NC	NC	–	Not Connected <i>Note: Less than 1Gb DDR2 SDRAMs</i>
161	A0	I	SSTL	Address Inputs 12:0, Address Input 10/Autoprecharge <i>Note: During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of $\overline{\text{CK}}$ and falling edge of $\overline{\text{CK}}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of $\overline{\text{CK}}$ and falling edge of $\overline{\text{CK}}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA[2:0] defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[2:0] to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA[2:0] inputs. If AP is LOW, then BA[2:0] are used to define which bank to precharge.</i>
159	A1	I	SSTL	
52	A2	I	SSTL	
158	A3	I	SSTL	
51	A4	I	SSTL	
50	A5	I	SSTL	
157	A6	I	SSTL	
48	A7	I	SSTL	
155	A8	I	SSTL	
54	A9	I	SSTL	
	AP	I	SSTL	
47	A10	I	SSTL	
153	A11	I	SSTL	
167	A12	I	SSTL	Address Input 13 <i>Note: Modules based on $\times 4/\times 8$ component</i>
	NC	NC	–	Not Connected <i>Note: Modules based on $\times 16$ component</i>

Table 5 Pin Configuration of MDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Data Signals				
3	DQ0	I/O	SSTL	Data Bus 0:38 <i>Note: Data Input/Output pins</i>
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
109	DQ4	I/O	SSTL	
110	DQ5	I/O	SSTL	
114	DQ6	I/O	SSTL	
115	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
117	DQ12	I/O	SSTL	
118	DQ13	I/O	SSTL	
125	DQ14	I/O	SSTL	
126	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
128	DQ20	I/O	SSTL	
129	DQ21	I/O	SSTL	
133	DQ22	I/O	SSTL	
134	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
38	DQ26	I/O	SSTL	
39	DQ27	I/O	SSTL	
136	DQ28	I/O	SSTL	
137	DQ29	I/O	SSTL	
142	DQ30	I/O	SSTL	
143	DQ31	I/O	SSTL	
67	DQ32	I/O	SSTL	
68	DQ33	I/O	SSTL	
73	DQ34	I/O	SSTL	
74	DQ35	I/O	SSTL	
174	DQ36	I/O	SSTL	
175	DQ37	I/O	SSTL	
179	DQ38	I/O	SSTL	

Table 5 Pin Configuration of MDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
180	DQ39	I/O	SSTL	Data Bus 39:57
76	DQ40	I/O	SSTL	
77	DQ41	I/O	SSTL	
81	DQ42	I/O	SSTL	
82	DQ43	I/O	SSTL	
182	DQ44	I/O	SSTL	
183	DQ45	I/O	SSTL	
188	DQ46	I/O	SSTL	
189	DQ47	I/O	SSTL	
84	DQ48	I/O	SSTL	
85	DQ49	I/O	SSTL	
92	DQ50	I/O	SSTL	
93	DQ51	I/O	SSTL	
191	DQ52	I/O	SSTL	
192	DQ53	I/O	SSTL	
200	DQ54	I/O	SSTL	
201	DQ55	I/O	SSTL	
95	DQ56	I/O	SSTL	
96	DQ57	I/O	SSTL	
101	DQ58	I/O	SSTL	
102	DQ59	I/O	SSTL	
203	DQ60	I/O	SSTL	
204	DQ61	I/O	SSTL	
208	DQ62	I/O	SSTL	
209	DQ63	I/O	SSTL	
7	DQS0	I/O	SSTL	Data Strobes 7:0
6	$\overline{\text{DQS0}}$	I/O	SSTL	
19	DQS1	I/O	SSTL	
18	$\overline{\text{DQS1}}$	I/O	SSTL	
28	DQS2	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
140	DQS3	I/O	SSTL	
139	$\overline{\text{DQS3}}$	I/O	SSTL	
71	DQS4	I/O	SSTL	
70	$\overline{\text{DQS4}}$	I/O	SSTL	
186	DQS5	I/O	SSTL	
185	$\overline{\text{DQS5}}$	I/O	SSTL	
198	DQS6	I/O	SSTL	
197	$\overline{\text{DQS6}}$	I/O	SSTL	
99	DQS7	I/O	SSTL	

Note: The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and DQS. If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to V_{SS} and DDR2 SDRAM mode registers programmed appropriately.

3. See block diagram for corresponding DQ signals

Table 5 Pin Configuration of MDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
98	DQS7	I/O	SSTL	
112	DM0	I	SSTL	Data Masks 7:0 <i>Note: The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect.</i> 4. $\times 8$ based module
120	DM1	I	SSTL	
131	DM2	I	SSTL	
36	DM3	I	SSTL	
177	DM4	I	SSTL	
79	DM5	I	SSTL	
90	DM6	I	SSTL	
206	DM7	I	SSTL	
EEPROM				
105	SCL	I	CMOS	Serial Bus Clock <i>Note: This signal is used to clock data into and out of the SPD EEPROM.</i>
104	SDA	I/O	OD	Serial Bus Data <i>Note: This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to V_{DDSPD} on the motherboard to act as a pull-up.</i>
211	SA0	I	CMOS	Serial Address Select Bus 1:0 <i>Note: Address pins used to select the Serial Presence Detect base address.</i>
213	SA1	I	CMOS	
Power Supplies				
1	V_{REF}	AI	–	I/O Reference Voltage <i>Note: Reference voltage for the SSTL-18 inputs.</i>
42, 45, 49, 53, 57, 61, 64, 146, 149, 152, 156, 160, 164, 168, 171	V_{DD}	PWR	–	Power Supply <i>Note: Power and ground for the DDR SDRAM</i>
107	V_{DDSPD}	PWR	–	EEPROM Power Supply <i>Note: Serial EEPROM positive power supply, wired to a separate power pin at the connector which supports from 1.7 Volt to 3.6 Volt.</i>

Table 5 Pin Configuration of MDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 37, 40, 66, 69, 72, 75, 78, 80, 83, 86, 89, 91, 94, 97, 100, 103, 108, 111, 113, 116, 119, 121, 124, 127, 130, 132, 135, 138, 141, 144, 173, 176, 178, 181, 184, 187, 190, 193, 196, 205, 199, 202, 207, 210	V_{SS}	GND	–	Ground Plane <i>Note: Power and ground for the DDR SDRAM</i>
Other Pins				
166	ODT0	I	SSTL	On-Die Termination Control 1:0
63	ODT1	I	SSTL	<i>Note: Asserts on-die termination for DQ, DM, DQS, and DQS signals if enabled via the DDR2 SDRAM mode register.</i> <i>5. 2-rank module</i>
	NC			Not Connected <i>Note: 1-rank module</i>
15, 16, 41, 44, 58, 59, 65, 87, 88, 106, 145, 148, 150, 151, 167, 169, 170, 172, 212, 214	NC	NC		Not connected <i>Note: Pins not connected on Infineon MDIMMs</i>

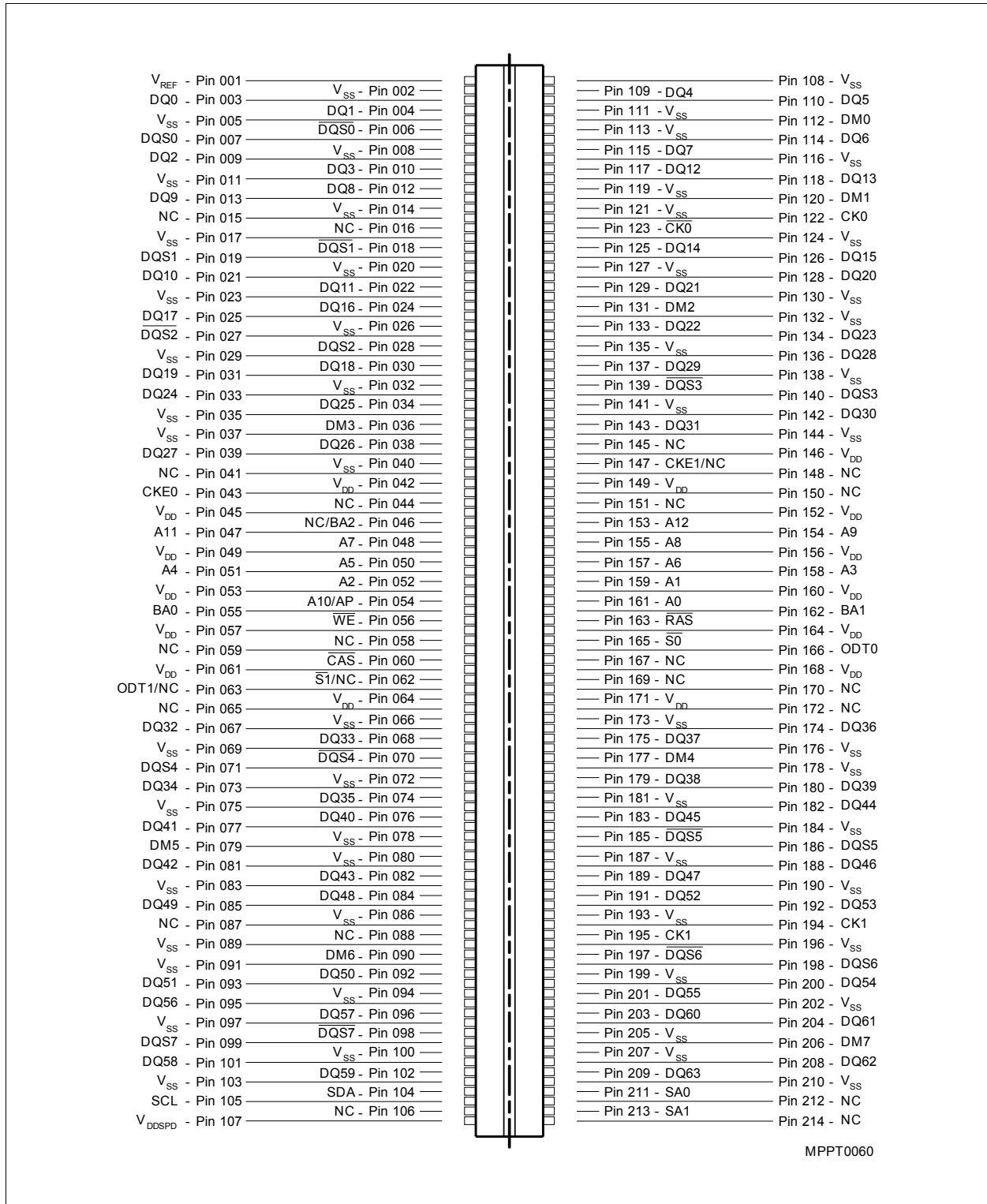
Table 6 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 7 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

Pin Configuration and Block Diagrams



MPPT0060

Figure 1 Pin Configuration for Two-Piece Mezzanine Socket on MDIMM (214 pins)

2.2 Block Diagrams

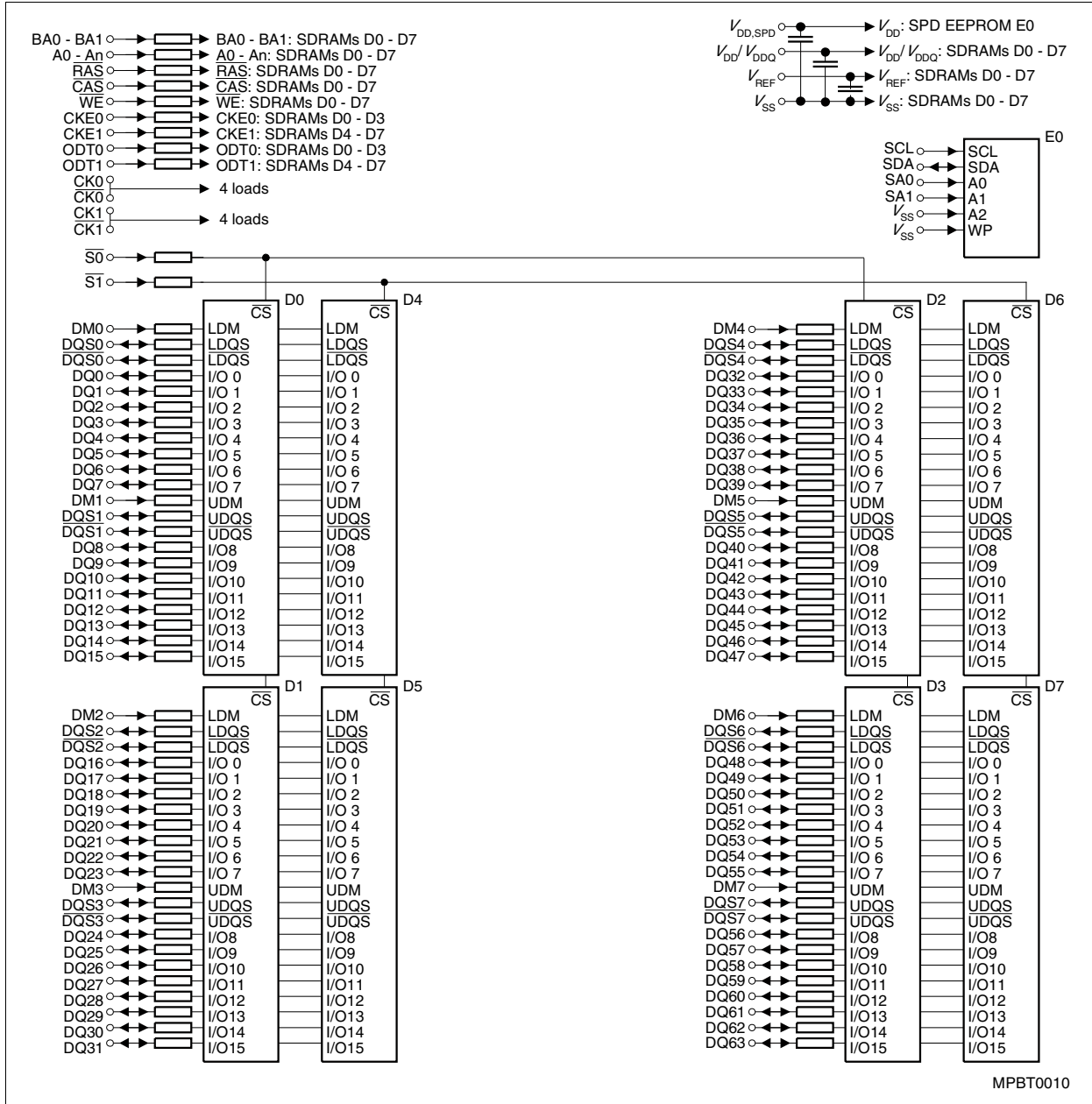


Figure 2 Block Diagram Raw Card A Micro-DIMM (x64, 2 Ranks, x16)

Notes

1. *DQ, DQS, DM resistors are 22 Ω ±5 %*
2. *S0, S1, BAn, An, RAS, CAS, WE, ODT0, ODT1, CKE0, CKE1 resistors are 3 Ω ±5 %*

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 8 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	2.3	V	1)
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0	2.3	V	1)
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5	2.3	V	1)
Storage Humidity (without condensation)	H_{STG}	5	95	%	1)

- 1) Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

3.2 DC Operating Conditions

Table 9 Operating Conditions

Parameter	Symbol	Values		Unit	Notes
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+65	°C	
DRAM Case Temperature	T_{CASE}	0	+95	°C	1)2)3)4)
Storage Temperature	T_{STG}	-50	+100	°C	
Barometric Pressure (operating & storage)	P_{BAR}	+69	+105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	

- 1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.
 2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported
 3) Above 85 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to $t_{REFI} = 3.9 \mu s$
 4) Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 °C Case Temperature before initiating Self-Refresh operation.
 5) Up to 3000 m.

Table 10 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Nom.	Max.		
Device Supply Voltage	VDD	1.7	1.8	1.9	V	
Output Supply Voltage	VDDQ	1.7	1.8	1.9	V	1)
Input Reference Voltage	VREF	0.49 x VDDQ	0.5 x VDDQ	0.51 x VDDQ	V	2)
SPD Supply Voltage	VDDSPD	1.7	—	3.6	V	
DC Input Logic High	VIH (DC)	VREF + 0.125	—	VDDQ + 0.3	V	

Table 10 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Nom.	Max.		
DC Input Logic Low	V _{IL} (DC)	- 0.30	—	V _{REF} - 0.125	V	
In / Output Leakage Current	I _L	- 5	—	5	μA	3)

- 1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
- 2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF(DC)}; V_{REF} is also expected to track noise in V_{DDQ}.
- 3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

3.3 AC Characteristics

3.3.1 Speed Grade Definitions

Table 11 Speed Grade Definition Speed Bins for DDR533 and DDR400

Speed Grade			DDR2-533C		DDR2-400B		Unit	Note
IFX Sort Name			-3.7		-5			
CAS-RCD-RP latencies			4-4-4		3-3-3		t _{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t _{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t _{CK}	3.75	8	5	8	ns	1)2)3)4)
	@ CL = 5	t _{CK}	3.75	8	5	8	ns	1)2)3)4)
Row Active Time		t _{RAS}	45	70000	40	70000	ns	1)2)3)4)5)
Row Cycle Time		t _{RC}	60	—	55	—	ns	1)2)3)4)
RAS-CAS-Delay		t _{RCD}	15	—	15	—	ns	1)2)3)4)
Row Precharge Time		t _{RP}	15	—	15	—	ns	1)2)3)4)

- 1) Timings are guaranteed with CK/CK differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
- 2) The CK/CK input reference level (for timing reference to CK/CK) is the point at which CK and CK cross. The DQS / DQS, RDQS / RDQS, input reference level is the crosspoint when in differential strobe mode
- 3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
- 4) The output timing reference voltage level is V_{TT}.
- 5) t_{RAS,MAX} is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

3.3.2 AC Timing Parameters

Table 12 Timing Parameter by Speed Grade - DDR2-400 & DDR2-533

Parameter	Symbol	DDR2-533		DDR2-400		Unit	Note ¹⁾ 2)3)4)5)6) 7)
		Min.	Max.	Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	t_{AC}	-500	+500	-600	+600	ps	
CAS A to CAS B command period	t_{CCD}	2	—	2	—	t_{CK}	
CK, $\overline{\text{CK}}$ high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	3	—	t_{CK}	
CK, $\overline{\text{CK}}$ low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	$t_{IS} + t_{CK} + t_{IH}$	—	ns	
DQ and DM input hold time (differential data strobe)	$t_{DH}(\text{base})$	225	—	275	—	ps	
DQ and DM input hold time (single ended data strobe)	$t_{DH1}(\text{base})$	-25	—	25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{\text{CK}}$	t_{DQSK}	-450	+450	-500	+500	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	—	350	ps	
Write command to 1st DQS latching transition	t_{DQSS}	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	$t_{DS}(\text{base})$	100	—	150	—	ps	
DQ and DM input setup time (single ended data strobe)	$t_{DS1}(\text{base})$	-25	—	25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	
Four Activate Window period	t_{FAW}	37.5	—	37.5	—	ns	8)9)
		50	—	50	—	ns	10)
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})		MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{\text{CK}}$	t_{HZ}	—	$t_{AC,MAX}$	—	$t_{AC,MAX}$	ps	

Electrical Characteristics

Table 12 Timing Parameter by Speed Grade - DDR2-400 & DDR2-533 (cont'd)

Parameter	Symbol	DDR2-533		DDR2-400		Unit	Note ¹⁾ 2)3)4)5)6) 7)
		Min.	Max.	Min.	Max.		
Address and control input hold time	$t_{IH}(\text{base})$	375	—	475	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	0.6	—	t_{CK}	
Address and control input setup time	$t_{IS}(\text{base})$	250	—	350	—	ps	
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ}(\text{DQ})$	$2 \cdot t_{AC.MIN}$	$t_{AC.MAX}$	$2 \cdot t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{LZ}(\text{DQS})$	$t_{AC.MIN}$	$t_{AC.MAX}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	$t_{HPQ} - t_{QHS}$	—		
Data hold skew factor	t_{QHS}	—	400	—	450	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	—	7.8	μs	
		—	3.9	—	3.9	μs	
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	127.5	—	127.5	—	ns	
Precharge-All (8 banks) command period	t_{RP}	$15 + 1t_{CK}$	—	$15 + 1t_{CK}$	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	7.5	—	ns	
		10	—	10	—	ns	⁹⁾
Internal Read to Precharge command delay	t_{RTP}	7.5	—	7.5	—	ns	
Write preamble	t_{WPRE}	$0.35xt_{CK}$	—	$0.35xt_{CK}$	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{WR}/t_{CK}		t_{CK}	
Internal Write to Read command delay	t_{WTR}	7.5	—	10	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	6 – AL	—	t_{CK}	

Table 12 Timing Parameter by Speed Grade - DDR2-400 & DDR2-533 (cont'd)

Parameter	Symbol	DDR2–533		DDR2–400		Unit	Note ¹⁾ 2)3)4)5)6) 7)
		Min.	Max.	Min.	Max.		
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	$t_{RFC} + 10$	—	$t_{RFC} + 10$	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	200	—	t_{CK}	

- 1) For details and notes see the relevant INFINEON component data sheet
- 2) VDDQ = 1.8V ± 0.1V; VDD = 1.8V ± 0.1 V. See notes ³⁾⁴⁾⁵⁾⁶⁾
- 3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) Timings are guaranteed with CK/CK differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see Chapter 8 of this data sheet. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the Reference Load for Timing Measurements according to Chapter 8.1 only.
- 5) The CK / CK input reference level (for timing reference to CK / CK) is the point at which CK and CK cross. The DQS / DQS, RDQS/ RDQS, input reference level is the crosspoint when in differential strobe mode; The input reference level for signals other than CK/CK, DQS / DQS, RDQS / RDQS is defined in Chapter 8.3 of this data sheet.
- 6) Inputs are not recognized as valid until VREF stabilizes. During the period before VREF stabilizes, CKE = 0.2 x VDDQ is recognized as low.
- 7) The output timing reference voltage level is VTT. See Chapter 8 for the reference load for timing measurements.
- 8) °4 & °8 (1k page size)
- 9) 8 bank device Sequential Activation Restriction. No more than 4 banks may be activated in a rolling t_{FAW} window.
- 10) °16 (2k page size), not on 256 Mbit component

Table 13 Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, $\overline{CK0}$	I	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0-CKEn	I	Active High	Activates the DDR2 SDRAM CK signal when 1 and deactivates the CK signal when 0. By deactivating the clocks, CKE 0 initiates the Power Down Mode or the Self Refresh Mode.
$\overline{S0}$ - \overline{Sn}	I	Active Low	Enables the associated DDR2 SDRAM command decoder when 0 and disables the command decoder when 1. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$. The input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When \overline{S} is high, all register outputs (except CK, ODT and Chip select) remain in the previous state.
RAS, CAS, \overline{WE}	I	Active Low	When sampled at the cross point of the rising edge of CK, and falling edge of CK, RAS, CAS and \overline{WE} define the operation to be executed by the SDRAM.
BA0-BA _n	I	—	Selects internal SDRAM memory bank

Table 13 Input/Output Functional Description

Symbol	Type	Polarity	Function
ODT0-ODTn	I	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR2 SDRAM mode register.
A[9:0], A10/AP, A[n:11]	I	—	During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{\text{CK}}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is 1, autoprecharge is selected and BA0-BA _n defines the bank to be precharged. If AP is 0, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is 1, all banks will be precharged regardless of the state of BA0-BA _n inputs. If AP is 0, then BA0-BA _n are used to define which bank to precharge.
DQ[63:0]	I/O	—	Data Input/Output pins
DM[8:0]	I	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is 0 but blocks the write operation if it is 1. In Read mode, DM lines have no effect.
DQS[17:0], $\overline{\text{DQS}}$ [17:0]	I/O	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{\text{DQS}}$. If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to V_{SS} through a 20 ohm to 10 Kohm resistor and DDR2 SDRAM mode registers programmed appropriately.
V_{DD} , V_{SS}	Supply	—	Power and ground for the DDR SDRAM input buffers and core logic.
V_{REF}	Supply	—	Reference voltage for the SSTL-18 inputs.
V_{DDSPD}	Supply	—	Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.
SDA	I/O	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to to V_{DDSPD} on the motherboard to act as a pull-up.
SCL	I	—	This signal is used to clock data into and out of the SPD EEPROM.

3.3.3 ODT AC Electrical Characteristics

Table 14 ODT AC Electrical Characteristics and Operating Conditions for DDR2-533

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX} + 1 \text{ ns}$	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX} + 0.6 \text{ ns}$	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

- 1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND} .
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD} .

3.4 I_{DD} Specifications and Conditions

Table 15 I_{DD} Measurement Conditions ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾

Parameter	Symbol
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, \overline{CS} is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}
Operating Current 1 One bank Active - Read - Precharge; $I_{OUT} = 0$ mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = CL _{MIN} ; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}
Precharge Standby Current All banks idle; \overline{CS} is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD2N}
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}
Precharge Quiet Standby Current All banks idle; \overline{CS} is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL _{MIN} ; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; $I_{OUT} = 0$ mA.	I_{DD3N}
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL _{MIN} ; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}
Burst Refresh Current $t_{CK} = t_{CK.MIN}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, \overline{CS} is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}
Distributed Refresh Current $t_{CK} = t_{CK.MIN}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and \overline{CS} is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}

Table 15 I_{DD} Measurement Conditions (cont'd)¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾

Parameter	Symbol
Self-Refresh Current CKE \leq 0.2 V; external clock off, CK and $\overline{\text{CK}}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. $I_{\text{out}} = 0$ mA.	I_{DD7}
1) $V_{\text{DDQ}} = 1.8 \text{ V} \pm 0.1 \text{ V}$; $V_{\text{DD}} = 1.8 \text{ V} \pm 0.1 \text{ V}$ 2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled. 3) Definitions for I_{DD} see Table 16 4) I_{DD1} , I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled ($I_{\text{OUT}} = 0$ mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH. 5) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P} 6) For details and notes see the relevant INFINEON component data sheet	

Table 16 Definitions for I_{DD}

Parameter	Description
LOW	$V_{\text{IN}} \leq V_{\text{IL(ac).MAX}}$, HIGH is defined as $V_{\text{IN}} \geq V_{\text{IH(ac).MIN}}$
STABLE	inputs are stable at a HIGH or LOW level
FLOATING	inputs are $V_{\text{REF}} = V_{\text{DDQ}}/2$
SWITCHING	inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes

Table 17 I_{DD} Specification for HYS64T128020HM-3.7-A

Product Type	HYS64T128020HM-3.7-A	Unit	Note ¹⁾
Organization	1 GB		
	2 Ranks		
	×64		
	-3.7		
Symbol	Max.		
I_{DD0}	340	mA	2)
I_{DD1}	400	mA	2)
I_{DD2P}	50	mA	3)
I_{DD2N}	370	mA	3)
I_{DD2Q}	260	mA	3)
I_{DD3P} (MRS = 0)	140	mA	3)
I_{DD3P} (MRS = 1)	50	mA	3)
I_{DD3N}	400	mA	3)
I_{DD4R}	720	mA	2)
I_{DD4W}	800	mA	2)
I_{DD5B}	760	mA	2)
I_{DD5D}	60	mA	3)
I_{DD6}	32	mA	3)
I_{DD7}	1220	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1} , I_{DD4R} , and I_{DD7} , are defined with the outputs disabled.

2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode

3) Both ranks are in the same I_{DD} current mode

Table 18 I_{DD} Specification for HYS64T128020HM-5-A

Product Type	HYS64T128020HM-5-A	Unit	Note ¹⁾
Organization	1 GB		
	2 Ranks		
	×64		
	-5		
Symbol	Max.		
I_{DD0}	320	mA	2)
I_{DD1}	380	mA	2)
I_{DD2P}	50	mA	3)
I_{DD2N}	280	mA	3)
I_{DD2Q}	220	mA	3)
I_{DD3P} (MRS = 0)	100	mA	3)
I_{DD3P} (MRS = 1)	50	mA	3)
I_{DD3N}	320	mA	3)
I_{DD4R}	580	mA	2)
I_{DD4W}	640	mA	2)
I_{DD5B}	740	mA	2)
I_{DD5D}	60	mA	3)
I_{DD6}	32	mA	3)
I_{DD7}	1080	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1} , I_{DD4R} , and I_{DD7} , are defined with the outputs disabled.

2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode

3) Both ranks are in the same I_{DD} current mode

3.4.1 I_{DD} Test Conditions

For testing the I_{DD} parameters, the timing parameters as in [Table 19](#) are used.

Table 19 I_{DD} Measurement Test Conditions for PC2-4200 & PC2-3200

Parameter	Symbol	-3.7	-5	Unit
		PC2-4200-4-4-4	PC2-3200-3-3-3	
CAS Latency	$CL_{(IDD)}$	4	3	t_{CK}
Clock Cycle Time	$t_{CK(IDD)}$	3.75	5	ns
Active to Read or Write delay	$t_{RCD(IDD)}$	15	15	ns
Active to Active / Auto-Refresh command period	$t_{RC(IDD)}$	60	55	ns
Active bank A to Active bank B command delay	$\times 8^{1)}$ $t_{RRD(IDD)}$	7.5	7.5	ns
	$\times 16^{2)}$ $t_{RRD(IDD)}$	10	10	ns
Active to Precharge Command	$t_{RAS.MIN(IDD)}$	45	40	ns
	$t_{RAS.MAX(IDD)}$	70000	70000	ns
Precharge Command Period	$t_{RP(IDD)}$	15	15	ns
Auto-Refresh to Active / Auto-Refresh command period	$t_{RFC(IDD)}$	127.5	127.5	ns
Average periodic Refresh interval	t_{REFI}	7.8	7.8	μs

1) For modules based on $\times 8$ components

2) For modules based on $\times 16$ components

3.4.2 On Die Termination (ODT) Current

On Die Termination (ODT) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A[6,2] in the EMRS(1) a

“weak” or “strong” termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tri-state or driving 0 or 1, as long a ODT is enabled during a given period of time.

Table 20 ODT current per terminated pin

Parameter	Symbol	Min.	Typ.	Max.	Unit	EMRS(1) State
Enabled ODT current per DQ ODT is HIGH; Data Bus inputs are FLOATING	I_{ODTO}	5	6	7.5	mA/DQ	A6 = 0, A2 = 1
		2.5	3	3.75	mA/DQ	A6 = 1, A2 = 0
Active ODT current per DQ ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	I_{ODTT}	10	12	15	mA/DQ	A6 = 0, A2 = 1
		5	6	7.5	mA/DQ	A6 = 1, A2 = 0

Note: For power consumption calculations the ODT duty cycle has to be taken into account

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

- [Table 21 “SPD codes for PC2–4200M–444” on Page 28](#)
- [Table 22 “SPD codes for PC2–3200M–333” on Page 32](#)

Table 21 SPD codes for PC2–4200M–444

Product Type		HYS64T128020HM–3.7–A
Organization		1 GByte
		×64
		2 Ranks (×16)
Label Code		PC2–4200M–444
JEDEC SPD Revision		Rev. 1.1
Byte#	Description	HEX
0	Programmed SPD Bytes in EEPROM	80
1	Total number of Bytes in EEPROM	08
2	Memory Type (DDR2)	08
3	Number of Row Addresses	0D
4	Number of Column Addresses	0A
5	DIMM Rank and Stacking Information	61
6	Data Width	40
7	Not used	00
8	Interface Voltage Level	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	3D
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	50
11	Error Correction Support (non-ECC, ECC)	00
12	Refresh Rate and Type	82
13	Primary SDRAM Width	10
14	Error Checking SDRAM Width	00
15	Not used	00
16	Burst Length Supported	0C
17	Number of Banks on SDRAM Device	08
18	Supported CAS Latencies	38
19	DIMM Mechanical Characteristics	00
20	DIMM Type Information	08
21	DIMM Attributes	00
22	Component Attributes	01
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	3D
24	t_{AC} SDRAM @ $CL_{MAX} -1$ [ns]	50
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50

Table 21 SPD codes for PC2–4200M–444 (cont'd)

Product Type		HYS64T128020HM–3.7–A
Organization		1 GByte
		×64
		2 Ranks (×16)
Label Code		PC2–4200M–444
JEDEC SPD Revision		Rev. 1.1
Byte#	Description	HEX
26	t_{AC} SDRAM @ $CL_{MAX} - 2$ [ns]	60
27	$t_{RP.MIN}$ [ns]	3C
28	$t_{RRD.MIN}$ [ns]	28
29	$t_{RCD.MIN}$ [ns]	3C
30	$t_{RAS.MIN}$ [ns]	2D
31	Module Density per Rank	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37
34	$t_{DS.MIN}$ [ns]	10
35	$t_{DH.MIN}$ [ns]	22
36	$t_{WR.MIN}$ [ns]	3C
37	$t_{WTR.MIN}$ [ns]	1E
38	$t_{RTP.MIN}$ [ns]	1E
39	Analysis Characteristics	00
40	t_{RC} and t_{RFC} Extension	00
41	$t_{RC.MIN}$ [ns]	3C
42	$t_{RFC.MIN}$ [ns]	7F
43	$t_{CK.MAX}$ [ns]	80
44	$t_{DQSQ.MAX}$ [ns]	1E
45	$t_{QHS.MAX}$ [ns]	28
46	PLL Relock Time	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	54
48	Psi(T-A) DRAM	58
49	ΔT_0 (DT0)	37
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	26
51	ΔT_{2P} (DT2P)	20
52	ΔT_{3N} (DT3N)	1C
53	$\Delta T_{3P.fast}$ (DT3P fast)	1C
54	$\Delta T_{3P.slow}$ (DT3P slow)	14
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	4A
56	ΔT_{5B} (DT5B)	1F
57	ΔT_7 (DT7)	32
58	Psi(ca) PLL	00
59	Psi(ca) REG	00
60	ΔT_{PLL} (DTPLL)	00

Table 21 SPD codes for PC2–4200M–444 (cont'd)

Product Type		HYS64T128020HM–3.7–A
Organization		1 GByte
		×64
		2 Ranks (×16)
Label Code		PC2–4200M–444
JEDEC SPD Revision		Rev. 1.1
Byte#	Description	HEX
61	ΔT_{REG} (DTREG) / Toggle Rate	00
62	SPD Revision	11
63	Checksum of Bytes 0-62	F3
64	JEDEC ID Code of Infineon (1)	C1
65	JEDEC ID Code of Infineon (2)	00
66	JEDEC ID Code of Infineon (3)	00
67	JEDEC ID Code of Infineon (4)	00
68	JEDEC ID Code of Infineon (5)	00
69	JEDEC ID Code of Infineon (6)	00
70	JEDEC ID Code of Infineon (7)	00
71	JEDEC ID Code of Infineon (8)	00
72	Module Manufacturer Location	xx
73	Product Type, Char 1	36
74	Product Type, Char 2	34
75	Product Type, Char 3	54
76	Product Type, Char 4	31
77	Product Type, Char 5	32
78	Product Type, Char 6	38
79	Product Type, Char 7	30
80	Product Type, Char 8	32
81	Product Type, Char 9	30
82	Product Type, Char 10	48
83	Product Type, Char 11	4D
84	Product Type, Char 12	33
85	Product Type, Char 13	2E
86	Product Type, Char 14	37
87	Product Type, Char 15	41
88	Product Type, Char 16	20
89	Product Type, Char 17	20
90	Product Type, Char 18	20
91	Module Revision Code	2x
92	Test Program Revision Code	xx
93	Module Manufacturing Date Year	xx
94	Module Manufacturing Date Week	xx

Table 21 SPD codes for PC2-4200M-444 (cont'd)

Product Type		HYS64T128020HM-3.7-A
Organization		1 GByte
		×64
		2 Ranks (×16)
Label Code		PC2-4200M-444
JEDEC SPD Revision		Rev. 1.1
Byte#	Description	HEX
95 - 98	Module Serial Number	xx
99 - 127	Not used	00

Table 22 SPD codes for PC2-3200M-333

Product Type		HYS64T128020HM-5-A
Organization		1 GByte
		×64
		2 Ranks (×16)
Label Code		PC2-3200M-333
JEDEC SPD Revision		Rev. 1.1
Byte#	Description	HEX
0	Programmed SPD Bytes in EEPROM	80
1	Total number of Bytes in EEPROM	08
2	Memory Type (DDR2)	08
3	Number of Row Addresses	0D
4	Number of Column Addresses	0A
5	DIMM Rank and Stacking Information	61
6	Data Width	40
7	Not used	00
8	Interface Voltage Level	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	50
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	60
11	Error Correction Support (non-ECC, ECC)	00
12	Refresh Rate and Type	82
13	Primary SDRAM Width	10
14	Error Checking SDRAM Width	00
15	Not used	00
16	Burst Length Supported	0C
17	Number of Banks on SDRAM Device	08
18	Supported CAS Latencies	38
19	DIMM Mechanical Characteristics	00
20	DIMM Type Information	08
21	DIMM Attributes	00
22	Component Attributes	01
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	50
24	t_{AC} SDRAM @ $CL_{MAX} -1$ [ns]	60
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50
26	t_{AC} SDRAM @ $CL_{MAX} -2$ [ns]	60
27	$t_{RP.MIN}$ [ns]	3C
28	$t_{RRD.MIN}$ [ns]	28
29	$t_{RCD.MIN}$ [ns]	3C
30	$t_{RAS.MIN}$ [ns]	28
31	Module Density per Rank	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	35
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	47

Table 22 SPD codes for PC2-3200M-333 (cont'd)

Product Type		HYS64T128020HM-5-A
Organization		1 GByte
		×64
		2 Ranks (×16)
Label Code		PC2-3200M-333
JEDEC SPD Revision		Rev. 1.1
Byte#	Description	HEX
34	$t_{DS.MIN}$ [ns]	15
35	$t_{DH.MIN}$ [ns]	27
36	$t_{WR.MIN}$ [ns]	3C
37	$t_{WTR.MIN}$ [ns]	28
38	$t_{RTP.MIN}$ [ns]	1E
39	Analysis Characteristics	00
40	t_{RC} and t_{RFC} Extension	00
41	$t_{RC.MIN}$ [ns]	37
42	$t_{RFC.MIN}$ [ns]	7F
43	$t_{CK.MAX}$ [ns]	80
44	$t_{DQSQ.MAX}$ [ns]	23
45	$t_{QHS.MAX}$ [ns]	2D
46	PLL Relock Time	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	53
48	Psi(T-A) DRAM	58
49	ΔT_0 (DT0)	33
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	1D
51	ΔT_{2P} (DT2P)	20
52	ΔT_{3N} (DT3N)	16
53	$\Delta T_{3P.fast}$ (DT3P fast)	16
54	$\Delta T_{3P.slow}$ (DT3P slow)	14
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	3A
56	ΔT_{5B} (DT5B)	1E
57	ΔT_7 (DT7)	2C
58	Psi(ca) PLL	00
59	Psi(ca) REG	00
60	ΔT_{PLL} (DTPLL)	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00
62	SPD Revision	11
63	Checksum of Bytes 0-62	3C
64	JEDEC ID Code of Infineon (1)	C1
65	JEDEC ID Code of Infineon (2)	00
66	JEDEC ID Code of Infineon (3)	00
67	JEDEC ID Code of Infineon (4)	00
68	JEDEC ID Code of Infineon (5)	00

Table 22 SPD codes for PC2–3200M–333 (cont'd)

Product Type		HYS64T128020HM–5–A
Organization		1 GByte
		×64
		2 Ranks (×16)
Label Code		PC2–3200M–333
JEDEC SPD Revision		Rev. 1.1
Byte#	Description	HEX
69	JEDEC ID Code of Infineon (6)	00
70	JEDEC ID Code of Infineon (7)	00
71	JEDEC ID Code of Infineon (8)	00
72	Module Manufacturer Location	xx
73	Product Type, Char 1	36
74	Product Type, Char 2	34
75	Product Type, Char 3	54
76	Product Type, Char 4	31
77	Product Type, Char 5	32
78	Product Type, Char 6	38
79	Product Type, Char 7	30
80	Product Type, Char 8	32
81	Product Type, Char 9	30
82	Product Type, Char 10	48
83	Product Type, Char 11	4D
84	Product Type, Char 12	35
85	Product Type, Char 13	41
86	Product Type, Char 14	20
87	Product Type, Char 15	20
88	Product Type, Char 16	20
89	Product Type, Char 17	20
90	Product Type, Char 18	20
91	Module Revision Code	2x
92	Test Program Revision Code	xx
93	Module Manufacturing Date Year	xx
94	Module Manufacturing Date Week	xx
95 - 98	Module Serial Number	xx
99 - 127	Not used	00

5 Package Outlines

Package Outline of Raw Card A for NDIMM

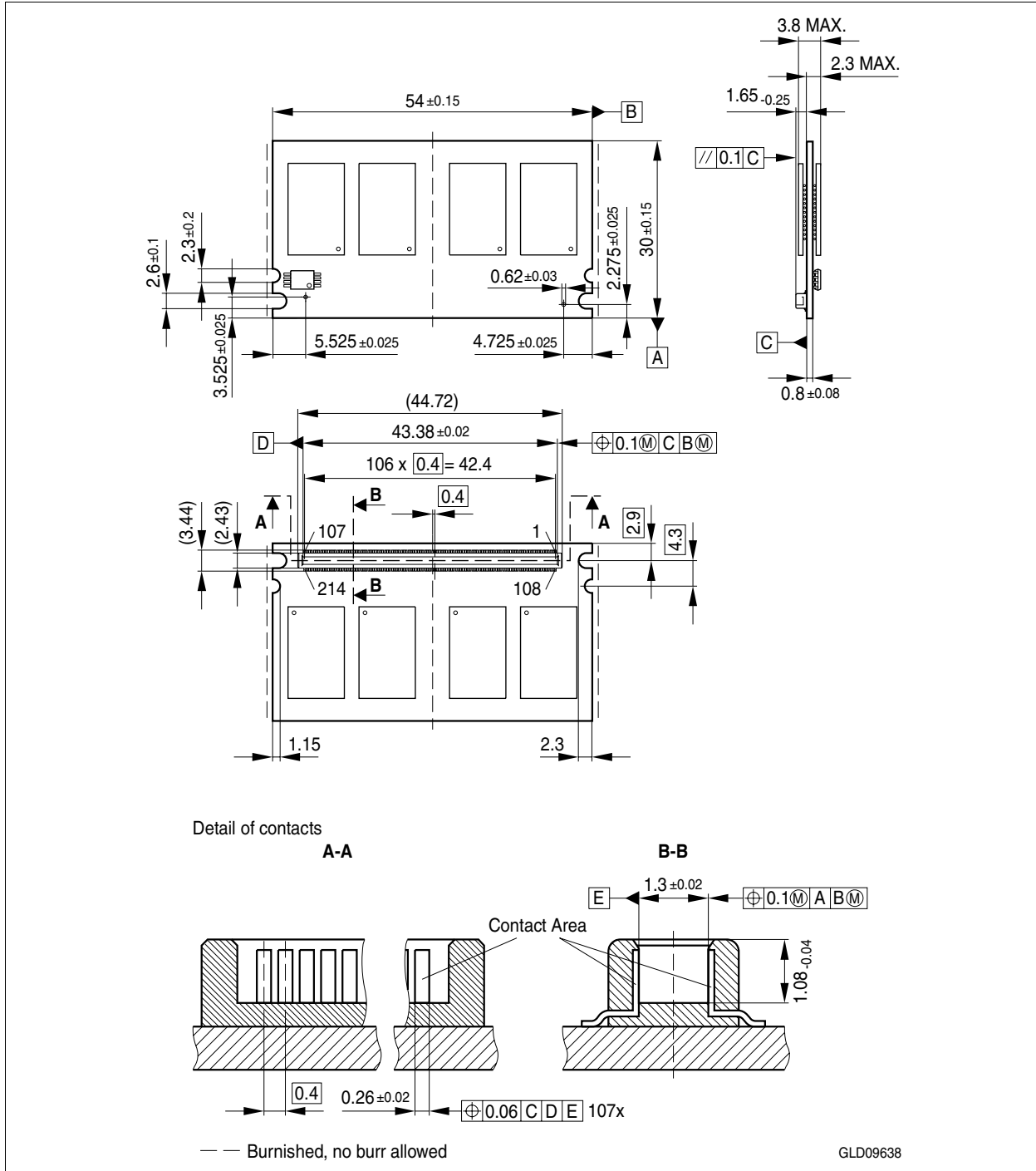


Figure 3 Package Outline Raw Card A L-DIM-214-1

6 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Infineon's nomenclature uses simple coding combined with some proprietary coding. **Table 23** provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 24** and for components in **Table 25**.

Table 23 Nomenclature Fields and Examples

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
Micro-DIMM	HYS	64	T	128	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	1G	16		0	A	C	–5	

Table 24 DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density ¹⁾	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-DIMM
		M	Micro-DIMM
		R	Registered
		U	Unbuffered
10	Speed Grade	–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–3.7F	PC2–4200 CL3
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying "Memory Density per I/O" with "Module Data Width" and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column "Coding".

Table 25 DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL1.8
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–2.5	DDR2-800E 6-6-6
		–3	DDR2-667C 4-4-4
		–3S	DDR2-667D 5-5-5
		–3.7	DDR2-533C 4-4-4
		–3.7F	DDR2-533C CL3
		–5	DDR2-400B 3-3-3
11	N/A for Components		

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