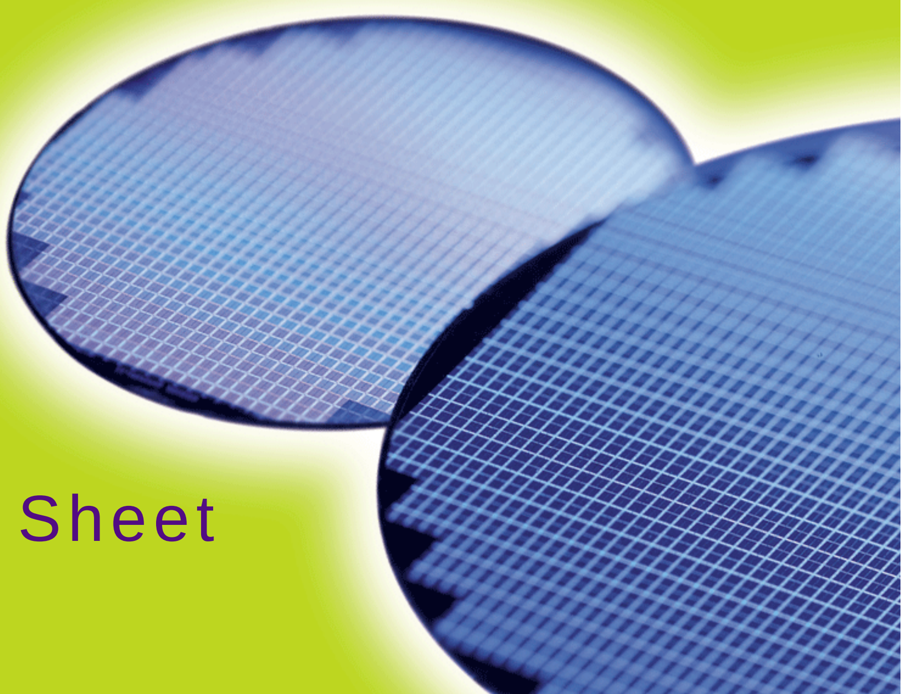
June 2008

# HYS64T128020EMV–2.5C2
# HYS64T128020EMV–3S–C2

*214-Pin 1.5V Unbuffered DDR2 SDRAM MicroDIMM Modules*
*MDIMM SDRAM*
*EU RoHS Compliant*



# Internet Data Sheet

*Rev. 1.00*

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| **HYS64T128020EMV–2.5C2, HYS64T128020EMV–3S–C2**<br><br>**Revision History: 2008-06, Rev. 1.00** | |
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| All | New Document |

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# 1 Overview

This chapter gives an overview of the 214-pin Micro-DIMM DDR2 SDRAM modules product family and describes its main characteristics.

## 1.1 Features

- 214-Pin PC2-6400 and PC2-5300 DDR2 SDRAM memory modules.
- Two rank 128M × 64 module organization, and 64M × 16 chip organization.
- 1GB Modules built with 1 Gbit DDR2 SDRAMs in chipsize packages PG-TFBGA-84.
- Power Supply
  $V_{DD.MIN} = V_{DDQ.MIN}$ =1.45 V
  $V_{DD.NOMINAL} = V_{DDQ.NOMINAL}$ =1.50 V
  $V_{DD.MAX} = V_{DDQ.MAX}$ =1.9 V
- All speed grades faster than DDR2-400 comply with DDR2-400 timing specifications.
- Programmable CAS Latencies (3, 4, 5, 6 and 7), Burst Length (8 & 4).
- Auto Refresh (CBR) and Self Refresh.
- Auto Refresh for temperatures above 85 °C $t_{REFI}$ = 3.9 µs.
- Programmable self refresh rate via EMRS2 setting.
- Programmable partial array refresh via EMRS2 settings.
- DCC enabling via EMRS2 setting.
- All inputs and outputs SSTL_1.5 and SSTL_1.8 compatible.
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT).
- 2-piece type Mezzanine Socket with 0,4 mm contact centers.
- Serial Presence Detect with $E^2$PROM.
- MDIMM Dimensions (nominal): 30 mm high, 54 mm wide
- Based on standard reference layouts Raw Cards 'A'.
- RoHS compliant products[1].

**TABLE 1**
**Performance Table**

| **QAG Speed Code** | | | **–2.5** | **–3S** | **Unit** | **Note** |
|---|---|---|---|---|---|---|
| **DRAM Speed Grade** | | **DDR2** | **–800E** | **–667D** | | |
| **Module Speed Grade** | | **PC2** | **–6400E** | **–5300D** | | |
| **CAS-RCD-RP latencies** | | | **6–6–6** | **5–5–5** | $t_{CK}$ | |
| Max. Clock Frequency | CL3 | $f_{CK3}$ | 200 | 200 | MHz | |
| | CL4 | $f_{CK4}$ | 266 | 266 | MHz | |
| | CL5 | $f_{CK5}$ | 333 | 333 | MHz | |
| | CL6 | $f_{CK6}$ | 400 | – | MHz | |
| Min. RAS-CAS-Delay | | $t_{RCD}$ | 15 | 15 | ns | |
| Min. Row Precharge Time | | $t_{RP}$ | 15 | 15 | ns | |
| Min. Row Active Time | | $t_{RAS}$ | 45 | 45 | ns | |

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit **www.qimonda.com/green_products** .

| QAG Speed Code | | –2.5 | –3S | Unit | Note |
|---|---|---|---|---|---|
| DRAM Speed Grade | DDR2 | –800E | –667D | | |
| Module Speed Grade | PC2 | –6400E | –5300D | | |
| CAS-RCD-RP latencies | | 6–6–6 | 5–5–5 | $t_{CK}$ | |
| Min. Row Cycle Time | $t_{RC}$ | 60 | 60 | ns | |
| Precharge-All (8 banks) command period | $t_{PREA}$ | 17.5 | 18 | ns | 1)2) |

1) This $t_{PREA}$ value is the minimum value at which this chip will be functional.
2) Precharge-All command for an 8 bank device will equal to $t_{RP}$ + 1 × $t_{CK}$ or $t_{nRP}$ + 1 × nCK, depending on the speed bin, where $t_{nRP}$ = RU{ $t_{RP}$ / $t_{CK(avg)}$ } and $t_{RP}$ is the value for a single bank precharge.

## 1.2 Description

The Qimonda HYS64T128020EMV–[2.5/3S](–)C2 module family are Micro-DIMM modules “MDIMMs” with 30 mm height based on DDR2 technology. DIMMs are available as non-ECC modules in128M × 64 (1GB) in organization and density, intended for mounting into 214-pin connector sockets.

The memory array is designed with 1 Gbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial $E^2$PROM device using the 2-pin $I^2$C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.

green Product

**TABLE 2**
**Ordering Information**

| Product Type[1] | Compliance Code[2] | Description | SDRAM Technology |
|---|---|---|---|
| **PC2-6400 (6-6-6)** | | | |
| HYS64T128020EMV-2.5C2 | 1GB 2R×16 PC2–6400M–666–12–A0 | 2 Ranks, Non-ECC | 1Gbit (×16) |
| **PC2-5300 (5-5-5)** | | | |
| HYS64T128020EMV-3S-C2 | 1GB 2R×16 PC2–5300M–555–12–A0 | 2 Ranks, Non-ECC | 1Gbit (×16) |

1) For detailed information regarding Product Type of Qimonda please see chapter "Product Type Nomenclature" of this data sheet.
2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC2–6400M–666–12–A0" where 6400M means Micro-DIMM modules with 6.40 GB/sec Module Bandwidth and "666–12" means Column Address Strobe (CAS) latency =6, Row Column Delay (RCD) latency = 6 and Row Precharge (RP) latency = 6 using the Industry Standard SPD Revision 1.2 and produced on the Raw Card "A".

**TABLE 3**
**Address Format**

| DIMM Density | Module Organization | Memory Ranks | ECC/ Non-ECC | # of SDRAMs | # of row/bank/column bits | Raw Card |
|---|---|---|---|---|---|---|
| 1GB | 128M × 64 | 2 | Non-ECC | 8 | 13/3/10 | A |

**TABLE 4**
**Components on Modules**

| Product Type[1)2)] | DRAM Components[1)] | DRAM Density | DRAM Organisation |
|---|---|---|---|
| HYS64T128020EMV | HYB15T1G160C2F | 1Gbit | 64M × 16 |

1) Green Product
2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

# 2 Pin Configurations

## 2.1 Pin Configurations

The pin configuration of the DDR2 SDRAM Micro-DIMM is listed by function in **Table 5** (214 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1**.

**TABLE 5**
**Pin Configuration of MDIMM**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Clock Signals** | | | | |
| 122 | CK0 | I | SSTL | **Clock Signal CK 1:0, Complementary Clock Signal CK 1:0**<br>Note: *The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.* |
| 194 | CK1 | I | SSTL | |
| 123 | $\overline{CK0}$ | I | SSTL | |
| 195 | $\overline{CK1}$ | I | SSTL | |
| 43 | CKE0 | I | SSTL | **Clock Enables 1:0**<br>**Notes:**<br>1. *Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE0 initiates the Power Down Mode or the Self Refresh Mode.*<br>2. *2-rank module* |
| 147 | CKE1 | I | SSTL | |
| | NC | NC | | **Not Connected**<br>Note: *1-rank module* |
| **Control Signals** | | | | |
| 165 | $\overline{S0}$ | I | SSTL | **Chip Select Rank 1:0**<br>**Notes:**<br>1. *Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$.*<br>2. *2-rank module* |
| 62 | $\overline{S1}$ | I | SSTL | |
| | NC | NC | | **Not Connected**<br>Note: *1-rank module* |

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 163 | $\overline{RAS}$ | I | | **Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**<br>Note: *When sampled at the cross point of the rising edge of CK,and falling edge of $\overline{CK}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.* |
| 60 | $\overline{CAS}$ | I | SSTL | |
| 56 | $\overline{WE}$ | I | SSTL | |
| **Address Signals** | | | | |
| 55 | BA0 | I | SSTL | **Bank Address Bus 1:0**<br>Note: *Select internal SDRAM memory bank* |
| 162 | BA1 | I | SSTL | |
| 46 | BA2 | I | SSTL | **Bank Address Bus 2**<br>Note: *Greater than 512Mb DDR2 SDRAMS* |
| | NC | NC | – | **Not Connected**<br>Note: *Less than 1Gb DDR2 SDRAMS* |
| 161 | A0 | I | SSTL | **Address Inputs 12:0, Address Input 10/Autoprecharge**<br>Note: *During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA[2:0] defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[2:0] to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA[2:0] inputs. If AP is LOW, then BA[2:0] are used to define which bank to precharge.* |
| 159 | A1 | I | SSTL | |
| 52 | A2 | I | SSTL | |
| 158 | A3 | I | SSTL | |
| 51 | A4 | I | SSTL | |
| 50 | A5 | I | SSTL | |
| 157 | A6 | I | SSTL | |
| 48 | A7 | I | SSTL | |
| 155 | A8 | I | SSTL | |
| 154 | A9 | I | SSTL | |
| 54 | A10 | I | SSTL | |
| | AP | I | SSTL | |
| 47 | A11 | I | SSTL | |
| 153 | A12 | I | SSTL | |
| 167 | A13 | I | SSTL | **Address Input 13**<br>Note: *Modules based on ×4/×8 component* |
| | NC | NC | – | **Not Connected**<br>Note: *Modules based on ×16 component* |
| **Data Signals** | | | | |
| 3 | DQ0 | I/O | SSTL | **Data Bus 63:0**<br>Note: *Data Input / Output pins* |
| 4 | DQ1 | I/O | SSTL | |
| 9 | DQ2 | I/O | SSTL | |
| 10 | DQ3 | I/O | SSTL | |
| 109 | DQ4 | I/O | SSTL | |
| 110 | DQ5 | I/O | SSTL | |
| 114 | DQ6 | I/O | SSTL | |
| 115 | DQ7 | I/O | SSTL | |
| 12 | DQ8 | I/O | SSTL | |
| 13 | DQ9 | I/O | SSTL | |

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 21 | DQ10 | I/O | SSTL | **Data Bus 63:0**<br>*Note: Data Input / Output pins* |
| 22 | DQ11 | I/O | SSTL | |
| 117 | DQ12 | I/O | SSTL | |
| 118 | DQ13 | I/O | SSTL | |
| 125 | DQ14 | I/O | SSTL | |
| 126 | DQ15 | I/O | SSTL | |
| 24 | DQ16 | I/O | SSTL | |
| 25 | DQ17 | I/O | SSTL | |
| 30 | DQ18 | I/O | SSTL | |
| 31 | DQ19 | I/O | SSTL | |
| 128 | DQ20 | I/O | SSTL | |
| 129 | DQ21 | I/O | SSTL | |
| 133 | DQ22 | I/O | SSTL | |
| 134 | DQ23 | I/O | SSTL | |
| 33 | DQ24 | I/O | SSTL | |
| 34 | DQ25 | I/O | SSTL | |
| 38 | DQ26 | I/O | SSTL | |
| 39 | DQ27 | I/O | SSTL | |
| 136 | DQ28 | I/O | SSTL | |
| 137 | DQ29 | I/O | SSTL | |
| 142 | DQ30 | I/O | SSTL | |
| 143 | DQ31 | I/O | SSTL | |
| 67 | DQ32 | I/O | SSTL | |
| 68 | DQ33 | I/O | SSTL | |
| 73 | DQ34 | I/O | SSTL | |
| 74 | DQ35 | I/O | SSTL | |
| 174 | DQ36 | I/O | SSTL | |
| 175 | DQ37 | I/O | SSTL | |
| 179 | DQ38 | I/O | SSTL | |
| 180 | DQ39 | I/O | SSTL | |
| 76 | DQ40 | I/O | SSTL | |
| 77 | DQ41 | I/O | SSTL | |
| 81 | DQ42 | I/O | SSTL | |
| 82 | DQ43 | I/O | SSTL | |
| 182 | DQ44 | I/O | SSTL | |
| 183 | DQ45 | I/O | SSTL | |
| 188 | DQ46 | I/O | SSTL | |
| 189 | DQ47 | I/O | SSTL | |
| 84 | DQ48 | I/O | SSTL | |
| 85 | DQ49 | I/O | SSTL | |

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 92 | DQ50 | I/O | SSTL | **Data Bus 63:0** *Note: Data Input / Output pins* |
| 93 | DQ51 | I/O | SSTL | |
| 191 | DQ52 | I/O | SSTL | |
| 192 | DQ53 | I/O | SSTL | |
| 200 | DQ54 | I/O | SSTL | |
| 201 | DQ55 | I/O | SSTL | |
| 95 | DQ56 | I/O | SSTL | |
| 96 | DQ57 | I/O | SSTL | |
| 101 | DQ58 | I/O | SSTL | |
| 102 | DQ59 | I/O | SSTL | |
| 203 | DQ60 | I/O | SSTL | |
| 204 | DQ61 | I/O | SSTL | |
| 208 | DQ62 | I/O | SSTL | |
| 209 | DQ63 | I/O | SSTL | |
| 7 | DQS0 | I/O | SSTL | **Data Strobe Bus 7:0 and Complementary Data Strobe Bus 7:0** **Notes:** 1. *The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and DQS. If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to $V_{SS}$ and DDR2 SDRAM mode registers programmed appropriately.* 2. *See block diagram for corresponding DQ signals* |
| 6 | $\overline{\text{DQS0}}$ | I/O | SSTL | |
| 19 | DQS1 | I/O | SSTL | |
| 18 | $\overline{\text{DQS1}}$ | I/O | SSTL | |
| 28 | DQS2 | I/O | SSTL | |
| 27 | $\overline{\text{DQS2}}$ | I/O | SSTL | |
| 140 | DQS3 | I/O | SSTL | |
| 139 | $\overline{\text{DQS3}}$ | I/O | SSTL | |
| 71 | DQS4 | I/O | SSTL | |
| 70 | $\overline{\text{DQS4}}$ | I/O | SSTL | |
| 186 | DQS5 | I/O | SSTL | |
| 185 | $\overline{\text{DQS5}}$ | I/O | SSTL | |
| 198 | DQS6 | I/O | SSTL | |
| 197 | $\overline{\text{DQS6}}$ | I/O | SSTL | |
| 99 | DQS7 | I/O | SSTL | |
| 98 | $\overline{\text{DQS7}}$ | I/O | SSTL | |
| 112 | DM0 | I | SSTL | **Data Masks 7:0** *Note: The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect.* |
| 120 | DM1 | I | SSTL | |
| 131 | DM2 | I | SSTL | |
| 36 | DM3 | I | SSTL | |
| 177 | DM4 | I | SSTL | |
| 79 | DM5 | I | SSTL | |
| 90 | DM6 | I | SSTL | |
| 206 | DM7 | I | SSTL | |
| **EEPROM** | | | | |

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 105 | SCL | I | CMOS | **Serial Bus Clock**<br>*Note: This signal is used to clock data into and out of the SPD EEPROM.* |
| 104 | SDA | I/O | OD | **Serial Bus Data**<br>*Note: This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to* $V_{DDSPD}$ *on the motherboard to act as a pull-up.* |
| 211 | SA0 | I | CMOS | **Serial Address Select Bus 1:0**<br>*Note: Address pins used to select the Serial Presence Detect base address.* |
| 213 | SA1 | I | CMOS | |
| **Power Supplies** | | | | |
| 1 | $V_{REF}$ | AI | – | **I/O Reference Voltage**<br>*Note: Reference voltage for the SSTL_15 and SSTL_18 inputs.* |
| 42, 45, 49, 53, 57, 61, 64, 146, 149, 152, 156, 160, 164, 168, 171 | $V_{DD}$ | PWR | – | **Power Supply**<br>*Note: Power and ground for the DDR SDRAM* |
| 107 | $V_{DDSPD}$ | PWR | – | **EEPROM Power Supply**<br>*Note: Serial EEPROM positive power supply, wired to a separate power pin at the connector which supports from 1.45 Volt to 3.6 Volt.* |
| 2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 37, 40, 66, 69, 72, 75, 78, 80, 83, 86, 89, 91, 94, 97, 100, 103, 108, 111, 113, 116, 119, 121, 124, 127, 130, 132, 135, 138, 141, 144, 173, 176, 178, 181, 184, 187, 190, 193, 196, 205, 199, 202, 207, 210 | $V_{SS}$ | GND | – | **Ground Plane**<br>*Note: Power and ground for the DDR2 SDRAM, DRAM's are DDR2 components and EEPROM are also connected to GND.* |
| **Other Pins** | | | | |

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 166 | ODT0 | I | SSTL | **On-Die Termination Control 1:0**<br>**Notes:**<br>*1. Asserts on-die termination for DQ, DM, DQS, and DQS\signals if enabled via the DDR2 SDRAM mode register.*<br>*2. 2-rank module* |
| 63 | ODT1 | I | SSTL | |
| | NC | | | **Not Connected**<br>*Note: 1-rank module* |
| 15, 16, 41, 44, 58, 59, 65, 87, 88, 106, 145, 148, 150, 151, 167, 169, 170, 172, 212, 214 | NC | NC | | **Not connected**<br>*Note: Pins not connected on Qimonda MDIMMs* |

## TABLE 6
### Abbreviations for Pin Type

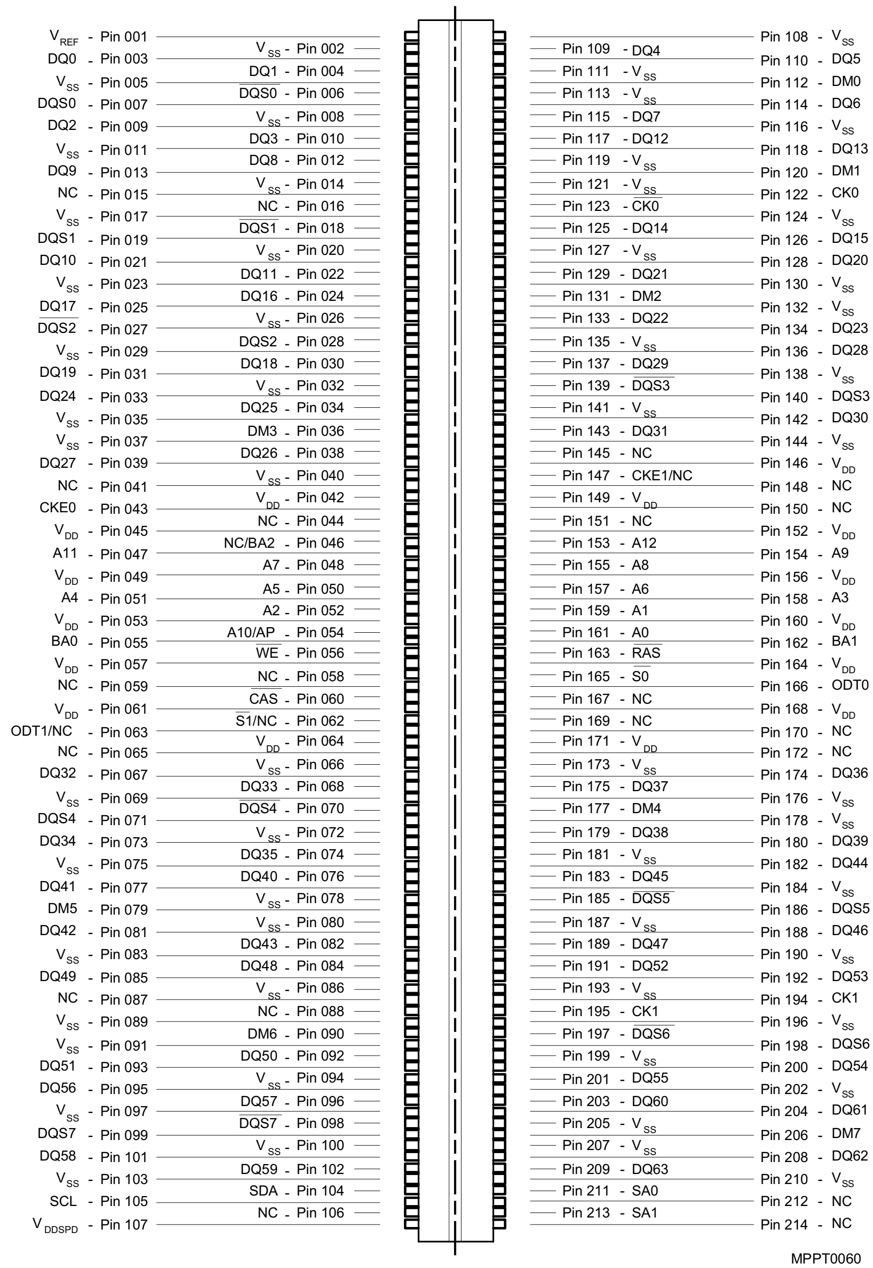
| Abbreviation | Description |
|---|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| PWR | Power |
| GND | Ground |
| NC | Not Connected |

## TABLE 7
### Abbreviations for Buffer Type

| Abbreviation | Description |
|---|---|
| SSTL | Serial Stub Terminated Logic (SSTL_15 and SSTL_18) |
| CMOS | CMOS Levels |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. |

## FIGURE 1

**Pin Configuration for Two-Piece Mezzanine Socket on MDIMM (214 pins)**



# 3 Electrical Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

## 3.1 Absolute Maximum Ratings

*Attention:* ***Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.***

**TABLE 8**
**Absolute Maximum Ratings**

| Symbol | Parameter | Rating | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $V_{DD}$ | Voltage on $V_{DD}$ pin relative to $V_{SS}$ | –1.0 | +2.3 | V | 1) |
| $V_{DDQ}$ | Voltage on $V_{DDQ}$ pin relative to $V_{SS}$ | –0.5 | +2.3 | V | |
| $V_{DDL}$ | Voltage on $V_{DDL}$ pin relative to $V_{SS}$ | –0.5 | +2.3 | V | |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | –0.5 | +2.3 | V | |

1) When $V_{DD}$ and $V_{DDQ}$ and $V_{DDL}$ are less than 500 mV; $V_{REF}$ may be equal to or less than 300 mV.

**TABLE 9**
**Environmental Requirements**

| Parameter | Symbol | Values | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Storage Temperature | $T_{STG}$ | – 50 | +100 | °C | 1) |
| Barometric Pressure (operating & storage) | PBar | +69 | +105 | kPa | 2) |
| Operating Humidity (relative) | $H_{OPR}$ | 10 | 90 | % | |
| Storage Humidity (without condensation) | $H_{STG}$ | 5 | 95 | % | |

1) Storage Temperature is the case surface temperature on the center/top side of the DRAM.
2) Up to 3000 m.

**TABLE 10**
**DRAM Component Operating Temperature Range**

| Symbol | Parameter | Rating | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $T_{CASE}$ | Operating Temperature | 0 | 95 | °C | 1)2)3)4) |

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 °C the Auto-Refresh command interval has to be reduced to $t_{REFI}$= 3.9 µs
4) When operating this product in the 85 °C to 95 °C $T_{CASE}$ temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of $I_{DD6}$ by approximately 50%

## 3.2 Operating Conditions

**TABLE 11**
**Supply Voltage Levels and AC / DC Operating Conditions**

| Parameter | Symbol | Values | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Device Supply Voltage | $V_{DD}$ | 1.45 | 1.5 | 1.9 | V | |
| Output Supply Voltage | $V_{DDQ}$ | 1.45 | 1.5 | 1.9 | V | 1) |
| Input Reference Voltage | $V_{REF}$ | 0.49 × $V_{DDQ}$ | 0.5 × $V_{DDQ}$ | 0.51 × $V_{DDQ}$ | V | 2) |
| SPD Supply Voltage | $V_{DDSPD}$ | 1.7 | — | 3.6 | V | |
| DC Input Logic High | $V_{IH(DC)}$ | $V_{REF}$ + 0.125 | — | $V_{DDQ}$ + 0.3 | V | |
| DC Input Logic Low | $V_{IL (DC)}$ | – 0.30 | — | $V_{REF}$ – 0.125 | V | |
| AC Input Logic High | $V_{IH(AC)}$ | $V_{REF}$ + 0.200 | — | $V_{DDQ}$ + $V_{PEAK}$ | V | |
| AC Input Logic Low | $V_{IL (AC)}$ | $V_{SSQ}$ – $V_{PEAK}$ | — | $V_{REF}$ –0.200 | V | |
| In / Output Leakage Current | $I_L$ | – 5 | — | 5 | µA | 3) |

1) Under all conditions, $V_{DDQ}$ must be less than or equal to $V_{DD}$
2) Peak to peak AC noise on $V_{REF}$ may not exceed ± 2% $V_{REF}$ (DC). $V_{REF}$ is also expected to track noise in $V_{DDQ}$.
3) Input voltage for any connector pin under test of 0 V ≤ $V_{IN}$ ≤ $V_{DDQ}$ + 0.3 V; all other pins at 0 V. Current is per pin

## 3.3 Speed Grade Definitions

**TABLE 12**
**Speed Grade Definition**

| **Speed Grade** | | | **DDR2–800E** | | **Unit** | **Note** |
|---|---|---|---|---|---|---|
| **QAG Sort Name** | | | **–2.5** | | | |
| **CAS-RCD-RP latencies** | | | **6–6–6** | | **$t_{CK}$** | |
| **Parameter** | | **Symbol** | **Min.** | **Max.** | **—** | |
| Clock Period | @ CL = 3 | $t_{CK}$ | 5 | 8 | ns | 1)2)3)4) |
| | @ CL = 4 | $t_{CK}$ | 3.75 | 8 | ns | 1)2)3)4) |
| | @ CL = 5 | $t_{CK}$ | 3 | 8 | ns | 1)2)3)4) |
| | @ CL = 6 | $t_{CK}$ | 2.5 | 8 | ns | 1)2)3)4) |
| Row Active Time | | $t_{RAS}$ | 45 | 70k | ns | 1)2)3)4)5) |
| Row Cycle Time | | $t_{RC}$ | 60 | — | ns | 1)2)3)4) |
| RAS-CAS-Delay | | $t_{RCD}$ | 15 | — | ns | 1)2)3)4) |
| Row Precharge Time | | $t_{RP}$ | 15 | — | ns | 1)2)3)4) |

**TABLE 13**
**Speed Grade Definition**

| **Speed Grade** | | | **DDR2–667D** | | **Unit** | **Note** |
|---|---|---|---|---|---|---|
| **QAG Sort Name** | | | **–3S** | | | |
| **CAS-RCD-RP latencies** | | | **5–5–5** | | **$t_{CK}$** | |
| **Parameter** | | **Symbol** | **Min.** | **Max.** | **—** | |
| Clock Period | @ CL = 3 | $t_{CK}$ | 5 | 8 | ns | 1)2)3)4) |
| | @ CL = 4 | $t_{CK}$ | 3.75 | 8 | ns | 1)2)3)4) |
| | @ CL = 5 | $t_{CK}$ | 3 | 8 | ns | 1)2)3)4) |
| Row Active Time | | $t_{RAS}$ | 45 | 70k | ns | 1)2)3)4)5) |
| Row Cycle Time | | $t_{RC}$ | 60 | — | ns | 1)2)3)4) |
| RAS-CAS-Delay | | $t_{RCD}$ | 15 | — | ns | 1)2)3)4) |
| Row Precharge Time | | $t_{RP}$ | 15 | — | ns | 1)2)3)4) |

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
3) Inputs are not recognized as valid until $V_{REF}$ stabilizes. During the period before $V_{REF}$ stabilizes, CKE = 0.2 x $V_{DDQ}$
4) The output timing reference voltage level is $V_{TT}$.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x $t_{REFI}$.

## 3.4 Component AC Timing Parameters

**TABLE 14**
**DRAM Component Timing Parameter by Speed Grade - DDR2–800 and DDR2–667**

| Parameter | Symbol | DDR2–800 | | DDR2–667 | | Unit | Note1)2)3)4)5)6)7) |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| DQ output access time from CK / $\overline{CK}$ | $t_{AC}$ | –400 | +400 | –450 | +450 | ps | 8) |
| CAS to CAS command delay | $t_{CCD}$ | 2 | — | 2 | — | nCK | |
| Average clock high pulse width | $t_{CH.AVG}$ | 0.48 | 0.52 | 0.48 | 0.52 | $t_{CK.AVG}$ | 9)10) |
| Average clock period | $t_{CK.AVG}$ | 2500 | 8000 | 3000 | 8000 | ps | |
| CKE minimum pulse width ( high and low pulse width) | $t_{CKE}$ | 3 | — | 3 | — | nCK | 11) |
| Average clock low pulse width | $t_{CL.AVG}$ | 0.48 | 0.52 | 0.48 | 0.52 | $t_{CK.AVG}$ | 9)10) |
| Auto-Precharge write recovery + precharge time | $t_{DAL}$ | WR + $t_{nRP}$ | — | WR + $t_{nRP}$ | — | nCK | 12)13) |
| Minimum time clocks remain ON after CKE asynchronously drops LOW | $t_{DELAY}$ | $t_{IS}$ + $t_{CK .AVG}$ + $t_{IH}$ | — | $t_{IS}$ + $t_{CK .AVG}$ + $t_{IH}$ | — | ns | |
| DQ and DM input hold time | $t_{DH.BASE}$ | 125 | — | 175 | — | ps | 14)18)19) |
| DQ and DM input pulse width for each input | $t_{DIPW}$ | 0.35 | — | 0.35 | — | $t_{CK.AVG}$ | |
| DQS input high pulse width | $t_{DQSH}$ | 0.35 | — | 0.35 | — | $t_{CK.AVG}$ | |
| DQS output access time from CK / $\overline{CK}$ | $t_{DQSCK}$ | –350 | +350 | –400 | +400 | ps | 8) |
| DQS input low pulse width | $t_{DQSL}$ | 0.35 | — | 0.35 | — | $t_{CK.AVG}$ | |
| DQS-DQ skew for DQS & associated DQ signals | $t_{DQSQ}$ | — | 200 | — | 240 | ps | 15) |
| DQS latching rising transition to associated clock edges | $t_{DQSS}$ | – 0.25 | + 0.25 | – 0.25 | + 0.25 | $t_{CK.AVG}$ | 16) |
| DQ and DM input setup time | $t_{DS.BASE}$ | 50 | — | 100 | — | ps | 17)18)19) |
| DQS falling edge hold time from CK | $t_{DSH}$ | 0.2 | — | 0.2 | — | $t_{CK.AVG}$ | 16) |
| DQS falling edge to CK setup time | $t_{DSS}$ | 0.2 | — | 0.2 | — | $t_{CK.AVG}$ | 16) |
| Four Activate Window for 1KB page size products | $t_{FAW}$ | 35 | — | 37.5 | — | ns | 34) |
| Four Activate Window for 2KB page size products | $t_{FAW}$ | 45 | — | 50 | — | ns | 34) |
| CK half pulse width | $t_{HP}$ | Min($t_{CH.ABS}$, $t_{CL.ABS}$) | — | Min($t_{CH.ABS}$, $t_{CL.ABS}$) | — | ps | 20) |
| Data-out high-impedance time from CK / $\overline{CK}$ | $t_{HZ}$ | — | $t_{AC.MAX}$ | — | $t_{AC.MAX}$ | ps | 8)21) |
| Address and control input hold time | $t_{IH.BASE}$ | 250 | — | 275 | — | ps | 22)24) |
| Control & address input pulse width for each input | $t_{IPW}$ | 0.6 | — | 0.6 | — | $t_{CK.AVG}$ | |
| Address and control input setup time | $t_{IS.BASE}$ | 175 | — | 200 | — | ps | 23)24) |

| Parameter | Symbol | DDR2–800 | | DDR2–667 | | Unit | Note[1)2)3)4)5)6)7)] |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| DQ low impedance time from CK/$\overline{CK}$ | $t_{LZ.DQ}$ | 2 x $t_{AC.MIN}$ | $t_{AC.MAX}$ | 2 x $t_{AC.MIN}$ | $t_{AC.MAX}$ | ps | 8)21) |
| DQS/$\overline{DQS}$ low-impedance time from CK / $\overline{CK}$ | $t_{LZ.DQS}$ | $t_{AC.MIN}$ | $t_{AC.MAX}$ | $t_{AC.MIN}$ | $t_{AC.MAX}$ | ps | 8)21) |
| MRS command to ODT update delay | $t_{MOD}$ | 0 | 12 | 0 | 12 | ns | 34) |
| Mode register set command cycle time | $t_{MRD}$ | 2 | — | 2 | — | nCK | |
| OCD drive mode output delay | $t_{OIT}$ | 0 | 12 | 0 | 12 | ns | 34) |
| DQ/DQS output hold time from DQS | $t_{QH}$ | $t_{HP} - t_{QHS}$ | — | $t_{HP} - t_{QHS}$ | — | ps | 25) |
| DQ hold skew factor | $t_{QHS}$ | — | 300 | — | 340 | ps | 26) |
| Average periodic refresh Interval | $t_{REFI}$ | — | 7.8 | — | 7.8 | µs | 27)28) |
| | | — | 3.9 | — | 3.9 | µs | 27)29) |
| Auto-Refresh to Active/Auto-Refresh command period | $t_{RFC}$ | 127.5 | — | 127.5 | — | ns | 30) |
| Read preamble | $t_{RPRE}$ | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK.AVG}$ | 31)32) |
| Read postamble | $t_{RPST}$ | 0.4 | 0.6 | 0.4 | 0.6 | $t_{CK.AVG}$ | 31)33) |
| Active to active command period for 2KB page size products | $t_{RRD}$ | 10 | — | 10 | — | ns | 34) |
| Internal Read to Precharge command delay | $t_{RTP}$ | 7.5 | — | 7.5 | — | ns | 34) |
| Write preamble | $t_{WPRE}$ | 0.35 | — | 0.35 | — | $t_{CK.AVG}$ | |
| Write postamble | $t_{WPST}$ | 0.4 | 0.6 | 0.4 | 0.6 | $t_{CK.AVG}$ | |
| Write recovery time | $t_{WR}$ | 15 | — | 15 | — | ns | 34) |
| Internal write to read command delay | $t_{WTR}$ | 7.5 | — | 7.5 | — | ns | 34)35) |
| Exit power down to read command | $t_{XARD}$ | 2 | — | 2 | — | nCK | |
| Exit active power-down mode to read command (slow exit, lower power) | $t_{XARDS}$ | 8 – AL | — | 7 – AL | — | nCK | |
| Exit precharge power-down to any valid command (other than NOP or Deselect) | $t_{XP}$ | 2 | — | 2 | — | nCK | |
| Exit self-refresh to a non-read command | $t_{XSNR}$ | $t_{RFC}$ +10 | — | $t_{RFC}$ +10 | — | ns | 34) |
| Exit self-refresh to read command | $t_{XSRD}$ | 200 | — | 200 | — | nCK | |
| Write command to DQS associated clock edges | WL | RL – 1 | | RL–1 | | nCK | |

1) $V_{DDQ}$ = 1.8 V ± 0.1V; $V_{DD}$ = 1.8 V ± 0.1 V.
2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
3) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
4) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
5) Inputs are not recognized as valid until $V_{REF}$ stabilizes. During the period before $V_{REF}$ stabilizes, CKE = 0.2 x $V_{DDQ}$ is recognized as low.
6) The output timing reference voltage level is $V_{TT}$.

7) New units, ‘$t_{CK.AVG}$‘ and ‘nCK‘, are introduced in DDR2–667 and DDR2–800. Unit ‘$t_{CK.AVG}$‘ represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit ‘nCK‘ represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2–400 and DDR2–533, ‘$t_{CK}$‘ is used for both concepts. Example: $t_{XP}$ = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.
8) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(6-10per)}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6-10PER).MIN}$ = – 272 ps and $t_{ERR(6-10PER).MAX}$ = + 293 ps, then $t_{DQSCK.MIN(DERATED)}$ = $t_{DQSCK.MIN}$ – $t_{ERR(6-10PER).MAX}$ = – 400 ps – 293 ps = – 693 ps and $t_{DQSCK.MAX(DERATED)}$ = $t_{DQSCK.MAX}$ – $t_{ERR(6-10PER).MIN}$ = 400 ps + 272 ps = + 672 ps. Similarly, $t_{LZ.DQ}$ for DDR2–667 derates to $t_{LZ.DQ.MIN(DERATED)}$ = - 900 ps – 293 ps = – 1193 ps and $t_{LZ.DQ.MAX(DERATED)}$ = 450 ps + 272 ps = + 722 ps. (Caution on the MIN/MAX usage!)
9) Input clock jitter spec parameter. The jitter specified is a random jitter meeting a Gaussian distribution.
10) These parameters are specified per their average values.
11) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS}$ + 2 x $t_{CK}$ + $t_{IH}$.
12) DAL = WR + RU{$t_{RP}$(ns) / $t_{CK}$(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For $t_{RP}$, if the result of the division is not already an integer, round up to the next highest integer. $t_{CK}$ refers to the application clock period. Example: For DDR2–533 at $t_{CK}$ = 3.75 ns with $t_{WR}$ programmed to 4 clocks. $t_{DAL}$ = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.
13) $t_{DAL.nCK}$ = WR [nCK] + $t_{nRP.nCK}$ = WR + RU{$t_{RP}$ [ps] / $t_{CK.AVG}$[ps] }, where WR is the value programmed in the EMR.
14) Input waveform timing $t_{DH}$ with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH.DC}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL.DC}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{IL.DC.MAX}$ and $V_{IH.DC.MIN}$. See **Figure 3**.
15) $t_{DQSQ}$: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
16) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
17) Input waveform timing $t_{DS}$ with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{IH.AC}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL.AC}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{il(DC)MAX}$ and $V_{ih(DC)MIN}$. See **Figure 3**.
18) If $t_{DS}$ or $t_{DH}$ is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
19) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing.
20) $t_{HP}$ is the minimum of the absolute half period of the actual input clock. $t_{HP}$ is an input parameter but not an input specification parameter. It is used in conjunction with $t_{QHS}$ to derive the DRAM output timing $t_{QH}$. The value to be used for $t_{QH}$ calculation is determined by the following equation; $t_{HP}$ = MIN ($t_{CH.ABS}$, $t_{CL.ABS}$), where, $t_{CH.ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL.ABS}$ is the minimum of the actual instantaneous clock low time.
21) $t_{HZ}$ and $t_{LZ}$ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving ($t_{HZ}$), or begins driving ($t_{LZ}$) .
22) input waveform timing is referenced from the input signal crossing at the $V_{IL.DC}$ level for a rising signal and $V_{IH.DC}$ for a falling signal applied to the device under test. See **Figure 4**.
23) Input waveform timing is referenced from the input signal crossing at the $V_{IH.AC}$ level for a rising signal and $V_{IL.AC}$ for a falling signal applied to the device under test. See **Figure 4**.
24) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
25) $t_{QH}$ = $t_{HP}$ – $t_{QHS}$, where: $t_{HP}$ is the minimum of the absolute half period of the actual input clock; and $t_{QHS}$ is the specification value under the max column. {The less half-pulse width distortion present, the larger the $t_{QH}$ value is; and the larger the valid data eye will be.} Examples: 1) If the system provides $t_{HP}$ of 1315 ps into a DDR2–667 SDRAM, the DRAM provides $t_{QH}$ of 975 ps minimum. 2) If the system provides $t_{HP}$ of 1420 ps into a DDR2–667 SDRAM, the DRAM provides $t_{QH}$ of 1080 ps minimum.
26) $t_{QHS}$ accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual $t_{HP}$ at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
27) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
28) 0 °C≤ $T_{CASE}$ ≤ 85 °C.

29) 85 °C < $T_{CASE}$ ≤ 95 °C.
30) A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 x $t_{REFI}$.
31) $t_{RPST}$ end point and $t_{RPRE}$ begin point are not referenced to a specific voltage level but specify when the device output is no longer driving ($t_{RPST}$), or begins driving ($t_{RPRE}$). **Figure 2** shows a method to calculate these points when the device is no longer driving ($t_{RPST}$), or begins driving ($t_{RPRE}$) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
32) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.PER.MIN}$ = – 72 ps and $t_{JIT.PER.MAX}$ = + 93 ps, then $t_{RPRE.MIN(DERATED)}$ = $t_{RPRE.MIN}$ + $t_{JIT.PER.MIN}$ = 0.9 x $t_{CK.AVG}$ – 72 ps = + 2178 ps and $t_{RPRE.MAX(DERATED)}$ = $t_{RPRE.MAX}$ + $t_{JIT.PER.MAX}$ = 1.1 x $t_{CK.AVG}$ + 93 ps = + 2843 ps. (Caution on the MIN/MAX usage!).
33) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.DUTY.MIN}$ = – 72 ps and $t_{JIT.DUTY.MAX}$ = + 93 ps, then $t_{RPST.MIN(DERATED)}$ = $t_{RPST.MIN}$ + $t_{JIT.DUTY.MIN}$ = 0.4 x $t_{CK.AVG}$ – 72 ps = + 928 ps and $t_{RPST.MAX(DERATED)}$ = $t_{RPST.MAX}$ + $t_{JIT.DUTY.MAX}$ = 0.6 x $t_{CK.AVG}$ + 93 ps = + 1592 ps. (Caution on the MIN/MAX usage!).
34) For these parameters, the DDR2 SDRAM device is characterized and verified to support $t_{nPARAM}$ = RU{$t_{PARAM}$ / $t_{CK.AVG}$}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support $t_{nRP}$ = RU{$t_{RP}$ / $t_{CK.AVG}$}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2–667 5–5–5, of which $t_{RP}$ = 15 ns, the device will support $t_{nRP}$ = RU{$t_{RP}$ / $t_{CK.AVG}$} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm + 5 is valid even if (Tm + 5 - Tm) is less than 15 ns due to input clock jitter.
35) $t_{WTR}$ is at lease two clocks (2 x $t_{CK}$) independent of operation frequency.
36) This timing parameter is relaxed than Industry Standard
1) $V_{DDQ}$ = 1.8 V ± 0.1V; $V_{DD}$ = 1.8 V ± 0.1 V.
2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
3) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
4) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
5) Inputs are not recognized as valid until $V_{REF}$ stabilizes. During the period before $V_{REF}$ stabilizes, CKE = 0.2 x $V_{DDQ}$ is recognized as low.
6) The output timing reference voltage level is $V_{TT}$.
7) For each of the terms, if not already an integer, round to the next highest integer. $t_{CK}$ refers to the application clock period. WR refers to the WR parameter stored in the MR.
8) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
9) For timing definition, refer to the Component data sheet.
10) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
11) MIN ($t_{CL}$, $t_{CH}$) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for $t_{CL}$ and $t_{CH}$).
12) The $t_{HZ}$, $t_{RPST}$ and $t_{LZ}$, $t_{RPRE}$ parameters are referenced to a specific voltage level, which specify when the device output is no longer driving ($t_{HZ}$, $t_{RPST}$), or begins driving ($t_{LZ}$, $t_{RPRE}$). $t_{HZ}$ and $t_{LZ}$ transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.
13) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
14) 0 °C≤ $T_{CASE}$ ≤ 85 °C.
15) 85 °C < $T_{CASE}$ ≤ 95 °C.
16) A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 x $t_{REFI}$.
17) The $t_{RRD}$ timing parameter depends on the page size of the DRAM organization.
18) The maximum limit for the $t_{WPST}$ parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
19) Minimum $t_{WTR}$ is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
20) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing $t_{XARD}$ can be used. In “low active power-down mode” (MR, A12 =”1”) a slow power-down exit timing $t_{XARDS}$ has to be satisfied.
21) WR must be programmed to fulfill the minimum requirement for the $t_{WR}$ timing parameter, where $WR_{MIN}$[cycles] = $t_{WR}$(ns)/$t_{CK}$(ns) rounded up to the next integer value. $t_{DAL}$ = WR + ($t_{RP}$/$t_{CK}$). For each of the terms, if not already an integer, round to the next highest integer. $t_{CK}$ refers to the application clock period. WR refers to the WR parameter stored in the MRS.

**FIGURE 2**
**Method for Calculating Transitions and Endpoint**

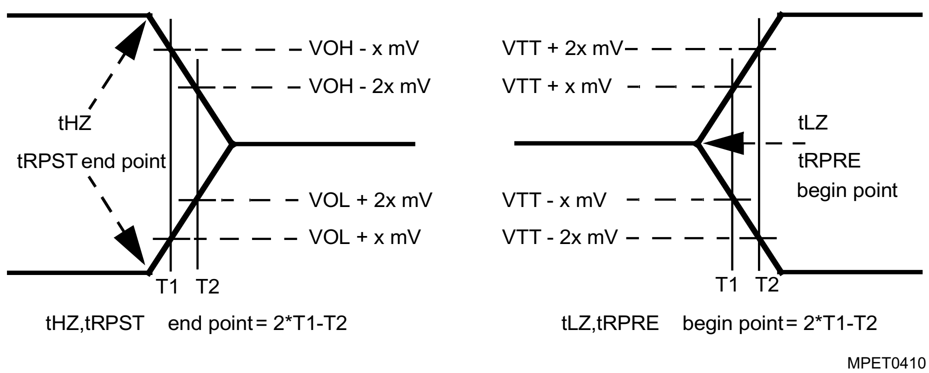
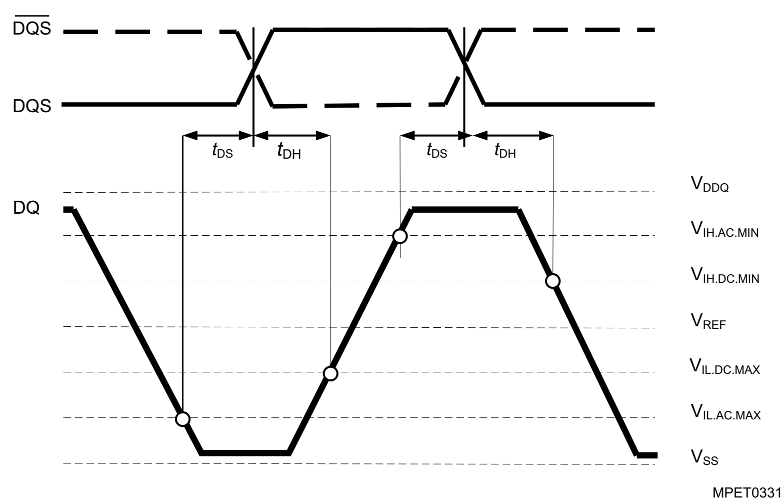
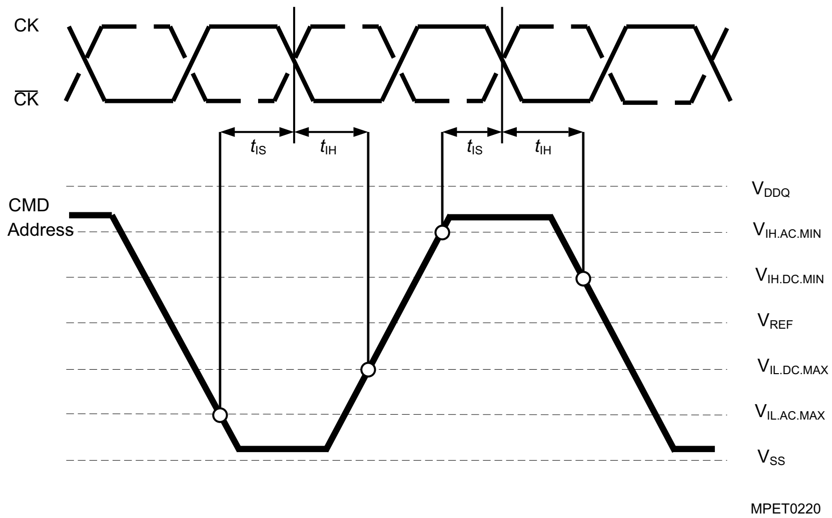



**FIGURE 3**
**Differential Input Waveform Timing $t_{DS}$ and $t_{DH}$**



## FIGURE 4
**Differential Input Waveform Timing $t_{IS}$ and $t_{IH}$**



## 3.5 ODT AC Electrical Characteristics

This chapter describes the ODT AC electrical characteristics.

**TABLE 15**
**ODT AC Characteristics and Operating Conditions for DDR2-667 , DDR2-800**

| Symbol | Parameter / Condition | Values | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $t_{AOND}$ | ODT turn-on delay | 2 | 2 | $n_{CK}$ | 1) |
| $t_{AON}$ | ODT turn-on | $t_{AC.MIN}$ | $t_{AC.MAX}$ + 0.7 ns | ns | 1)2) |
| $t_{AONPD}$ | ODT turn-on (Power-Down Modes) | $t_{AC.MIN}$ + 2 ns | 2 $t_{CK}$ + $t_{AC.MAX}$ + 1 ns | ns | 1) |
| $t_{AOFD}$ | ODT turn-off delay | 2.5 | 2.5 | $n_{CK}$ | 1) |
| $t_{AOF}$ | ODT turn-off | $t_{AC.MIN}$ | $t_{AC.MAX}$ + 0.6 ns | ns | 1)3) |
| $t_{AOFPD}$ | ODT turn-off (Power-Down Modes) | $t_{AC.MIN}$ + 2 ns | 2.5 $t_{CK}$ + $t_{AC.MAX}$ + 1 ns | ns | 1) |
| $t_{ANPD}$ | ODT to Power Down Mode Entry Latency | 3 | — | $n_{CK}$ | 1) |
| $t_{AXPD}$ | ODT Power Down Exit Latency | 8 | — | $n_{CK}$ | 1) |

1) New units, "$t_{CK.AVG}$" and "$n_{CK}$", are introduced in DDR2-667 and DDR2-800 Unit "$t_{CK.AVG}$" represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit "$n_{CK}$" represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, "$t_{CK}$" is used for both concepts. Example: $t_{XP}$ = 2 [$n_{CK}$] means; if Power Down exit is registered at $T_m$, an Active command may be registered at $T_m$ + 2, even if ($T_m$ + 2 - $T_m$) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.

2) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from $t_{AOND}$, which is interpreted differently per speed bin. For DDR2-667/800 $t_{AOND}$ is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

3) ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from $t_{AOFD}$, which is interpreted differently per speed bin. For DDR2-667/800, if $t_{CK(avg)}$ = 3 ns is assumed, $t_{AOFD}$ is 1.5 ns (= 0.5 x 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

## 3.6 $I_{DD}$ Specifications and Conditions

List of tables defining $I_{DD}$ Specifications and Conditions.

**TABLE 16**
**$I_{DD}$ Measurement Conditions**

| Parameter | Symbol | Note[1)2)3)4)5)] |
|---|---|---|
| **Operating Current 0**<br>One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING. | $I_{DD0}$ | |
| **Operating Current 1**<br>One bank Active - Read - Precharge; $I_{OUT}$ = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = $CL_{MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING. | $I_{DD1}$ | 6) |
| **Precharge Standby Current**<br>All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING. | $I_{DD2N}$ | |
| **Precharge Power-Down Current**<br>Other control and address inputs are STABLE, Data bus inputs are FLOATING. | $I_{DD2P}$ | |
| **Precharge Quiet Standby Current**<br>All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING. | $I_{DD2Q}$ | |
| **Active Standby Current**<br>Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{MIN}$; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; $I_{OUT}$ = 0 mA. | $I_{DD3N}$ | |
| **Active Power-Down Current**<br>All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit); | $I_{DD3P(0)}$ | |
| **Active Power-Down Current**<br>All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit); | $I_{DD3P(1)}$ | |
| **Operating Current - Burst Read**<br>All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{MIN}$; $t_{CK} = t_{CKMIN}$; $t_{RAS} = t_{RASMAX}$; $t_{RP} = t_{RPMIN}$; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; $I_{OUT}$ = 0mA. | $I_{DD4R}$ | 6) |
| **Operating Current - Burst Write**<br>All banks open; Continuous burst writes; BL = 4; AL = 0, CL = $CL_{MIN}$; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; | $I_{DD4W}$ | |
| **Burst Refresh Current**<br>$t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING. | $I_{DD5B}$ | |
| **Distributed Refresh Current**<br>$t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING. | $I_{DD5D}$ | |

| Parameter | Symbol | Note[1)2)3)4)5)] |
|---|---|---|
| **Self-Refresh Current**<br>CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. $I_{DD6}$ current values are guaranteed up to $T_{CASE}$ of 85 °C max. | $I_{DD6}$ | |
| **All Bank Interleave Read Current**<br>All banks are being interleaved at minimum $t_{RC}$ without violating $t_{RRD}$ using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. $I_{out}$ = 0 mA. | $I_{DD7}$ | 6) |

1) $V_{DDQ}$ = 1.8 V ± 0.1 V; $V_{DD}$ = 1.8 V ± 0.1 V
2) $I_{DD}$ specifications are tested after the device is properly initialized and $I_{DD}$ parameter are specified with ODT disabled.
3) Definitions for $I_{DD}$ see **Table 17**
4) For two rank modules: All active current measurements in the same $I_{DD}$ current mode. The other rank is in $I_{DD2P}$ Precharge Power-Down Mode.
5) For details and notes see the relevant Qimonda component data sheet.
6) $I_{DD1}$, $I_{DD4R}$ and $I_{DD7}$ current measurements are defined with the outputs disabled ($I_{OUT}$ = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

## TABLE 17
### Definitions for $I_{DD}$

| Parameter | Description |
|---|---|
| LOW | $V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$ |
| STABLE | Inputs are stable at a HIGH or LOW level. |
| FLOATING | Inputs are $V_{REF} = V_{DDQ}/2$ |
| SWITCHING | Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes. |

**TABLE 18**
**$I_{DD}$ Specification at 1.8V for HYS64T128020EMV-[2.5/3S](-)C2**

| Product Type | HYS64T128020EMV-2.5C2 | HYS64T128020EMV-3S-C2 | Unit | Note[1)2)] |
|---|---|---|---|---|
| Organization | 1 GB | 1 GB | | |
| | 2 Ranks (×16) | 2 Ranks (×16) | | |
| | ×64 | ×64 | | |
| | –2.5 | –3S | | |
| Symbol | Max. | Max. | | |
| $I_{DD0}$ | 472 | 452 | mA | 3) |
| $I_{DD1}$ | 512 | 488 | mA | 3) |
| $I_{DD2N}$ | 472 | 432 | mA | 4) |
| $I_{DD2P}$ | 104 | 104 | mA | 4) |
| $I_{DD2Q}$ | 456 | 416 | mA | 4) |
| $I_{DD3N}$ | 536 | 496 | mA | 4) |
| $I_{DD3P(MRS = 0)}$ | 336 | 320 | mA | 4)5) |
| $I_{DD3P(MRS = 1)}$ | 160 | 160 | mA | 4)6) |
| $I_{DD4R}$ | 744 | 672 | mA | 3) |
| $I_{DD4W}$ | 800 | 720 | mA | 3) |
| $I_{DD5B}$ | 964 | 948 | mA | 3) |
| $I_{DD5D}$ | 128 | 128 | mA | 4)7) |
| $I_{DD6}$ | 56 | 56 | mA | 4)7) |
| $I_{DD7}$ | 1360 | 1276 | mA | 3) |

**TABLE 19**
**$I_{DD}$ Specification at 1.5V for HYS64T128020EMV-[2.5/3S](-)C2**

| Product Type | HYS64T128020EMV-2.5C2 | HYS64T128020EMV-3S-C2 | Unit | Note[1)2)] |
|---|---|---|---|---|
| Organization | 1 GB | 1 GB | | |
| | 2 Ranks (×16) | 2 Ranks (×16) | | |
| | ×64 | ×64 | | |
| | –2.5 | –3S | | |
| Symbol | Typ. | Typ. | | |
| $I_{DD0}$ | 303 | 287 | mA | 3) |
| $I_{DD1}$ | 324 | 308 | mA | 3) |
| $I_{DD2N}$ | 337 | 306 | mA | 4) |
| $I_{DD2P}$ | 29 | 28 | mA | 4) |
| $I_{DD2Q}$ | 299 | 273 | mA | 4) |
| $I_{DD3N}$ | 378 | 344 | mA | 4) |
| $I_{DD3P(MRS = 0)}$ | 163 | 149 | mA | 4)5) |
| $I_{DD3P(MRS = 1)}$ | 44 | 43 | mA | 4)6) |
| $I_{DD4R}$ | 539 | 482 | mA | 3) |
| $I_{DD4W}$ | 570 | 511 | mA | 3) |
| $I_{DD5B}$ | 628 | 603 | mA | 3) |
| $I_{DD5D}$ | 46 | 45 | mA | 4)7) |
| $I_{DD6}$ | 31 | 31 | mA | 4)7) |
| $I_{DD7}$ | 840 | 764 | mA | 3) |

1) Calculated values from component data. ODT disabled. $I_{DD1}$, $I_{DD4R}$ and $I_{DD7}$ are defined with the outputs disabled.
2) $I_{DDX (rank)}$ = Number of components x $I_{DDX (component)}$
3) $I_{DDX} = I_{DDX (rank)} + I_{DD2P (rank)}$
4) $I_{DDX} = 2 \times I_{DDX (rank)}$
5) Fast: MRS(12)=0
6) Slow: MRS(12)=1
7) $I_{DD5D}$ and $I_{DD6}$ values are for $0°C \leq T_{Case} \leq 85°C$

# 4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

**List of SPD Code Tables**



**TABLE 20**
**HYS64T128020EMV-[2.5/3S](-)C2**

| Product Type | | HYS64T128020EMV–2.5C2 | HYS64T128020EMV–3S–C2 |
|---|---|---|---|
| Organization | | 1 GByte | 1 GByte |
| | | ×64 | ×64 |
| | | 2 Ranks (×16) | 2 Ranks (×16) |
| Label Code | | PC2–6400M–666 | PC2–5300M–555 |
| JEDEC SPD Revision | | Rev. 1.2 | Rev. 1.2 |
| **Byte#** | **Description** | **HEX** | **HEX** |
| 0 | Programmed SPD Bytes in EEPROM | 80 | 80 |
| 1 | Total number of Bytes in EEPROM | 08 | 08 |
| 2 | Memory Type (DDR2) | 08 | 08 |
| 3 | Number of Row Addresses | 0D | 0D |
| 4 | Number of Column Addresses | 0A | 0A |
| 5 | DIMM Rank and Stacking Information | 61 | 61 |
| 6 | Data Width | 40 | 40 |
| 7 | Not used | 00 | 00 |
| 8 | Interface Voltage Level | 05 | 05 |
| 9 | $t_{CK}$ @ $CL_{MAX}$ (Byte 18) [ns] | 25 | 30 |
| 10 | $t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns] | 40 | 45 |
| 11 | Error Correction Support (non-ECC, ECC) | 00 | 00 |
| 12 | Refresh Rate and Type | 82 | 82 |
| 13 | Primary SDRAM Width | 10 | 10 |

| **Product Type** | | **HYS64T128020EMV–2.5C2** | **HYS64T128020EMV–3S–C2** |
|---|---|---|---|
| **Organization** | | **1 GByte** | **1 GByte** |
| | | **×64** | **×64** |
| | | **2 Ranks (×16)** | **2 Ranks (×16)** |
| **Label Code** | | **PC2–6400M–666** | **PC2–5300M–555** |
| **JEDEC SPD Revision** | | **Rev. 1.2** | **Rev. 1.2** |
| **Byte#** | **Description** | **HEX** | **HEX** |
| 14 | Error Checking SDRAM Width | 00 | 00 |
| 15 | Not used | 00 | 00 |
| 16 | Burst Length Supported | 0C | 0C |
| 17 | Number of Banks on SDRAM Device | 08 | 08 |
| 18 | Supported CAS Latencies | 70 | 38 |
| 19 | DIMM Mechanical Characteristics | 01 | 01 |
| 20 | DIMM Type Information | 08 | 08 |
| 21 | DIMM Attributes | 00 | 00 |
| 22 | Component Attributes | 07 | 07 |
| 23 | $t_{CK}$ @ $CL_{MAX}$ -1 (Byte 18) [ns] | 30 | 3D |
| 24 | $t_{AC}$ SDRAM @ $CL_{MAX}$ -1 [ns] | 45 | 50 |
| 25 | $t_{CK}$ @ $CL_{MAX}$ -2 (Byte 18) [ns] | 3D | 50 |
| 26 | $t_{AC}$ SDRAM @ $CL_{MAX}$ -2 [ns] | 50 | 60 |
| 27 | $t_{RP.MIN}$ [ns] | 3C | 3C |
| 28 | $t_{RRD.MIN}$ [ns] | 28 | 28 |
| 29 | $t_{RCD.MIN}$ [ns] | 3C | 3C |
| 30 | $t_{RAS.MIN}$ [ns] | 2D | 2D |
| 31 | Module Density per Rank | 80 | 80 |
| 32 | $t_{AS.MIN}$ and $t_{CS.MIN}$ [ns] | 17 | 20 |
| 33 | $t_{AH.MIN}$ and $t_{CH.MIN}$ [ns] | 25 | 27 |
| 34 | $t_{DS.MIN}$ [ns] | 05 | 10 |
| 35 | $t_{DH.MIN}$ [ns] | 12 | 17 |
| 36 | $t_{WR.MIN}$ [ns] | 3C | 3C |
| 37 | $t_{WTR.MIN}$ [ns] | 1E | 1E |
| 38 | $t_{RTP.MIN}$ [ns] | 1E | 1E |
| 39 | Analysis Characteristics | 00 | 00 |

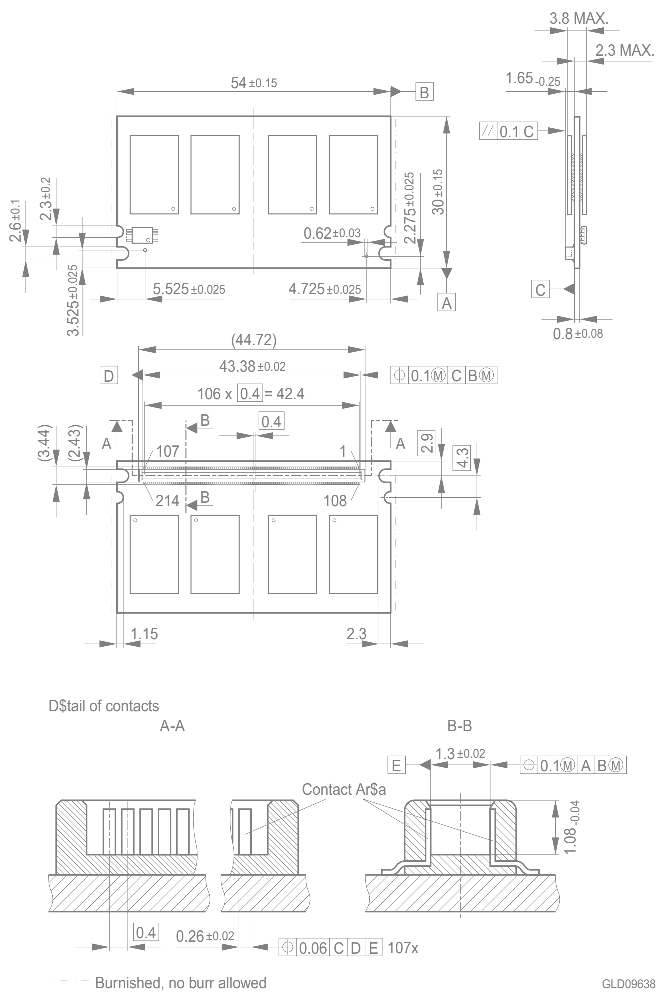
| Product Type | | HYS64T128020EMV–2.5C2 | HYS64T128020EMV–3S–C2 |
|---|---|---|---|
| **Organization** | | **1 GByte** | **1 GByte** |
| | | **×64** | **×64** |
| | | **2 Ranks (×16)** | **2 Ranks (×16)** |
| **Label Code** | | **PC2–6400M–666** | **PC2–5300M–555** |
| **JEDEC SPD Revision** | | **Rev. 1.2** | **Rev. 1.2** |
| **Byte#** | **Description** | **HEX** | **HEX** |
| 40 | $t_{RC}$ and $t_{RFC}$ Extension | 06 | 06 |
| 41 | $t_{RC.MIN}$ [ns] | 3C | 3C |
| 42 | $t_{RFC.MIN}$ [ns] | 7F | 7F |
| 43 | $t_{CK.MAX}$ [ns] | 80 | 80 |
| 44 | $t_{DQSQ.MAX}$ [ns] | 14 | 18 |
| 45 | $t_{QHS.MAX}$ [ns] | 1E | 22 |
| 46 | PLL Relock Time | 00 | 00 |
| 47 | $T_{CASE.MAX}$ Delta / $\Delta T_{4R4W}$ Delta | 53 | 53 |
| 48 | Psi(T-A) DRAM | 58 | 58 |
| 49 | $\Delta T_0$ (DT0) | 53 | 4F |
| 50 | $\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM) | 31 | 2D |
| 51 | $\Delta T_{2P}$ (DT2P) | 48 | 48 |
| 52 | $\Delta T_{3N}$ (DT3N) | 25 | 23 |
| 53 | $\Delta T_{3P.fast}$ (DT3P fast) | 46 | 43 |
| 54 | $\Delta T_{3P.slow}$ (DT3P slow) | 43 | 43 |
| 55 | $\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W) | 48 | 40 |
| 56 | $\Delta T_{5B}$ (DT5B) | 26 | 25 |
| 57 | $\Delta T_7$ (DT7) | 37 | 33 |
| 58 | Psi(ca) PLL | 00 | 00 |
| 59 | Psi(ca) REG | 00 | 00 |
| 60 | $\Delta T_{PLL}$ (DTPLL) | 00 | 00 |
| 61 | $\Delta T_{REG}$ (DTREG) / Toggle Rate | 00 | 00 |
| 62 | SPD Revision | 12 | 12 |
| 63 | Checksum of Bytes 0-62 | 41 | 5D |
| 64 | Manufacturer’s JEDEC ID Code (1) | 7F | 7F |
| 65 | Manufacturer’s JEDEC ID Code (2) | 7F | 7F |

| Product Type | | HYS64T128020EMV–2.5C2 | HYS64T128020EMV–3S–C2 |
|---|---|---|---|
| **Organization** | | **1 GByte** | **1 GByte** |
| | | **×64** | **×64** |
| | | **2 Ranks (×16)** | **2 Ranks (×16)** |
| **Label Code** | | **PC2–6400M–666** | **PC2–5300M–555** |
| **JEDEC SPD Revision** | | **Rev. 1.2** | **Rev. 1.2** |
| **Byte#** | **Description** | **HEX** | **HEX** |
| 66 | Manufacturer's JEDEC ID Code (3) | 7F | 7F |
| 67 | Manufacturer's JEDEC ID Code (4) | 7F | 7F |
| 68 | Manufacturer's JEDEC ID Code (5) | 7F | 7F |
| 69 | Manufacturer's JEDEC ID Code (6) | 51 | 51 |
| 70 | Manufacturer's JEDEC ID Code (7) | 00 | 00 |
| 71 | Manufacturer's JEDEC ID Code (8) | 00 | 00 |
| 72 | Module Manufacturer Location | xx | xx |
| 73 | Product Type, Char 1 | 36 | 36 |
| 74 | Product Type, Char 2 | 34 | 34 |
| 75 | Product Type, Char 3 | 54 | 54 |
| 76 | Product Type, Char 4 | 31 | 31 |
| 77 | Product Type, Char 5 | 32 | 32 |
| 78 | Product Type, Char 6 | 38 | 38 |
| 79 | Product Type, Char 7 | 30 | 30 |
| 80 | Product Type, Char 8 | 32 | 32 |
| 81 | Product Type, Char 9 | 30 | 30 |
| 82 | Product Type, Char 10 | 45 | 45 |
| 83 | Product Type, Char 11 | 4D | 4D |
| 84 | Product Type, Char 12 | 56 | 56 |
| 85 | Product Type, Char 13 | 32 | 33 |
| 86 | Product Type, Char 14 | 2E | 53 |
| 87 | Product Type, Char 15 | 35 | 43 |
| 88 | Product Type, Char 16 | 43 | 32 |
| 89 | Product Type, Char 17 | 32 | 20 |
| 90 | Product Type, Char 18 | 20 | 20 |
| 91 | Module Revision Code | 0x | 0x |

| **Product Type** | | **HYS64T128020EMV–2.5C2** | **HYS64T128020EMV–3S–C2** |
|---|---|---|---|
| **Organization** | | **1 GByte** | **1 GByte** |
| | | **×64** | **×64** |
| | | **2 Ranks (×16)** | **2 Ranks (×16)** |
| **Label Code** | | **PC2–6400M–666** | **PC2–5300M–555** |
| **JEDEC SPD Revision** | | **Rev. 1.2** | **Rev. 1.2** |
| **Byte#** | **Description** | **HEX** | **HEX** |
| 92 | Test Program Revision Code | xx | xx |
| 93 | Module Manufacturing Date Year | xx | xx |
| 94 | Module Manufacturing Date Week | xx | xx |
| 95 - 98 | Module Serial Number | xx | xx |
| 99 - 127 | Not used | 00 | 00 |
| 128 - 255 | Blank for customer use | FF | FF |

# 5 Package Outlines

**FIGURE 5**
**Package Outline L-DIM-214-1 Raw Card A**




### Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

# 6 Product Type Nomenclature

Qimonda’s nomenclature uses simple coding combined with some proprietary coding. **Table 21** provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 22** and for components in **Table 23**.

**TABLE 21**
**Nomenclature Fields and Examples**

| Example for | Field Number | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| Micro-DIMM | HYS | 64 | T | 64/128 | 0 | 2 | 0 | K | M | –5 | –A |
| DDR2 DRAM | HYB | 18 | T | 512/1G | 16 | | 0 | A | C | –5 | |

**TABLE 22**
**DDR2 DIMM Nomenclature**

| Field | Description | Values | Coding |
|---|---|---|---|
| 1 | Qimonda Module Prefix | HYS | Constant |
| 2 | Module Data Width [bit] | 64 | Non-ECC |
| | | 72 | ECC |
| 3 | DRAM Technology | T | DDR2 |
| 4 | Memory Density per I/O [Mbit]; Module Density[1)] | 32 | 256 MByte |
| | | 64 | 512 MByte |
| | | 128 | 1 GByte |
| | | 256 | 2 GByte |
| | | 512 | 4 GByte |
| 5 | Raw Card Generation | 0 .. 9 | Look up table |
| 6 | Number of Module Ranks | 0, 2, 4 | 1, 2, 4 |
| 7 | Product Variations | 0 .. 9 | Look up table |
| 8 | Package, Lead-Free Status | A .. Z | Look up table |
| 9 | Module Type | D | SO-**D**IMM |
| | | M | **M**icro-DIMM |
| | | R | **R**egistered |
| | | U | **U**nbuffered |
| | | F | **F**ully Buffered |

| Field | Description | Values | Coding |
|---|---|---|---|
| 10 | Speed Grade | –19F | PC2–8500 6–6–6 |
| | | –1.9 | PC2–8500 7–7–7 |
| | | –25F | PC2–6400 5–5–5 |
| | | –2.5 | PC2–6400 6–6–6 |
| | | –3 | PC2–5300 4–4–4 |
| | | –3S | PC2–5300 5–5–5 |
| | | –3.7 | PC2–4200 4–4–4 |
| | | –5 | PC2–3200 3–3–3 |
| 11 | Die Revision | –A | First |
| | | –B | Second |

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

## TABLE 23
### DDR2 DRAM Nomenclature

| Field | Description | Values | Coding |
|---|---|---|---|
| 1 | Qimonda Component Prefix | HYB | Constant |
| 2 | Interface Voltage [V] | 18 | SSTL_18 |
| 3 | DRAM Technology | T | DDR2 |
| 4 | Component Density [Mbit] | 256 | 256 Mbit |
| | | 512 | 512 Mbit |
| | | 1G | 1 Gbit |
| | | 2G | 2 Gbit |
| 5+6 | Number of I/Os | 40 | ×4 |
| | | 80 | ×8 |
| | | 16 | ×16 |
| 7 | Product Variations | 0 .. 9 | Look up table |
| 8 | Die Revision | A | First |
| | | B | Second |
| 9 | Package, Lead-Free Status | C | FBGA, lead-containing |
| | | F | FBGA, lead-free |
| 10 | Speed Grade | –19F | PC2–8500 6–6–6 |
| | | –1.9 | PC2–8500 7–7–7 |
| | | –25F | PC2–6400 5–5–5 |
| | | –2.5 | PC2–6400 6–6–6 |
| | | –3 | PC2–5300 4–4–4 |
| | | –3S | PC2–5300 5–5–5 |
| | | –3.7 | PC2–4200 4–4–4 |
| | | –5 | PC2–3200 3–3–3 |

# Contents

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