

SDRAM Unbuffered SODIMM

144pin Unbuffered SODIMM based on 256Mb J-die

54 TSOP-II/sTSOP II with Lead-Free and Halogen-Free
(RoHS compliant)

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Revision History

Revision	Month	Year	History
1.0	November	2007	- Initial Release
1.1	August	2008	- Changed module part number

144Pin Unbuffered SODIMM based on 256Mb J-die (x8, x16)

1.0 Ordering Information

Part Number	Density	Organization	Component Composition	Component Package	Height
M464S3254JLS-C(L)7A	256MB	32M x 64	16M x 16 (K4S561632J) * 8EA	54-TSOP(II)	1,250mil
M464S6453J60-C(L)7A	512MB	64M x 64	32M x 8 (K4S560832J) * 16EA	54-sTSOP(II)	1,250mil

Note:

1. "L" and "6" of Part number(11th digit) stand for Lead-Free, Halogen-Free, and RoHS compliant products.

2.0 Operating Frequencies

	7A	
	Speed @CL3	Speed @CL2
Maximum Clock Frequency	133MHz(7.5ns)	100MHz(10ns)
CL-tRCD-tRP	3-3-3	2-2-2

3.0 Feature

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V \pm 0.3V power supply
- MRS cycle with address key programs Latency (Access from column address)
Burst length (1, 2, 4, 8)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- 54pin TSOP II & sTSOP II **Lead-Free and Halogen Free** package
- All of products are Lead-Free and Halogen-Free, and RoHS compliant

4.0 Pin Configuration (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{SS}	2	V _{SS}	51	DQM14	52	DQM46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQM15	54	DQM47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	V _{SS}	56	V _{SS}	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	V _{DD}	102	V _{DD}
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	V _{DD}	12	V _{DD}	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	V _{SS}	108	VSS
15	DQ5	16	DQ37	109	A9	110	BA1				
17	DQ6	18	DQ38	61	**CLK0	62	**CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	V _{DD}	64	V _{DD}	113	V _{DD}	114	V _{DD}
21	V _{SS}	22	V _{SS}	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	**CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	**CS0	70	A12	119	V _{SS}	120	V _{SS}
27	V _{DD}	28	V _{DD}	71	**CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	**CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	V _{SS}	76	V _{SS}	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	V _{SS}	36	V _{SS}	79	NC	80	NC	129	V _{DD}	130	V _{DD}
37	DQ8	38	DQ40	81	V _{DD}	82	V _{DD}	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	V _{DD}	46	V _{DD}	89	DQ19	90	DQ51	139	V _{SS}	140	V _{SS}
47	DQ12	48	DQ44	91	V _{SS}	92	V _{SS}	141	SDA	142	SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	V _{DD}	144	V _{DD}

Note :

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

5.0 Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A12	Address input (Multiplexed)	WE	Write enable
BA0 ~ BA1	Select bank	DQM0 ~ 7	DQM
DQ0 ~ DQ63	Data input/output	V _{DD}	Power supply (3.3V)
CLK0, CLK1	Clock input	V _{SS}	Ground
CKE0, CKE1	Clock enable input	SDA	Serial data I/O
CS0, CS1	Chip select input	SCL	Serial clock
RAS	Row address strobe	DU	Don't use
CAS	Column address strobe	NC	No connection

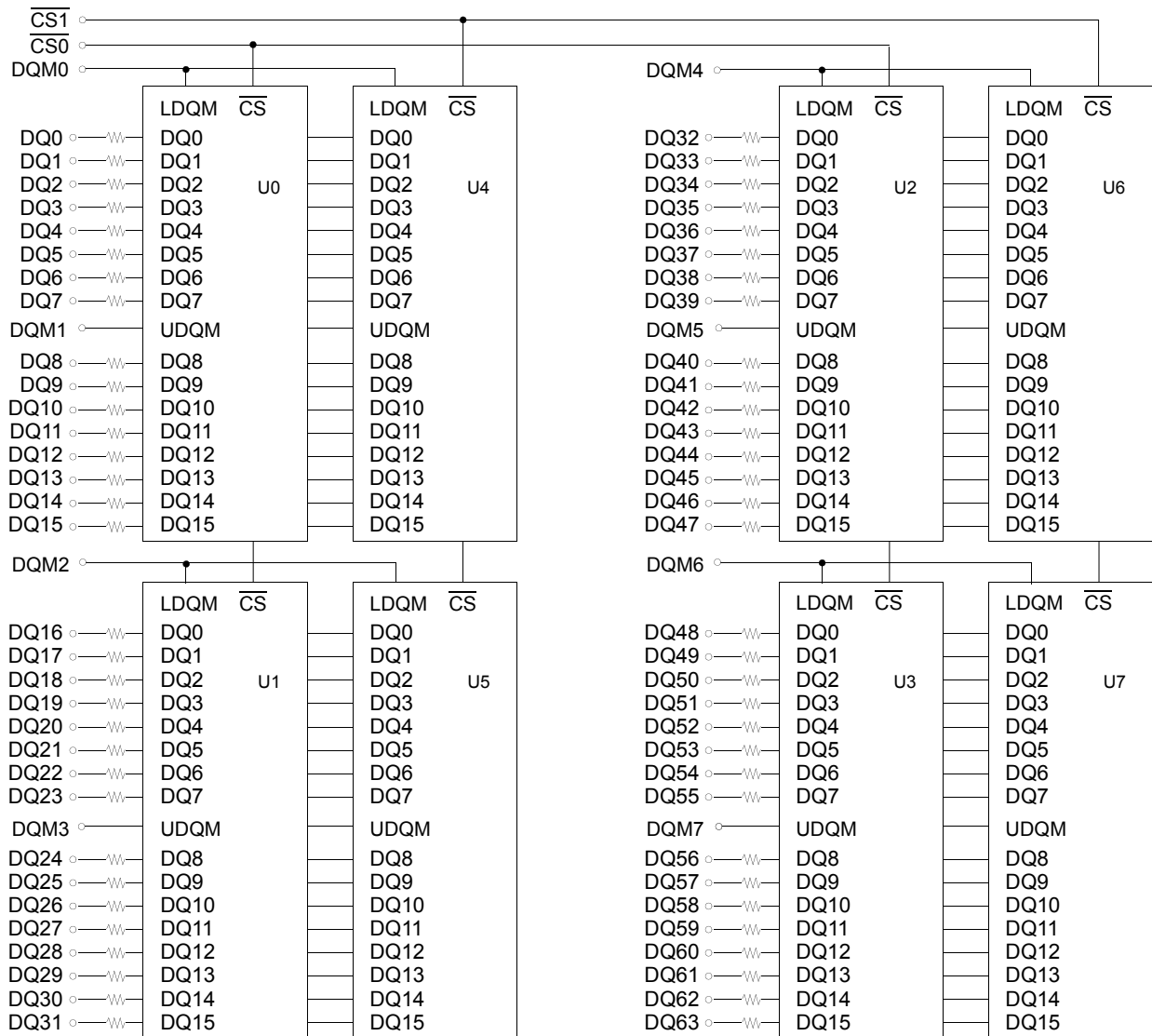
6.0 Pin Configuration Description

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12 Column address : (x16 : CA0 ~ CA9)
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
V _{DD} /V _{SS}	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

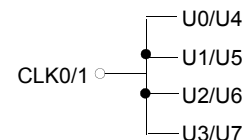
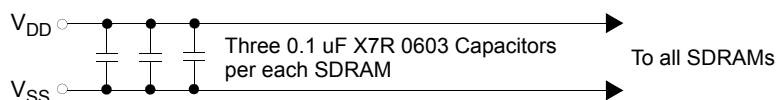
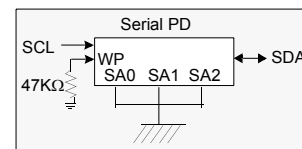
7.0 Functional Block Diagram

7.1 256MB, 32Mx64 Module (M464S3254JLS)

(Populated as 2 bank of x16 SDRAM Module)

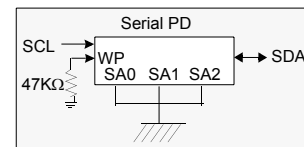
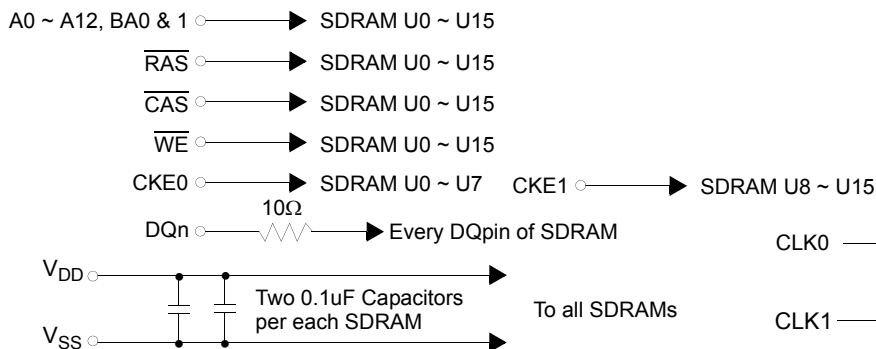
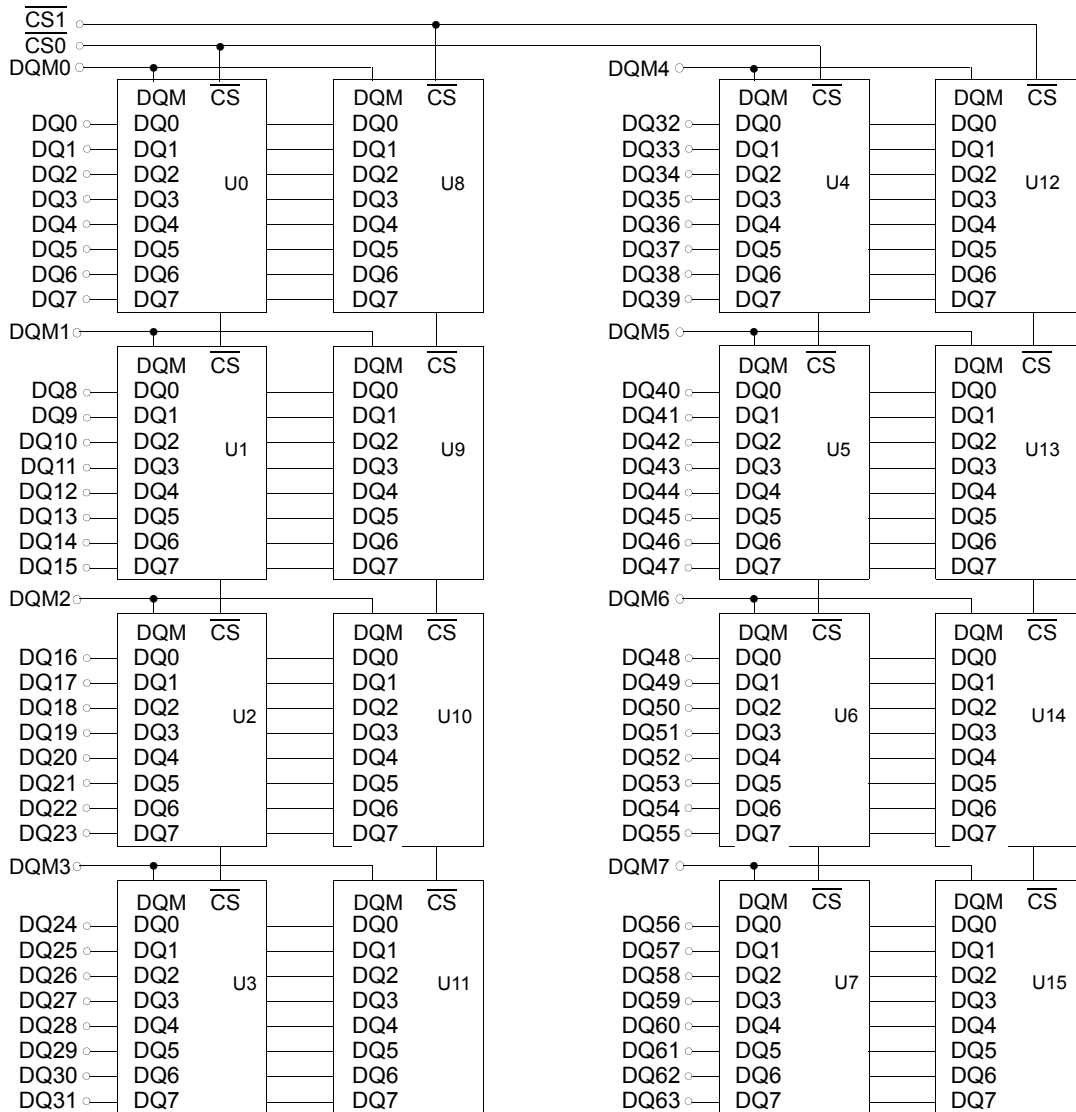


- A0 ~ A12, BA0 & 1 → SDRAM U0 ~ U7
- $\overline{\text{RAS}}$ → SDRAM U0 ~ U7
- $\overline{\text{CAS}}$ → SDRAM U0 ~ U7
- $\overline{\text{WE}}$ → SDRAM U0 ~ U7
- CKE0 → SDRAM U0 ~ U3
- CKE1 → SDRAM U4 ~ U7
- 10Ω DQn → Every DQ pin of SDRAM



7.2 512MB, 64Mx64 Module (M464S6453J60)

(Populated as 2 bank of x8 SDRAM Module)



8.0 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.0 * # of component	W
Short circuit current	I_{OS}	50	mA

Note :

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

9.0 DC Operating Conditions And Characteristics

Recommended operating conditions (Voltage referenced to $V_{SS} = 0V$, $T_A = 0$ to $70^\circ C$)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	$V_{DDQ}+0.3$	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	$I_{OH} = -2mA$
Output low voltage	V_{OL}	-	-	0.4	V	$I_{OL} = 2mA$
Input leakage current	I_{LI}	-10	-	10	μA	3

Note :

1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is $\leq 3ns$.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is $\leq 3ns$.

3. Any input $0V \leq V_{IN} \leq V_{DDQ}$. Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

10.0 Capacitance(Max.)

($V_{DD} = 3.3V$, $T_A = 23^\circ C$, $f = 1MHz$, $V_{REF} = 1.4V \pm 200 mV$)

Parameter	Symbol	M464S3254JLS		M464S6453J60		Unit
		Min	Max	Min	Max	
Input capacitance ($A_0 \sim A_{12}$, $BA_0 \sim BA_1$)	C_{IN1}	25	45	45	90	pF
Input capacitance (\overline{RAS} , \overline{CAS} , \overline{WE})	C_{IN2}	25	45	45	90	pF
Input capacitance ($CKE_0 \sim CKE_1$)	C_{IN3}	15	25	25	45	pF
Input capacitance ($CLK_0 \sim CLK_1$)	C_{IN4}	15	21	15	21	pF
Input capacitance ($\overline{CS_0} \sim \overline{CS_1}$)	C_{IN5}	15	25	15	25	pF
Input capacitance ($DQM_0 \sim DQM_7$)	C_{IN6}	10	12	10	15	pF
Data input/output capacitance ($DQ_0 \sim DQ_{63}$)	C_{OUT}	10	12	13	18	pF

11.0 DC CHARACTERISTICS

11.1 M464S3254JLS (32M x 64, 256MB Module)

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note	
			7A			
Operating current (One bank active)	Icc1	Burst length = 1, $t_{RC} \geq t_{RC}(\text{min})$, $I_O = 0$ mA	392	mA	1	
Precharge standby current in power-down mode	Icc2P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	16	mA		
	Icc2PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	16			
Precharge standby current in non power-down mode	Icc2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	120	mA		
	Icc2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	80			
Active standby current in power-down mode	Icc3P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	40	mA		
	Icc3PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	40			
Active standby current in non power-down mode (One bank active)	Icc3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	224	mA		
	Icc3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	160	mA		
Operating current (Burst mode)	Icc4	$I_O = 0$ mA, Page burst 4Banks activated $t_{CCD} = 2\text{CLKs}$	552	mA	1	
Refresh current	Icc5	$t_{RC} \geq t_{RC}(\text{min})$	752	mA	2	
Self refresh current	Icc6	$\text{CKE} \leq 0.2\text{V}$	C	24	mA	
			L	12	mA	

11.2 M464S6453J60 (64M x64, 512MB Module)

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note	
			7A			
Operating current (One bank active)	Icc1	Burst length = 1, $t_{RC} \geq t_{RC}(\text{min})$, $I_O = 0$ mA	784	mA	1	
Precharge standby current in power-down mode	Icc2P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	32	mA		
	Icc2PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	32			
Precharge standby current in non power-down mode	Icc2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	240	mA		
	Icc2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	160			
Active standby current in power-down mode	Icc3P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	80	mA		
	Icc3PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	80			
Active standby current in non power-down mode (One bank active)	Icc3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	448	mA		
	Icc3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	320	mA		
Operating current (Burst mode)	Icc4	$I_O = 0$ mA, Page burst 4Banks activated $t_{CCD} = 2\text{CLKs}$	1,104	mA	1	
Refresh current	Icc5	$t_{RC} \geq t_{RC}(\text{min})$	1,504	mA	2	
Self refresh current	Icc6	$\text{CKE} \leq 0.2\text{V}$	C	48	mA	
			L	24	mA	

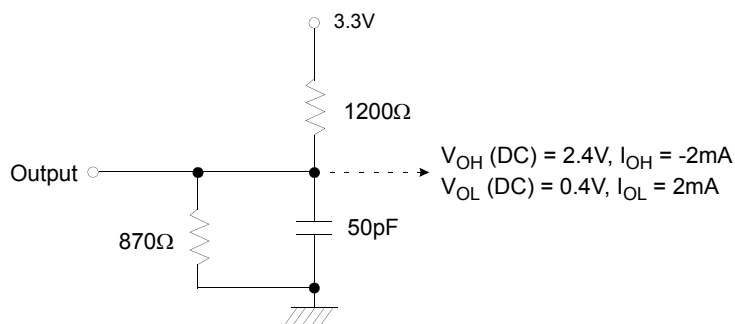
Note :

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is $\text{CMOS}(V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ})$

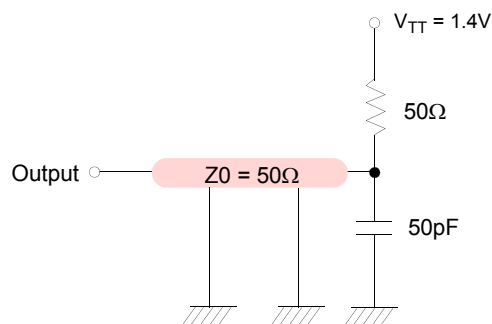
12.0 AC Operating Test Conditions

($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^{\circ}C$)

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

13.0 OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		7A		
Row active to row active delay	$t_{RRD}(\min)$	15	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	ns	1
Row active time	$t_{RAS}(\min)$	45	ns	1
	$t_{RAS}(\max)$	100	us	
Row cycle time	$t_{RC}(\min)$	65	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + t_{RP}	-	
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

Note :

- The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
- Minimum delay is required to complete write.
- All parts allow every cycle column address change.
- In case of row precharge interrupt, auto precharge and read burst stop.

14.0 AC CHARACTERISTICS

REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

(AC operating conditions unless otherwise noted)

Parameter		Symbol	7A		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
	CAS latency=2		10			
CLK to valid output delay	CAS latency=3	tSAC	-	5.4	ns	1,2
	CAS latency=2		-	6		
Output data hold time	CAS latency=3	tOH	3	-	ns	2
	CAS latency=2		3	-		
CLK high pulse width		tCH	2.5	-	ns	3
CLK low pulse width		tCL	2.5	-	ns	3
Input setup time		tSS	1.5	-	ns	3
Input hold time		tSH	0.8	-	ns	3
CLK to output in Low-Z		tSLZ	1	-	ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	5.4	ns	
	CAS latency=2		-	6		

Note :

- Parameters depend on programmed CAS latency.
- If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
- Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.
If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered, i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

15.0 SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Command		CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	DQM	BA0,1	A10/AP	A0 ~ A9, A11, A12	Note
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh	H	H	L	L	L	H	X	X	X		3
	Entry		L									3
	Self refresh	Exit	L	H	L	H	H	H	X	X		3
					H	X	X	X				3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address	4
	Auto precharge enable									H		4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address	4
	Auto precharge enable									H		4,5
Burst stop		H	X	L	H	H	L	X	X			6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	All banks								X	H		
Clock suspend or active power down	Entry	H	L	H	X	X	X	X	X	X		
				L	V	V	V					
Precharge power down mode	Entry	H	L	H	X	X	X	X	X	X		
				L	H	H	H					
	Exit	L	H	H	X	X	X	X	X	X		
				L	V	V	V					
DQM		H		X				V	X			7
No operation command		H	X	H	X	X	X	X	X	X		
				L	H	H	H					

Note :

1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

