

# DDR2 SDRAM RDIMM

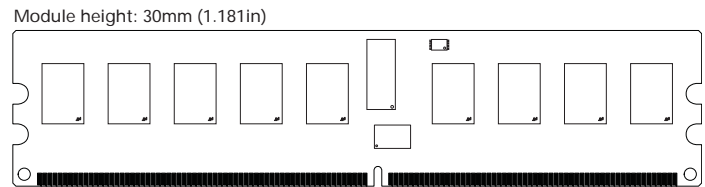
## MT9HTF12872PZ – 1GB

For component data sheets, refer to Micron's Web site: [www.micron.com](http://www.micron.com)

### Features

- 240-pin, registered dual in-line memory module (RDIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- 1GB (128 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD} = V_{DDQ} = +1.8V$
- $V_{DDSPD} = +1.7V$  to  $+3.6V$
- JEDEC-standard 1.8V I/O (SSTL\_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Single rank
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 tCK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Halogen-free
- Gold edge contacts

Figure 1: 240-Pin RDIMM (MO-237 R/C F)



### Options

- Parity
- Operating temperature<sup>1</sup>
  - Commercial ( $0^{\circ}C \leq T_A \leq +70^{\circ}C$ )
  - Industrial ( $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ )
- Package
  - 240-pin DIMM (halogen-free)
- Frequency/CAS latency<sup>2</sup>
  - 2.5ns @ CL = 5 (DDR2-800)
  - 2.5ns @ CL = 6 (DDR2-800)
  - 3.0ns @ CL = 5 (DDR2-667)

### Marking

- P
- None
- I
- Z
- 80E
- 800
- 667

Notes: 1. Contact Micron for industrial temperature module offerings.

2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				t <sub>RCD</sub> (ns)	t <sub>RP</sub> (ns)	t <sub>RC</sub> (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	800	800	533	400	12.5	12.5	55
-800	PC2-6400	800	667	533	400	15	15	55
-667	PC2-5300	-	667	533	400	15	15	55
-53E	PC2-4200	-	-	533	400	15	15	55
-40E	PC2-3200	-	-	400	400	15	15	55

**Table 2: Addressing**

Parameter	1GB
Refresh count	8K
Row address	16K A[13:0]
Device bank address	8 BA[2:0]
Device page size per bank	1KB
Device configuration	1Gb (128 Meg x 8)
Column address	1K A[9:0]
Module rank address	1 S0#

**Table 3: Part Numbers and Timing Parameters – 1GB Modules**

Base device: MT47H128M8,<sup>1</sup> 1Gb DDR2 SDRAM

Part Number <sup>2</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL- <sup>t</sup> RCD- <sup>t</sup> RP)
MT9HTF12872P(I)Z-80E__	1GB	128 Meg x 72	6.2 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF12872P(I)Z-800__	1GB	128 Meg x 72	6.2 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF12872P(I)Z-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5

- Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
  2. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9HTF12872PZ-80EH1.

## Pin Assignments and Descriptions

Table 4: Pin Assignments

240-Pin DDR2 RDIMM Front								240-Pin DDR2 RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol		
1	V <sub>REF</sub>	31	DQ19	61	A4	91	V <sub>SS</sub>	121	V <sub>SS</sub>	151	V <sub>SS</sub>	181	V <sub>DDQ</sub>	211	DM5/ DQS14
2	V <sub>SS</sub>	32	V <sub>SS</sub>	62	V <sub>DDQ</sub>	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NF/ DQS14#
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	V <sub>SS</sub>
4	DQ1	34	DQ25	64	V <sub>DD</sub>	94	V <sub>SS</sub>	124	V <sub>SS</sub>	154	V <sub>SS</sub>	184	V <sub>DD</sub>	214	DQ46
5	V <sub>SS</sub>	35	V <sub>SS</sub>	65	V <sub>SS</sub>	95	DQ42	125	DM0/ DQS9	155	DM3/ DQS12	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	V <sub>SS</sub>	96	DQ43	126	NF/ DQS9#	156	NF/ DQS12#	186	CK0#	216	V <sub>SS</sub>
7	DQS0	37	DQS3	67	V <sub>DD</sub>	97	V <sub>SS</sub>	127	V <sub>SS</sub>	157	V <sub>SS</sub>	187	V <sub>DD</sub>	217	DQ52
8	V <sub>SS</sub>	38	V <sub>SS</sub>	68	Par_In	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	V <sub>DD</sub>	99	DQ49	129	DQ7	159	DQ31	189	V <sub>DD</sub>	219	V <sub>SS</sub>
10	DQ3	40	DQ27	70	A10	100	V <sub>SS</sub>	130	V <sub>SS</sub>	160	V <sub>SS</sub>	190	BA1	220	NC
11	V <sub>SS</sub>	41	V <sub>SS</sub>	71	BA0	101	SA2	131	DQ12	161	CB4	191	V <sub>DDQ</sub>	221	NC
12	DQ8	42	CB0	72	V <sub>DDQ</sub>	102	NC	132	DQ13	162	CB5	192	RAS#	222	V <sub>SS</sub>
13	DQ9	43	CB1	73	WE#	103	V <sub>SS</sub>	133	V <sub>SS</sub>	163	V <sub>SS</sub>	193	S0#	223	DM6/ DQS15
14	V <sub>SS</sub>	44	V <sub>SS</sub>	74	CAS#	104	DQS6#	134	DM1/ DQS10	164	DM8/ DQS17	194	V <sub>DDQ</sub>	224	NF/ DQS15#
15	DQS1#	45	DQS8#	75	V <sub>DDQ</sub>	105	DQS6	135	NF/ DQS10#	165	NF/ DQS17#	195	ODT0	225	V <sub>SS</sub>
16	DQS1	46	DQS8	76	NC	106	V <sub>SS</sub>	136	V <sub>SS</sub>	166	V <sub>SS</sub>	196	A13	226	DQ54
17	V <sub>SS</sub>	47	V <sub>SS</sub>	77	NC	107	DQ50	137	NC	167	CB6	197	V <sub>DD</sub>	227	DQ55
18	RESET#	48	CB2	78	V <sub>DDQ</sub>	108	DQ51	138	NC	168	CB7	198	V <sub>SS</sub>	228	V <sub>SS</sub>
19	NC	49	CB3	79	V <sub>SS</sub>	109	V <sub>SS</sub>	139	V <sub>SS</sub>	169	V <sub>SS</sub>	199	DQ36	229	DQ60
20	V <sub>SS</sub>	50	V <sub>SS</sub>	80	DQ32	110	DQ56	140	DQ14	170	V <sub>DDQ</sub>	200	DQ37	230	DQ61
21	DQ10	51	V <sub>DDQ</sub>	81	DQ33	111	DQ57	141	DQ15	171	NC	201	V <sub>SS</sub>	231	V <sub>SS</sub>
22	DQ11	52	CKE0	82	V <sub>SS</sub>	112	V <sub>SS</sub>	142	V <sub>SS</sub>	172	V <sub>DD</sub>	202	DM4/ DQS13	232	DM7/ DQS16
23	V <sub>SS</sub>	53	V <sub>DD</sub>	83	DQS4#	113	DQS7#	143	DQ20	173	A15	203	NF/ DQS13#	233	NF/ DQS16#
24	DQ16	54	BA2	84	DQS4	114	DQS7	144	DQ21	174	A14	204	V <sub>SS</sub>	234	V <sub>SS</sub>
25	DQ17	55	Err_Out	85	V <sub>SS</sub>	115	V <sub>SS</sub>	145	V <sub>SS</sub>	175	V <sub>DDQ</sub>	205	DQ38	235	DQ62
26	V <sub>SS</sub>	56	V <sub>DDQ</sub>	86	DQ34	116	DQ58	146	DM2/ DQS11	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NF/ DQS11#	177	A9	207	V <sub>SS</sub>	237	V <sub>SS</sub>
28	DQS2	58	A7	88	V <sub>SS</sub>	118	V <sub>SS</sub>	148	V <sub>SS</sub>	178	V <sub>DD</sub>	208	DQ44	238	V <sub>DDSPD</sub>
29	V <sub>SS</sub>	59	V <sub>DD</sub>	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	V <sub>SS</sub>	240	SA1

**Table 5: Pin Descriptions**

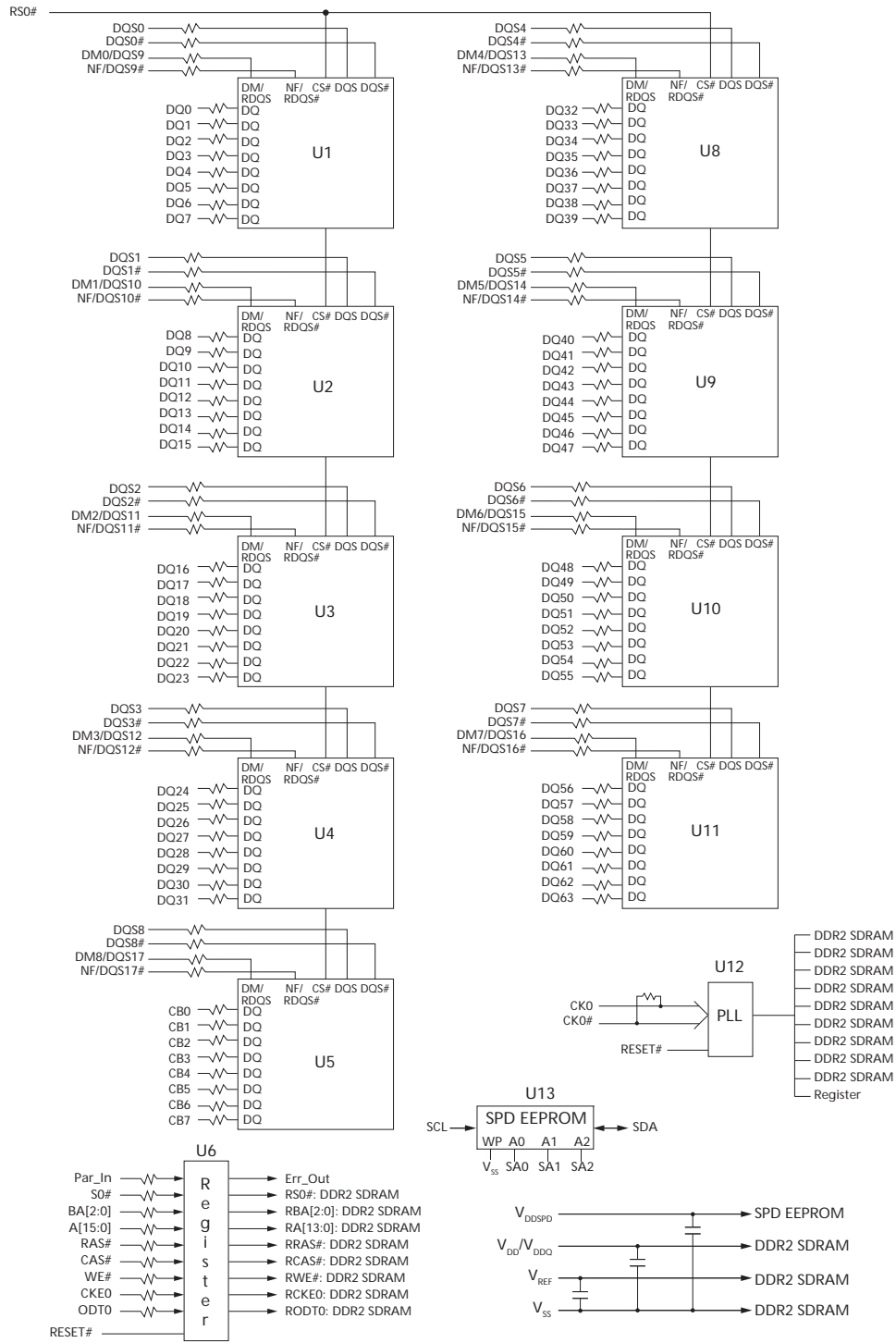
Symbol	Type	Description
A[15:0]	Input	<b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA[2:0]) or all device banks (A10 HIGH). A[13:0] (1GB). A[15:14] are connected for parity.
BA[2:0]	Input	<b>Bank address inputs:</b> BA[2:0] define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR, EMR1, EMR2, and EMR3) is loaded during the LOAD MODE command.
CK0, CK0#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ, DQS, and DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input	<b>Clock enable:</b> CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM.
DM[8:0]/ DQS[17:9], DQS#[17:9]	Input	<b>Input data mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of DQS. Although the DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins. If RDQS is disabled, DQS[17:9] become DM[8:0] and DQS#[17:9] are no function.
ODT0	Input	<b>On-die termination:</b> ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	<b>Parity input:</b> Parity bit for the address, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	<b>Command inputs:</b> RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	<b>Reset:</b> Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
S0#	Input	<b>Chip select:</b> S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	<b>Serial address inputs:</b> These pins are used to configure the SPD EEPROM address range on the I <sup>2</sup> C bus.
SCL	Input	<b>Serial clock for SPD EEPROM:</b> SCL is used to synchronize communication to and from the SPD EEPROM.
CB[7:0]	I/O	Check bits.
DQ[63:0]	I/O	<b>Data input/output:</b> Bidirectional data bus.
DQS[8:0], DQS#[8:0]	I/O	<b>Data strobe:</b> DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	<b>Serial data:</b> SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module on the I <sup>2</sup> C bus.
Err_Out	Output (open drain)	<b>Parity error output:</b> Parity error found on the command and address bus.
EVENT#	Output (open drain)	<b>Temperature event:</b> The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V <sub>DD</sub> /V <sub>DDQ</sub>	Supply	<b>Power supply:</b> 1.8V ±0.1V. The component V <sub>DD</sub> and V <sub>DDQ</sub> are connected to the module V <sub>DD</sub> .
V <sub>DDSPD</sub>	Supply	<b>SPD EEPROM power supply:</b> +1.7V to +3.6V.
V <sub>REF</sub>	Supply	<b>Reference voltage:</b> V <sub>DD</sub> /2.
V <sub>SS</sub>	Supply	Ground.

Table 5: Pin Descriptions (continued)

Symbol	Type	Description
NC	-	<b>No connect:</b> These pins are not connected on the module.
NF	-	<b>No function:</b> Connected within the module, but provides no functionality.

## Functional Block Diagram

Figure 2: Functional Block Diagram



## General Description

The MT9HTF12872PZ DDR2 SDRAM module is a high-speed, CMOS, dynamic random access 1GB memory module organized in a x72 configuration. This DDR2 SDRAM module uses internally configured, 8-bank DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a  $4n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single  $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

## Register and PLL Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The register(s) and PLL reduce address, command, control, and clock signal loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

## Parity Operations

The registering clock driver can accept a parity bit from the system's memory controller, providing even parity for the control, command, and address bus. Parity errors are flagged on the Err\_Out# pin. Systems not using parity are expected to function without issue if Par\_In and Err\_Out# are left as no connects to the system.

## Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I<sup>2</sup>C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is connected to V<sub>SS</sub>, permanently disabling hardware write protect.

## Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions above those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 6: Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Units	
$V_{DD}/V_{DDQ}$	$V_{DD}/V_{DDQ}$ supply voltage relative to $V_{SS}$	-0.5	+2.3	V	
$V_{IN}, V_{OUT}$	Voltage on any pin relative to $V_{SS}$	-0.5	+2.3	V	
$I_I$	Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$ ; $V_{REF}$ input $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = $0V$ )	Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA	-5	+5	$\mu A$
		CK, CK#	-250	+250	
		DM	-5	+5	
$I_{OZ}$	Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$ ; DQ and ODT are disabled	-5	+5	$\mu A$	
$I_{VREF}$	$V_{REF}$ leakage current; $V_{REF}$ = valid $V_{REF}$ level	-18	+18	$\mu A$	
$T_A$	Module ambient operating temperature	Commercial	0	+70	$^{\circ}C$
		Industrial	-40	+85	$^{\circ}C$
$T_C^1$	DDR2 SDRAM component case operating temperature <sup>2</sup>	Commercial	0	+85	$^{\circ}C$
		Industrial	-40	+95	$^{\circ}C$

- Notes: 1. The refresh rate is required to double when  $85^{\circ}C < T_C \leq 95^{\circ}C$ .  
2. For further information, refer to technical note [TN-00-08: Thermal Applications](#), available on Micron's Web site.



## DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 7.

**Table 7: Module and Component Speed Grades**  
DDR2 components may exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-5E

## Design Considerations

### Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

### Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

## I<sub>DD</sub> Specifications

**Table 8: DDR2 I<sub>DD</sub> Specifications and Conditions – 1GB**

Values shown for MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition	Symbol	-80E/ -800	-667	Units	
<b>Operating one bank active-precharge current:</b> $t_{CK} = t_{CK}(I_{DD})$ , $t_{RC} = t_{RC}(I_{DD})$ , $t_{RAS} = t_{RAS\ MIN}(I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I <sub>DD0</sub>	810	765	mA	
<b>Operating one bank active-read-precharge current:</b> I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK}(I_{DD})$ , $t_{RC} = t_{RC}(I_{DD})$ , $t_{RAS} = t_{RAS\ MIN}(I_{DD})$ , $t_{RCD} = t_{RCD}(I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I <sub>DD4W</sub>	I <sub>DD1</sub>	990	900	mA	
<b>Precharge power-down current:</b> All device banks idle; $t_{CK} = t_{CK}(I_{DD})$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I <sub>DD2P</sub>	63	63	mA	
<b>Precharge quiet standby current:</b> All device banks idle; $t_{CK} = t_{CK}(I_{DD})$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	I <sub>DD2Q</sub>	450	360	mA	
<b>Precharge standby current:</b> All device banks idle; $t_{CK} = t_{CK}(I_{DD})$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	I <sub>DD2N</sub>	450	360	mA	
<b>Active power-down current:</b> All device banks open; $t_{CK} = t_{CK}(I_{DD})$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I <sub>DD3P</sub>	Fast PDN exit MR[12] = 0	360	270	mA
		Slow PDN exit MR[12] = 1	90	90	mA
<b>Active standby current:</b> All device banks open; $t_{CK} = t_{CK}(I_{DD})$ , $t_{RAS} = t_{RAS\ MAX}(I_{DD})$ , $t_{RP} = t_{RP}(I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I <sub>DD3N</sub>	540	495	mA	
<b>Operating burst write current:</b> All device banks open; Continuous burst writes; BL = 4, CL = CL(I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK}(I_{DD})$ , $t_{RAS} = t_{RAS\ MAX}(I_{DD})$ , $t_{RP} = t_{RP}(I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I <sub>DD4W</sub>	1440	1215	mA	
<b>Operating burst read current:</b> All device banks open; Continuous burst reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK}(I_{DD})$ , $t_{RAS} = t_{RAS\ MAX}(I_{DD})$ , $t_{RP} = t_{RP}(I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I <sub>DD4R</sub>	1440	1215	mA	
<b>Burst refresh current:</b> $t_{CK} = t_{CK}(I_{DD})$ ; REFRESH command at every $t_{RFC}(I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I <sub>DD5</sub>	2115	1935	mA	
<b>Self refresh current:</b> CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	I <sub>DD6</sub>	63	63	mA	
<b>Operating bank interleave read current:</b> All device banks interleaving reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>DD</sub> ), AL = $t_{RCD}(I_{DD}) - 1 \times t_{CK}(I_{DD})$ ; $t_{CK} = t_{CK}(I_{DD})$ , $t_{RC} = t_{RC}(I_{DD})$ , $t_{RRD} = t_{RRD}(I_{DD})$ , $t_{RCD} = t_{RCD}(I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching	I <sub>DD7</sub>	3015	2520	mA	

## Register and PLL Specifications

**Table 9: Register Specifications**  
SSTU32866 devices or equivalent

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	$V_{IH(DC)}$	Address, control, command	SSTL_18	$V_{REF(DC)} + 125$	$V_{DDQ} + 250$	mV
DC low-level input voltage	$V_{IL(DC)}$	Address, control, command	SSTL_18	0	$V_{REF(DC)} - 125$	mV
AC high-level input voltage	$V_{IH(AC)}$	Address, control, command	SSTL_18	$V_{REF(DC)} + 250$	$V_{DD}$	mV
AC low-level input voltage	$V_{IL(AC)}$	Address, control, command	SSTL_18	0	$V_{REF(DC)} - 250$	mV
Output high voltage	$V_{OH}$	Parity output	LVC MOS	1.2	–	V
Output low voltage	$V_{OL}$	Parity output	LVC MOS	–	0.5	V
Input current	$I_I$	All pins	$V_I = V_{DDQ}$ or $V_{SSQ}$	–5	+5	$\mu$ A
Static standby	$I_{DD}$	All pins	RESET# = $V_{SSQ}$ ( $I_O = 0$ )	–	100	$\mu$ A
Static operating	$I_{DD}$	All pins	RESET# = $V_{SSQ}$ ; $V_I = V_{IH(AC)}$ or $V_{IL(DC)}$ $I_O = 0$	–	40	mA
Dynamic operating (clock tree)	$I_{DDD}$	n/a	RESET# = $V_{DD}$ , $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , $I_O = 0$ ; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	$\mu$ A
Dynamic operating (per each input)	$I_{DDD}$	n/a	RESET# = $V_{DD}$ , $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , $I_O = 0$ ; CK and CK# switching 50% duty cycle; One data input switching at $t_{CK}/2$ , 50% duty cycle	–	Varies by manufacturer	$\mu$ A
Input capacitance (per device, per pin)	$C_I$	All inputs except RESET#	$V_I = V_{REF} \pm 250$ mV; $V_{DDQ} = 1.8$ V	2.5	3.5	pF
Input capacitance (per device, per pin)	$C_I$	RESET#	$V_I = V_{DDQ}$ or $V_{SSQ}$	–	Varies by manufacturer	pF

Notes: 1. Timing and switching specifications for the registers listed above are critical for proper operation of the DDR2 SDRAM registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC Standard JESD82.

**Table 10: PLL Specifications**  
 CU877 device or equivalent

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	$V_{IH}$	RESET#	LVC MOS	$0.65 \times V_{DD}$	-	V
DC low-level input voltage	$V_{IL}$	RESET#	LVC MOS	-	$0.35 \times V_{DD}$	V
Input voltage (limits)	$V_{IN}$	RESET#, CK, CK#		-0.3	$V_{DDQ} + 0.3$	V
DC high-level input voltage	$V_{IH}$	CK, CK#	Differential input	$0.65 \times V_{DD}$	-	V
DC low-level input voltage	$V_{IL}$	CK, CK#	Differential input	-	$0.35 \times V_{DD}$	V
Input differential-pair cross voltage	$V_{IX}$	CK, CK#	Differential input	$(V_{DDQ}/2) - 0.15$	$(V_{DDQ}/2) + 0.15$	V
Input differential voltage	$V_{ID(DC)}$	CK, CK#	Differential input	0.3	$V_{DDQ} + 0.4$	V
Input differential voltage	$V_{ID(AC)}$	CK, CK#	Differential input	0.6	$V_{DDQ} + 0.4$	V
Input current	$I_I$	RESET#	$V_I = V_{DDQ}$ or $V_{SSQ}$	-10	+10	$\mu A$
		CK, CK#	$V_I = V_{DDQ}$ or $V_{SSQ}$	-250	+250	$\mu A$
Output disabled current	$I_{ODL}$		RESET# = $V_{SSQ}$ ; $V_I = V_{IH(AC)}$ or $V_{IL(DC)}$	100	-	$\mu A$
Static supply current	$I_{DDLD}$		CK = CK# = LOW	-	500	$\mu A$
Dynamic supply	$I_{DD}$	n/a	CK, CK# = 410 MHz, all outputs open (not connected to PCB)	-	300	mA
Input capacitance	$C_{IN}$	Each input	$V_I = V_{DDQ}$ or $V_{SSQ}$	2	3	pF

**Table 11: PLL Clock Driver Timing Requirements and Switching Characteristics**

Parameter	Symbol	Min	Max	Units
Stabilization time	$t_L$	-	15	$\mu s$
Input clock slew rate	slr(i)	1.0	4	V/ns
SSC modulation frequency		30	33	kHz
SSC clock input frequency deviation		0.0	-0.50	%
PLL loop bandwidth (-3dB from unity gain)		2.0	-	MHz

Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC Standard JESD82.

## Serial Presence-Detect

**Table 12: Serial Presence-Detect EEPROM DC Operating Conditions**  
All voltages referenced to  $V_{SS}$

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	$V_{DDSPD}$	1.7	3.6	V
Input high voltage: Logic 1; All inputs	$V_{IH}$	$V_{DDSPD} \times 0.7$	$V_{DDSPD} + 0.5$	V
Input low voltage: Logic 0; All inputs	$V_{IL}$	-0.6	$V_{DDSPD} \times 0.3$	V
Output low voltage: $I_{OUT} = 3\text{mA}$	$V_{OL}$	-	0.4	V
Input leakage current: $V_{IN} = \text{GND to } V_{DD}$	$I_{LI}$	0.10	3	$\mu\text{A}$
Output leakage current: $V_{OUT} = \text{GND to } V_{DD}$	$I_{LO}$	0.05	3	$\mu\text{A}$
Standby current	$I_{SB}$	1.6	4	$\mu\text{A}$
Power supply current, READ: SCL clock frequency = 100 kHz	$I_{CCR}$	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	$I_{CCW}$	2	3	mA

**Table 13: Serial Presence-Detect EEPROM AC Operating Conditions**  
All voltages referenced to  $V_{SS}$

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	$t_{AA}$	0.2	0.9	$\mu\text{s}$	1
Time the bus must be free before a new transition can start	$t_{BUF}$	1.3	-	$\mu\text{s}$	
Data-out hold time	$t_{DH}$	200	-	ns	
SDA and SCL fall time	$t_F$	-	300	ns	2
Data-in hold time	$t_{HD:DAT}$	0	-	$\mu\text{s}$	
Start condition hold time	$t_{HD:STA}$	0.6	-	$\mu\text{s}$	
Clock HIGH period	$t_{HIGH}$	0.6	-	$\mu\text{s}$	
Noise suppression time constant at SCL, SDA inputs	$t_I$	-	50	ns	
Clock LOW period	$t_{LOW}$	1.3	-	$\mu\text{s}$	
SDA and SCL rise time	$t_R$	-	0.3	$\mu\text{s}$	2
SCL clock frequency	$f_{SCL}$	-	400	kHz	
Data-in setup time	$t_{SU:DAT}$	100	-	ns	
Start condition setup time	$t_{SU:STA}$	0.6	-	$\mu\text{s}$	3
Stop condition setup time	$t_{SU:STO}$	0.6	-	$\mu\text{s}$	
WRITE cycle time	$t_{WRC}$	-	10	ms	4

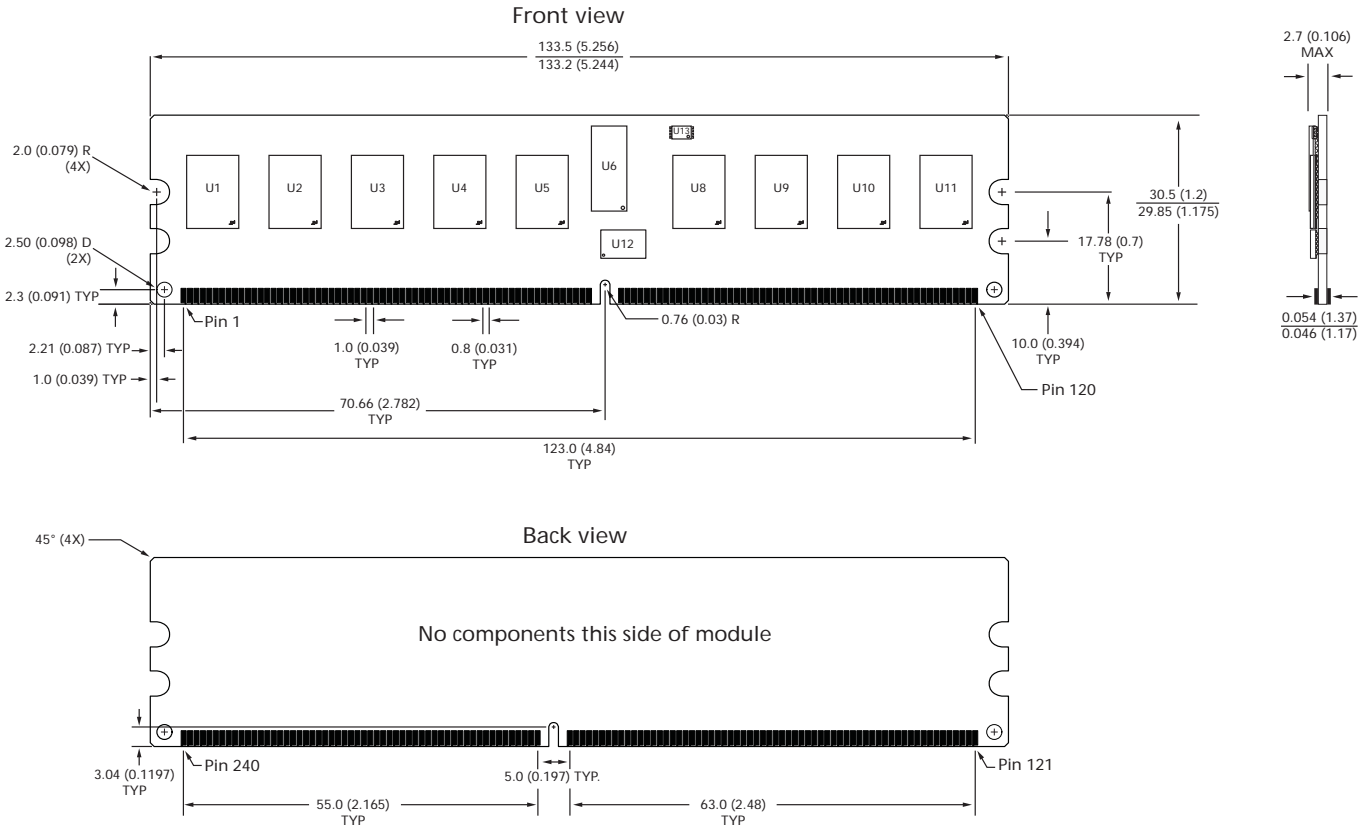
- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
  2. This parameter is sampled.
  3. For a restart condition, or following a WRITE cycle.
  4. The SPD EEPROM WRITE cycle time ( $t_{WRC}$ ) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

## Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page:  
[www.micron.com/SPD](http://www.micron.com/SPD).

## Module Dimensions

Figure 3: 240-Pin DDR2 RDIMM



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
  2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.

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