1.5V DDR2 SDRAM FBDIMM

MT18GTF25672FDY – 2GB

For the component data sheet, refer to Micron's Web site: www.micron.com

Features

- 240-pin, fully buffered DIMM (FBDIMM)
- Very low-power DDR2 operation
- 1.425V ≤ V_{DD} ≤ 1.625V for DDR2 SDRAM
- 1.425V ≤ V_{DD} ≤ 1.625V for advanced memory buffer (AMB) DRAM I/O
- V_{DD} = 1.50V (NOM)
- 1.8V tolerant for ≤ 100ms
- Dual rank
- Component configuration: 128 Meg x 8

Functionality

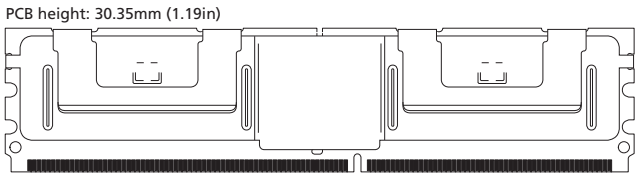
The 2GB FBDIMM at 1.50V (MT18GTF25672FD) consumes less power than the standard 1.8V FBDIMM.

The low-voltage FBDIMM has identical timing and operating parameters as standard FBDIMMs. Unregulated power rails allow for maximum power conservation.

The module can be powered on at 1.8V for up to 100ms to allow for system initialization and module voltage configuration.

Except where stated in this data sheet, information in the corresponding 1.8V DDR2 FBDIMM data sheet is directly applicable to the 1.5V DDR2 FBDIMM.

Figure 1: 240-Pin FBDIMM (MO-256 R/C B)



Options	Marking
• Package	
– 240-pin DIMM (Pb-free)	Y
• Frequency/CL[1]	
– 3.0ns @ CL = 5 (DDR2-667)	-667

Notes: 1. CL = CAS (READ) latency.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)		t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)
		CL = 5	CL = 4			
-667	PC2-5300	667	533	15	15	55

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Table 2: Addressing

Parameter	2GB
Refresh count	8K
Device bank address	8 (BA0–BA2)
Device page size per bank	1KB
Device configuration	1Gb (128 Meg x 8)
Row address	16K (A0–A13)
Column address	1K (A0–A9)
Module rank address	2 (S0#, S1#)

Table 3: Part Numbers and Timing Parameters – 2GB

Base device: MT47J256M8,[1] 1Gb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)	Link Transfer Rate
MT18GTF25672FDY-667__	2GB	256 Meg x 72	PC2-5300	3.0ns/ 667 MT/s	5-5-5	4.0 GT/s

Notes:
1. Data sheets for the base device can be found on Micron's Web site: www.micron.com.
2. All part numbers end with a four-place code (as indicated by underline), designating component, AMB vendor, and PCB revision. Consult factory for current revision codes. Example: MT18GTF25672FDY-667E1D4.

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Pin Assignments and Descriptions

Table 4: Pin Assignments

240-Pin FBDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VDD	31	PN3	61	PN9#	91	PS9#[1]
2	VDD	32	PN3#	62	VSS	92	VSS
3	VDD	33	VSS	63	PN10	93	PS5
4	VSS	34	PN4	64	PN10#	94	PS5#
5	VDD	35	PN4#	65	VSS	95	VSS
6	VDD	36	VSS	66	PN11	96	PS6
7	VDD	37	PN5	67	PN11#	97	PS6#
8	VSS	38	PN5#	68	VSS	98	VSS
9	VCC	39	VSS	69	VSS	99	PS7
10	VCC	40	PN13[1]	70	PS0	100	PS7#
11	VSS	41	PN13#[1]	71	PS0#	101	VSS
12	VCC	42	VSS	72	VSS	102	PS8
13	VCC	43	VSS	73	PS1	103	PS8#
14	VSS	44	DNU	74	PS1#	104	VSS
15	VTT	45	DNU	75	VSS	105	DNU
16	DNU	46	VSS	76	PS2	106	DNU
17	RESET#	47	VSS	77	PS2#	107	VSS
18	VSS	48	PN12[1]	78	VSS	108	VDD
19	DNU	49	PN12#[1]	79	PS3	109	VDD
20	DNU	50	VSS	80	PS3#	110	VSS
21	VSS	51	PN6	81	VSS	111	VDD
22	PN0	52	PN6#	82	PS4	112	VDD
23	PN0#	53	VSS	83	PS4#	113	VDD
24	VSS	54	PN7	84	VSS	114	VSS
25	PN1	55	PN7#	85	VSS	115	VDD
26	PN1#	56	VSS	86	DNU	116	VDD
27	VSS	57	PN8	87	DNU	117	VTT
28	PN2	58	PN8#	88	VSS	118	SA2
29	PN2#	59	VSS	89	VSS	119	SDA
30	VSS	60	PN9	90	PS9[1]	120	SCL

240-Pin FBDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	VDD	151	SN3	181	SN9#	211	SS9#[1]
122	VDD	152	SN3#	182	VSS	212	VSS
123	VDD	153	VSS	183	SN10	213	SS5
124	VSS	154	SN4	184	SN10#	214	SS5#
125	VDD	155	SN4#	185	VSS	215	VSS
126	VDD	156	VSS	186	SN11	216	SS6
127	VDD	157	SN5	187	SN11#	217	SS6#
128	VSS	158	SN5#	188	VSS	218	VSS
129	VCC	159	VSS	189	VSS	219	SS7
130	VCC	160	SN13[1]	190	SS0	220	SS7#
131	VSS	161	SN13#[1]	191	SS0#	221	VSS
132	VCC	162	VSS	192	VSS	222	SS8
133	VCC	163	VSS	193	SS1	223	SS8#
134	VSS	164	DNU	194	SS1#	224	VSS
135	VTT	165	DNU	195	VSS	225	DNU
136	VID0	166	VSS	196	SS2	226	DNU
137	M_Test (DNU)	167	VSS	197	SS2#	227	VSS
138	VSS	168	SN12[1]	198	VSS	228	SCK
139	DNU	169	SN12#[1]	199	SS3	229	SCK#
140	DNU	170	VSS	200	SS3#	230	VSS
141	VSS	171	SN6	201	VSS	231	VDD
142	SN0	172	SN6#	202	SS4	232	VDD
143	SN0#	173	VSS	203	SS4#	233	VDD
144	VSS	174	SN7	204	VSS	234	VSS
145	SN1	175	SN7#	205	VSS	235	VDD
146	SN1#	176	VSS	206	DNU	236	VDD
147	VSS	177	SN8	207	DNU	237	VTT
148	SN2	178	SN8#	208	VSS	238	VDDSPD
149	SN2#	179	VSS	209	VSS	239	SA0
150	VSS	180	SN9	210	SS9[1]	240	SA1

Notes: 1. The following signals are CRC bits and thus appear out of the normal sequence: PN12/PN12#, SN12/SN12#, PN13/PN13#, SN13/SN13#, PS9/PS9#, and SS9/SS9#.

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Table 5: Pin Descriptions

Symbol	Type	Description
SCK	Input	System clock input, positive line.
SCK#	Input	System clock input, negative line.
PS0–PS9	Input	Primary southbound data, positive lines.
PS0#–PS9#	Input	Primary southbound data, negative lines.
SS0–SS9	Input	Secondary southbound data, positive lines.
SS0#–SS9#	Input	Secondary southbound data, negative lines.
SCL	Input	Serial presence-detect (SPD) clock input.
PN0–PN13	Output	Primary northbound data, positive lines.
PN0#–PN13#	Output	Primary northbound data, negative lines.
SN0–SN13	Output	Secondary northbound data, positive lines.
SN0#–SN13#	Output	Secondary northbound data, negative lines.
VID0	Output	Voltage identification, connected to Vss. Indicates 1.5V DRAM present on module.
SDA	I/O	SPD data input/output.
SA0–SA2	I/O	SPD address inputs, also used to select the FBDIMM number in the AMB.
RESET#	Supply	AMB reset signal.
V_{CC}	Supply	AMB core power and AMB channel interface power (1.5V).
V_{DD}	Supply	DRAM power and AMB DRAM I/O power (1.5V).
V_{TT}	Supply	DRAM address/command/clock termination power (V_{DD}/2).
V_{DDSPD}	Supply	SPD/AMB SMBus power.
V_{SS}	Supply	Ground.
M_Test	–	The M_Test pin provides an external connection for testing the margin of V_{REF}, which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and will be included in this specification at that time.
DNU	–	Do not use.

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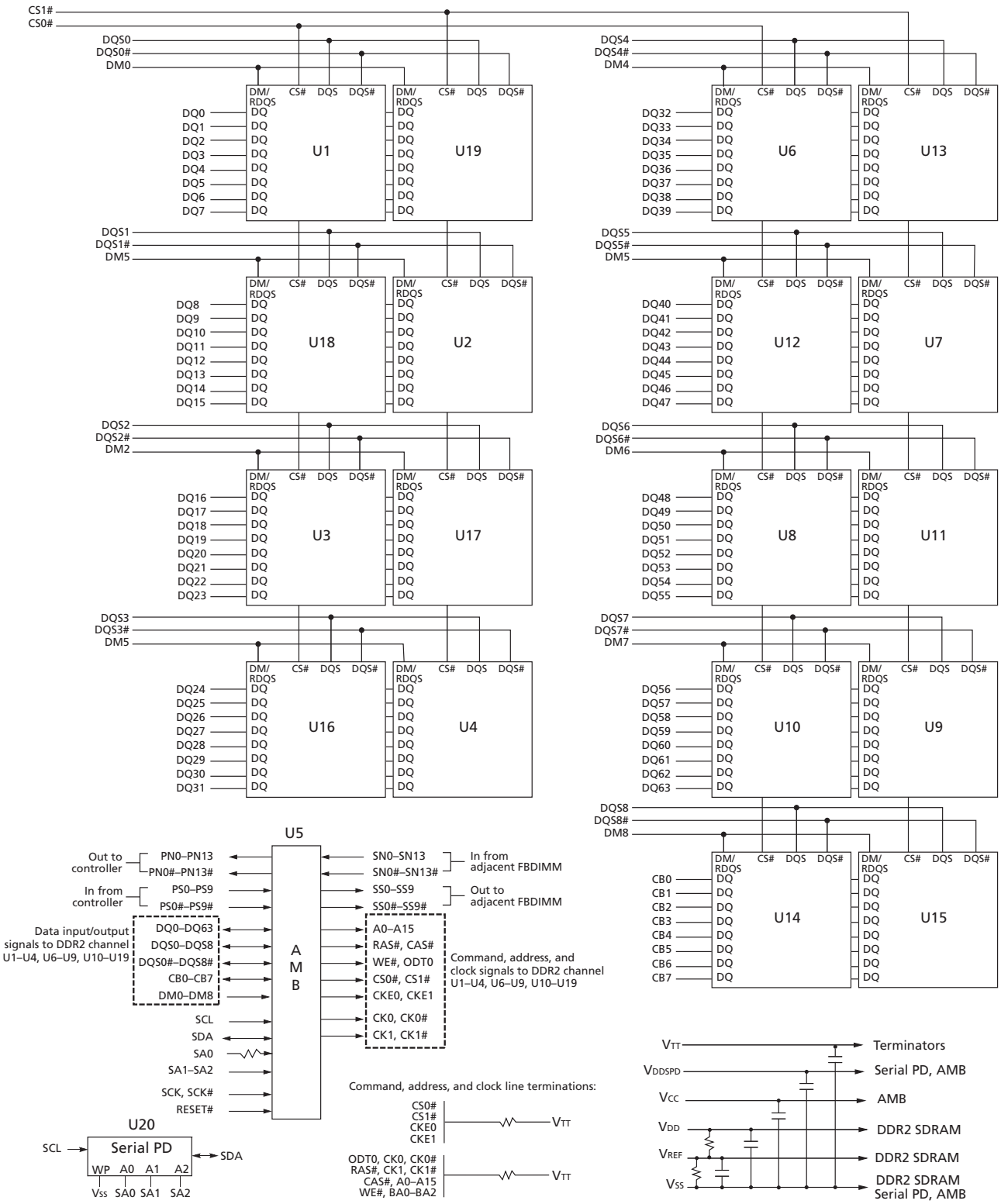
Functional Block Diagram

Figure 2: FBDIMM Functional Block Diagram



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Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet are not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Voltage on any signal pin relative to V_{SS}	V_{IN}, V_{OUT}	–0.3	1.75	V	1
Voltage on V_{CC} pin relative to V_{SS}	V_{CC}	–0.3	1.75	V	
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	–0.5	1.8	V	
Voltage on V_{TT} pin relative to V_{SS}	V_{TT}	–0.5	1.8	V	
DDR2 SDRAM device operating case temperature	T_C	0	95	°C	2, 3
AMB device operating case temperature		0	110	°C	

Notes:
1. V_{IN} should not be greater than V_{CC}.
2. T_C is specified at 95°C only when using 2X refresh timing (^tREFI = 7.8µs at or below 85°C; ^tREFI = 3.9µs above 85°C); see DDR2 SDRAM component data sheet.
3. See applicable DDR2 SDRAM component data sheet for ^tREFI and extended mode register settings. The ^tREFI parameter is used to specify the doubled refresh interval necessary to sustain <85°C operation.

Table 7: Input DC Voltage and Operating Conditions

Parameter	Symbol	Min	Nom	Max	Units	Notes
AMB supply voltage	V_{CC}	1.455	1.50	1.575	V	
DDR2 SDRAM supply voltage	V_{DD}	1.425	1.50	1.625	V	1
Termination voltage	V_{TT}	0.48 × V_{DD}	0.50 × V_{DD}	0.52 × V_{DD}	V	
EEPROM supply voltage	V_{DDSPD}	3.0	–	3.6	V	2
SPD input high (logic 1) voltage	$V_{IH(DC)}$	2.1	–	V_{DDSPD}	V	3
SPD input low (logic 0) voltage	$V_{IL(DC)}$	–0.6	–	0.8	V	3
RESET input high (logic 1) voltage	$V_{IH(DC)}$	1.0	–	–	V	4
RESET input low (logic 0) voltage	$V_{IL(DC)}$	–	–	0.5	V	3
Leakage current (RESET)	I_L	–90	–	90	µA	4
Leakage current (link)	I_L	–5	–	5	µA	5

Notes:
1. During the initial power ramp, V_{DD} may exceed V_{DD} (MAX) and be as much as 1.8V for up to 100ms prior to the start of the DRAM initialization process. The 100ms of excess V_{DD} voltage time must be less than 0.01 percent of the total DRAM powered-up time.
2. Applies to AMB and SPD.
3. Applies to SMBus and SPD bus signals.
4. Applies to AMB CMOS signal RESET#.
5. For all other AMB-related DC parameters, please refer to the high-speed differential link interface specification.

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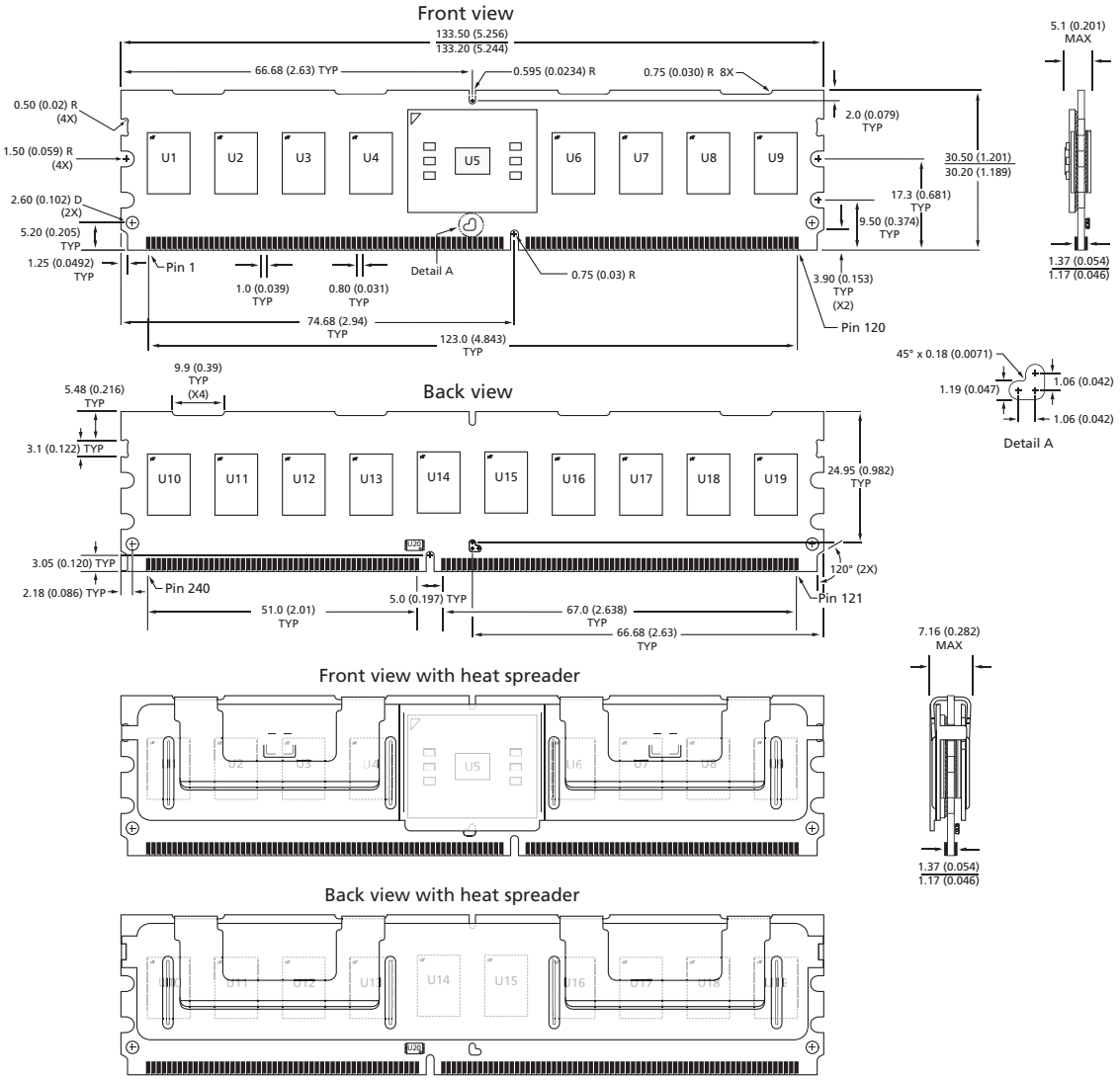
Module Dimensions

Figure 3: 240-Pin DDR2 FBDIMM



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted. The dimensional diagram is for reference only.

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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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