1.35V DDR3 SDRAM RDIMM

MT18KSF25672P – 2GB

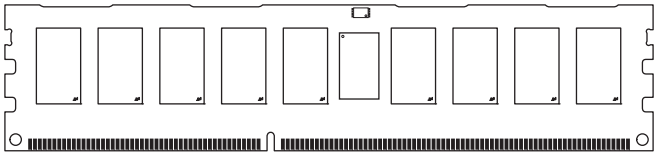
For component data sheets, refer to Micron's Web site: www.micron.com

Features

- Low voltage DDR3 functionality and operations supported as defined in the component data sheet
- V_{DD} = 1.35V ±0.0675V
- Backward-compatible with standard 1.5V DDR3 systems
- 240-pin, registered dual in-line memory module (RDIMM)
- Fast data transfer rates: PC3-8500 or PC3-6400
- 2GB (256 Meg x 72)
- V_{DDSPD} = +3.0V to +3.6V
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data and strobe signals
- Single rank
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 8 internal device banks for concurrent operation
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Lead-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 240-Pin RDIMM (MO-269)

PCB height: 30.0mm (1.18in)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
• Package	
– 240-pin DIMM	Y
• Frequency/CAS latency	
– 1.87ns @ CL = 7 (DDR3-1066)	-1G1
– 2.5ns @ CL = 6 (DDR3-800)	-80B

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)
		CL = 8	CL = 7	CL = 6			
-1G1	PC3-8500	1066	1066	800	13.125	13.125	50.625
-80B	PC3-6400	–	–	800	15	15	52.5

‡This data sheet contains the present description of a product in definition with no formal design in progress.

Table 2: Addressing

Parameter	2GB
Refresh count	8K
Row address	16K (A[13:0])
Device bank address	8 (BA[2:0])
Device configuration	1Gb (256 Meg x 4)
Column address	2K (A[11, 9:0])
Module rank address	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT41K256M4,[1] 1Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT18KSF25672PY-1G1__	2GB	256 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7
MT18KSF25672PY-80B__	2GB	256 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT18KSF25672PY-1G1D1.

Pin Assignments and Descriptions

Table 4: Pin Assignments

240-Pin DDR3 RDIMM Front								240-Pin DDR3 RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	31	DQ25	61	A2	91	DQ41	121	VSS	151	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	152	DQS12	182	VDD	212	DQS14
3	DQ0	33	DQS3#	63	NF	93	DQS5#	123	DQ5	153	DQS12#	183	VDD	213	DQS14#
4	DQ1	34	DQS3	64	NF	94	DQS5	124	VSS	154	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DQS9	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	VDD	96	DQ42	126	DQS9#	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	VSS	157	VSS	187	EVENT#	217	VSS
8	VSS	38	VSS	68	PAR_IN	98	VSS	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	159	CB5	189	VDD	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	VSS	160	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0	101	VSS	131	DQ12	161	DQS17	191	VDD	221	DQS15
12	DQ8	42	DQS8#	72	VDD	102	DQS6#	132	DQ13	162	DQS17#	192	RAS#	222	DQS15#
13	DQ9	43	DQS8	73	WE#	103	DQS6	133	VSS	163	VSS	193	S0#	223	VSS
14	VSS	44	VSS	74	CAS#	104	VSS	134	DQS10	164	CB6	194	VDD	224	DQ54
15	DQS1#	45	CB2	75	VDD	105	DQ50	135	DQS10#	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	NC	106	DQ51	136	VSS	166	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	NC	107	VSS	137	DQ14	167	NC	197	VDD	227	DQ60
18	DQ10	48	VTT	78	VDD	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	VTT	79	NC	109	DQ57	139	VSS	169	NC	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ36	230	DQS16
21	DQ16	51	VDD	81	DQ32	111	DQS7#	141	DQ21	171	A15	201	DQ37	231	DQS16#
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	VSS	172	A14	202	VSS	232	VSS
23	VSS	53	ERR_OUT#	83	VSS	113	VSS	143	DQS11	173	VDD	203	DQS13	233	DQ62
24	DQS2#	54	VDD	84	DQS4#	114	DQ58	144	DQS11#	174	A12	204	DQS13#	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23#	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	VSS	178	A6	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	SA2	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

Table 5: Pin Descriptions

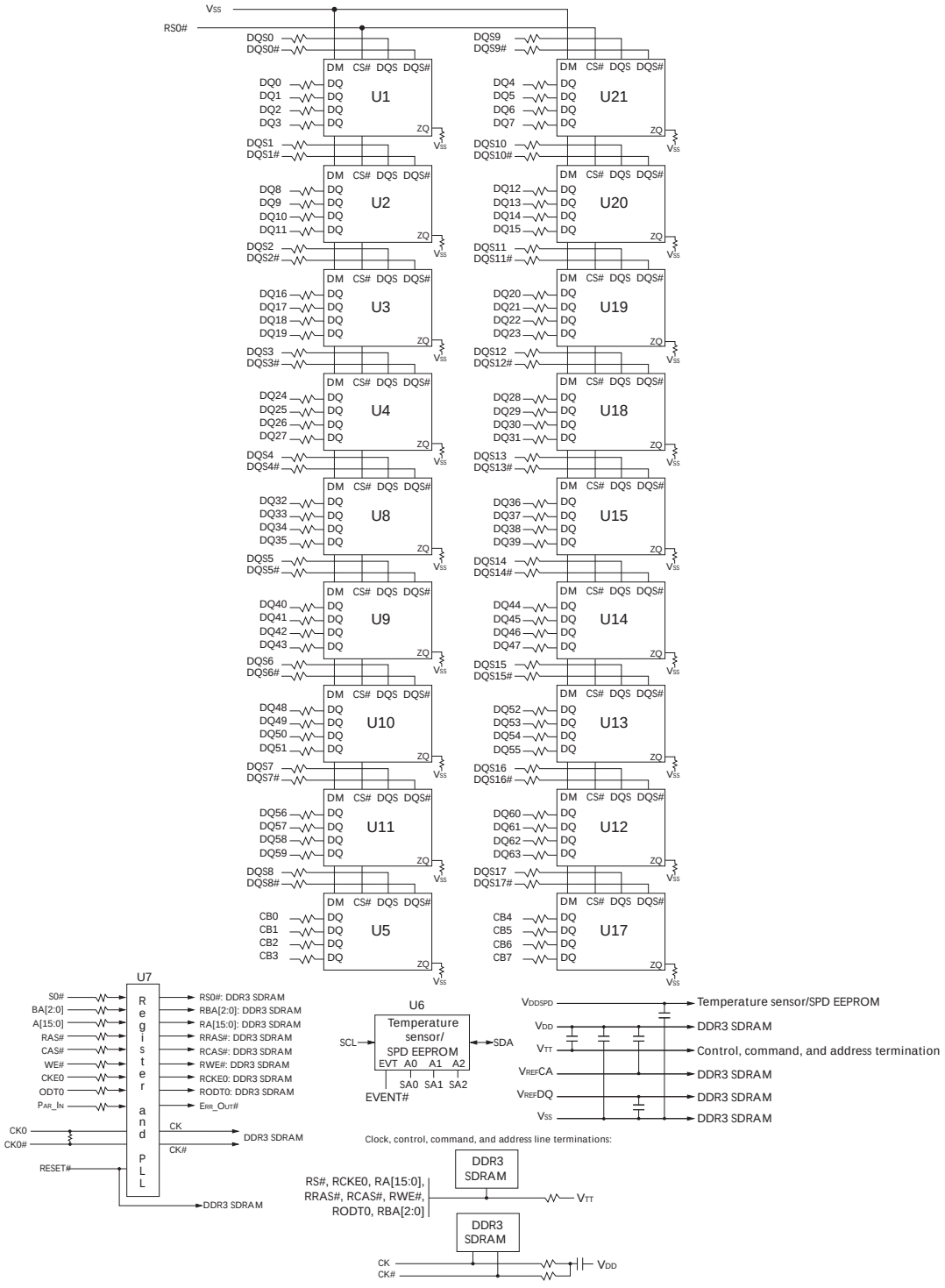
Symbol	Type	Description
A[15:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as "BL on-the-fly" during CAS commands. The address inputs also provide the op-code during the mode register command set. A[13:0] address the 1Gb DDR3 devices. A[15:14] are needed to calculate parity on the command/address bus.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command. BA[1:0] are used as part of the parity calculation.
CK0, CK0#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE0	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
ODT0	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
PAR_IN	Input	**Parity input:** Parity bit for the address, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** An active LOW CMOS input referenced to V_{SS} and not referenced to $V_{REF}CA$ or $V_{REF}DQ$.
S0#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Serial address inputs:** These pins are used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** SCL is used to synchronize communication to and from the temperature sensor/SPD EEPROM.
CB[7:0]	I/O	**Check bits:** Data used for ECC.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[17:0], DQS#[17:0]	I/O	**Data strobe:** DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the module on the I^2C bus.
ERR_OUT#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.35V ±0.0675V or 1.5V ±0.075V. The component V_{DD} and $V_{DD}Q$ are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** +3.0V to +3.6V.
$V_{REF}CA$	Supply	**Reference voltage:** Control, command, and address ($V_{DD}/2$).
$V_{REF}DQ$	Supply	**Reference voltage:** DQ, DM ($V_{DD}/2$).

Table 5: Pin Descriptions (continued)

Symbol	Type	Description
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address ($V_{DD}/2$).
NF	–	**No function:** Connected within the module, but provides no functionality.
NC	–	**No connect:** These pins are not connected on the module.

Functional Block Diagram

Figure 2: Functional Block Diagram



Notes: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

The MT18KSF25672P 1.35V DDR3 SDRAM modules is a high-speed, CMOS dynamic random access 2GB memory module organized in a x72 configuration. These 1.35V DDR3 SDRAM modules use internally configured, 8-bank 1Gb DDR3 SDRAM devices.

1.35V DDR3 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the 1.35V DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

1.35V DDR3 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Fly-By Topology

These 1.35V DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Registering Clock Driver Operation

Registered 1.35V DDR3 SDRAM modules use a registering clock driver consisting of a register and a phase-lock loop (PLL) and comply with the JEDEC standard, "Definition of the SSTE32882 Registering Clock Driver with Parity and Quad Chip Selects for DDR3 RDIMM Applications."

The register section of the registering clock driver latches command and address input signals on the rising clock edge. The PLL section of the registering clock driver receives and redrives the differential clock signals (CK, CK#) to the DDR3 SDRAM devices. The register(s) and PLL reduce clock, control, command, and address signals loading by isolating DRAM from the system controller.

Parity Operations

The registering clock driver can accept a parity bit from the system's memory controller, providing even parity for the control, command, and address bus. Parity errors are flagged on the ERR_OUT# pin. Systems not using parity are expected to function without issue if PAR_IN and ERR_OUT# are left as no connects to the system.

Temperature Sensor with Serial Presence-Detect EEPROM

Thermal Sensor Operations

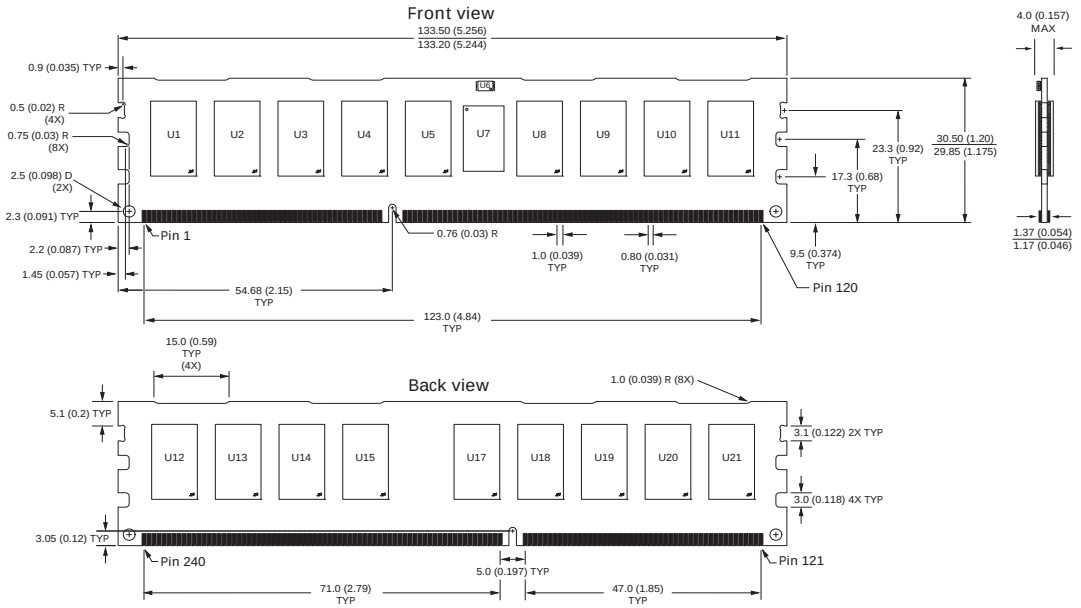
The temperature from the integrated thermal sensor is monitored and converts into a digital word via the I^2C bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC Standard No. 21-C, page 4.7-1, "Mobile Platform Memory Module Thermal Sensor Component Specification."

Serial Presence-Detect EEPROM Operation

1.35V DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC Standard JC-45 "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. User-specific information can be written into the remaining 128 bytes of storage. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protect.

Module Dimensions

Figure 3: 240-Pin DDR3 RDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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