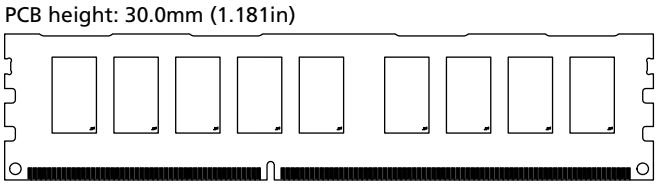
DDR3 SDRAM UDIMM

MT18JSF25672AZ – 2GB
MT18JSF51272AZ – 4GB

Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 240-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 2GB (256 Meg x 72), 4GB (512 Meg x 72)
- Vdd = 1.5V ±0.075V
- Vddspd = +3.0V to +3.6V
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Dual rank
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 240-Pin UDIMM (MO-269 R/C E)



Options	Marking
• Operating temperature[1]	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
– Industrial (–40°C ≤ T_A ≤ +85°C)	I
• Package	
– 240-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 1.25ns @ CL = 11 (DDR3-1600)	-1G6
– 1.5ns @ CL = 9 (DDR3-1333)	-1G4
– 1.87ns @ CL = 7 (DDR3-1066)	-1G1
– 1.87ns @ CL = 8 (DDR3-1066)[2]	-1G0
– 2.5ns @ CL = 5 (DDR3-800)[2]	-80C
– 2.5ns @ CL = 6 (DDR3-800)[2]	-80B

Notes:
1. Contact Micron for industrial temperature module offerings.
2. Not recommended for new designs.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G6	PC3-12800	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	1066	–	800	667	15	15	52.5
-80C	PC3-6400	–	–	–	–	–	800	800	12.5	12.5	50
-80B	PC3-6400	–	–	–	–	–	800	667	15	15	52.5

Table 2: Addressing

Parameter	2GB	4GB
Refresh count	8K	8K
Row address	16K A[13:0]	32K A[14:0]
Device bank address	8 BA[2:0]	8 BA[2:0]
Device configuration	1Gb (128 Meg x 8)	2Gb (256 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]
Module rank address	2 S#[1:0]	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT41J128M8,[1] 1Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT18JSF25672A(I)Z-1G6__	2GB	256 Meg x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT18JSF25672A(I)Z-1G4__	2GB	256 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT18JSF25672A(I)Z-1G1__	2GB	256 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7
MT18JSF25672A(I)Z-1G0__	2GB	256 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	8-8-8
MT18JSF25672A(I)Z-80C__	2GB	256 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT18JSF25672A(I)Z-80B__	2GB	256 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6

Table 4: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT41J256M8,[1] 2Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT18JSF51272A(I)Z-1G6__	4GB	512 Meg x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT18JSF51272A(I)Z-1G4__	4GB	512 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT18JSF51272A(I)Z-1G1__	4GB	512 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7
MT18JSF51272A(I)Z-1G0__	4GB	512 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	8-8-8
MT18JSF51272A(I)Z-80C__	4GB	512 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT18JSF51272A(I)Z-80B__	4GB	512 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT18JSF25672AZ-1G1D1.

Pin Assignments and Descriptions

Table 5: Pin Assignments

240-Pin DDR3 UDIMM Front								240-Pin DDR3 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VrefDQ	31	DQ25	61	A2	91	DQ41	121	Vss	151	Vss	181	A1	211	Vss
2	Vss	32	Vss	62	Vdd	92	Vss	122	DQ4	152	DM3	182	Vdd	212	DM5
3	DQ0	33	DQS3#	63	CK1	93	DQS5#	123	DQ5	153	NC	183	Vdd	213	NC
4	DQ1	34	DQS3	64	CK1#	94	2.26	124	Vss	154	Vss	184	CK0	214	Vss
5	Vss	35	Vss	65	Vdd	95	Vss	125	DM0	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	Vdd	96	DQ42	126	NC	156	DQ31	186	Vdd	216	DQ47
7	DQS0	37	DQ27	67	VrefCA	97	DQ43	127	Vss	157	Vss	187	EVENT#	217	Vss
8	Vss	38	Vss	68	NC	98	Vss	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	Vdd	99	DQ48	129	DQ7	159	CB5	189	Vdd	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	Vss	160	Vss	190	BA1	220	Vss
11	Vss	41	Vss	71	BA0	101	Vss	131	DQ12	161	DM8	191	Vdd	221	DM6
12	DQ8	42	DQS8#	72	Vdd	102	DQS6#	132	DQ13	162	NC	192	RAS#	222	NC
13	DQ9	43	DQS8	73	WE#	103	DQS6	133	Vss	163	Vss	193	S0#	223	Vss
14	Vss	44	Vss	74	CAS#	104	Vss	134	DM1	164	CB6	194	Vdd	224	DQ54
15	DQS1#	45	CB2	75	Vdd	105	DQ50	135	NC	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	S1#	106	DQ51	136	Vss	166	Vss	196	A13	226	Vss
17	Vss	47	Vss	77	ODT1	107	Vss	137	DQ14	167	NU	197	Vdd	227	DQ60
18	DQ10	48	NC	78	Vdd	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	NC	79	NC	109	DQ57	139	Vss	169	CKE1	199	Vss	229	Vss
20	Vss	50	CKE0	80	Vss	110	Vss	140	DQ20	170	Vdd	200	DQ36	230	DM7
21	DQ16	51	Vdd	81	DQ32	111	DQS7#	141	DQ21	171	NF	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	Vss	172	NF/A14	202	Vss	232	Vss
23	Vss	53	NC	83	Vss	113	Vss	143	DM2	173	Vdd	203	DM4	233	DQ62
24	DQS2#	54	Vdd	84	DQS4#	114	DQ58	144	NC	174	A12	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	Vss	175	A9	205	Vss	235	Vss
26	Vss	56	A7	86	Vss	116	Vss	146	DQ22	176	Vdd	206	DQ38	236	Vddspd
27	DQ18	57	Vdd	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	Vss	178	A6	208	Vss	238	SDA
29	Vss	59	A4	89	Vss	119	SA2	149	DQ28	179	Vdd	209	DQ44	239	Vss
30	DQ24	60	Vdd	90	DQ40	120	Vtt	150	DQ29	180	A3	210	DQ45	240	Vtt

Table 6: Pin Descriptions

Symbol	Type	Description
A[13:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as "BL on-the-fly" during CAS commands. The address inputs also provide the op-code during the mode register command set. A[13:0] address the 1Gb DDR3 devices. A[14:0] address the 2Gb DDR3 devices. A15 is needed to calculate parity on the command/address bus.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command.
CK[1:0], CK#[1:0]	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE[1:0]	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DM[8:0]	Input	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of the DQS. Although the DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
ODT[1:0]	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** An active LOW CMOS input referenced to Vss. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × Vdd and DC LOW ≤ 0.2 × Vdd.
S#[1:0]	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Presence-detect address inputs:** These pins are used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the communication to and from the temperature sensor/SPD EEPROM.
CB[7:0]	I/O	**Check bits:** Data used for ECC.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[8:0], DQS#[8:0]	I/O	**Data strobe:** DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the module on the I^2C bus.

Table 6: Pin Descriptions (Continued)

Symbol	Type	Description
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
Vdd	Supply	**Power supply:** 1.5V ±0.075V.
Vddspd	Supply	**Serial EEPROM positive power supply:** +3.0V to +3.6V. The component Vdd and Vddq are connected to the module Vdd.
VrefCA	Supply	**Reference voltage:** Control, command, and address (Vdd/2).
VrefDQ	Supply	**Reference voltage:** DQ, DM (Vdd/2).
Vss	Supply	Ground.
Vtt	Supply	**Termination voltage:** Used for control, command, and address (Vdd/2).
NC	–	**No connect:** These pins are not connected on the module.
NU	–	**Not usable**: No connections allowed.

DQ Map

Table 7: Component-to-Module DQ Map

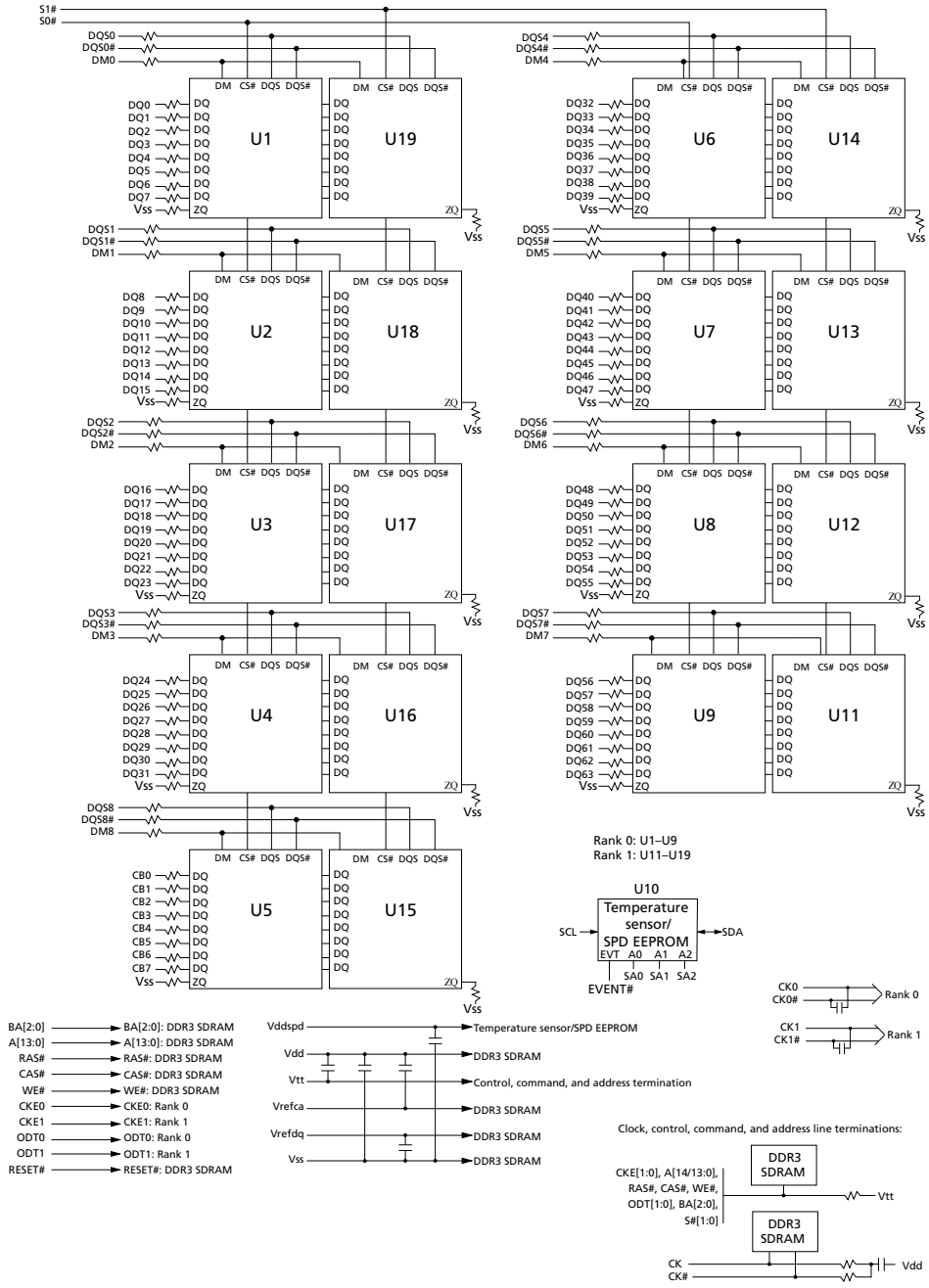
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	9	U2	0	10	18
	1	5	123		1	13	132
	2	7	129		2	15	138
	3	0	3		3	8	12
	4	6	128		4	14	137
	5	4	122		5	12	131
	6	3	10		6	11	19
	7	1	4		7	9	13
U3	0	18	27	U4	0	26	36
	1	21	141		1	29	150
	2	23	147		2	31	156
	3	6	21		3	24	30
	4	22	146		4	30	155
	5	20	140		5	28	149
	6	19	28		6	27	37
	7	17	22		7	25	31
U5	0	CB2	45	U6	0	34	87
	1	CB5	159		1	37	201
	2	CB7	165		2	39	207
	3	CB0	39		3	33	82
	4	CB6	164		4	38	206
	5	CB4	158		5	36	200
	6	CB3	46		6	35	88
	7	CB1	40		7	32	81
U7	0	42	96	U8	0	50	105
	1	45	210		1	53	219
	2	47	216		2	55	225
	3	41	91		3	49	100
	4	46	215		4	54	224
	5	44	209		5	52	218
	6	43	97		6	51	106
	7	40	90		7	48	99
U9	0	58	114	U11	0	61	228
	1	61	228		1	58	114
	2	63	234		2	57	109
	3	57	109		3	63	234
	4	62	233		4	56	108
	5	60	227		5	59	115
	6	59	115		6	60	227
	7	56	108		7	62	233

Table 7: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U12	0	53	219	U13	0	45	210
	1	50	105		1	42	96
	2	49	100		2	41	91
	3	55	225		3	47	216
	4	48	99		4	40	90
	5	51	106		5	43	97
	6	52	218		6	44	209
	7	54	224		7	46	215
U14	0	37	201	U15	0	CB5	159
	1	34	87		1	CB2	45
	2	33	82		2	CB0	39
	3	39	207		3	CB7	165
	4	32	81		4	CB1	40
	5	35	88		5	CB3	46
	6	36	200		6	CB4	158
	7	38	206		7	CB6	164
U16	0	29	150	U17	0	21	141
	1	26	36		1	18	27
	2	24	30		2	16	21
	3	31	156		3	23	147
	4	25	31		4	17	22
	5	27	37		5	19	28
	6	28	149		6	20	140
	7	30	155		7	22	146
U18	0	13	132	U19	0	5	123
	1	10	18		1	2	9
	2	8	12		2	0	3
	3	15	138		3	7	129
	4	9	13		4	1	4
	5	11	19		5	3	10
	6	12	131		6	4	122
	7	14	137		7	6	128

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
Vdd	Vdd supply voltage relative to Vss	–0.4	+1.975	V
Vin, Vout	Voltage on any pin relative to Vss	–0.4	+1.975	V

Table 9: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
Vdd	Vdd supply voltage		1.425	1.5	1.575	V	
Ivtt	Termination reference current from Vtt		–600	–	+600	mA	
Vtt	Termination reference voltage (DC) – command/address bus		0.49 × Vdd - 20mV	0.5 × Vdd	0.51 × Vdd + 20mV	V	1
Ii	Input leakage current; Any input 0V ≤ Vin ≤ Vdd; Vref input 0V ≤ Vin ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA	–36	0	+36	µA	
		S#, CKE, ODT, CK, CK#	–18	0	+18		
		DM	–4	0	+4		
Ioz	Output leakage current; 0V ≤ Vout ≤ Vddq; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	–10	0	+10	µA	
Ivref	Vref supply leakage current; VrefDQ = Vdd/2 or VrefCA = Vdd/2 (All other pins not under test = 0V)		–18	0	+18	µA	
T_A	Module ambient operating temperature	Commercial	0	–	+70	°C	2, 3
		Industrial	–40	–	+85	°C	
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	+85	°C	2, 3, 4
		Industrial	–40	–	+95	°C	

Notes:
1. Vtt termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
4. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown below.

Table 10: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

Idd Specifications

Table 11: DDR3 Idd Specifications and Conditions – 2GB

Values are for the MT41J128M8 DDR3 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0[1]	1188	1098	1008	918	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1[1]	1368	1278	1188	1098	mA
Precharge power-down current: Slow exit	Idd2P[2]	216	216	216	216	mA
Precharge power-down current: Fast exit	Idd2P[2]	810	720	630	540	mA
Precharge quiet standby current	Idd2Q[2]	1206	1080	954	828	mA
Precharge standby current	Idd2N[2]	1260	1170	990	900	mA
Precharge standby ODT current	Idd2NT[1]	963	873	783	693	mA
Active power-down current	Idd3P[2]	810	720	630	540	mA
Active standby current	Idd3N[2]	1206	1116	1026	963	mA
Burst read operating current	Idd4R[1]	2358	1908	1548	1278	mA
Burst write operating current	Idd4W[1]	2358	2088	1818	1548	mA
Refresh current	Idd5B[2]	4680	4320	3960	3600	mA
Self refresh temperature current: MAX T_C = 85°C	Idd6[2]	108	108	108	108	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	Idd6ET[2]	162	162	162	162	mA
All banks interleaved read current	Idd7[1]	5508	4518	3618	3258	mA
Reset current	Idd8[2]	252	252	252	252	mA

Notes:
1. One module rank in the active Idd; the other rank in Idd2P (slow exit).
2. All ranks in this Idd condition.

Table 12: DDR3 Idd Specifications and Conditions – 4GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1333	1066	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0[1]	918	828	738	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1[1]	1143	1008	873	mA
Precharge power-down current: Slow exit	Idd2P[2]	216	216	216	mA
Precharge power-down current: Fast exit	Idd2P[2]	630	540	540	mA
Precharge quiet standby current	Idd2Q[2]	1170	990	810	mA
Precharge standby current	Idd2N[2]	1170	990	810	mA
Precharge standby ODT current	Idd2NT[1]	873	783	648	mA
Active power-down current	Idd3P[2]	810	720	630	mA
Active standby current	Idd3N[2]	1350	1080	900	mA
Burst read operating current	Idd4R[1]	1908	1548	1233	mA
Burst write operating current	Idd4W[1]	2268	1908	1503	mA
Refresh current	Idd5B[2]	4590	4410	4050	mA
Self refresh temperature current: MAX T_C = 85°C	Idd6[2]	162	162	162	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	Idd6ET[2]	216	216	216	mA
All banks interleaved read current	Idd7[1]	3393	2988	2718	mA
Reset current	Idd8[2]	252	252	252	mA

Notes: 1. One module rank in the active Idd; the other rank in Idd2P (slow exit).
2. All ranks in this Idd condition.

Temperature Sensor with Serial Presence-Detect EEPROM

The temperature from the integrated thermal sensor is monitored and converts into a digital word via the I^2C bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. User-specific information can be written into the remaining 128 bytes of storage. READ/WRITE operations between the system (master) and the EEPROM (slave) device occur via an I^2C bus. Write protect (WP) is connected to Vss, permanently disabling hardware write protect. For further information please refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Table 13: Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	Vddspd	+3.0	+3.6	V
Supply current: Vdd = 3.3V	Idd	–	+2.0	mA
Input high voltage: Logic 1; SCL, SDA	Vih	+1.45	Vddspd + 1	V
Input low voltage: Logic 0; SCL, SDA	Vil	–	+0.55	V
Output low voltage: Iout = 2.1mA	Vol	–	+0.4	V
Input current	Iin	–5.0	+5.0	µA
Temperature sensing range	–	–40	+125	°C
Temperature sensor accuracy (initial release)	–	–2.0	+2.0	°C
Temperature sensor accuracy (class B)	–	–1.0	+1.0	°C

Table 14: Sensor and EEPROM Serial Interface Timing

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	^tBUF	4.7	–	µs
SDA fall time	^tF	20	300	ns
SDA rise time	^tR	–	1,000	ns
Data hold time	$^tHD:DAT$	200	900	ns
Start condition hold time	$^tH:STA$	4.0	–	µs
Clock HIGH period	^tHIGH	4.0	50	µs
Clock LOW period	^tLOW	4.7	–	µs

Table 14: Sensor and EEPROM Serial Interface Timing (Continued)

Parameter/Condition	Symbol	Min	Max	Units
SCL clock frequency	^{t}SCL	10	100	kHz
Data setup time	^{t}SU:DAT	250	–	ns
Start condition setup time	^{t}SU:STA	4.7	–	µs
Stop condition setup time	^{t}SU:STO	4.0	–	µs

EVENT# Pin

The temperature sensor also adds the EVENT# pin (open drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. The open-drain output of EVENT# under the three separate operating modes is illustrated below. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and only returns to the logic HIGH state when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

SM Bus Slave Subaddress Decoding

The temperature sensor's physical address differs from the SPD EEPROM's physical address: binary 0011 for A0, A1, A2, and RW#, where A2, A1, and A0 are the three slave subaddress pins and the RW# bit is the READ/WRITE flag.

If the slave base address is fixed for the temperature sensor/SPD EEPROM, then the pins set the subaddress bits of the slave address, enabling the devices to be located anywhere within the eight slave address locations. For example, they could be set from 30h to 3Eh.

Figure 3: EVENT# Pin Functionality

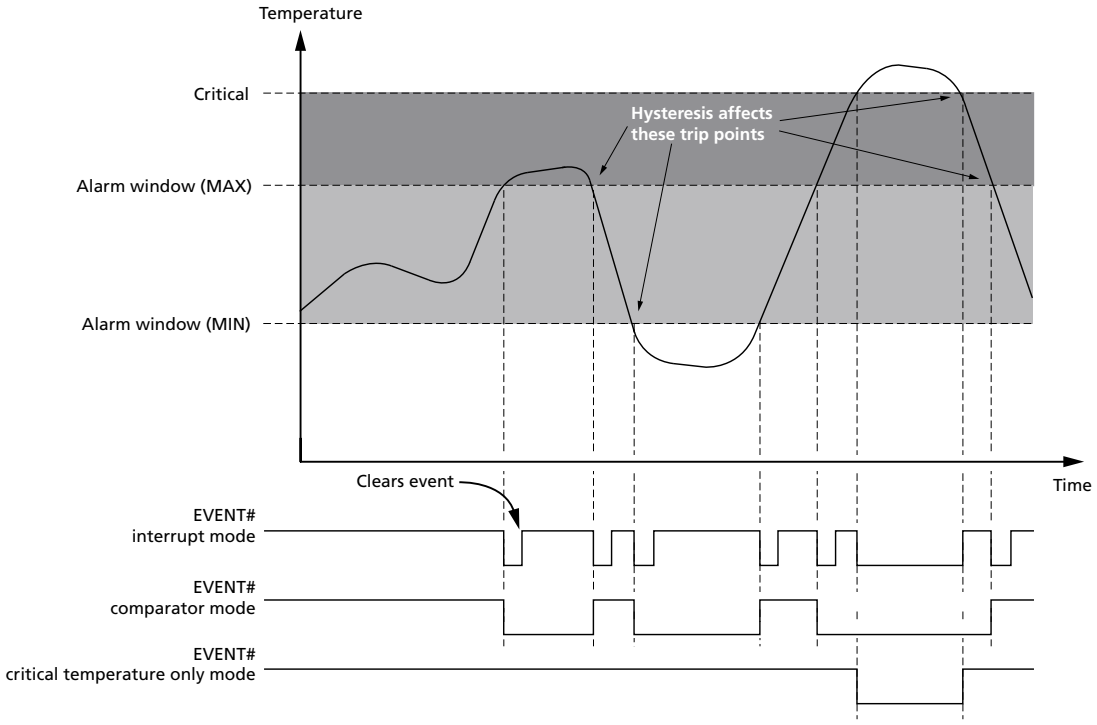


Table 15: Temperature Sensor Registers

Name	Address	Power-on Default
Pointer register	Not applicable	Undefined
Capability register	0x00	0x0001
Configuration register	0x01	0x0000
Alarm temperature upper boundary register	0x02	0x0000
Alarm temperature lower boundary register	0x03	0x0000
Critical temperature register	0x04	0x0000
Temperature register	0x05	Undefined

Pointer Register

The pointer register selects which of the 16-bit registers is being accessed in subsequent READ and WRITE operations. This register is a write-only register.

Table 16: Pointer Register Bits 0–7

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	Register select	Register select	Register select	Register select

Table 17: Pointer Register Bits 0–2 Descriptions

Bit			Register
2	1	0	
0	0	0	Capability register
0	0	1	Configuration register
0	1	0	Alarm temperature upper boundary register
0	1	1	Alarm temperature lower boundary register
1	0	0	Critical temperature register
1	0	1	Temperature register

Capability Register

The capability register indicates the features and functionality supported by the temperature sensor. This register is a read-only register.

Table 18: Capability Register (Address: 0x00)

Bit							
15	14	13	12	11	10	9	8
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Bit							
7	6	5	4	3	2	1	0
RFU	RFU	RFU	Temperature resolution		Wider range	Precision	Has alarm and critical temperature

Table 19: Capability Register Bit Description

Bit	Description
0	Basic capability 1: Has alarm and critical trip point capabilities
1	Accuracy 0: ±2°C over the active range and ±3°C over the monitor range 1: ±1°C over the active range and ±2°C over the monitor range

Table 19: Capability Register Bit Description (Continued)

Bit	Description
2	Wider range 0: Temperatures lower than 0°C are clamped to a binary value of 0 1: Temperatures below 0°C can be read
4:3	Temperature resolution 00: 0.5°C LSB 01: 0.25°C LSB 10: 0.125°C LSB 11: 0.0625°C LSB
15:5	0: Must be set to zero

Configuration Register

Table 20: Configuration Register (Address: 0x01)

Bit							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RFU	RFU	RFU	RFU	RFU	Hysteresis		Shutdown mode
Bit							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Critical lock bit	Alarm lock bit	Clear event	Event output status	Event output control	Critical event only	Event polarity	Event mode

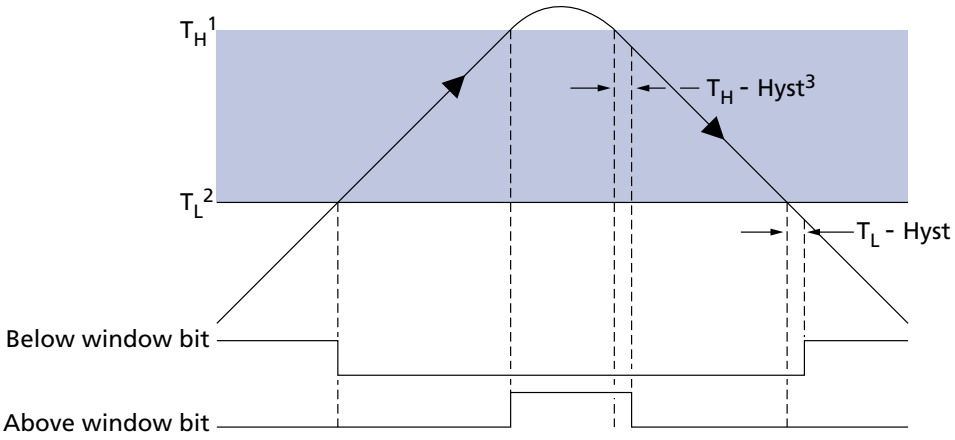
Table 21: Configuration Register Bit Descriptions

Bit	Description	Notes
0	Event mode 0: Comparator mode 1: Interrupt mode	Event mode cannot be changed if either of the lock bits is set.
1	EVENT# polarity 0: Active LOW 1: Active HIGH	EVENT# polarity cannot be changed if either of the lock bits is set.
2	Critical event only 0: EVENT# trips on alarm or critical temperature event 1: EVENT# trips only if critical temperature is reached	
3	Event output control 0: Event output disabled 1: Event output enabled	

Table 21: Configuration Register Bit Descriptions (Continued)

Bit	Description	Notes
4	Event status 0: EVENT# has not been asserted by this device 1: EVENT# is being asserted due to an alarm window or critical temperature condition	This is a read-only field in the register. The event causing the event can be determined from the read temperature register.
5	Clear event 0: No effect 1: Clears the event when the temperature sensor is in the interrupt mode	
6	Alarm window lock bit 0: Alarm trips are not locked and can be changed 1: Alarm trips are locked and cannot be changed	
7	Critical trip lock bit 0: Critical trip is not locked and can be changed 1: Critical trip is locked and cannot be changed	
8	Shutdown mode 0: Enabled 1: Shutdown	The shutdown mode is a power-saving mode that disables the temperature sensor.
10:9	Hysteresis enable 00: Disable 01: Enable at 1.5°C 10: Enable at 3°C 11: Enable at 6°C	When enabled, a hysteresis is applied to temperature movement around the trip points (see Figure 4 (page 20)). As an example, if the hysteresis register is enabled to a delta of 6°C, the preset trip points will toggle when the temperature reaches the programmed value. These values will reset when the temperature drops below the trip points minus the set hysteresis level. In this case, this would be critical temperature minus 6°C. The hysteresis is applied to both the above alarm window and the below alarm window bits found in the read-only temperature register (see Table 22 (page 20)). EVENT# is also affected by this register.

Figure 4: Hysteresis Applied to Temperature Around Trip Points



Notes:
1. T_H is the value set in the alarm temperature upper boundary trip register.
2. T_L is the value set in the alarm temperature lower boundary trip register.
3. Hyst is the value set in the hysteresis bits of the configuration register.

Table 22: Hysteresis Applied to Alarm Window Bits in the Temperature Register

Condition	Below Alarm Window Bit		Above Alarm Window Bit	
	Temperature Gradient	Critical Temperature	Temperature Gradient	Critical Temperature
Sets	Falling	T_L - Hyst	Rising	T_H
Clears	Rising	T_L	Falling	T_H - Hyst

Temperature Format

The temperature trip point registers and temperature readout register use a 2's complement format to enable negative numbers. The least significant bit (LSB) is equal to 0.0625°C or 0.25°C, depending on which register is referenced. For example, assuming an LSB of 0.0625°C:

- A value of 0x018C would equal 24.75°C
- A value of 0x06C0 would equal 108°C
- A value of 0x1E74 would equal –24.75°C

Temperature Trip Point Registers

The upper and lower temperature boundary registers are used to set the maximum and minimum values of the alarm window. LSB for these registers is 0.25°C. All RFU bits in the register will always report zero.

Table 23: Alarm Temperature Lower Boundary Register (Address: 0x02)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Alarm window upper boundary temperature												

Table 24: Alarm Temperature Lower Boundary Register (Address: 0x03)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Alarm window lower boundary temperature												

Critical Temperature Register

The critical temperature register is used to set the maximum temperature above the alarm window. The LSB for this register is 0.25°C. All RFU bits in the register will always report zero.

Table 25: Critical Temperature Register (Address: 0x04)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Critical temperature trip point												

Temperature Register

The temperature register is a read-only register that provides the current temperature detected by the temperature sensor. The LSB for this register is 0.0625°C with a resolution of 0.0625°C. The most significant bit (MSB) is 128°C in the readout section of this register.

The upper three bits of the register are used to monitor the trip points that are set in the previous three registers.

Table 26: Temperature Register (Address: 0x05)

Bit															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Above critical trip	Above alarm window	Below alarm window	MSB												LSB
			Temperature												

Table 27: Temperature Register Bit Descriptions

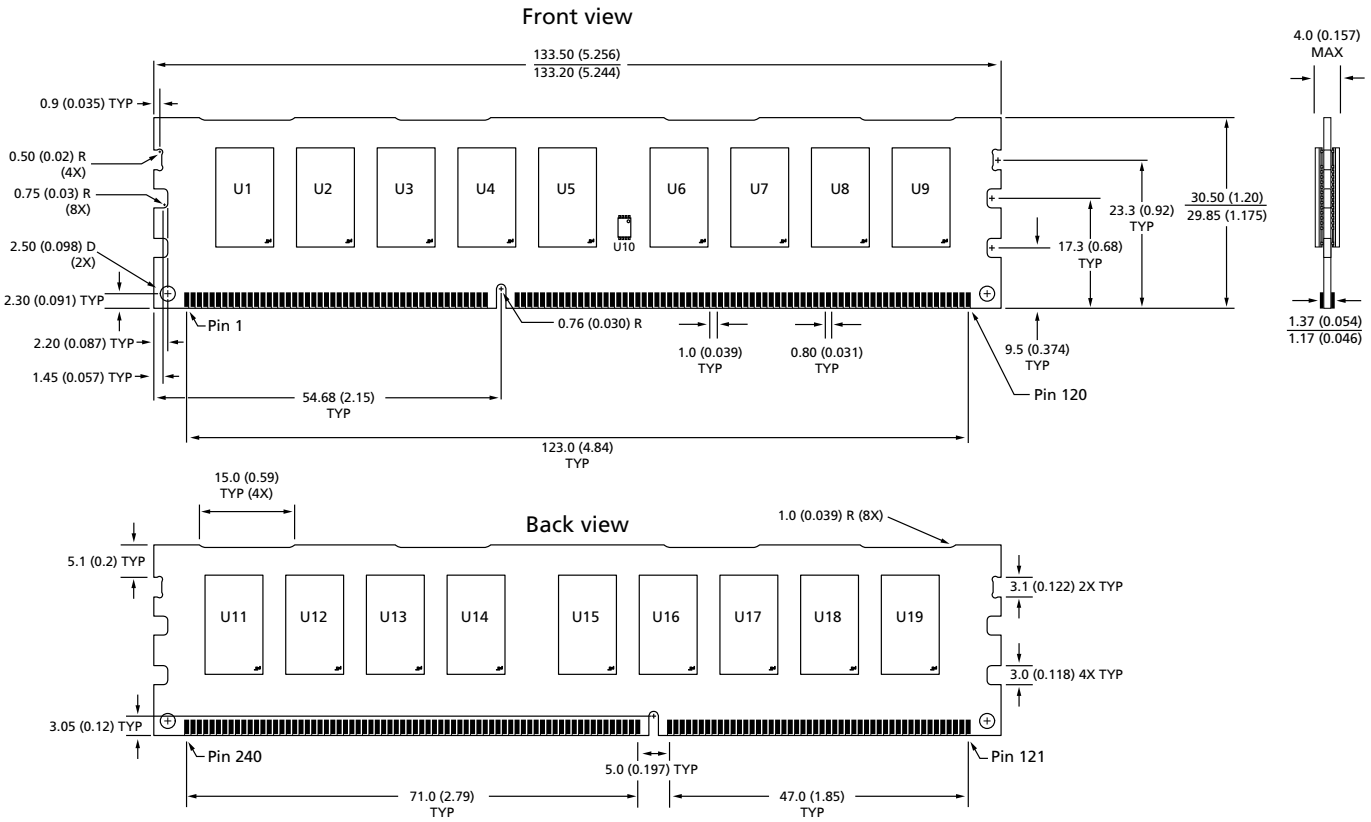
Bit	Description
13	Below alarm window 0: Temperature is equal to or above the lower boundary 1: Temperature is below alarm window
14	Above alarm window 0: Temperature is equal to or below the upper boundary 1: Temperature is above alarm window
15	Above critical trip point 0: Temperature is below critical trip point 1: Temperature is above critical trip point

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 5: 240-Pin DDR3 UDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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