

DRAM MODULE

MT9LD272(X), MT18LD472(F)(X)

 For the latest data sheet, please refer to the Micron Web site: www.micronsemi.com/datasheets/datasheet.html

FEATURES

- JEDEC-standard ECC pinout in a 168-pin, dual in-line memory module (DIMM)
- 16MB (2 Meg x 72) and 32MB (4 Meg x 72)
- High-performance CMOS silicon-gate process
- Single +3.3V \pm 0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE- RAS# (CBR) and HIDDEN
- All inputs are buffered except RAS#
- 2,048 cycles (11 row, 11 column addresses) or 4,096 cycles (12 row, 10 column addresses)
- FAST-PAGE-MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles

OPTIONS

- Package
168-pin DIMM (gold)

- Timing
50ns access
60ns access

- Access Cycles
FAST PAGE MODE
EDO PAGE MODE

- Refresh
2,048 cycles across 32ms
4,096 cycles across 64ms (32MB only)

* EDO version only

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{CAS}
-5	84ns	50ns	20ns	30ns	18ns	8ns
-6	104ns	60ns	25ns	35ns	20ns	10ns

FPM Operating Mode

SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{RP}
-6	110ns	60ns	35ns	35ns	20ns	40ns

NOTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

MARKING

G

-5*

-6

None

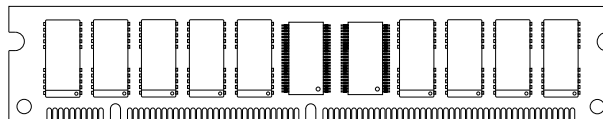
X

None

F

PIN ASSIGNMENT (Front View)

168-Pin DIMM



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	OE2#	86	DQ36	128	RFU
3	DQ1	45	RAS2#	87	DQ37	129	NC
4	DQ2	46	CAS4#	88	DQ38	130	NC
5	DQ3	47	RFU	89	DQ39	131	RFU
6	V _{DD}	48	WE2#	90	V _{DD}	132	PDE#
7	DQ4	49	V _{DD}	91	DQ40	133	V _{DD}
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	V _{DD}	101	DQ49	143	V _{DD}
18	V _{DD}	60	DQ24	102	V _{DD}	144	DQ60
19	DQ14	61	RFU	103	DQ50	145	RFU
20	DQ15	62	RFU	104	DQ51	146	RFU
21	DQ16	63	RFU	105	DQ52	147	RFU
22	DQ17	64	RFU	106	DQ53	148	RFU
23	V _{SS}	65	DQ25	107	V _{SS}	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	V _{DD}	68	V _{SS}	110	V _{DD}	152	V _{SS}
27	WE0#	69	DQ28	111	RFU	153	DQ64
28	CAS0#	70	DQ29	112	NC	154	DQ65
29	RFU	71	DQ30	113	RFU	155	DQ66
30	RAS0#	72	DQ31	114	NC	156	DQ67
31	OE0#	73	V _{DD}	115	RFU	157	V _{DD}
32	V _{SS}	74	DQ32	116	V _{SS}	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC (A12)	81	PD5	123	NC (A13)	165	PD6
40	V _{DD}	82	PD7	124	V _{DD}	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	V _{DD}	126	B0	168	V _{DD}



PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT9LD272G-xX	2 Meg x 72 ECC	2K Refresh
MT18LD472G-xX	4 Meg x 72 ECC	2K Refresh
MT18LD472FG-xX	4 Meg x 72 ECC	4K Refresh

x = speed

FPM Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT9LD272G-x	2 Meg x 72 ECC	2K Refresh
MT18LD472G-x	4 Meg x 72 ECC	2K Refresh
MT18LD472FG-x	4 Meg x 72 ECC	4K Refresh

x = speed

GENERAL DESCRIPTION

The MT9LD272(X) and MT18LD472(F)(X) are randomly accessed 16MB and 32MB memories organized in a x72 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the address bits. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for four-byte applications which interleave between two four-byte banks. A0 is common to the DRAMs used for DQ0-DQ35, while B0 is common to the DRAMs used for DQ36-DQ71. RAS# is used to latch the first 11/12 bits and CAS# the latter 10/11 bits.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data-outputs will drive read data from the accessed location.

FAST PAGE MODE

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^tCP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

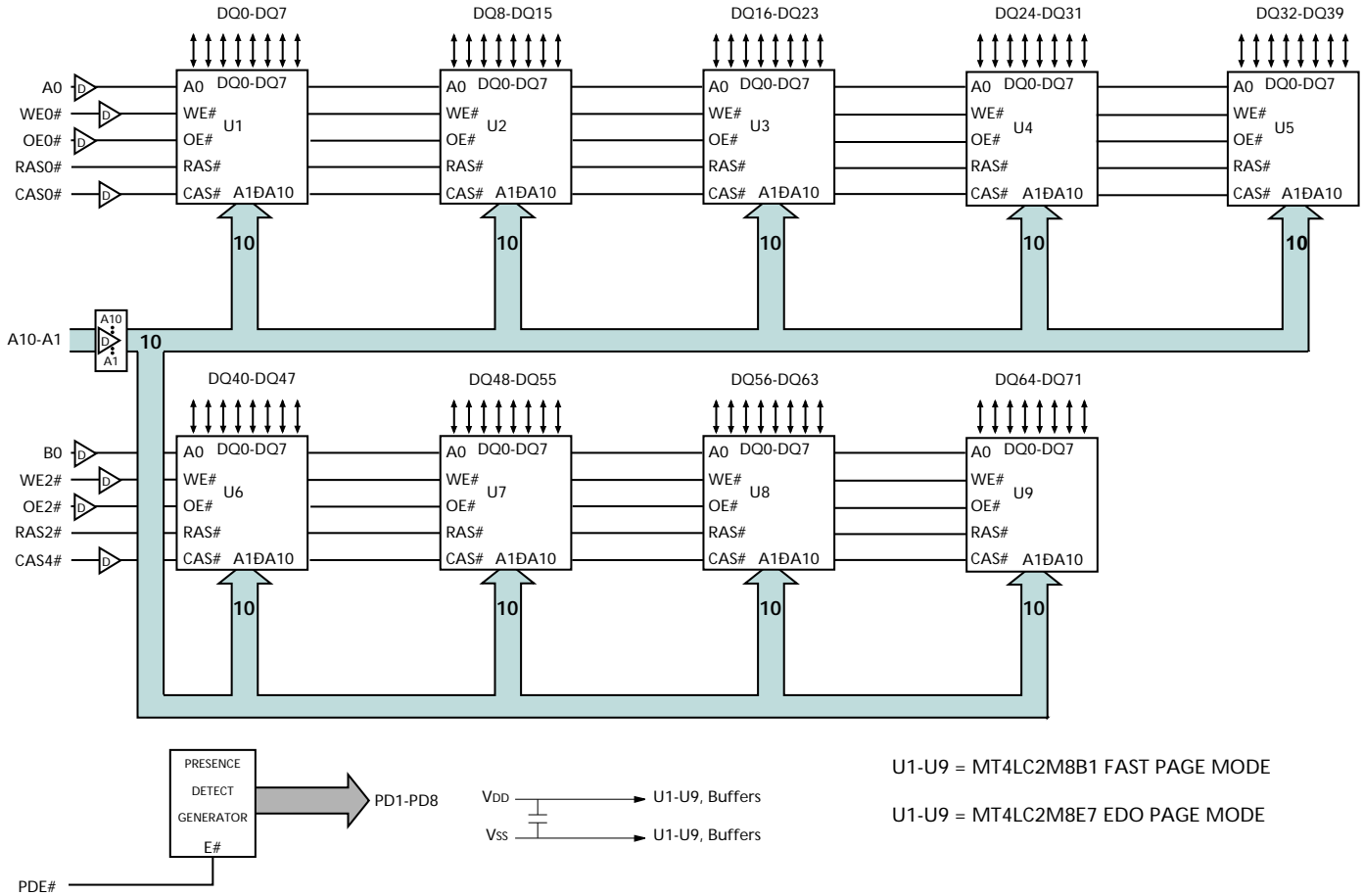
FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also High-Z the outputs. Independent of OE# control, the outputs will disable after ^tOFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last. (Refer to the 4 Meg x 4 [MT4LC4M4E8] DRAM data sheet for additional information on EDO functionality.)

REFRESH

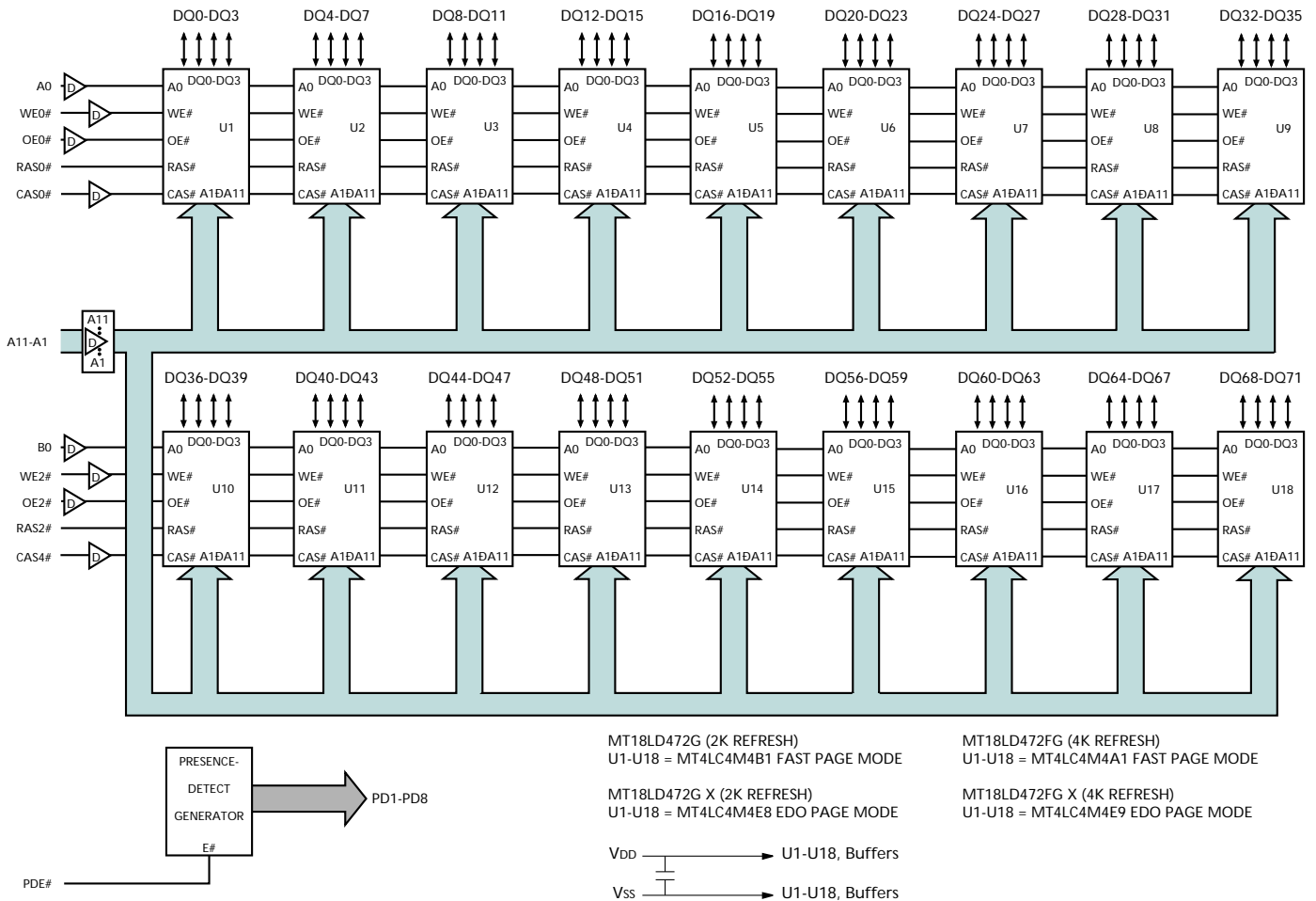
Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses are executed at least every ^tREF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

**FUNCTIONAL BLOCK DIAGRAM
MT9LD272(X) (16MB)**



NOTE: 1. All inputs, with the exception of RAS#, are redriven.
2. D = line buffers.

**FUNCTIONAL BLOCK DIAGRAM
MT18LD472(F)(X) (32MB)**



NOTE: 1. All inputs with the exception of RAS# are redriven.
2. D = line buffers.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	RAS0#, RAS2#	Input	Row-Address Strobe: RAS# is used to clock-in the row-address bits. Two RAS# inputs allow for one x72 bank or two x36 banks.
28, 46	CAS0#, CAS4#	Buffered Input	Column-Address Strobe: CAS# is used to clock-in the column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
27, 48	WE0#, WE2#	Buffered Input	Write Enable: WE# is the READ/WRITE control for the DQ pins. WE0# controls DQ0-DQ35. WE2# controls DQ36-DQ71. If WE# is LOW prior to CAS# going LOW, the access is an EARLY WRITE cycle. If WE# is HIGH while CAS# is LOW, the access is a READ cycle, provided OE# is also LOW. If WE# goes LOW after CAS# goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	OE0#, OE2#	Buffered Input	Output Enable: OE# is the input/output control for the DQ pins. OE0# controls DQ0-DQ35. OE2# controls DQ36-DQ71. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-122, 126	A0-A11, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by RAS# and CAS#. A0 is common to the DRAMs used for DQ0-DQ35 while B0 is common to the DRAMs used for DQ36-DQ71
2-5, 7-11, 13-17, 19-22, 52-53, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-106, 136-137, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ71	Input/Output	Data I/O: For WRITE cycles, DQ0-DQ71 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ71 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either no connect (1), or they will be driven to V _{OL} (0).
29, 41-42, 47, 61-64, 111, 113, 115, 125, 128, 131, 145-148	RFU	-	Reserved for Future Use: These pins should be left unconnected.
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V _{DD}	Supply	Power Supply: +3.3V ± 0.3V.
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	V _{SS}	Supply	Ground.
83, 167	ID0, ID1	Output	ID Bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (V _{SS}).
132	PDE#	Input	Presence-Detect Enable: PDE# is the READ control for the buffered presence-detect pins.

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Configuration	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			1	1	1	1				
8MB	1 Meg x 64/72	10/9			1	1	0	0				
8MB	1 Meg x 64/72	10/10			0	0	1	0				
16MB	2 Meg x 64/72	10/10			1	0	1	0				
• 16MB	2 Meg x 64/72	11/10			1	0	0	1				
32MB	4 Meg x 64/72	11/10			0	1	0	1				
• 32MB	4 Meg x 64/72	12*/11*			1	1	0	1				
64MB	8 Meg x 64/72	12*/11*			0	0	1	1				
Page Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		70ns								0	1	
		60ns								1	1	
		50ns									0	0
Refresh Control		Standard		Vss								
Data Width		x64, No Parity	Vss									1
		x72, ECC	Vss									0

NOTE: V_{SS} = Ground; V_{OL} = 0; NC = 1.

* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting.


ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Pin Relative to V_{SS} -1V to +4.6V
 Voltage on Inputs or I/O Pins

Relative to V_{SS} -1V to +4.6V
 Operating Temperature, T_A (ambient) .. 0°C to +70°C
 Storage Temperature (plastic) -55°C to +125°C
 Power Dissipation 9W

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES	
SUPPLY VOLTAGE	V _{DD}	3	3.6	V		
INPUT HIGH VOLTAGE: Logic 1; All inputs	V _{IH}	2	V _{DD} + 0.3	V	36	
INPUT LOW VOLTAGE: Logic 0; All inputs	V _{IL}	-0.5	0.8	V	36	
INPUT LEAKAGE CURRENT: Any input 0V ≤ V _{IN} ≤ V _{DD} + 0.3V (All other pins not under test = 0V)	CAS0#, CAS4#, A0-A11, B0, PDE#, WE0#, WE2#, OE0#, OE2#	I _{I1}	-2	2	μA	
	RAS0#-RAS3#	I _{I2}	-18	18	μA	
OUTPUT LEAKAGE CURRENT: DQ is disabled; 0V ≤ V _{OUT} ≤ V _{DD} + 0.3V	DQ0-DQ71, PD1-PD8	I _{OZ}	-5	5	μA	
OUTPUT LEVELS: Output High Voltage (I _{OUT} = -2mA) Output Low Voltage (I _{OUT} = 2mA)	V _{OH}	2.4	-	V		
	V _{OL}	-	0.4	V		

2,048-CYCLE REFRESH I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS
(Notes: 1, 5, 6) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX		UNITS	NOTES
			-5*	-6		
STANDBY CURRENT: TTL (RAS# = CAS# = V _{IH})	I _{CC1}	16MB 32MB	72 90	72 90	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# = V _{DD} - 0.2V)	I _{CC2}	16MB 32MB	9 9	9 9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: t _{RC} = t _{RC} [MIN])	I _{CC3}	16MB 32MB	990 1,980	900 1,800	mA	3, 29
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V _{IL} , CAS#, address cycling: t _{PC} = t _{PC} [MIN])	I _{CC4}	16MB 32MB	- -	720 1,440	mA	3, 29
OPERATING CURRENT: EDO PAGE MODE ("X" version only) Average power supply current (RAS# = V _{IL} , CAS#, address cycling: t _{PC} = t _{PC} [MIN])	I _{CC5} (X only)	16MB 32MB	990 1,980	900 1,800	mA	3, 29
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V _{IH} : t _{RC} = t _{RC} [MIN])	I _{CC6}	16MB 32MB	990 1,980	900 1,800	mA	3, 29
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: t _{RC} = t _{RC} [MIN])	I _{CC7}	16MB 32MB	990 1,980	900 1,800	mA	3, 4

4,096-CYCLE REFRESH I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS
(Notes: 1, 5, 6) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX		UNITS	NOTES
			-5*	-6		
STANDBY CURRENT: TTL (RAS# = CAS# = V _{IH})	I _{CC1}	32MB	90	90	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# = V _{DD} - 0.2V)	I _{CC2}	32MB	9	9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: t _{RC} = t _{RC} [MIN])	I _{CC3}	32MB	1,620	1,440	mA	3, 29
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V _{IL} , CAS#, address cycling: t _{PC} = t _{PC} [MIN])	I _{CC4}	32MB	-	1,260	mA	3, 29
OPERATING CURRENT: EDO PAGE MODE ("X" version only) Average power supply current (RAS# = V _{IL} , CAS#, address cycling: t _{PC} = t _{PC} [MIN])	I _{CC5} (X only)	32MB	1,800	1,620	mA	3, 29
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V _{IH} : t _{RC} = t _{RC} [MIN])	I _{CC6}	32MB	1,620	1,440	mA	3, 29
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: t _{RC} = t _{RC} [MIN])	I _{CC7}	32MB	1,620	1,440	mA	3, 4

* EDO version only



CAPACITANCE

PARAMETER	SYMBOL	MAX		UNITS	NOTES
		16MB	32MB		
Input Capacitance: A0-A11, B0, PDE#, OE0#, OE2#	C _{I1}	9	9	pF	2
Input Capacitance: WE0#, WE2#, CAS0#, CAS4#	C _{I2}	9	9	pF	2
Input Capacitance: RAS0#, RAS2#	C _{I3}	39	67	pF	2
Input/Output Capacitance: DQ0-DQ71	C _{I0}	10	10	pF	2
Output Capacitance: PD1-PD8	C _O	10	10	pF	2

FAST PAGE MODE

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 35) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX		
Access time from column address	t _{AA}		35	ns	23
Column-address hold time (referenced to RAS#)	t _{AR}	43		ns	22
Column-address setup time	t _{ASC}	2		ns	21
Row-address setup time	t _{ASR}	5		ns	23
Column address to WE# delay time	t _{AWD}	57		ns	21, 28
Access time from CAS#	t _{CAC}		20	ns	14, 23
Column-address hold time	t _{CAH}	15		ns	23
CAS# pulse width	t _{CAS}	15	10,000	ns	
CAS# hold time (CBR Refresh)	t _{CHR}	8		ns	4, 22
CAS# to output in Low-Z	t _{CLZ}	5		ns	21, 30
CAS# precharge time	t _{CP}	10		ns	15
Access time from CAS# precharge	t _{CPA}		40	ns	23
CAS# to RAS# precharge time	t _{CRP}	10		ns	23
CAS# hold time	t _{CSH}	58		ns	22
CAS# setup time (CBR Refresh)	t _{CSR}	7		ns	4, 21
CAS# to WE# delay time	t _{CWD}	42		ns	21, 28
WRITE command to CAS# lead time	t _{CWL}	15		ns	
Data-in hold time	t _{DH}	15		ns	23, 27
Data-in setup time	t _{DS}	-2		ns	22, 27
Output disable	t _{OD}	3	15	ns	
Output enable	t _{OE}		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t _{OEH}	13		ns	22, 26
Output buffer turn-off delay	t _{OFF}	5	20	ns	19, 25, 33
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t _{ORD}	0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t _{PC}	35		ns	

**FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS**

 (Notes: 5, 6, 7, 8, 9, 12, 35) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - FAST PAGE MODE OPTION PARAMETER	SYMBOL	-6		UNITS	NOTES
		MIN	MAX		
PDE# to valid presence-detect data	t_{PD}		10	ns	32
PDE# inactive to presence-detects inactive	t_{PDOFF}	2		ns	31
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	87		ns	21
Access time from RAS#	t_{RAC}		60	ns	13
RAS# to column-address delay time	t_{RAD}	13		ns	17, 24
Row-address hold time	t_{RAH}	8		ns	22
RAS# pulse width	t_{RAS}	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	t_{RASP}	60	125,000	ns	
Random READ or WRITE cycle time	t_{RC}	110		ns	
RAS# to CAS# delay time	t_{RCD}	18		ns	16, 24
READ command hold time (referenced to CAS#)	t_{RCH}	2		ns	18, 21
READ command setup time	t_{RCS}	2		ns	21
Refresh period (2,048 cycles) (16MB)	t_{REF}		32	ms	
Refresh period (4,096 cycles) (32MB)	t_{REF}		64	ms	
RAS# precharge time	t_{RP}	40		ns	
RAS# to CAS# precharge time	t_{RPC}	0		ns	
READ command hold time (referenced to RAS#)	t_{RRH}	0		ns	18
RAS# hold time	t_{RSH}	20		ns	23
READ-WRITE cycle time	t_{RWC}	160		ns	23
RAS# to WE# delay time	t_{RWD}	87		ns	21, 28
WRITE command to RAS# lead time	t_{RWL}	20		ns	23
Transition time (rise or fall)	t_T	2	50	ns	
WRITE command hold time	t_{WCH}	15		ns	23
WRITE command hold time (referenced to RAS#)	t_{WCR}	43		ns	22
WE# command setup time	t_{WCS}	2		ns	21, 28
WRITE command pulse width	t_{WCP}	10		ns	
WE# hold time (CBR Refresh)	t_{WRH}	8		ns	22
WE# setup time (CBR Refresh)	t_{WRP}	12		ns	21


EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

 (Notes: 5, 6, 7, 8, 9, 12, 35) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
Access time from column address	t_{AA}		30		35	ns	23
Column-address setup to CAS# precharge	t_{ACH}	12		15		ns	
Column-address hold time (referenced to RAS#)	t_{AR}	36		43		ns	22
Column-address setup time	t_{ASC}	2		2		ns	21
Row-address setup time	t_{ASR}	5		5		ns	23
Column address to WE# delay time	t_{AWD}	44		51		ns	21, 28
Access time from CAS#	t_{CAC}		18		20	ns	14, 23
Column-address hold time	t_{CAH}	13		15		ns	23
CAS# pulse width	t_{CAS}	8	10,000	10	10,000	ns	
CAS# hold time (CBR Refresh)	t_{CHR}	6		8		ns	4, 22
CAS# to output in Low-Z	t_{CLZ}	2		2		ns	21
Data output hold after next CAS# LOW	t_{COH}	5		5		ns	21
CAS# precharge time	t_{CP}	8		10		ns	15
Access time from CAS# precharge	t_{CPA}		33		40	ns	23
CAS# to RAS# precharge time	t_{CRP}	10		10		ns	23
CAS# hold time	t_{CSH}	36		43		ns	22
CAS# setup time (CBR Refresh)	t_{CSR}	7		7		ns	4, 21
CAS# to WE# delay time	t_{CWD}	30		37		ns	21, 28
WRITE command to CAS# lead time	t_{CWL}	8		10		ns	
Data-in hold time	t_{DH}	13		15		ns	23, 27
Data-in setup time	t_{DS}	-2		-2		ns	22, 27
Output disable	t_{OD}	0	12	0	15	ns	
Output enable	t_{OE}		12		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t_{OEHL}	6		8		ns	22, 26
OE# HIGH hold from CAS# HIGH	t_{OEHC}	5		10		ns	26
OE# HIGH pulse width	t_{OEP}	5		5		ns	
OE# LOW to CAS# HIGH setup time	t_{OES}	4		5		ns	
Output buffer turn-off delay	t_{OFF}	2	17	2	20	ns	19, 25, 33


**EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS**

 (Notes: 5, 6, 7, 8, 9, 12, 35) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t_{ORD}	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	20		25		ns	
PDE# to valid presence-detect data	t_{PD}		10		10	ns	32
PDE# inactive to presence-detect inactive	t_{PDOFF}	2		2		ns	31
EDO-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	49		58		ns	21
Access time from RAS#	t_{RAC}		50		60	ns	13
RAS# to column-address delay time	t_{RAD}	7		10		ns	17, 22
Row-address hold time	t_{RAH}	7		8		ns	22
RAS# pulse width	t_{RAS}	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	t_{RASP}	50	125,000	60	125,000	ns	
Random READ or WRITE cycle time	t_{RC}	84		104		ns	
RAS# to CAS# delay time	t_{RCD}	9		12		ns	16, 24
READ command hold time (referenced to CAS#)	t_{RCH}	2		2		ns	18, 21
READ command setup time	t_{RCS}	2		2		ns	21
Refresh period (2,048 cycles) (16MB)	t_{REF}		32		32	ms	
Refresh period (4,096 cycles) (32MB)	t_{REF}		64		64	ms	
RAS# precharge time	t_{RP}	30		40		ns	
RAS# to CAS# precharge time	t_{RPC}	5		5		ns	
READ command hold time (referenced to RAS#)	t_{RRH}	0		0		ns	18
RAS# hold time	t_{RSH}	18		20		ns	23
READ-ZWRITE cycle time	t_{RWC}	121		145		ns	23
RAS# to WE# delay time	t_{RWD}	69		81		ns	21, 28
WRITE command to RAS# lead time	t_{RWL}	18		20		ns	23
Transition time (rise or fall)	t_T	2	50	2	50	ns	
WRITE command hold time	t_{WCH}	13		15		ns	23
WRITE command hold time (referenced to RAS#)	t_{WCR}	36		43		ns	22
WE# command setup time	t_{WCS}	2		2		ns	21, 28
Output disable delay from WE#	t_{WHZ}	2	17	2	20	ns	25
WRITE command pulse width	t_{WP}	5		5		ns	
WE# pulse to disable at CAS# HIGH	t_{WPZ}	10		10		ns	
WE# hold time (CBR Refresh)	t_{WRH}	6		8		ns	22
WE# setup time (CBR Refresh)	t_{WRP}	10		12		ns	21

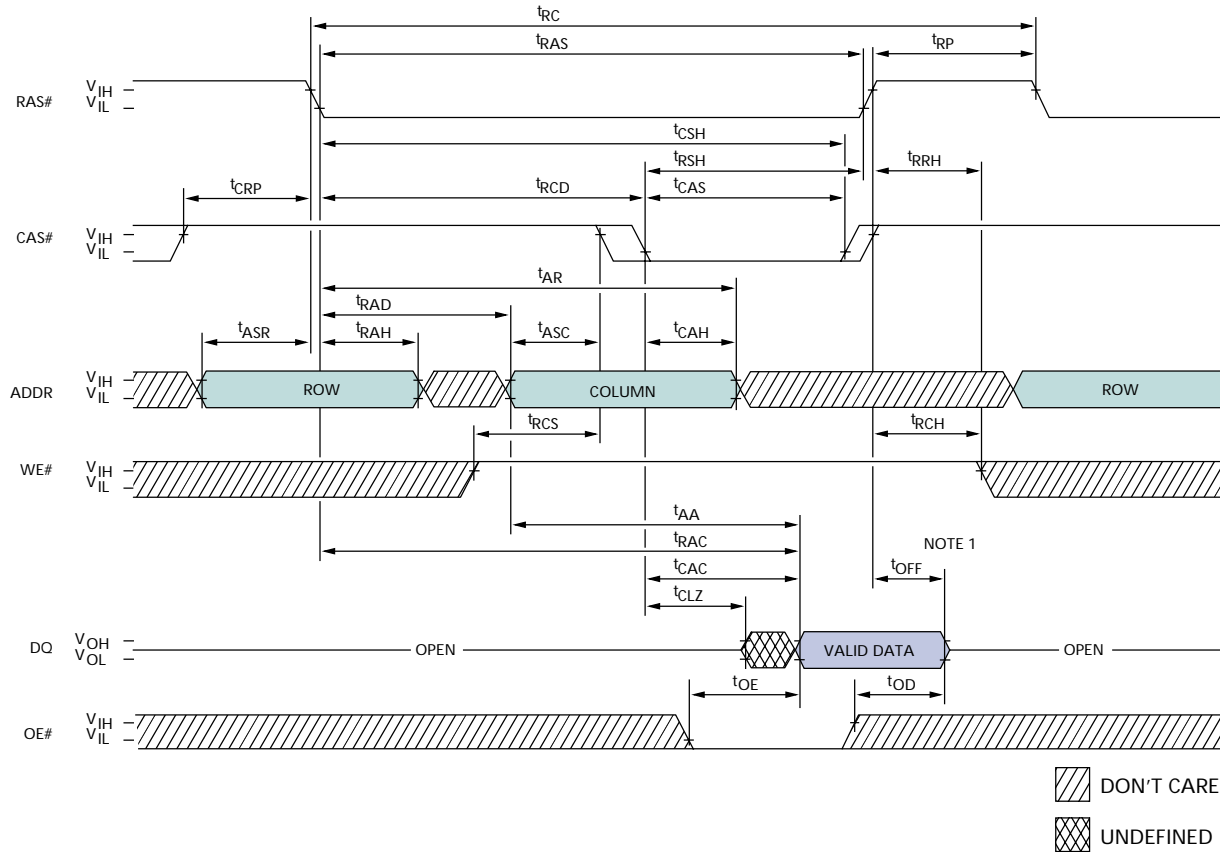
NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{DD} = +3.3V$; $f = 1$ MHz.
3. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of $100\mu s$ is required after power-up, followed by eight RAS# REFRESH cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume $t_T = 5ns$ for FPM and $2.5ns$ for EDO.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH} , data output is High-Z.
11. If CAS# = V_{IL} , data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and $100pF$ and $V_{OL} = 0.8V$ and $V_{OH} = 2V$.
13. Requires that t_{AA} and t_{CAC} are not violated.
14. Requires that t_{AA} and t_{RAC} are not violated.
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for t_{CP} .
16. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With or without the t_{RCD} (MAX) limit, t_{AA} and t_{CAC} must always be met.
17. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA} , t_{RAC} and t_{CAC} must always be met.
18. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
19. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
22. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
23. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OE} met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after t_{OE} is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
27. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
28. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY WRITE cycles. t_{RWD} , t_{AWD} and t_{CWD} apply to READ-MODIFY-WRITE cycles. If $t_{WCS} \geq t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{WCS} < t_{WCS}$ (MIN) and $t_{RWD} \geq t_{RWD}$ (MIN), $t_{AWD} \geq t_{AWD}$ (MIN) and $t_{CWD} \geq t_{CWD}$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not applicable in a LATE WRITE cycle.
29. Column address changed once each cycle.
30. The 3ns minimum parameter guaranteed by design.

**NOTES (continued)**

31. $t_{P\text{DOFF MAX}}$ is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
32. Measured with specified current load and 100pF.
33. With the FPM option, t_{OFF} is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, t_{OFF} on an EDO option is determined by the latter of the RAS# and CAS# signals to transition HIGH.
34. Applies to both FPM and EDO operating modes.
35. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
36. V_{IH} overshoot: $V_{\text{IH}} (\text{MAX}) = V_{\text{DD}} + 2V$ for a pulse width $\leq 10\text{ns}$, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: $V_{\text{IL}} (\text{MIN}) = -2V$ for a pulse width $\leq 10\text{ns}$, and the pulse width cannot be greater than one third of the cycle rate.

READ CYCLE ³⁴



FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

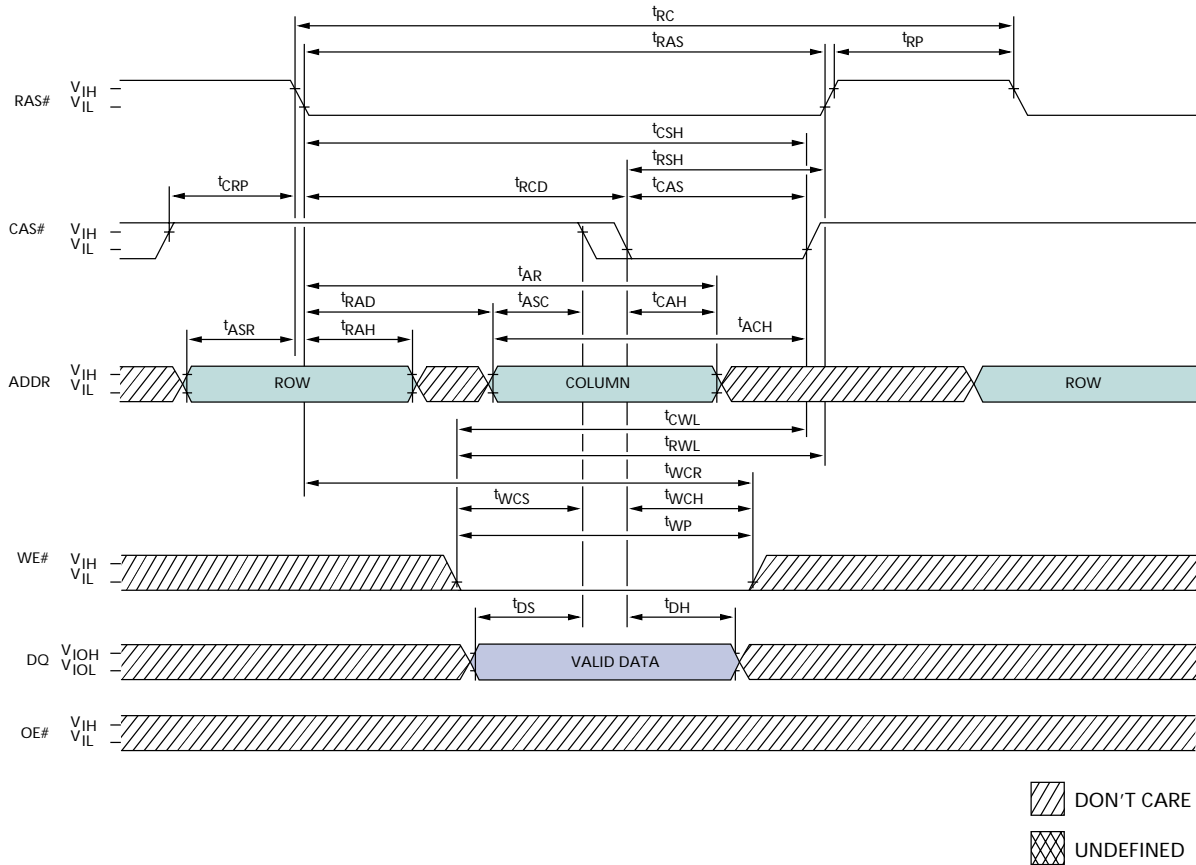
SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		30		35	ns
tACH (EDO)	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	-	-	15	10,000	ns
tCLZ (EDO)	2		2		ns
tCLZ (FPM)	-		5		ns
tCRP	10		10		ns
tCSH (EDO)	36		43		ns
tCSH (FPM)	-		58		ns
tOD (EDO)	0	12	0	15	ns
tOD (FPM)	-	-	3	15	ns
tOE		12		15	ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
tOFF (EDO)	2	17	2	20	ns
tOFF (FPM)	-	-	5	20	ns
tRAC		50		60	ns
tRAD (EDO)	7		10		ns
tRAD (FPM)	-		13		ns
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns
tRC (EDO)	84		104		ns
tRC (FPM)	-		110		ns
tRCD (EDO)	9		12		ns
tRCD (FPM)	-		18		ns
tRCH	2		2		ns
tRCS	2		2		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	18		20		ns

*EDO version only

NOTE: 1. For EDO, tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last. For FPM, tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs first.

EARLY WRITE CYCLE ³⁴



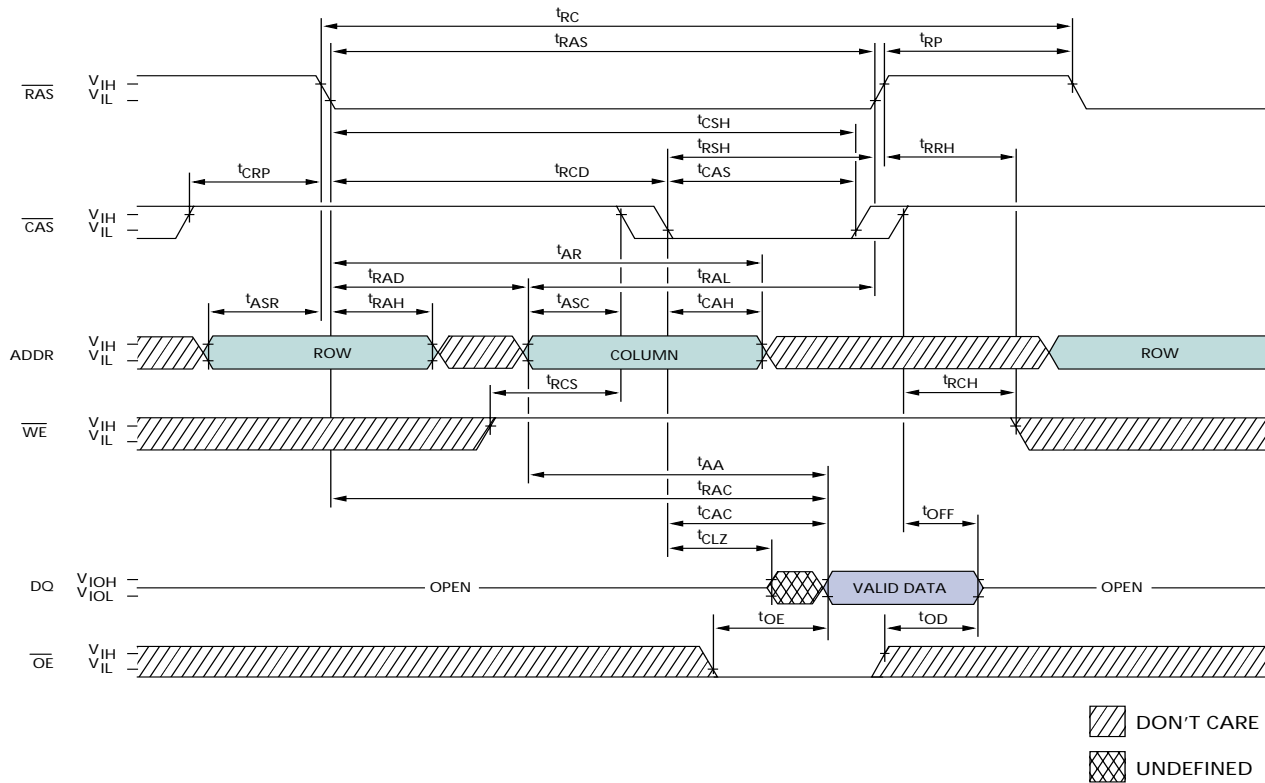
FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
tACH (EDO)	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAH	13		15		ns
tCAS (FPM)	-	-	15	10,000	ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCRP	10		10		ns
tCSH (FPM)	-		58		ns
tCSH (EDO)	36		43		ns
tCWL (FPM)	-		15		ns
tCWL (EDO)	8		10		ns
tDH	13		15		ns
tDS	-2		-2		ns
tRAD (FPM)	-		13		ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
tRAD (EDO)	7		10		ns
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	-		110		ns
tRC (EDO)	84		104		ns
tRCD (FPM)	-		18		ns
tRCD (EDO)	9		12		ns
tRP	30		40		ns
tRSH	18		20		ns
tRWL	18		20		ns
tWCH	13		15		ns
tWCR	36		43		ns
tWCS	2		2		ns
tWP (FPM)	-		10		ns
tWP (EDO)	5		5		ns

*EDO version only

FAST-PAGE-MODE READ CYCLE



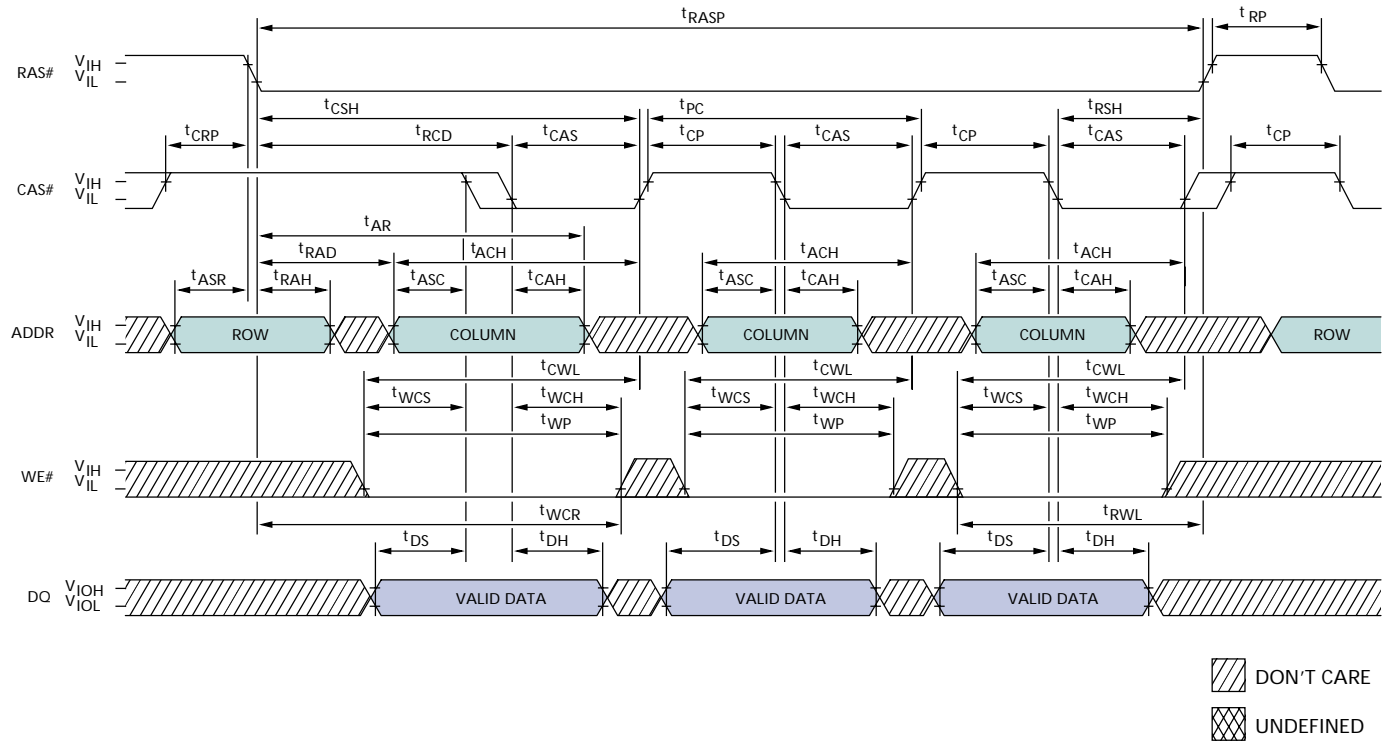
DON'T CARE
 UNDEFINED

FAST PAGE MODE
TIMING PARAMETERS

SYMBOL	-6		UNITS
	MIN	MAX	
t_{AA}		35	ns
t_{AR}	43		ns
t_{ASC}	2		ns
t_{ASR}	5		ns
t_{CAC}		20	ns
t_{CAH}	15		ns
t_{CAS}	15	10,000	ns
t_{CLZ}	5		ns
t_{CP}	10		ns
t_{CPA}		40	ns
t_{CRP}	10		ns
t_{CSH}	58		ns
t_{OD}	3	15	ns

SYMBOL	-6		UNITS
	MIN	MAX	
t_{OE}		15	ns
t_{OFF}	5	20	ns
t_{PC}	35		ns
t_{RAC}		60	ns
t_{RAD}	13		ns
t_{RAH}	8		ns
t_{RASP}	60	125,000	ns
t_{RCD}	18		ns
t_{RCH}	2		ns
t_{RCS}	2		ns
t_{RP}	40		ns
t_{RRH}	0		ns
t_{RSH}	20		ns

FAST/EDO-PAGE-MODE EARLY WRITE CYCLE³⁴



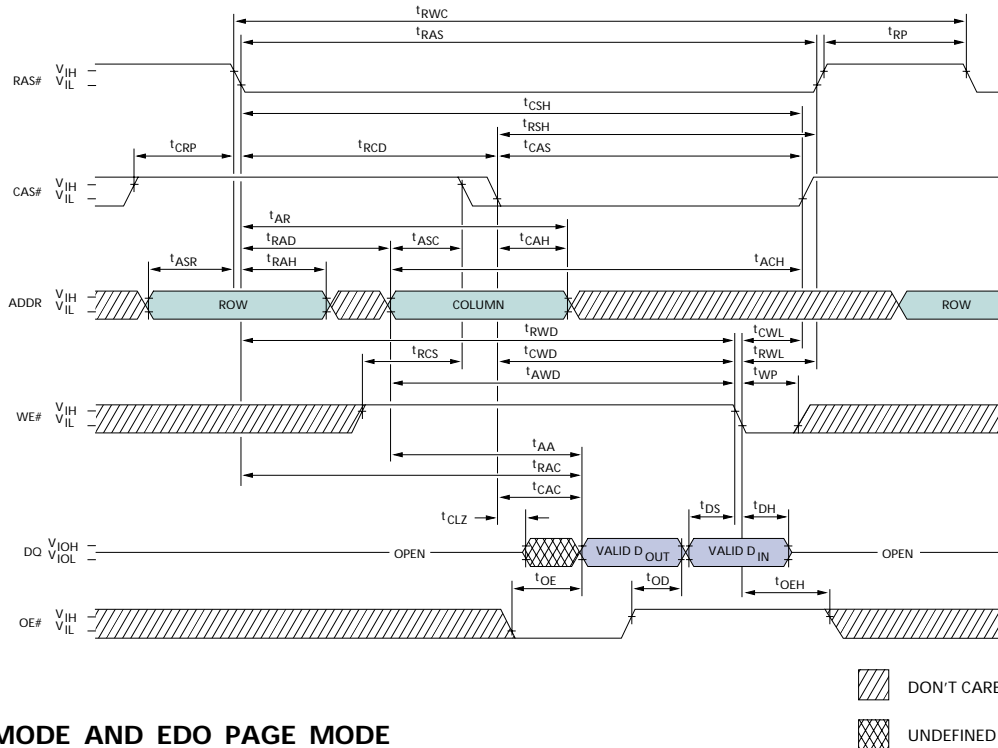
FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{ACH} (EDO)	12		15		ns
t _{AR}	36		43		ns
t _{ASC}	2		2		ns
t _{ASR}	5		5		ns
t _{CAH}	13		15		ns
t _{CAS} (EDO)	8	10,000	10	10,000	ns
t _{CAS} (FPM)	-	-	15	10,000	ns
t _{CP}	8		10		ns
t _{CRP}	10		10		ns
t _{CSH} (EDO)	36		43		ns
t _{CSH} (FPM)	-		58		ns
t _{CWL} (EDO)	8		10		ns
t _{CWL} (FPM)	-		15		ns
t _{DH}	13		15		ns
t _{DS}	-2		-2		ns
t _{PC} (EDO)	20		25		ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{PC} (FPM)	-		35		ns
t _{RAD} (EDO)	7		10		ns
t _{RAD} (FPM)	-		13		ns
t _{RAH}	7		8		ns
t _{RASP}	50	125,000	60	125,000	ns
t _{RCD} (EDO)	9		12		ns
t _{RCD} (FPM)	-		18		ns
t _{RP}	30		40		ns
t _{RSH}	18		20		ns
t _{RWL}	18		20		ns
t _{WCH}	13		15		ns
t _{WCR}	36		43		ns
t _{WCS}	2		2		ns
t _{WP} (EDO)	5		5		ns
t _{WP} (FPM)	-		10		ns

*EDO version only

READ-WRITE CYCLE ³⁴ (LATE WRITE and READ-MODIFY-WRITE cycles)



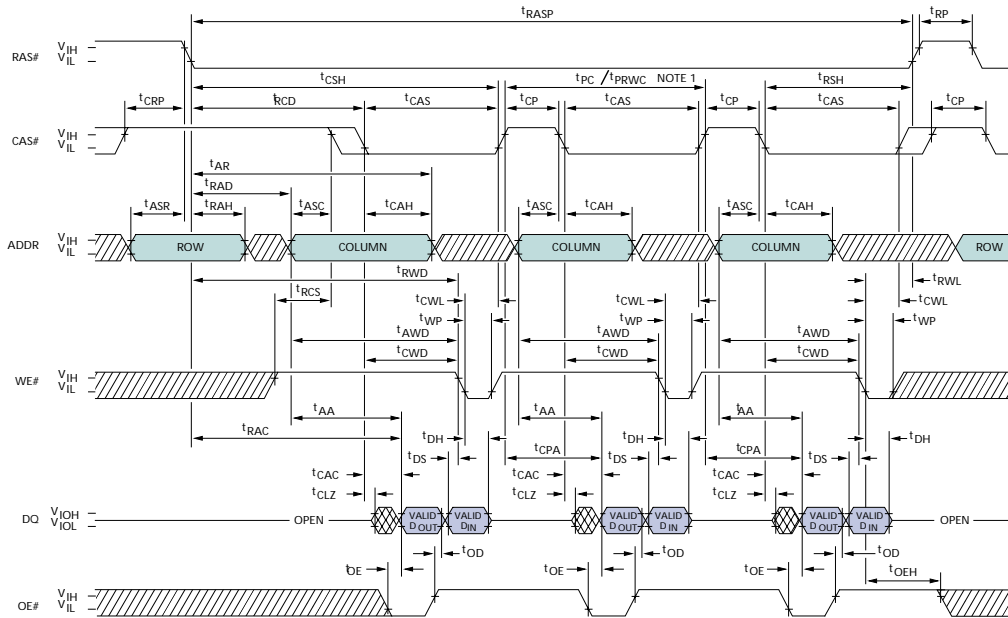
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		30		35	ns
t _{ACH} (EDO)	12		15		ns
t _{AR}	36		43		ns
t _{ASC}	2		2		ns
t _{ASR}	5		5		ns
t _{AWD} (EDO)	42		49		ns
t _{AWD} (FPM)	-		57		ns
t _{CAC}		18		20	ns
t _{CAH}	13		15		ns
t _{CAS} (EDO)	8	10,000	10	10,000	ns
t _{CAS} (FPM)	-	-	15	10,000	ns
t _{CLZ} (EDO)	2		2		ns
t _{CLZ} (FPM)	-		5		ns
t _{CRP}	10		10		ns
t _{CSH} (EDO)	36		43		ns
t _{CSH} (FPM)	-		58		ns
t _{CWD} (EDO)	30		37		ns
t _{CWD} (FPM)	-		42		ns
t _{CWL} (EDO)	8		10		ns
t _{CWL} (FPM)	-		15		ns
t _{DH}	13		15		ns
t _{DS}	-2		-2		ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OD} (EDO)	0	12	0	15	ns
t _{OD} (FPM)	-	-	3	15	ns
t _{OE}		12		15	ns
t _{OEH} (EDO)	6		8		ns
t _{OEH} (FPM)	-		13		ns
t _{RAC}		50		60	ns
t _{RAD} (EDO)	7		10		ns
t _{RAD} (FPM)	-		13		ns
t _{RAH}	7		8		ns
t _{RAS}	50	10,000	60	10,000	ns
t _{RCD} (EDO)	9		12		ns
t _{RCD} (FPM)	-		18		ns
t _{RCS}	2		2		ns
t _{RP}	30		40		ns
t _{RSH}	18		20		ns
t _{RWC} (EDO)	121		145		ns
t _{RWC} (FPM)	-		160		ns
t _{RWD} (EDO)	69		81		ns
t _{RWD} (FPM)	-		87		ns
t _{RWL}	18		20		ns
t _{WP} (EDO)	5		5		ns
t _{WP} (FPM)	-		10		ns

*EDO version only

FAST/EDO-PAGE-MODE READ-WRITE CYCLE³⁴
(LATE WRITE and READ-MODIFY-WRITE cycles)



▨ DON'T CARE
▩ UNDEFINED

**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

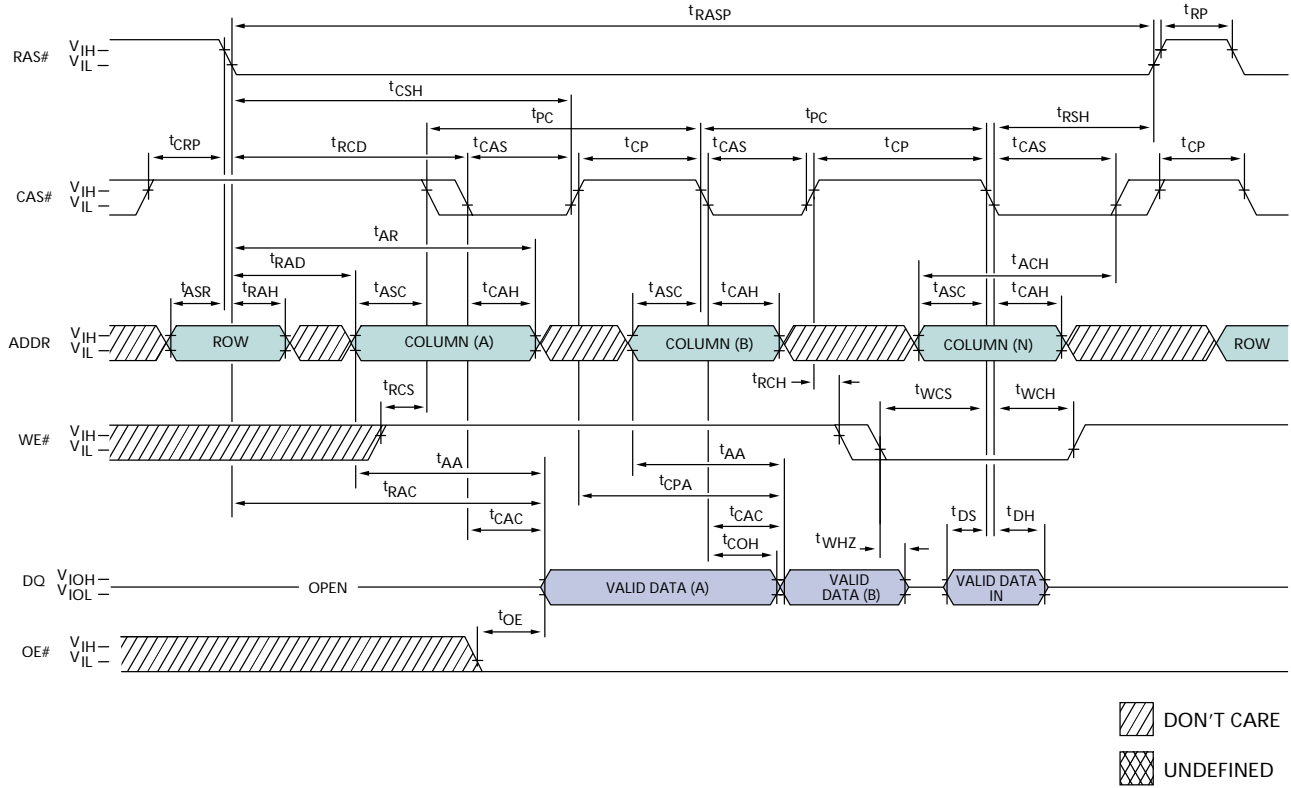
SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		30	43	35	ns
tAR	36				ns
tASC	2		2		ns
tASR	5		5		ns
tAWD (EDO)	42		49		ns
tAWD (FPM)	-		57		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	-	-	15	10,000	ns
tCLZ (EDO)	2		2		ns
tCLZ (FPM)	-		5		ns
tCP	8		10		ns
tCPA		33		40	ns
tCRP	10		10		ns
tCSH (EDO)	36		43		ns
tCSH (FPM)	-		58		ns
tCWD (EDO)	30		37		ns
tCWD (FPM)	-		42		ns
tCWL (EDO)	8		10		ns
tCWL (FPM)	-		15		ns
tDH	13		15		ns
tDS	-2		-2		ns
tOD (EDO)	0	12	0	15	ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
tOD (FPM)	-	-	3	15	ns
tOE		12		15	ns
tOE (EDO)	6		8		ns
tOE (FPM)	-		13		ns
tPC (EDO)	20		25		ns
tPC (FPM)	-		35		ns
tPRWC (EDO)	49		58		ns
tPRWC (FPM)	-		87		ns
tRAC		50		60	ns
tRAD (EDO)	7		10		ns
tRAD (FPM)	-		13		ns
tRAH	7		8		ns
tRASP	50	125,000	60	125,000	ns
tRCD (EDO)	9		12		ns
tRCD (FPM)	-		18		ns
tRCS	2		2		ns
tRP	30		40		ns
tRSH	18		20		ns
tRWD (EDO)	69		81		ns
tRWD (FPM)	-		87		ns
tRWL	18		20		ns
tWP (EDO)	5		5		ns
tWP (FPM)	-		10		ns

NOTE: 1. tPC is for LATE WRITE cycles only.

*EDO version only

EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

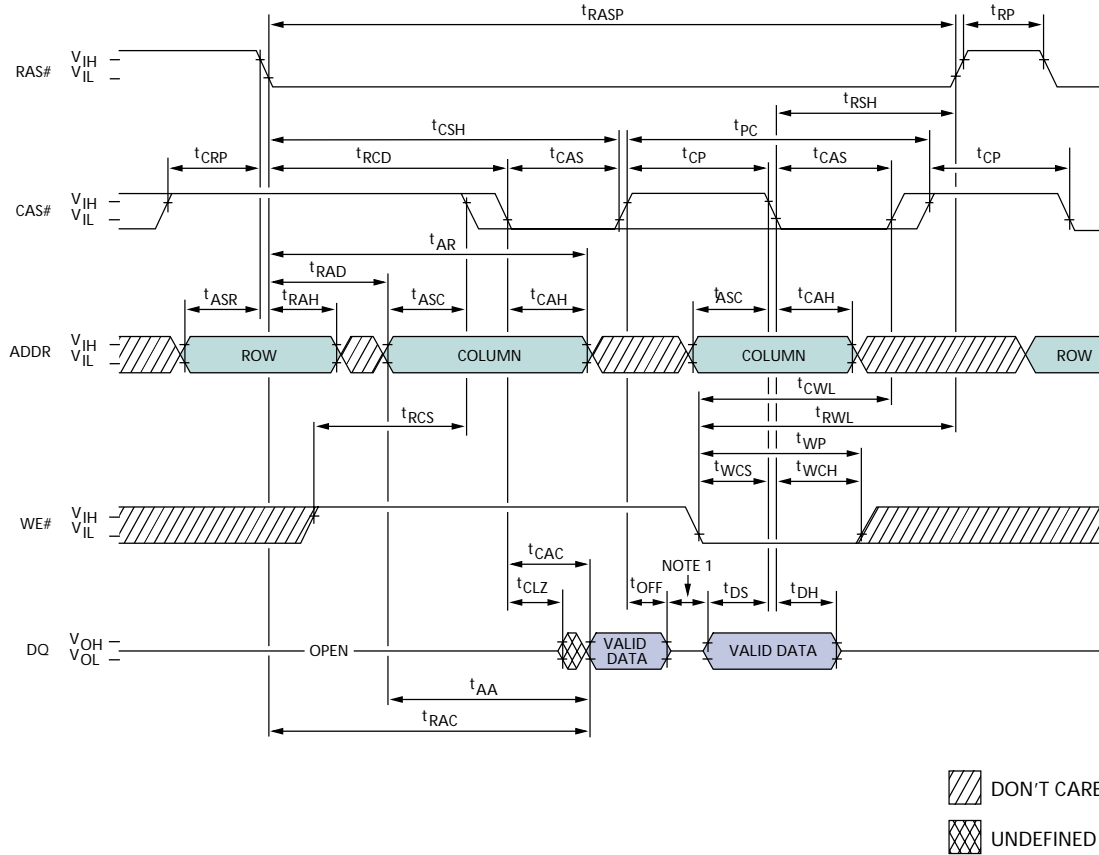


**EDO PAGE MODE
TIMING PARAMETERS**

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		30		35	ns
tACH	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCOH	5		5		ns
tCP	8		10		ns
tCPA		33		40	ns
tCRP	10		10		ns
tCSH	36		43		ns
tDH	13		15		ns
tDS	-2		-2		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tOE		12		15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	7		10		ns
tRAH	7		8		ns
tRASP	50	125,000	60	125,000	ns
tRCD	9		12		ns
tRCH	2		2		ns
tRCS	2		2		ns
tRP	30		40		ns
tRSH	18		20		ns
tWCH	13		15		ns
tWCS	2		2		ns
tWHZ	2	17	2	20	ns

FAST-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



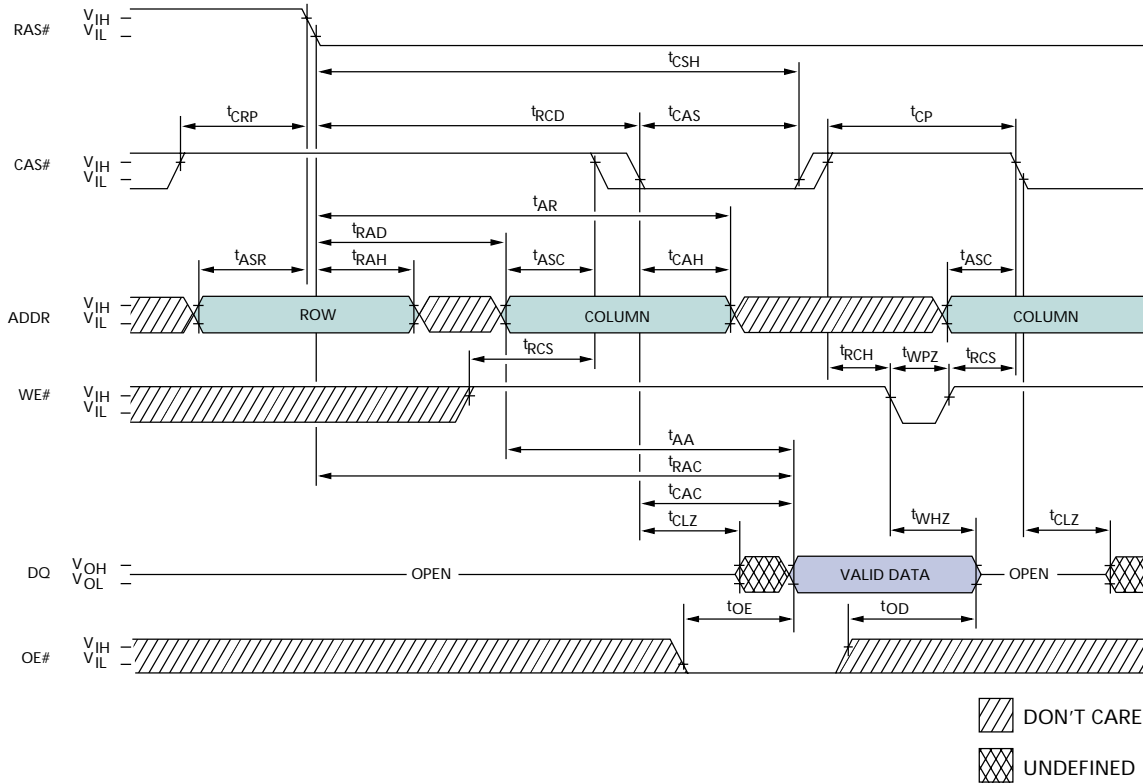
**FAST PAGE MODE
TIMING PARAMETERS**

SYMBOL	-6		UNITS
	MIN	MAX	
tAA		35	ns
tAR	43		ns
tASC	2		ns
tASR	5		ns
tCAC		20	ns
tCAH	15		ns
tCAS	15	10,000	ns
tCLZ	5		ns
tCP	10		ns
tCRP	10		ns
tCSH	58		ns
tCWL	15		ns
tDH	15		ns
tDS	-2		ns

SYMBOL	-6		UNITS
	MIN	MAX	
tOFF	5	20	ns
tPC	35		ns
tRAC		60	ns
tRAD	13		ns
tRAH	8		ns
tRASP	60	125,000	ns
tRCD	18		ns
tRCS	2		ns
tRP	40		ns
tRSH	20		ns
tRWL	20		ns
tWCH	15		ns
tWCS	2		ns
tWP	10		ns

NOTE: 1. Do not drive data prior to tristate.

EDO READ CYCLE
(with WE#-controlled disable)

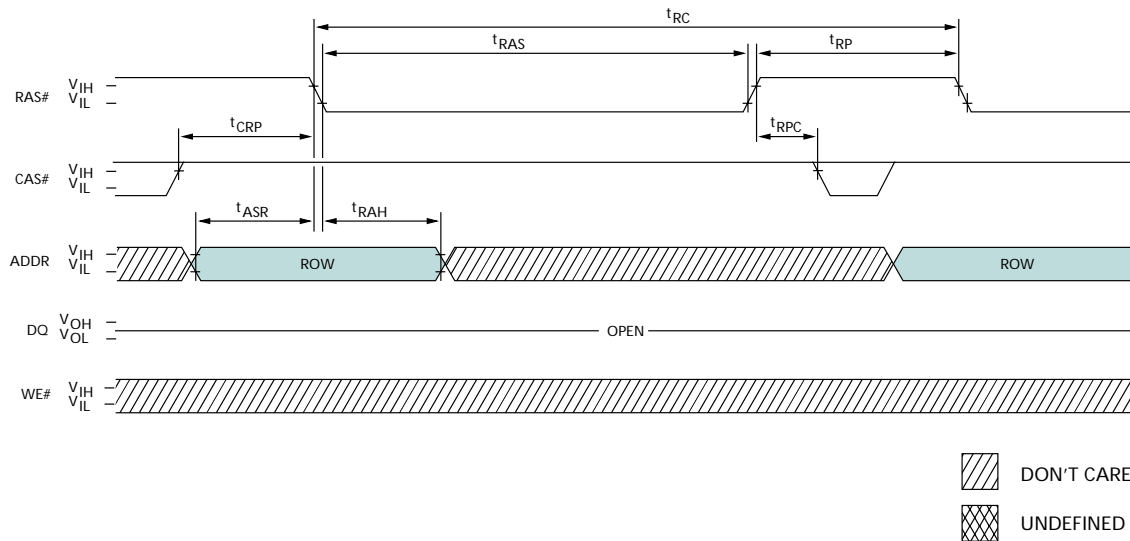


EDO PAGE MODE
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		30		35	ns
t_{AR}	36		43		ns
t_{ASC}	2		2		ns
t_{ASR}	5		5		ns
t_{CAC}		18		20	ns
t_{CAH}	13		15		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	2		2		ns
t_{CP}	8		10		ns
t_{CRP}	10		10		ns
t_{CSH}	36		43		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{OD}	0	12	0	15	ns
t_{OE}		12		15	ns
t_{RAC}		50		60	ns
t_{RAD}	7		10		ns
t_{RAH}	7		8		ns
t_{RCD}	9		12		ns
t_{RCH}	2		2		ns
t_{RCS}	2		2		ns
t_{WHZ}	2	17	2	20	ns
t_{WPZ}	10		10		ns

RAS#-ONLY REFRESH CYCLE ³⁴



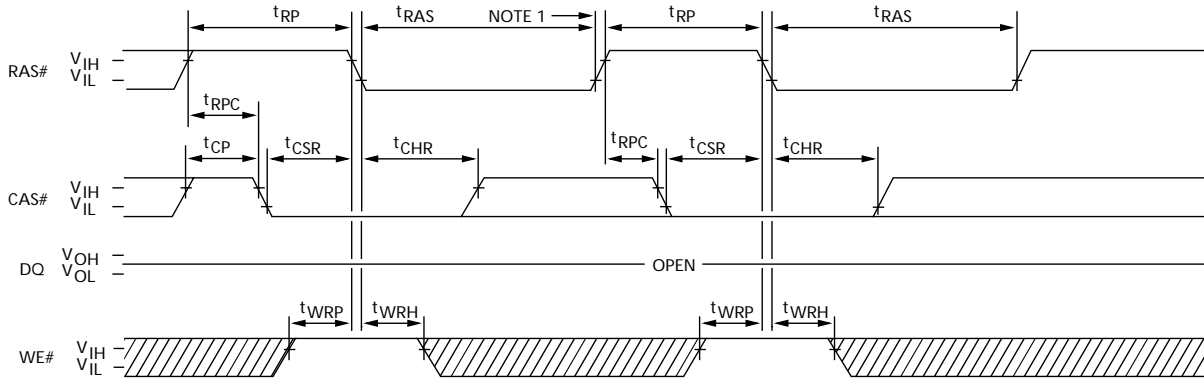
FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{ASR}	5		5		ns
t _{CRP}	10		10		ns
t _{CSR}	7		7		ns
t _{RAH}	7		8		ns
t _{RAS}	50	10,000	60	10,000	ns

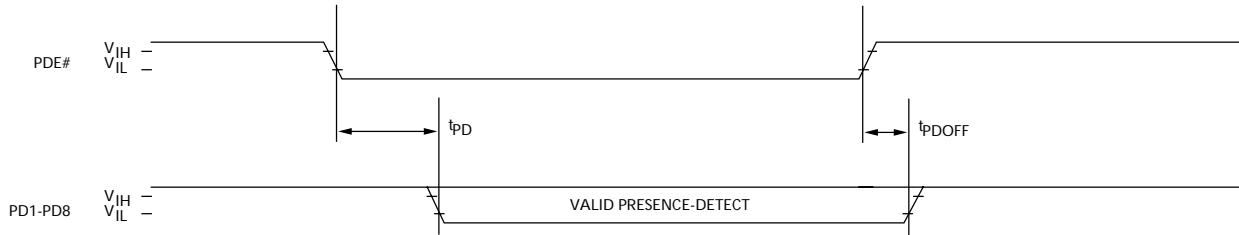
SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{RC} (FPM)	-		110		ns
t _{RC} (EDO)	84		104		ns
t _{RP}	30		40		ns
t _{RPC} (FPM)	-		0		ns
t _{RPC} (EDO)	5		5		ns

*EDO version only

CBR REFRESH CYCLE ³⁴
(Addresses, OE# = DON'T CARE)



PRESENCE-DETECT READ CYCLE ³⁴



DON'T CARE
 UNDEFINED

**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

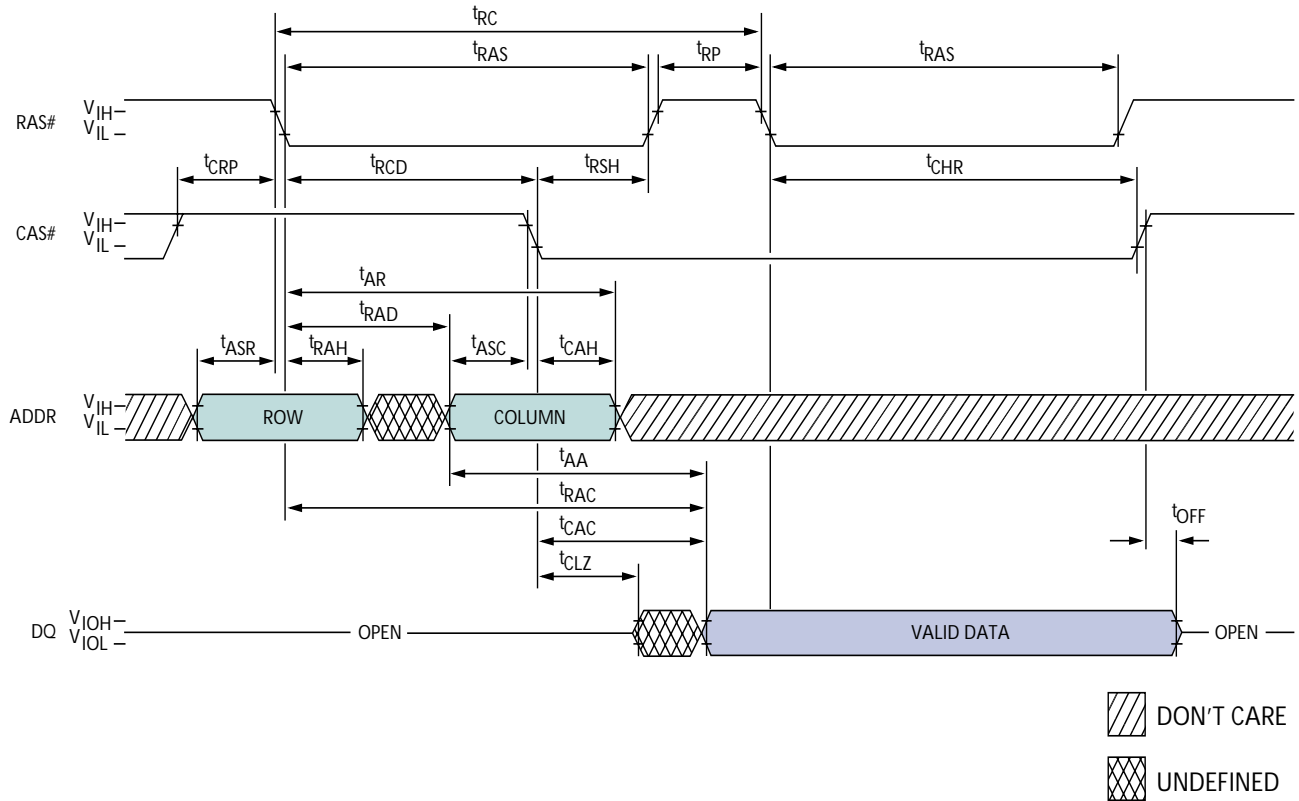
SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{CHR}	6		8		ns
t_{CP}	8		10		ns
t_{CSR}	7		7		ns
t_{PD}		10		10	ns
t_{PDOFF}	2		2		ns
t_{RAS}	50	10,000	60	10,000	ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RP}	30		40		ns
t_{RPC} (FPM)	-		0		ns
t_{RPC} (EDO)	5		5		ns
t_{WRH}	6		8		ns
t_{WRP}	10		12		ns

*EDO version only

NOTE: 1. PD pins must be pulled HIGH at next level of assembly.

HIDDEN REFRESH CYCLE ^{20, 34}
(WE# = HIGH; OE# = LOW)



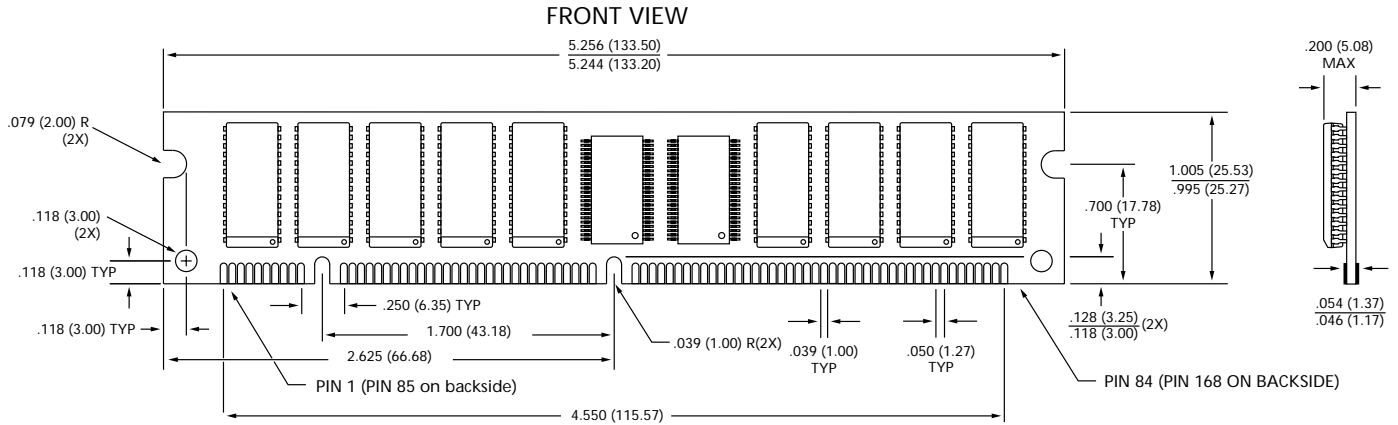
**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		30		35	ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCHR	6		8		ns
tCLZ (FPM)	-		5		ns
tCLZ (EDO)	2		2		ns
tCRP	10		10		ns
tOD (FPM)	-	-	3	15	ns
tOD (EDO)	0	12	0	15	ns
tOE		12		15	ns

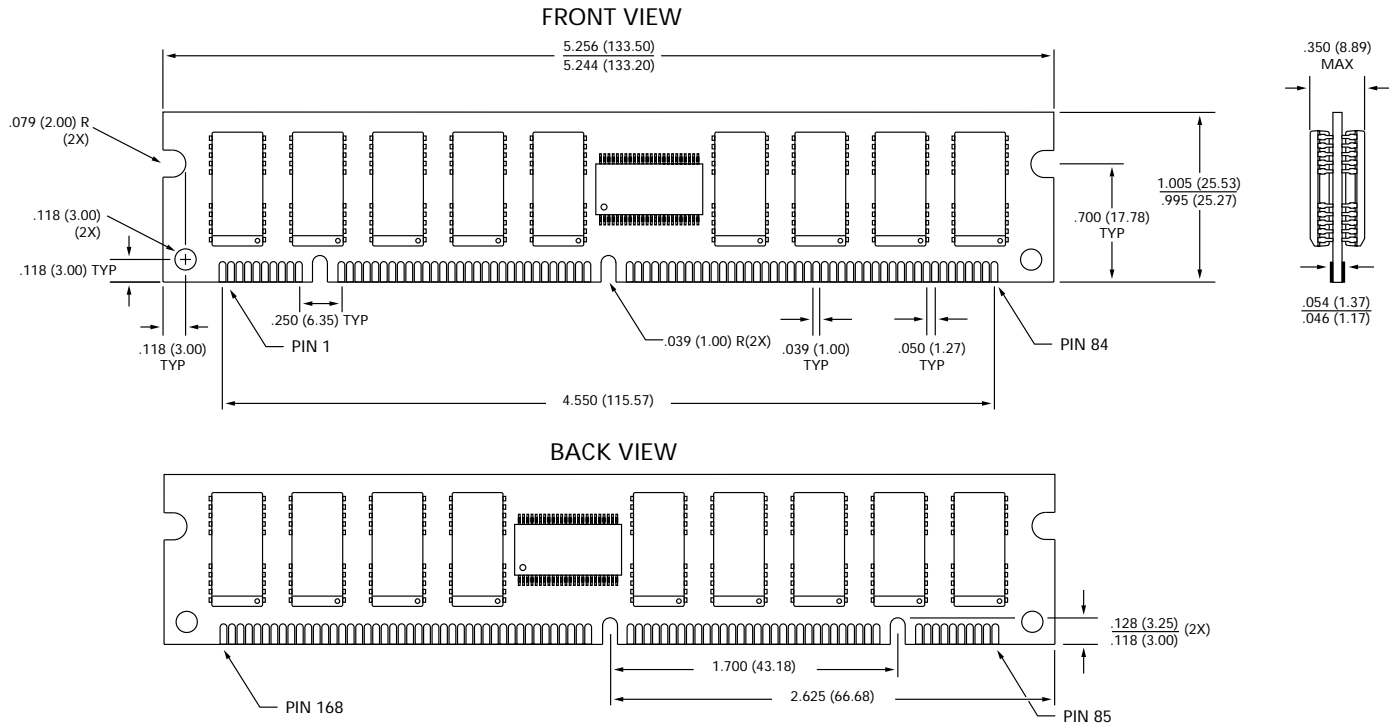
SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
tOFF (FPM)	-	-	5	20	ns
tOFF (EDO)	2	17	2	20	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD (FPM)	-		13		ns
tRAD (EDO)	7		10		ns
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns
tRCD (FPM)	-		18		ns
tRCD (EDO)	9		12		ns
tRP	30		40		ns
tRSH	18		20		ns

*EDO version only

168-PIN DIMM
DF-8 (16MB)



168-PIN DIMM
DF-7 (32MB)



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

OBSOLETE



**2, 4 MEG x 72
BUFFERED DRAM DIMMs**



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