

DDR SDRAM VLP RDIMM

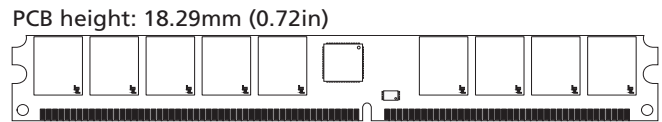
MT18VDVF12872D – 1GB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 184-pin, very low profile registered dual in-line memory module (VLP RDIMM)
- Fast data transfer rates: PC2700 or PC3200
- 1GB (128 Meg x 72)
- Supports ECC error detection and correction
- VDD = VDDQ = +2.5V
(-40B: VDD = VDDQ = +2.6V)
- VDDSPD = +2.3V to +3.6V
- 2.5V I/O (SSTL_2-compatible)
- Internal, pipelined, double data rate (DDR) 2n-prefetch architecture
- Bidirectional data strobe (DQS) transmitted/received with data—that is, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Multiple internal device banks for concurrent operation
- Dual rank
- Selectable burst lengths (BL) 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes: 7.8125µs maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable CAS latency (CL) for maximum compatibility
- Gold edge contacts

Figure 1: 184-Pin VLP RDIMM (MO-206)



Options

- Operating temperature¹
 - Commercial (0°C ≤ T_A ≤ +70°C) None
 - Industrial (-40°C ≤ T_A ≤ +85°C) I
- Package
 - 184-pin DIMM (standard) G
 - 184-pin DIMM (Pb-free) Y
- Memory clock, speed, CAS latency²
 - 5.0ns (200 MHz), 400 MT/s, CL = 3.0 -40B
 - 6.0ns (166 MHz), 333 MT/s, CL = 2.5 -335

Marking

Notes: 1. Contact Micron for industrial temperature module offerings.
2. CL = CAS (READ) latency; registered mode adds one clock cycle to CL.

Table 1: Key Timing Parameters

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) | | | t _{RCD} (ns) | t _{RP} (ns) | t _{RC} (ns) |
|-------------|-----------------------|------------------|----------|--------|-----------------------|----------------------|----------------------|
| | | CL = 3 | CL = 2.5 | CL = 2 | | | |
| -40B | PC3200 | 400 | 333 | 266 | 15 | 15 | 55 |
| -335 | PC2700 | – | 333 | 266 | 15 | 15 | 60 |

Table 2: Addressing

| Parameter | 1GB |
|----------------------|--------------------|
| Refresh count | 8K |
| Row address | 8K (A0–A12) |
| Device bank address | 4 (BA0, BA1) |
| Device configuration | 512Mb (64 Meg x 8) |
| Column address | 2K (A0–A9, A11) |
| Module rank address | 2 (S0#, S1#) |

Table 3: Part Numbers and Timing Parameters – 1GB Modules

 Base device: MT46V64M8,¹ 512Mb DDR SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL- ^t RCD- ^t RP) |
|--------------------------|----------------|---------------|------------------|----------------------------|---|
| MT18VDVF12872DG-40B__ | 1GB | 128 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT18VDVF12872DY-40B__ | 1GB | 128 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT18VDVF12872DG-335__ | 1GB | 128 Meg x 72 | 2.7 GB/s | 6.0ns/333 MT/s | 3-3-3 |
| MT18VDVF12872DY-335__ | 1GB | 128 Meg x 72 | 2.7 GB/s | 6.0ns/333 MT/s | 3-3-3 |

- Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes.
Example: MT18VDVF12872DY-335F1.

Pin Assignments and Descriptions

Table 4: Pin Assignments

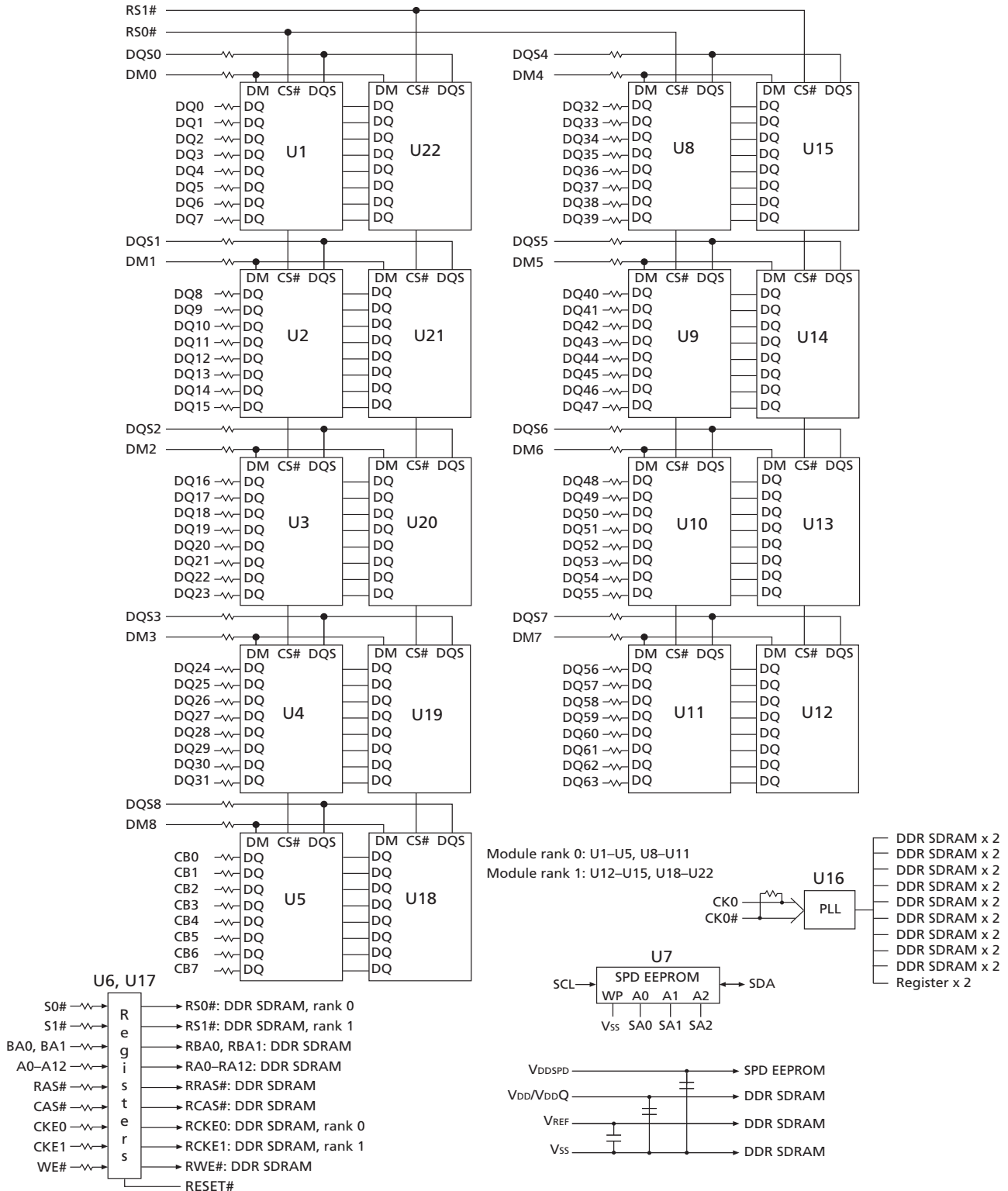
| 184-Pin DDR VLP RDIMM Front | | | | | | | | 184-Pin DDR VLP RDIMM Back | | | | | | | |
|-----------------------------|--------|-----|--------|-----|--------|-----|--------|----------------------------|--------|-----|--------|-----|--------|-----|--------|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | | |
| 1 | VREF | 24 | DQ17 | 47 | DQS8 | 70 | VDD | 93 | Vss | 116 | Vss | 139 | Vss | 162 | DQ47 |
| 2 | DQ0 | 25 | DQS2 | 48 | A0 | 71 | NC | 94 | DQ4 | 117 | DQ21 | 140 | DM8 | 163 | NC |
| 3 | Vss | 26 | Vss | 49 | CB2 | 72 | DQ48 | 95 | DQ5 | 118 | A11 | 141 | A10 | 164 | VDDQ |
| 4 | DQ1 | 27 | A9 | 50 | Vss | 73 | DQ49 | 96 | VDDQ | 119 | DM2 | 142 | CB6 | 165 | DQ52 |
| 5 | DQS0 | 28 | DQ18 | 51 | CB3 | 74 | Vss | 97 | DM0 | 120 | VDD | 143 | VDDQ | 166 | DQ53 |
| 6 | DQ2 | 29 | A7 | 52 | BA1 | 75 | NC | 98 | DQ6 | 121 | DQ22 | 144 | CB7 | 167 | NC |
| 7 | VDD | 30 | VDDQ | 53 | DQ32 | 76 | NC | 99 | DQ7 | 122 | A8 | 145 | Vss | 168 | VDD |
| 8 | DQ3 | 31 | DQ19 | 54 | VDDQ | 77 | VDDQ | 100 | Vss | 123 | DQ23 | 146 | DQ36 | 169 | DM6 |
| 9 | NC | 32 | A5 | 55 | DQ33 | 78 | DQS6 | 101 | NC | 124 | Vss | 147 | DQ37 | 170 | DQ54 |
| 10 | RESET# | 33 | DQ24 | 56 | DQS4 | 79 | DQ50 | 102 | NC | 125 | A6 | 148 | VDD | 171 | DQ55 |
| 11 | Vss | 34 | Vss | 57 | DQ34 | 80 | DQ51 | 103 | NC | 126 | DQ28 | 149 | DM4 | 172 | VDDQ |
| 12 | DQ8 | 35 | DQ25 | 58 | Vss | 81 | Vss | 104 | VDDQ | 127 | DQ29 | 150 | DQ38 | 173 | NC |
| 13 | DQ9 | 36 | DQS3 | 59 | BA0 | 82 | NC | 105 | DQ12 | 128 | VDDQ | 151 | DQ39 | 174 | DQ60 |
| 14 | DQS1 | 37 | A4 | 60 | DQ35 | 83 | DQ56 | 106 | DQ13 | 129 | DM3 | 152 | Vss | 175 | DQ61 |
| 15 | VDDQ | 38 | VDD | 61 | DQ40 | 84 | DQ57 | 107 | DM1 | 130 | A3 | 153 | DQ44 | 176 | Vss |
| 16 | NC | 39 | DQ26 | 62 | VDDQ | 85 | VDD | 108 | VDD | 131 | DQ30 | 154 | RAS# | 177 | DM7 |
| 17 | NC | 40 | DQ27 | 63 | WE# | 86 | DQS7 | 109 | DQ14 | 132 | Vss | 155 | DQ45 | 178 | DQ62 |
| 18 | Vss | 41 | A2 | 64 | DQ41 | 87 | DQ58 | 110 | DQ15 | 133 | DQ31 | 156 | VDDQ | 179 | DQ63 |
| 19 | DQ10 | 42 | Vss | 65 | CAS# | 88 | DQ59 | 111 | CKE1 | 134 | CB4 | 157 | S0# | 180 | VDDQ |
| 20 | DQ11 | 43 | A1 | 66 | Vss | 89 | Vss | 112 | VDDQ | 135 | CB5 | 158 | S1# | 181 | SA0 |
| 21 | CKE0 | 44 | CB0 | 67 | DQS5 | 90 | NC | 113 | NC | 136 | VDDQ | 159 | DM5 | 182 | SA1 |
| 22 | VDDQ | 45 | CB1 | 68 | DQ42 | 91 | SDA | 114 | DQ20 | 137 | CK0 | 160 | Vss | 183 | SA2 |
| 23 | DQ16 | 46 | VDD | 69 | DQ43 | 92 | SCL | 115 | A12 | 138 | CK0# | 161 | DQ46 | 184 | VDDSPD |

Table 5: Pin Descriptions

| Symbol | Type | Description |
|-----------------|--------|---|
| A0–A12 | Input | Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. |
| BA0, BA1 | Input | Bank address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. |
| CK0, CK0#, | Input | Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#. |
| CKE0, CKE1 | Input | Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates the internal clock, input buffers, and output drivers. |
| DM0–DM8 | Input | Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. |
| RESET# | Input | Reset: Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z. |
| S0#, S1# | Input | Chip selects: S# enables (registered LOW) and S# disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code. |
| SA0–SA2 | Input | Presence-detect address inputs: These pins are used to configure the presence-detect device. |
| SCL | Input | Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module. |
| WE#, CAS#, RAS# | Input | Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| CB0–CB7 | I/O | Check bits. |
| DQ0–DQ63 | I/O | Data input/output: Data bus. |
| DQS0–DQS8 | I/O | Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned with write data. Used to capture data. |
| SDA | I/O | Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module. |
| VDD/VDDQ | Supply | Power supply: +2.5V ±0.2V (-40B: +2.6V ±0.1V). |
| VDDSPD | Supply | Serial EEPROM positive power supply: +2.3V to +3.6V. |
| VREF | Supply | SSTL_2 reference voltage (VDD/2). |
| VSS | Supply | Ground. |
| NC | – | No connect: These pins are not connected on the module. |

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT18VDFV12872D is a high-speed CMOS, dynamic random access 1GB memory module organized in a x72 configuration. These modules use DDR SDRAM devices with four internal banks.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for DDR SDRAM modules effectively consists of a single $2n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL Operation

These DDR SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR SDRAM devices. The register(s) and PLL reduce address, command, control, and clock signal loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I²C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to Vss on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | |
|-----------|---|---|------|---------|---------|
| VDD/VDDQ | VDD/VDDQ supply voltage relative to Vss | -1.0 | +3.6 | V | |
| VIN, VOUT | Voltage on any pin relative to Vss | -0.5 | +3.2 | V | |
| II | Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$; VREF input $0V \leq V_{IN} \leq 1.35V$ (All other pins not under test = 0V) | Address inputs RAS#, CAS#, WE#, BA, S#, CKE | -5 | +5 | μA |
| | | CK, CK0 | -10 | +10 | |
| | | DM | -4 | +4 | |
| Ioz | Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQs are disabled | -10 | +10 | μA | |
| TA | DRAM ambient operating temperature ¹ | Commercial | 0 | +70 | °C |
| | | Industrial | -40 | +85 | °C |

Notes: 1. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 7.

Table 7: Module and Component Speed Grades

| Module Speed Grade | Component Speed Grade |
|--------------------|-----------------------|
| -40B | -5B |
| -335 | -6 |

IDD Specifications

Table 8: IDD Specifications and Conditions – 1GB

Values are shown for the MT46V64M8 DDR SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

| Parameter/Condition | Symbol | -40B | -335 | Units | |
|--|----------------------------------|--------------------|-------|-------|----|
| Operating one bank active-precharge current: $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | IDD0 ¹ | 1,440 | 1,215 | mA | |
| Operating one bank active-read-precharge current: BL = 2; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; IOUT = 0mA; Address and control inputs changing once per clock cycle | IDD1 ¹ | 1,710 | 1,485 | mA | |
| Precharge power-down standby current: All device banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW | IDD2P ² | 90 | 90 | mA | |
| Idle standby current: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK}(\text{MIN})$; CKE = HIGH; Address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS, and DM | IDD2F ² | 990 | 810 | mA | |
| Active power-down standby current: One device bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW | IDD3P ² | 810 | 630 | mA | |
| Active standby current: CS# = HIGH; CKE = HIGH; One device bank; Active-precharge; $t_{RC} = t_{RAS}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | IDD3N ² | 1,800 | 900 | mA | |
| Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; IOUT = 0mA | IDD4R ¹ | 1,755 | 1,530 | mA | |
| Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle | IDD4W ¹ | 1,800 | 1,620 | mA | |
| Auto refresh current | $t_{REFC} = t_{RFC}(\text{MIN})$ | IDD5 ² | 6,210 | 5,220 | mA |
| | $t_{REFC} = 7.8125\mu\text{s}$ | IDD5A ² | 198 | 180 | mA |
| Self refresh current: CKE \leq 0.2V | IDD6 ² | 90 | 90 | mA | |
| Operating bank interleave read current: Four device bank interleaving reads; BL = 4 with auto precharge; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs change only during active READ or WRITE commands | IDD7 ¹ | 4,095 | 3,690 | mA | |

- Notes:
1. Value calculated as one module rank in this operating condition; all other module ranks are in IDD2P (CKE LOW) mode.
 2. Value calculated reflects all module ranks in this operating condition.

Register and PLL Specifications

Table 9: Register Specifications
SSTV16859 devices or equivalent JESD82-4B

| Parameter | Symbol | Pins | Condition | Min | Max | Units |
|---|---------------------|---------------------------|---|----------------------------|----------------------------|-------|
| DC high-level input voltage | V _{IH(DC)} | Address, control, command | SSTL_25 | V _{REF(DC)} + 150 | – | mV |
| DC low-level input voltage | V _{IL(DC)} | Address, control, command | SSTL_25 | – | V _{REF(DC)} – 150 | mV |
| AC high-level input voltage | V _{IH(AC)} | Address, control, command | SSTL_25 | V _{REF(DC)} + 310 | V _{DD} | mV |
| AC low-level input voltage | V _{IL(AC)} | Address, control, command | SSTL_25 | – | V _{REF(DC)} – 310 | mV |
| Output high voltage | V _{OH} | Parity output | LVC MOS | V _{DD} – 0.2 | – | V |
| Output low voltage | V _{OL} | Parity output | LVC MOS | – | 0.2 | V |
| Input current | I _I | All pins | V _I = V _{DDQ} or V _{SSQ} | –5.0 | +5.0 | μA |
| Static standby | I _{DD} | All pins | RESET# = V _{SSQ} (I _O = 0) | – | 100 | μA |
| Static operating | I _{DD} | All pins | RESET# = V _{SSQ} ; V _I = V _{IH(AC)} or V _{IL(DC)} I _O = 0 | – | Varies by manufacturer | mA |
| Dynamic operating (clock tree) | I _{DDD} | n/a | RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _O = 0; CK and CK# switching 50 percent duty cycle | – | Varies by manufacturer | μA |
| Dynamic operating (per each input) | I _{DDD} | n/a | RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _O = 0; CK and CK# switching 50 percent duty cycle; One data input switching at ^t CK/2, 50 percent duty cycle | – | Varies by manufacturer | μA |
| Input capacitance (per device, per pin) | C _I | All inputs except RESET# | V _I = V _{REF} ±250mV; V _{DDQ} = 1.8V | 2.5 | 3.5 | pF |
| Input capacitance (per device, per pin) | C _I | RESET# | V _I = V _{DDQ} or V _{SSQ} | – | Varies by manufacturer | pF |

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC-standard JESD82.

Table 10: PLL Specifications
CVF857 device or equivalent JESD82-1A

| Parameter | Symbol | Pins | Condition | Min | Max | Units |
|---------------------------------------|---------------------|-----------------|--|-----------------------------|-----------------------------|-------|
| DC high-level input voltage | V _{IH} | RESET# | LVC MOS | 1.7 | V _{DDQ} + 0.3 | V |
| DC low-level input voltage | V _{IL} | RESET# | LVC MOS | -0.3 | 0.7 | V |
| Input voltage (limits) | V _{IN} | RESET#, CK, CK# | - | -0.3 | V _{DDQ} + 0.3 | V |
| Input differential-pair cross voltage | V _{IX} | CK, CK# | Differential input | (V _{DDQ} /2) - 0.2 | (V _{DDQ} /2) + 0.2 | V |
| Input differential voltage | V _{ID(DC)} | CK, CK# | Differential input | 0.36 | V _{DDQ} + 0.6 | V |
| Input differential voltage | V _{ID(AC)} | CK, CK# | Differential input | 0.7 | V _{DDQ} + 0.6 | V |
| Input current | I _I | RESET# | V _I = V _{DDQ} or V _{SSQ} | -10 | +10 | μA |
| | | CK, CK# | V _I = V _{DDQ} or V _{SSQ} | -10 | +10 | μA |
| Output disabled current | I _{ODL} | - | RESET# = V _{SSQ} ; V _I = V _{IH(AC)} or V _{IL(DC)} | 100 | - | μA |
| Static supply current | I _{DDPD} | - | CK = CK# = LOW | - | 200 | μA |
| Dynamic supply | I _{DD} | n/a | CK, CK# = 270 MHz, all outputs open (not connected to PCB) | - | 300 | mA |
| Input capacitance | C _I | Each input | V _I = V _{DDQ} or V _{SSQ} | 2.0 | 3.5 | pF |

Table 11: PLL Clock Driver Timing Requirements and Switching Characteristics

| Parameter | Symbol | Min | Max | Units |
|---|---------------------|-----|-------|-------|
| Stabilization time | t _L | - | 100 | μs |
| Input clock slew rate | t _{slr(i)} | 1.0 | 4.0 | V/ns |
| SSC modulation frequency | - | 30 | 50 | kHz |
| SSC clock input frequency deviation | - | 0 | -0.50 | % |
| PLL loop bandwidth (-3dB from unity gain) | - | 2.0 | - | MHz |

- Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC-standard JESD82-1A.

Serial Presence-Detect

Table 12: Serial Presence-Detect EEPROM DC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units |
|--|-----------------|--------------|--------------|-------|
| Supply voltage | VDDSPD | 2.3 | 3.6 | V |
| Input high voltage: Logic 1; All inputs | V _{IH} | VDDSPD × 0.7 | VDDSPD + 0.5 | V |
| Input low voltage: Logic 0; All inputs | V _{IL} | -1.0 | VDDSPD × 0.3 | V |
| Output low voltage: I _{OUT} = 3mA | V _{OL} | - | 0.4 | V |
| Input leakage current: V _{IN} = GND to V _{DD} | I _{LI} | - | 10 | μA |
| Output leakage current: V _{OUT} = GND to V _{DD} | I _{LO} | - | 10 | μA |
| Standby current: SCL = SDA = V _{DD} - 0.3V; All other inputs = V _{SS} or V _{DD} | I _{SB} | - | 30 | μA |
| Power supply current: SCL clock frequency = 100 kHz | I _{CC} | - | 2.0 | mA |

Table 13: Serial Presence-Detect EEPROM AC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units | Notes |
|---|---------------------|-----|-----|-------|-------|
| SCL LOW to SDA data-out valid | t ^{AA} | 0.2 | 0.9 | μs | 1 |
| Time the bus must be free before a new transition can start | t ^{BUF} | 1.3 | - | μs | |
| Data-out hold time | t ^{DH} | 200 | - | ns | |
| SDA and SCL fall time | t ^F | - | 300 | ns | 2 |
| Data-in hold time | t ^{HD:DAT} | 0 | - | μs | |
| Start condition hold time | t ^{HD:STA} | 0.6 | - | μs | |
| Clock HIGH period | t ^{HIGH} | 0.6 | - | μs | |
| Noise suppression time constant at SCL, SDA inputs | t ^I | - | 50 | ns | |
| Clock LOW period | t ^{LOW} | 1.3 | - | μs | |
| SDA and SCL rise time | t ^R | - | 0.3 | μs | 2 |
| SCL clock frequency | f ^{SCL} | - | 400 | kHz | |
| Data-in setup time | t ^{SU:DAT} | 100 | - | ns | |
| Start condition setup time | t ^{SU:STA} | 0.6 | - | μs | 3 |
| Stop condition setup time | t ^{SU:STO} | 0.6 | - | μs | |
| WRITE cycle time | t ^{WRC} | - | 10 | ms | 4 |

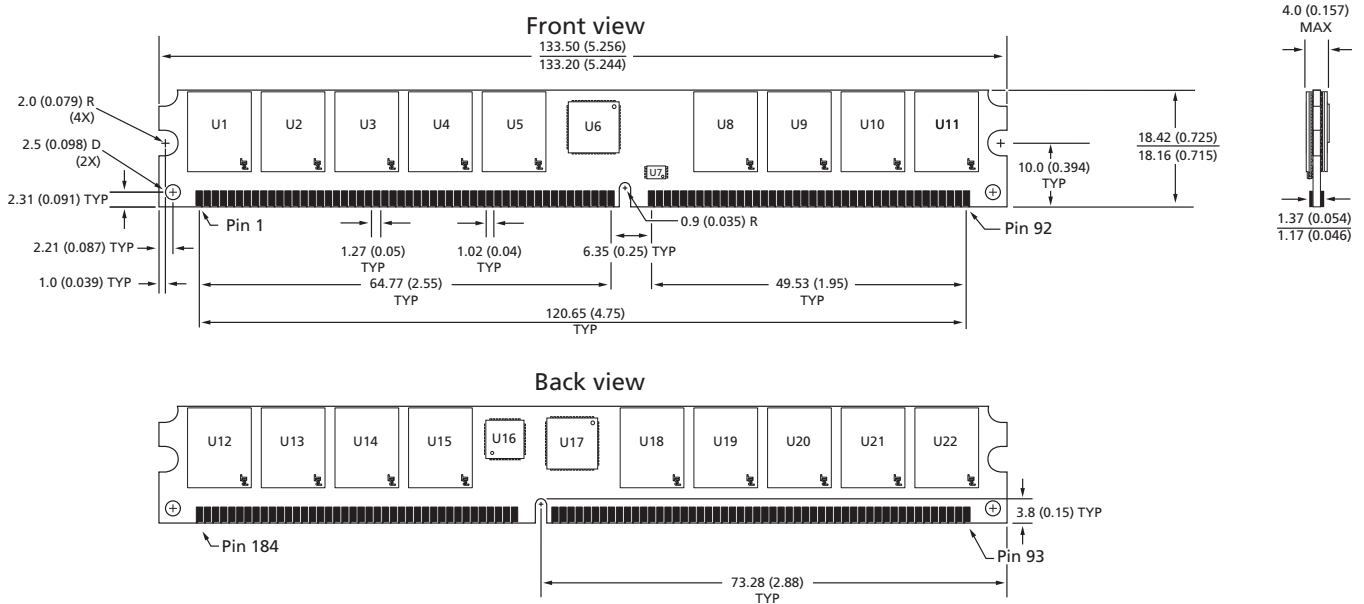
- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
 2. This parameter is sampled.
 3. For a restart condition or following a WRITE cycle.
 4. The SPD EEPROM WRITE cycle time (t^{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page:
www.micron.com/SPD.

Module Dimensions

Figure 3: 184-Pin DDR VLP RDIMM



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.



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