DDR2 SDRAM RDIMM

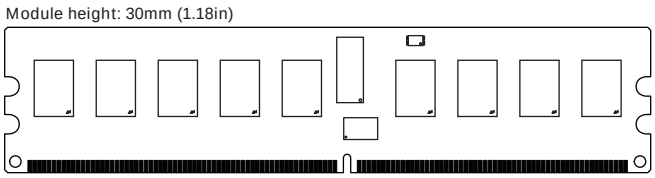
MT18HTF25672PDZ – 2GB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 240-pin, registered dual in-line memory module
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- 2GB (256 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD} = V_{DDQ} = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Dual rank
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Halogen-free

Figure 1: 240-Pin DIMM (MO-237 R/C G)



Options	Marking
• Parity	P
• Operating temperature[1]	
– Commercial ($0°C \le T_A \le +70°C$)	None
– Industrial ($-40°C \le T_A \le +85°C$)	T
• Package	
– 240-pin DIMM (halogen-free)	Z
• Frequency/CAS latency[2]	
– 2.5ns @ CL = 5 (DDR2-800)	-80E
– 2.5ns @ CL = 6 (DDR2-800)	-800
– 3.0ns @ CL = 5 (DDR2-667)	-667

Notes: 1. Contact Micron for industrial temperature module offerings.
2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	800	800	533	400	12.5	12.5	55
-800	PC2-6400	800	667	533	400	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Table 2: Addressing

	2GB
Refresh count	8K
Row address	16K A[13:0]
Device bank address	8 BA[2:0]
Device configuration	1Gb (128 Meg x 8)
Column address	1K A[9:0]
Module rank address	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT47H128M8[1], 1Gb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL-^{t}RCD-^{t}RP)
MT18HTF25672PDZ-80E__	2GB	256 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT18HTF25672PTZ-80E__	2GB	256 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT18HTF25672PDZ-800__	2GB	256 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT18HTF25672PTZ-800__	2GB	256 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT18HTF25672PDZ-667__	2GB	256 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT18HTF25672PTZ-667__	2GB	256 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5

Notes: 1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18HTF25672PDZ-667H1.

Pin Assignments and Descriptions

Table 4: Pin Assignments

240-Pin RDIMM Front								240-Pin RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REF}	31	DQ19	61	A4	91	V_{SS}	121	V_{SS}	151	V_{SS}	181	V_{DDQ}	211	DM5/ DQS14
2	V_{SS}	32	V_{SS}	62	V_{DDQ}	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NF/ DQS14#
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	V_{SS}
4	DQ1	34	DQ25	64	V_{DD}	94	V_{SS}	124	V_{SS}	154	V_{SS}	184	V_{DD}	214	DQ46
5	V_{SS}	35	V_{SS}	65	V_{SS}	95	DQ42	125	DM0/ DQS9	155	DM3/ DQS12	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	V_{SS}	96	DQ43	126	NF/ DQS9#	156	NF/ DQS12#	186	CK0#	216	V_{SS}
7	DQS0	37	DQS3	67	V_{DD}	97	V_{SS}	127	V_{SS}	157	V_{SS}	187	V_{DD}	217	DQ52
8	V_{SS}	38	V_{SS}	68	Par_In	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	V_{DD}	99	DQ49	129	DQ7	159	DQ31	189	V_{DD}	219	V_{SS}
10	DQ3	40	DQ27	70	A10/AP	100	V_{SS}	130	V_{SS}	160	V_{SS}	190	BA1	220	NC
11	V_{SS}	41	V_{SS}	71	BA0	101	SA2	131	DQ12	161	CB4	191	V_{DDQ}	221	NC
12	DQ8	42	CB0	72	V_{DDQ}	102	NC	132	DQ13	162	CB5	192	RAS#	222	V_{SS}
13	DQ9	43	CB1	73	WE#	103	V_{SS}	133	V_{SS}	163	V_{SS}	193	S0#	223	DM6/ DQS15
14	V_{SS}	44	V_{SS}	74	CAS#	104	DQS6#	134	DM1/ DQS10	164	DM8/ DQS17	194	V_{DDQ}	224	NF/ DQS15#
15	DQS1#	45	DQS8#	75	V_{DDQ}	105	DQS6	135	NF/ DQS10#	165	NF/ DQS17#	195	ODT0	225	V_{SS}
16	DQS1	46	DQS8	76	S1#	106	V_{SS}	136	V_{SS}	166	V_{SS}	196	A13	226	DQ54
17	V_{SS}	47	V_{SS}	77	ODT1	107	DQ50	137	NC	167	CB6	197	V_{DD}	227	DQ55
18	RESET#	48	CB2	78	V_{DDQ}	108	DQ51	138	NC	168	CB7	198	V_{SS}	228	V_{SS}
19	NC	49	CB3	79	V_{SS}	109	V_{SS}	139	V_{SS}	169	V_{SS}	199	DQ36	229	DQ60
20	V_{SS}	50	V_{SS}	80	DQ32	110	DQ56	140	DQ14	170	V_{DDQ}	200	DQ37	230	DQ61
21	DQ10	51	V_{DDQ}	81	DQ33	111	DQ57	141	DQ15	171	CKE1	201	V_{SS}	231	V_{SS}
22	DQ11	52	CKE0	82	V_{SS}	112	V_{SS}	142	V_{SS}	172	V_{DD}	202	DM4/ DQS13	232	DM7/ DQS16
23	V_{SS}	53	V_{DD}	83	DQS4#	113	DQS7#	143	DQ20	173	A15	203	NF/ DQS13#	233	NF/ DQS16#
24	DQ16	54	BA2	84	DQS4	114	DQS7	144	DQ21	174	A14	204	V_{SS}	234	V_{SS}
25	DQ17	55	Err_Out	85	V_{SS}	115	V_{SS}	145	V_{SS}	175	V_{DDQ}	205	DQ38	235	DQ62
26	V_{SS}	56	V_{DDQ}	86	DQ34	116	DQ58	146	DM2/ DQS11	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NF/ DQS11#	177	A9	207	V_{SS}	237	V_{SS}
28	DQS2	58	A7	88	V_{SS}	118	V_{SS}	148	V_{SS}	178	V_{DD}	208	DQ44	238	V_{DDSPD}
29	V_{SS}	59	V_{DD}	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	V_{SS}	240	SA1

Table 5: Pin Descriptions

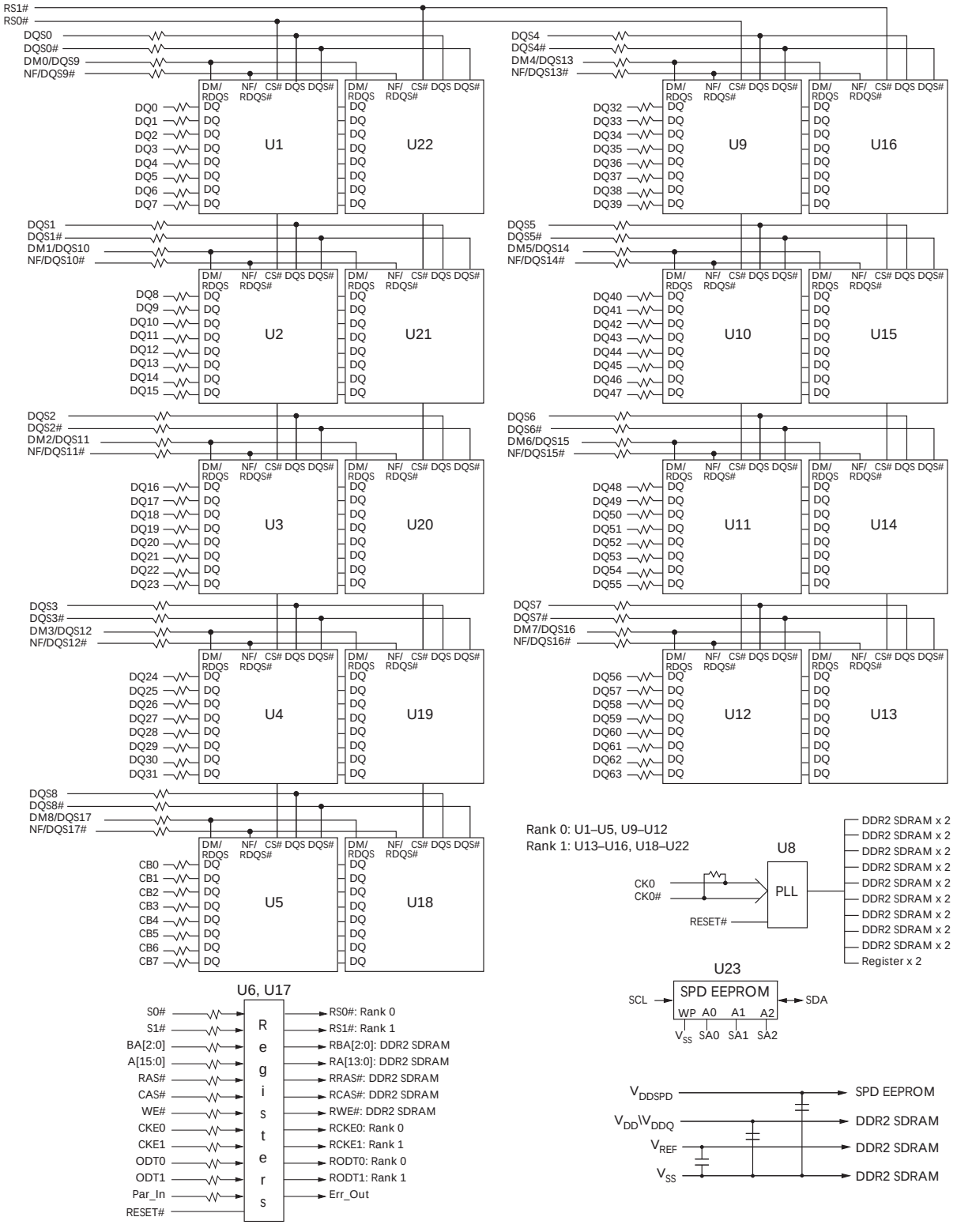
Symbol	Type	Description
A[15:0]	Input (SSTL_18)	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA[2/1:0]) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. A[13:0] (2GB). A[15:14] are connected for parity.
BA[2:0]	Input (SSTL_18)	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR, EMR1, EMR2, and EMR3) is loaded during the LOAD MODE command.
CK0, CK0#	Input (SSTL_18)	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE[1:0]	Input (SSTL_18)	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM.
DM[8:0] DQS[17:9] DQS#[17:9]	Input (SSTL_18)	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of DQS. Although the DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins. If RDQS is disabled, RDQS[17:9] become DM[8:0] and RDQS#[17:9] are no function.
ODT[1:0]	Input (SSTL_18)	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for the address, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input (SSTL_18)	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
S#[1:0]	Input (SSTL_18)	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Serial address inputs:** These pins are used to configure the SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for SPD EEPROM:** SCL is used to synchronize communication to and from the SPD EEPROM.
CB[7:0]	I/O	Check bits.
DQ[63:0]	I/O (SSTL_18)	**Data input/output:** Bidirectional data bus.
DQS[8:0], DQS#[8:0]	I/O (SSTL_18)	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the I^2C bus.
Err_Out	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
V_{DD}/V_{DDQ}	Supply	**Power supply:** 1.8V ±0.1V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**SPD EEPROM power supply:** +1.7V to +3.6V.
V_{REF}	Supply	**Reference voltage:** $V_{DD}/2$.
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Table 5: Pin Descriptions (continued)

Symbol	Type	Description
NF	–	**No function:** These pins are connected within the module but provide no functionality.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT18HTF25672PDZ DDR2 SDRAM module is a high-speed, CMOS, dynamic random-access 2GB memory module organized in a x72 configuration. This DDR2 SDRAM module use internally configured 8-bank 1Gb DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL EEPROM Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The register(s) and PLL reduce address, command, control, and clock signal loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Parity Operations

The registering clock driver can accept a parity bit from the system's memory controller, providing even parity for the control, command, and address bus. Parity errors are flagged on the Err_Out pin. Systems not using parity are expected to function without issue if Par_In and Err_Out are left as no connects to the system.

Serial Presence-Detect EEPROM Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection.

Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the DRAM devices on the module. This is a stress rating only, and functional operation of the module at these or any other conditions above those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}/V_{DDQ}	V_{DD} supply voltage relative to V_{SS}		–0.5	+2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	+2.3	V
I_I	Input leakage current; Any input $0V \le V_{IN} \le V_{DD}$; V_{REF} input $0V \le V_{IN} \le 0.95V$; (All other pins not under test = 0V)	Command/address RAS#, CAS#, WE#, S#, CKE, ODT, BA	–5	+5	µA
		CK, CK#	–250	+250	
		DM	–10	+10	
I_{OZ}	Output leakage current; $0V \le V_{OUT} \le V_{DDQ}$; DQs and ODT are disabled	DQ, DQS, DQS#	–10	+10	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level		–36	+36	µA
T_A	Module ambient operating temperature	Commercial	0	+70	°C
		Industrial	–40	+85	
T_C[1]	DDR2 SDRAM component case operating temperature[2]	Commercial	0	+85	°C
		Industrial	–40	+95	

Notes: 1. The refresh rate is required to double when $85°C < T_C \le 95°C$.
2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 7.

Table 7: Module and Component Speed Grades
DDR2 components may exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-5E

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 8: DDR2 I_{DD} Specifications and Conditions – 2GB

Values shown for MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E -800	-667	Units
Operating one bank active-precharge current: $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MIN (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD0}[1]	873	828	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MIN (I_{DD}), $^{t}RCD = {}^{t}RCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as $I_{DD}4W$		I_{DD1}[1]	1053	963	mA
Precharge power-down current: All device banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2P}[2]	126	126	mA
Precharge quiet standby current: All device banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2Q}[2]	900	720	mA
Precharge standby current: All device banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD2N}[2]	900	720	mA
Active power-down current: All device banks open; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	I_{DD3P}[2]	720	540	mA
	Slow PDN exit MR[12] = 1		180	180	mA
Active standby current: All device banks open; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MAX (I_{DD}), $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD3N}[2]	1080	990	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MAX (I_{DD}), $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4W}[2]	1503	1278	mA
Operating burst read current: All device banks open; Continuous burst reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MAX (I_{DD}), $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4R}[2]	1503	1278	mA
Burst refresh current: $^{t}CK = {}^{t}CK (I_{DD})$; REFRESH command at every $^{t}RFC (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD5}[2]	4230	3870	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		I_{DD6}[2]	126	126	mA
Operating bank interleave read current: All device banks interleaving reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = $^{t}RCD (I_{DD})$ - 1 x $^{t}CK (I_{DD})$; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RRD = {}^{t}RRD (I_{DD})$, $^{t}RCD = {}^{t}RCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		I_{DD7}[1]	3078	2583	mA

Notes: 1. Value calculated as one module rank in this operating condition, all other module ranks in I_{DD2P} (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Register and PLL Specifications

Table 9: Register Specifications
SSTU32866 devices or equivalent JESD82-16

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	$V_{IH(DC)}$	Address, control, command	SSTL_18	$V_{REF(DC)}$ +125	V_{DDQ} + 250	mV
DC low-level input voltage	$V_{IL(DC)}$	Address, control, command	SSTL_18	0	$V_{REF(DC)}$ - 125	mV
AC high-level input voltage	$V_{IH(AC)}$	Address, control, command	SSTL_18	$V_{REF(DC)}$ + 250	V_{DD}	mV
AC low-level input voltage	$V_{IL(AC)}$	Address, control, command	SSTL_18	0	$V_{REF(DC)}$ - 250	mV
Output high voltage	V_{OH}	Parity output	LVCMOS	1.2	–	V
Output low voltage	V_{OL}	Parity output	LVCMOS	–	0.5	V
Input current	I_I	All pins	$V_I = V_{DDQ}$ or V_{SSQ}	–5	5	µA
Static standby	I_{DD}	All pins	RESET# = V_{SSQ} (I_O = 0)	–	100	µA
Static operating	I_{DD}	All pins	RESET# = V_{SSQ}; $V_I = V_{IH(AC)}$ or $V_{IL(DC)}$ I_O = 0	–	40	mA
Dynamic operating (clock tree)	I_{DDD}	n/a	RESET# = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	µA
Dynamic operating (per each input)	I_{DDD}	n/a	RESET# = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle; One data input switching at $^tCK/2$, 50% duty cycle	–	Varies by manufacturer	µA
Input capacitance (per device, per pin)	C_I	All inputs except RESET#	$V_I = V_{REF}$ ±250mV; V_{DDQ} = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)	C_I	RESET#	$V_I = V_{DDQ}$ or V_{SSQ}	–	Varies by manufacturer	pF

Note: Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC standard JESD82.

Table 10: PLL Specifications
CU877 device or equivalent JESD82-8.01

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V_{IH}	RESET#	LVCMOS	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	RESET#	LVCMOS	–	0.35 × V_{DD}	V
Input voltage (limits)	V_{IN}	RESET#, CK, CK#		–0.3	V_{DDQ} + 0.3	V
DC high-level input voltage	V_{IH}	CK, CK#	Differential input	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	CK, CK#	Differential input	–	0.35 × V_{DD}	V
Input differential-pair cross voltage	V_{IX}	CK, CK#	Differential input	(V_{DDQ}/2) - 0.15	(V_{DDQ}/2) + 0.15	V
Input differential voltage	$V_{ID(DC)}$	CK, CK#	Differential input	0.3	V_{DDQ} + 0.4	V
Input differential voltage	$V_{ID(AC)}$	CK, CK#	Differential input	0.6	V_{DDQ} + 0.4	V
Input current	I_I	RESET#	V_I = V_{DDQ} or V_{SSQ}	–10	10	µA
		CK, CK#	V_I = V_{DDQ} or V_{SSQ}	–250	250	µA
Output disabled current	I_{ODL}		RESET# = V_{SSQ}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$	100	–	µA
Static supply current	I_{DDLD}		CK = CK# = LOW	–	500	µA
Dynamic supply	I_{DD}	n/a	CK, CK# = 270 MHz, all outputs open (not connected to PCB)	–	300	mA
Input capacitance	C_{IN}	Each input	V_I = V_{DDQ} or V_{SSQ}	2	3	pF

Table 11: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	^tL	–	15	µs
Input clock slew rate	^tLS_I	1.0	4	V/ns
SSC modulation frequency		30	33	kHz
SSC clock input frequency deviation		0.0	–0.50	%
PLL loop bandwidth (–3dB from unity gain)		2.0	–	MHz

Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC standard JESD82.

Serial Presence-Detect

Table 12: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 kHz	I_{CCR}	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I_{CCW}	2	3	mA

Table 13: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	^{t}DH	200	–	ns	
SDA and SCL fall time	^{t}F	–	300	ns	2
Data-in hold time	$^{t}HD:DAT$	0	–	µs	
Start condition hold time	$^{t}HD:STA$	0.6	–	µs	
Clock HIGH period	$^{t}HIGH$	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I	–	50	ns	
Clock LOW period	^{t}LOW	1.3	–	µs	
SDA and SCL rise time	^{t}R	–	0.3	µs	2
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	$^{t}SU:DAT$	100	–	ns	
Start condition setup time	$^{t}SU:STA$	0.6	–	µs	3
Stop condition setup time	$^{t}SU:STO$	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	10	ms	4

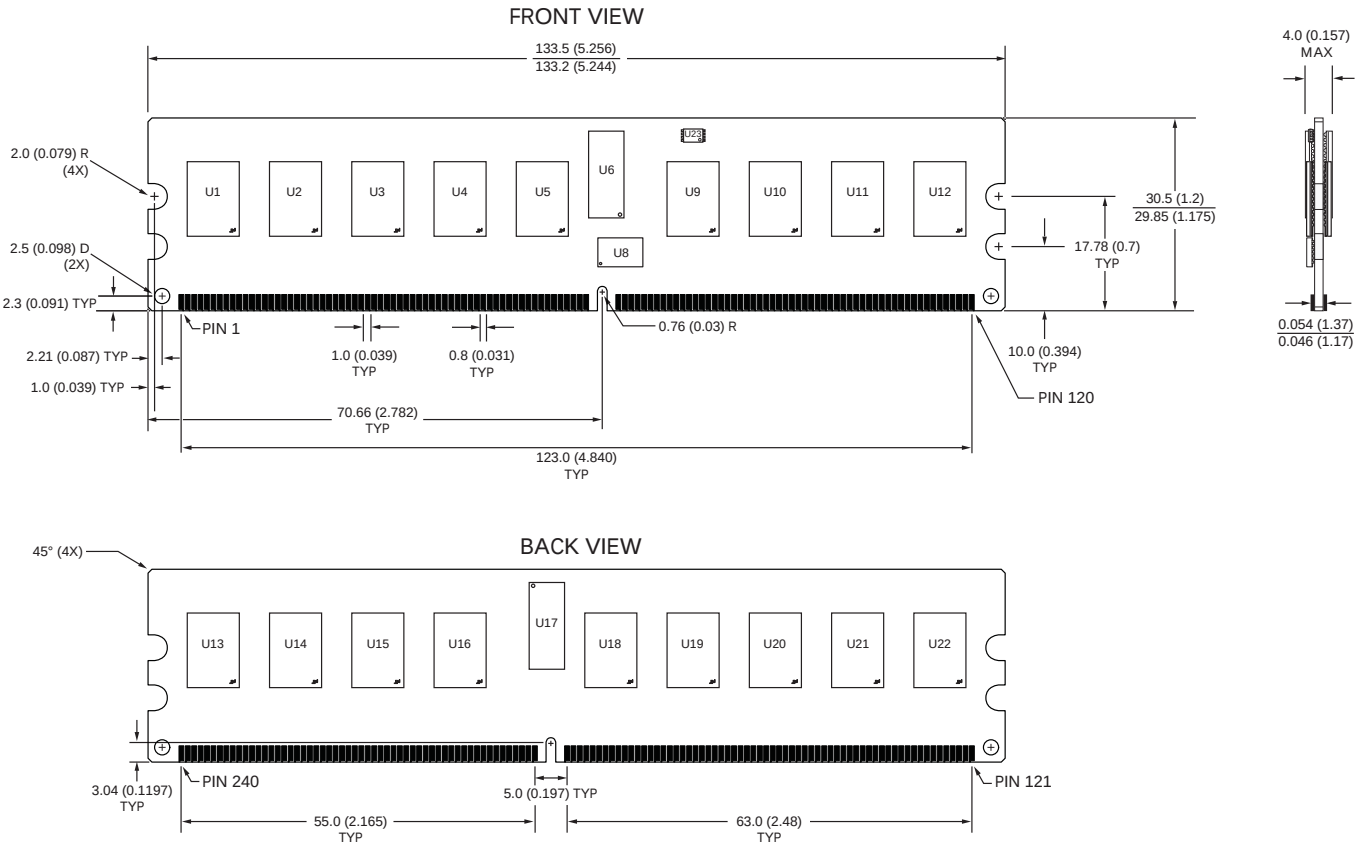
Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 3: 240-Pin DDR2 DIMM



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.

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