

# DATA SHEET

## **SAA4700T** VPS dataline processor

Preliminary specification  
File under Integrated Circuits, IC02

March 1991

## VPS dataline processor

## SAA4700T



## FEATURES

- Adaptive sync slicer with buffered composite sync output VCS
- Adaptive data slicer
- Data rate clock regenerator
- Field selection and line 16 decoding
- Startcode and biphase check
- Data valid output
- Storage of data line information in a 40 bit register bank
- I<sup>2</sup>C-bus transmission

## GENERAL DESCRIPTION

The SAA4700T is a bipolar integrated circuit designed for use in dataline receivers and incorporates a dataline slicer and decoder. The slicer extracts the dataline signal from the video signal and regenerates the data clock. It also provides signals for the decoder in order to decode the binary data that is transmitted in line 16 of every first field of the composite video signal (video programming signal and video recording programming by Teletext, VPS and VPT systems). The decoded information out of words 5 and 11 to 14 is accessed via the built-in I<sup>2</sup>C-bus interface. This information then can be used for programming a video cassette recorder in order to start and stop a recording of a television program at the correct aligned time, regardless of a delay or extension in the transmission time of the required program.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>P</sub>	supply voltage (pins 17 and 18)	4.5	5	5.5	V
I <sub>P</sub>	total supply current	–	18	23	mA
V <sub>i CVBS</sub>	CVBS input signal sync-to-white (peak-to-peak value)	0.5	1	1.4	V
T <sub>amb</sub>	operating ambient temperature	0	–	+70	°C

## ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA4700T	20	mini-pack	plastic	SOT163A <sup>(1)</sup>

## Note

1. SOT163-1; 1996 November 13.

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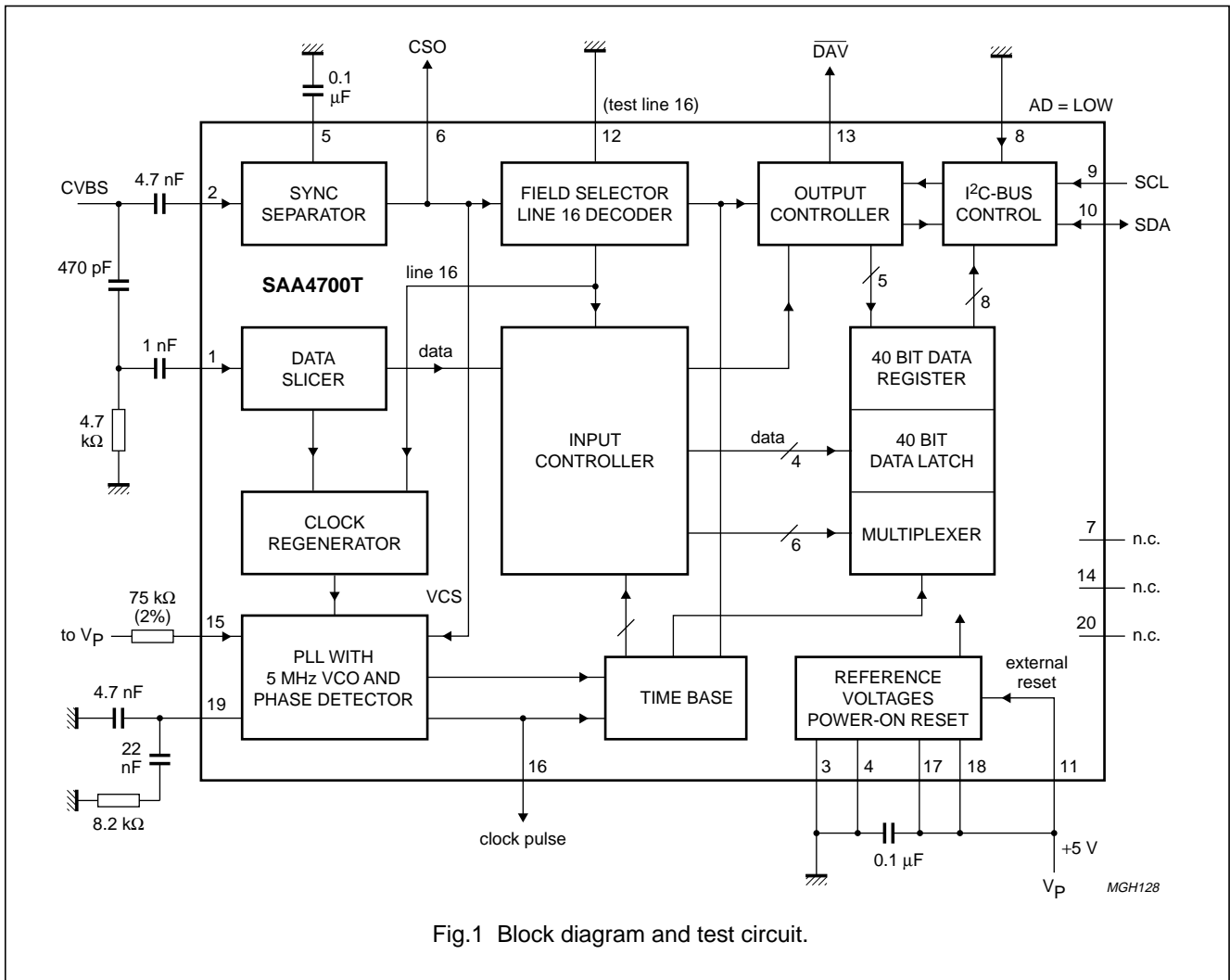


Fig.1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

Dataline 16

The information in dataline 16 consists of fifteen 8-bit words; the total information content is shown in Table 1; and the organization of transmitted bytes is shown in Table 2.

Out of the fifteen possible 8-bit words the SAA4700T extracts words 5 and 11 to 14. The contents of these words can be read via the built-in I2C-bus interface. The circuit is fully transparent, thus each bit is transferred without modification with only the sequence of words being changed. Words 11 to 14 are transmitted first followed by word 5.

By evaluating the sliced sync signal the circuit can identify the beginning of dataline 16 in the first field. The dataline decoder stage releases the start code detector. When a

correct start code is detected (for timing of start code detection see Fig.3) words 5 and 11 to 14 are decoded, checked for biphas errors and stored in a register bank. If no biphas error has occurred, the contents of the register bank are transferred to a second register bank by the data valid control signal. If the system has been addressed, this transfer will be delayed until the next start or stop condition of the I2C-bus has been received.

The last bit of correct information on the dataline remains available until it is read via the I2C-bus. Once the stored information has been read it is considered to be no longer valid and the internal new data flag is reset. Subsequently, if the circuit is addressed, the only VPS data that will be sent back is "FFF to F". The same conditions apply after power-up when no data can be read out. New data is available after reception of another error-free dataline 16.

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## PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	video signal input (CVBS from TV)
SYNC	2	sync amplitude input (CVBS from TV)
GND1	3	analog ground (0 V)
GND2	4	digital ground (0 V)
C <sub>black</sub>	5	capacitor for black level
CSO	6	composite sync output
n.c.	7	not connected
AD	8	address set input
SCL	9	I <sup>2</sup> C-bus clock line
SDA	10	I <sup>2</sup> C-bus data line
$\overline{RS}$	11	reset input active LOW
TP	12	test point for line 16 decoder
$\overline{DAV}$	13	data available output active LOW
n.c.	14	not connected
R <sub>osc</sub>	15	oscillator resistor for frequency adjustment
CP	16	test point clock pulse
V <sub>P1</sub>	17	+5 V supply voltage (digital part)
V <sub>P2</sub>	18	+5 V supply voltage (analog part)
C <sub>ph</sub>	19	capacitor of phase detector
n.c.	20	not connected

## External reset

The circuit provides an internal power-on reset. When using this facility pin 11 should be connected to V<sub>P</sub> or, if external reset (RESET = LOW) is to be used pin 11 should be prepared by connecting pin 11 via a 10 k $\Omega$  pull-up resistor to V<sub>P</sub>.

Reset forces the following:

- I<sup>2</sup>C-bus not to acknowledge
- $\overline{DAV}$  output to go HIGH (pin 13)
- I<sup>2</sup>C-bus transfer register to "FFF"

## PIN CONFIGURATION

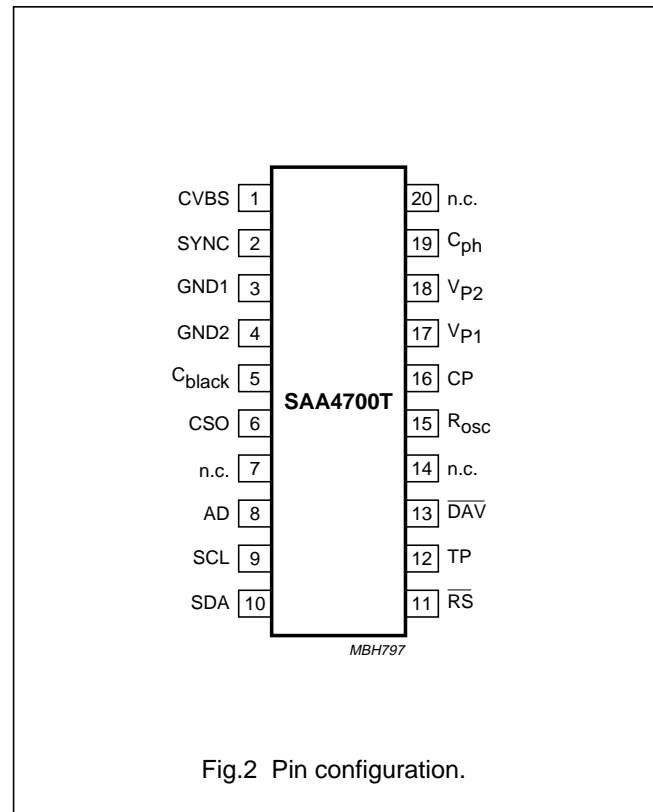


Fig.2 Pin configuration.

## CVBS input

The CVBS signal is applied to the sync separator (pin 2) via a decoupling capacitor and to the data slicer (pin 1) via an RC high-pass filter. To enable proper storage of the sync value in the decoupling capacitor, the sync generator output resistance should not exceed 1 k $\Omega$ .

## Black level

The capacitor connected to pin 5 stores the black level value for the adaptive sync slicer.

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**Composite sync output (CSO)**

A composite sync output signal for customer application is provided (pin 6).

 **$\overline{\text{DAV}}$  output**

The data available output pin 13 is set LOW after an error free data line 16 is received.  $\overline{\text{DAV}}$  returns to HIGH after the beginning of the next first field. If no valid data is available  $\overline{\text{DAV}}$  remains HIGH.

A short duration pulse of 1  $\mu\text{s}$  (Fig.5) is inserted at the beginning of dataline 16; it will ensure that a HIGH-to-LOW transmission occurs which can then be used for triggering.

**5 MHz VCO and phase detector**

The resistor connected between pin 15 and  $V_{P2}$  determines the current into the voltage controlled oscillator. The RC network connected to pin 19 acts as a low-pass filter for the phase detector.

**Power supply**

To prevent crosscoupling the circuit is provided with separate ground and supply pins for analog and digital parts (pins 3, 4, 17 and 18).

**Table 1** Information per word in dataline 16

WORD NUMBER	CONTENT
1	run in
2	start code
3	program source identification (binary coded)
4	program source identification (ASCII sequential)
5	sound and VTR control information
6	program/test picture identification
7	internal information exchange
8	address assignment of signal distribution
9	
10	messages/commands
11	VTR control / information
12	
13	
14	
15	reserve

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**Table 2** VTR control information of dataline 16

		VTR CONTROL INFORMATION																																						
Word number	5			11		12		13		14																														
Bit number	1 8 X X X X X X X X			0 7 X X X X X X X X		8 15 X X X X X X X X		16 23 X X X X X X X X		24 31 X X X X X X X X																														
Label binary	<table border="1"> <tr><td colspan="3">Word 5:</td></tr> <tr><td>Bit1</td><td>Bit2</td><td>Status</td></tr> <tr><td>0</td><td>0</td><td>2-channel</td></tr> <tr><td>0</td><td>1</td><td>Mono</td></tr> <tr><td>1</td><td>0</td><td>Stereo</td></tr> <tr><td>1</td><td>1</td><td>2-channel</td></tr> <tr><td colspan="3"> </td></tr> <tr><td>Bit3</td><td>Bit4</td><td>Status</td></tr> <tr><td>1</td><td>0</td><td>free</td></tr> <tr><td>0</td><td>1</td><td>free</td></tr> </table>			Word 5:			Bit1	Bit2	Status	0	0	2-channel	0	1	Mono	1	0	Stereo	1	1	2-channel				Bit3	Bit4	Status	1	0	free	0	1	free	AD (1)	Day	Month	Hour	Minute	Nation	Progr. source
Word 5:																																								
Bit1	Bit2	Status																																						
0	0	2-channel																																						
0	1	Mono																																						
1	0	Stereo																																						
1	1	2-channel																																						
Bit3	Bit4	Status																																						
1	0	free																																						
0	1	free																																						
				Special system code																																				
System status code				1 X 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1				NC...NC	PC...PC																															
Pause code				1 X 0 0 0 0 1 1 1 1 1 1 1 0 1 1 1 1 1				NC...NC	PC...PC																															
Interrupt code				1 X 0 0 0 0 1 1 1 1 1 1 1 0 1 1 1 1 1				NC...NC	PC...PC																															

**Note**

1. address range; NC = nation code; PC = program source code; X = 0 or 1 (bit)

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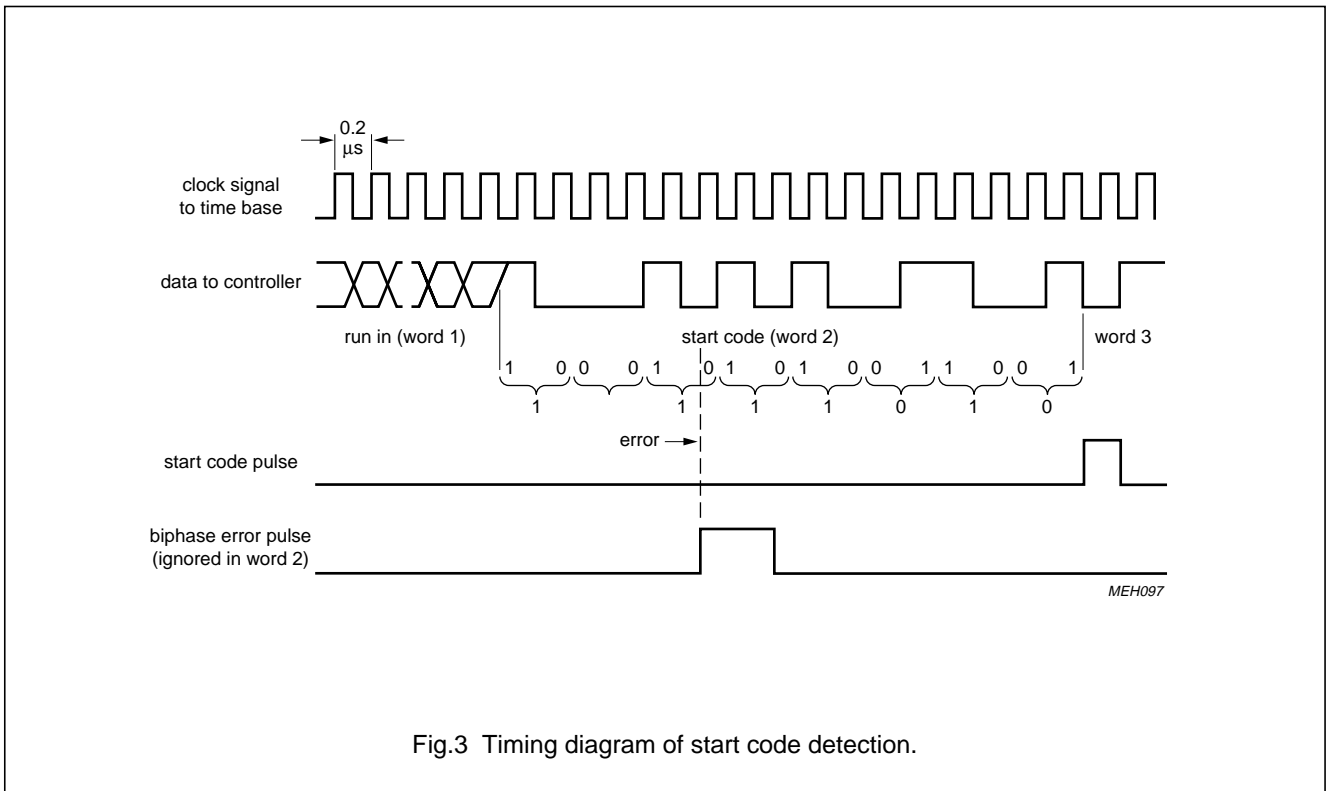


Fig.3 Timing diagram of start code detection.

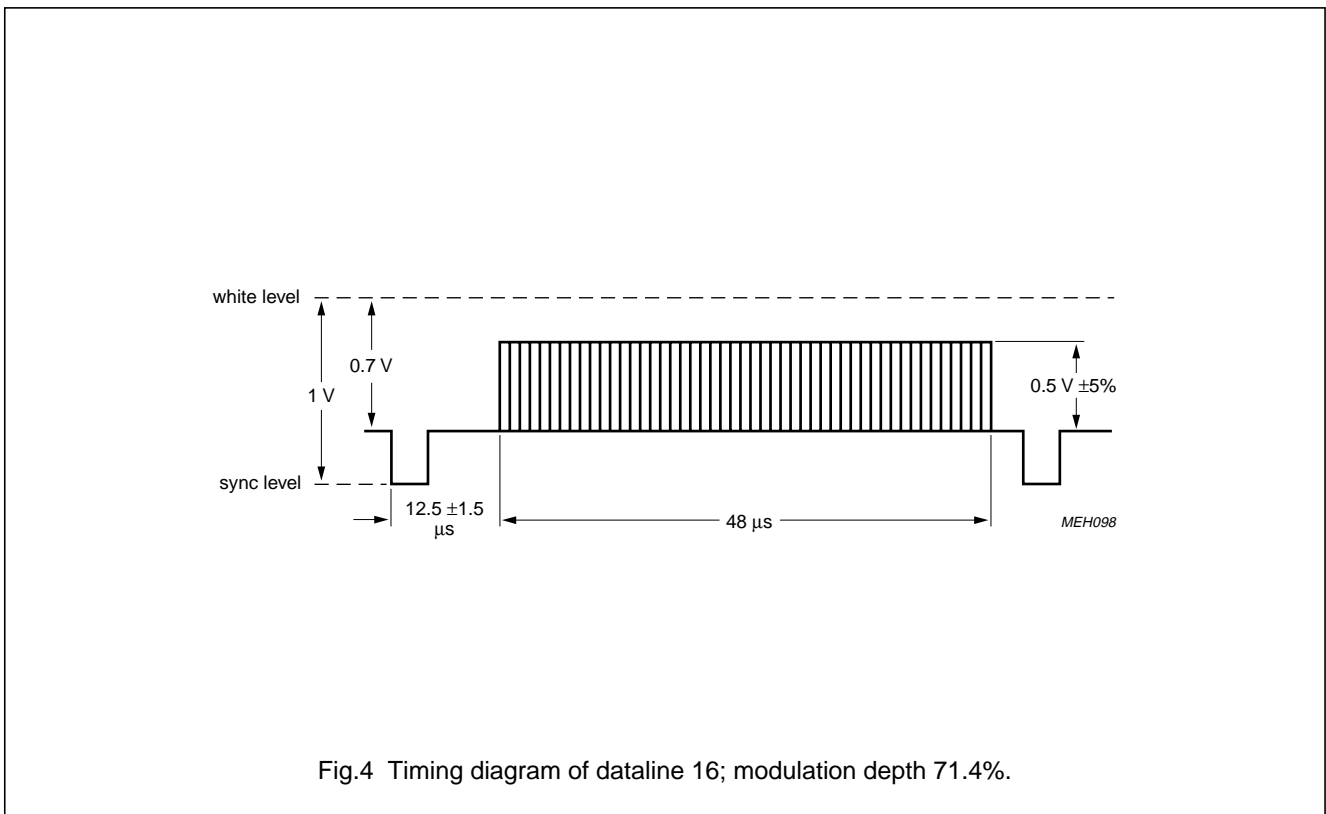


Fig.4 Timing diagram of dataline 16; modulation depth 71.4%.

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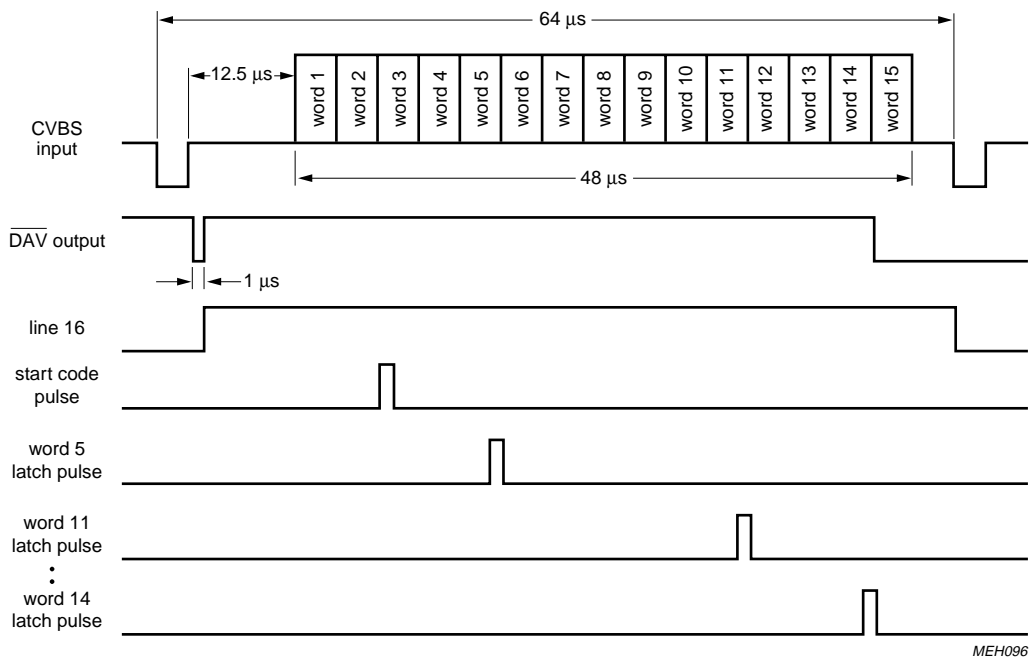


Fig.5 Timing diagram of the data available output and word latch pulses.



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**LIMITING VALUES**

In accordance with the Absolute Maximum System (IEC 134).

Ground pins 3 and 4 as well as supply pins 17 and 18 tied together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{P1}$	supply voltage (pin 17)	-0.5	6.0	V
$V_{P2}$	supply voltage (pin 18)	-0.5	6.0	V
$T_{stg}$	storage temperature range	-20	125	°C
$T_{amb}$	operating ambient temperature range	0	+70	°C

**THERMAL RESISTANCE**

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j-a}$	from junction to ambient in free air	–	130	K/W

**CHARACTERISTICS**

$V_{P1} = V_{P2} = 5\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; CVBS signal according to VPS and VPT standard and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{P1}, V_{P2}$	supply voltages (pins 17 and 18)		4.5	5	5.5	V
$I_P$	total supply current	$I_{17} + I_{18}$	–	18	23	mA
<b>CVBS and sync inputs (pins 1 and 2)</b>						
$V_{i\ CVBS}$	CVBS input signal (peak-to-peak value)	sync-to-white note 1; Fig.4	0.5	1	1.4	V
$V_{i\ data}$	data input signal (peak-to-peak value, pin 1)	line 16; Fig.4	250	500	700	mV
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 2)		100	–	600	mV
$R_S$	source resistance		–	–	1	k $\Omega$
<b>Composite sync output (pin 6)</b>						
$V_{OL}$	output voltage LOW		–	–	0.4	V
$V_{OH}$	output voltage HIGH		2.4	–	–	V
$I_{OL}$	output current LOW		–	–	200	$\mu\text{A}$
$I_{OH}$	output current HIGH		–	–	–500	$\mu\text{A}$
$t_d$	sync separator delay time		–	0.3	–	$\mu\text{s}$
<b>DAV output (pin 13)</b>		note 2				
$V_{OL}$	output voltage LOW		–	–	0.4	V
$V_{OH}$	output voltage HIGH		2.4	–	–	V
$I_{OL}$	output current LOW		–	–	500	$\mu\text{A}$
$I_{OH}$	output current HIGH		–	0.01	1	$\mu\text{A}$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>SCL and SDA (pins 9 and 10)</b>						
V <sub>IL</sub>	input voltage LOW		–	–	1.5	V
V <sub>IH</sub>	input voltage HIGH		3	–	–	V
I <sub>I</sub>	input current	0.9V <sub>P</sub>	–	–	±10	µA
C <sub>I</sub>	input capacitance		–	–	10	pF
V <sub>O ACK</sub>	output voltage during acknowledge on pin 10	I <sub>OL</sub> = 3 mA	–	–	0.4	V
t <sub>r</sub>	rise time		–	–	1	µs
t <sub>f</sub>	fall time		–	–	0.3	µs
t <sub>pL</sub>	pulse duration LOW		4.7	–	–	µs
t <sub>pH</sub>	pulse duration HIGH		4.0	–	–	µs
SCL	clock frequency		–	–	100	kHz
<b>AD set input (pin 8)</b>		note 2				
V <sub>IL</sub>	input voltage LOW	address 23H	0	–	0.4	V
V <sub>IH</sub>	input voltage HIGH	address 21H	2.4	–	V <sub>P</sub>	V
<b>RESET input (pin 11)</b>		note 2				
V <sub>IL</sub>	input voltage LOW	reset active	–	–	0.4	V
V <sub>IH</sub>	input voltage HIGH	reset non-active	2.4	–	–	V
I <sub>IL</sub>	input current LOW		–	–	–10	µA
I <sub>IH</sub>	input current HIGH		–	0.01	1	µA

**Notes**

1. With standard sync and data amplitude of 68% to 75% black-white.
2. If the open collector output  $\overline{DAV}$  is used, a pull-up resistor to V<sub>P1</sub> is necessary.

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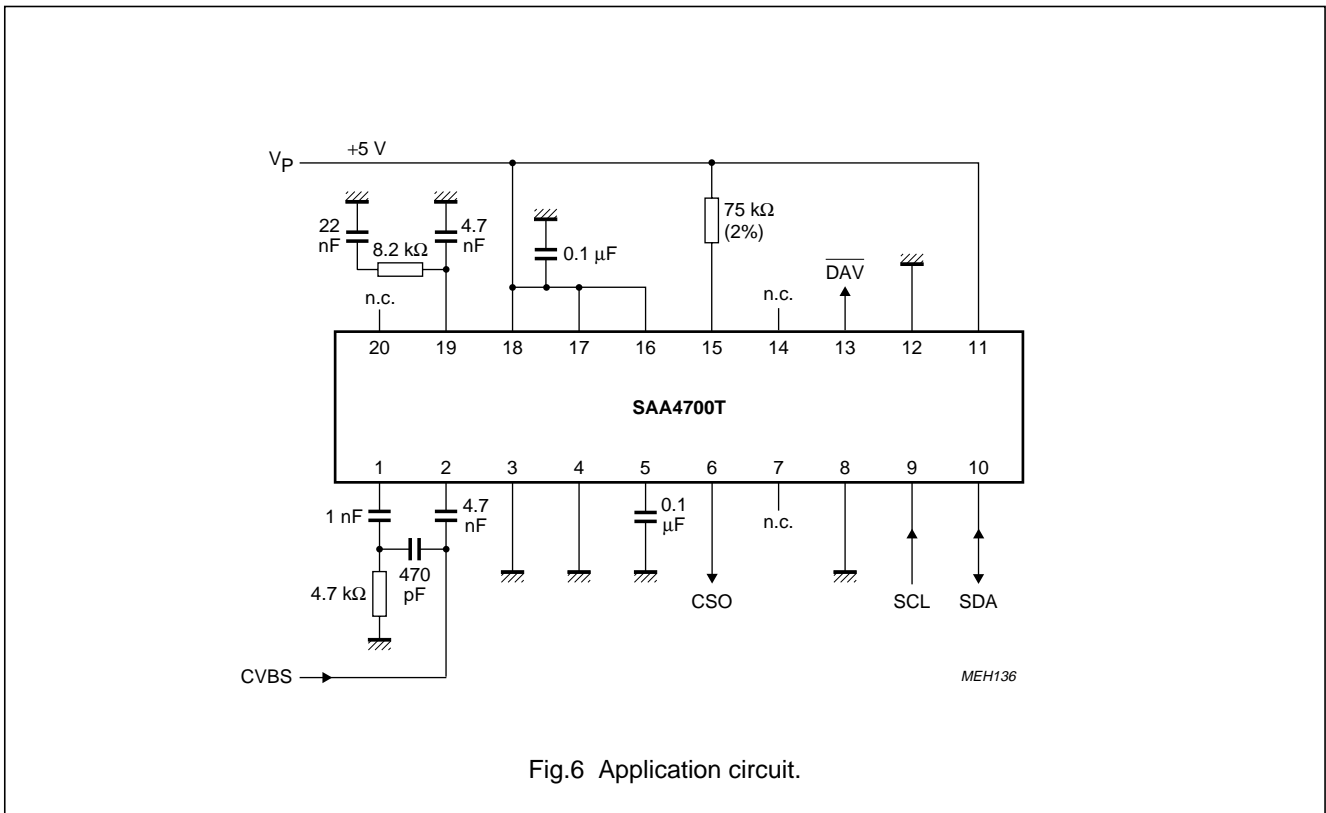


Fig.6 Application circuit.

I<sup>2</sup>C-BUS FORMAT

S	SLAVE ADDRESS	A	DATA	A	DATA	A	DATA	A	DATA	A	DATA	P
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- S = start condition
- SLAVE ADDRESS = 0010 0001 or 0010 0011 for set input AD = HIGH respectively LOW on pin 8 (the circuit is only a slave transmitter)
- A = acknowledge, generated by the slave or the master
- DATA = five data bytes, see words in Table 1
- P = stop condition respectively non-acknowledge by the microcontroller

Remarks to I<sup>2</sup>C-bus transmission

- the MSB of each word is transmitted first
- there is no restriction on the number of words to be transmitted, but if more than five words are requested, the following content will be "FF" continuously.
- Normally every dataline transmission has to be ended with STOP condition by non-acknowledge of the controller.

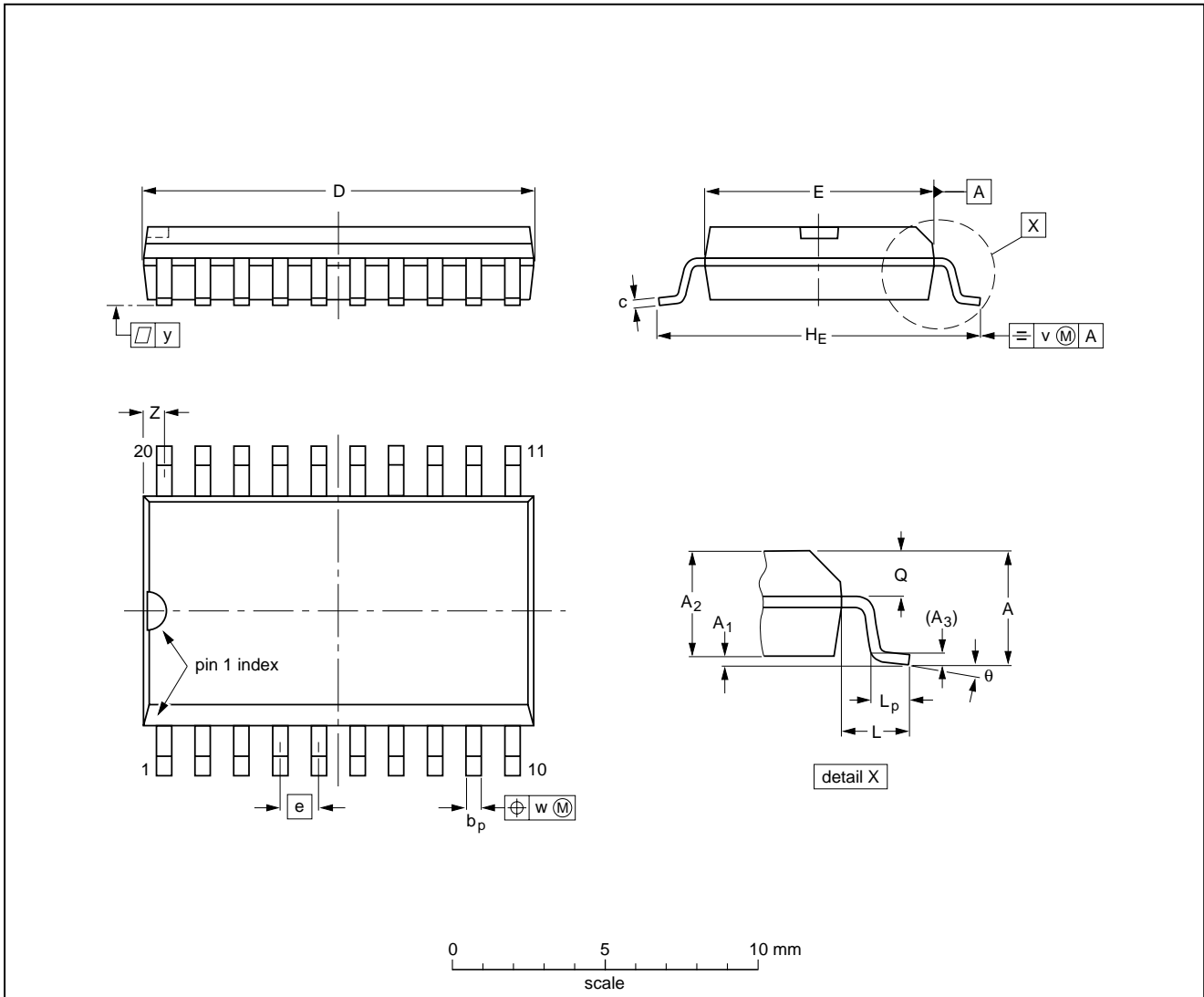
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PACKAGE OUTLINE

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "*IC Package Databook*" (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.