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PHASE CONTROL THYRISTOR

AT980

Repetitive voltage up to **6000 V**
Mean on-state current **3036 A**
Surge current **50 kA**

TARGET SPECIFICATION

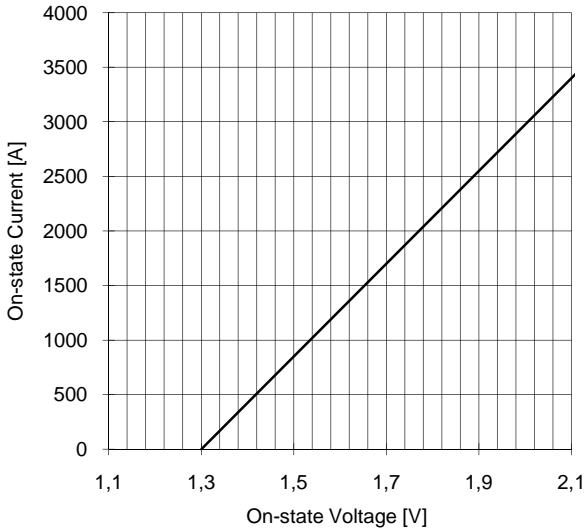
set 08 - ISSUE : 05

Symbol	Characteristic	Conditions	T _j [°C]	Value	Unit
BLOCKING					
V _{RRM}	Repetitive peak reverse voltage		120	6000	V
V _{RSM}	Non-repetitive peak reverse voltage		120	6100	V
V _{DRM}	Repetitive peak off-state voltage		120	6000	V
I _{RRM}	Repetitive peak reverse current	V=V _{RRM}	120	300	mA
I _{DRM}	Repetitive peak off-state current	V=V _{DRM}	120	300	mA
CONDUCTING					
I _{T(AV)}	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		3036	A
I _{T(AV)}	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		2244	A
I _{TSM}	Surge on-state current	sine wave, 10 ms	120	50,0	kA
I ² t	I ² t	without reverse voltage		12500 x1E3	A ² s
V _T	On-state voltage	On-state current = 6280 A	120	2,78	V
V _{T(TO)}	Threshold voltage		120	1,30	V
r _T	On-state slope resistance		120	0,235	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% V _{DRM} , gate 10V, 5ohm	120	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V _{DRM}	120	1000	V/μs
t _d	Gate controlled delay time, typical	V _D =100V, gate source 10V, 10 ohm, tr=.5 μs	25		μs
t _q	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% V _{DRM}		600	μs
Q _{rr}	Reverse recovery charge	di/dt=-20 A/μs, I= 2150 A	120		μC
I _{rr}	Peak reverse recovery current	V _R = 50 V			A
I _H	Holding current, typical	V _D =5V, gate open circuit	25	500	mA
I _L	Latching current, typical	V _D =12V, tp=30μs	25	1000	mA
GATE					
V _{GT}	Gate trigger voltage	V _D =12V	25	3,5	V
I _{GT}	Gate trigger current	V _D =12V	25	400	mA
V _{GD}	Non-trigger gate voltage, min.	V _D =V _{DRM}	120	0,25	V
V _{FGM}	Peak gate voltage (forward)			10	V
I _{FGM}	Peak gate current			10	A
V _{RGM}	Peak gate voltage (reverse)			10	V
P _{GM}	Peak gate power dissipation	Pulse width 100 μs		150	W
P _G	Average gate power dissipation			3	W
MOUNTING					
R _{th(j-h)}	Thermal impedance, DC	Junction to heatsink, double side cooled		7,0	°C/kW
R _{th(c-h)}	Thermal impedance	Case to heatsink, double side cooled		1,0	°C/kW
T _j	Operating junction temperature			-30 / 120	°C
F	Mounting force			80 / 100	kN
	Mass			3000	g
ORDERING INFORMATION : AT980 S 60					
standard specification <input type="checkbox"/> <input type="checkbox"/> VDRM&VRRM/100					

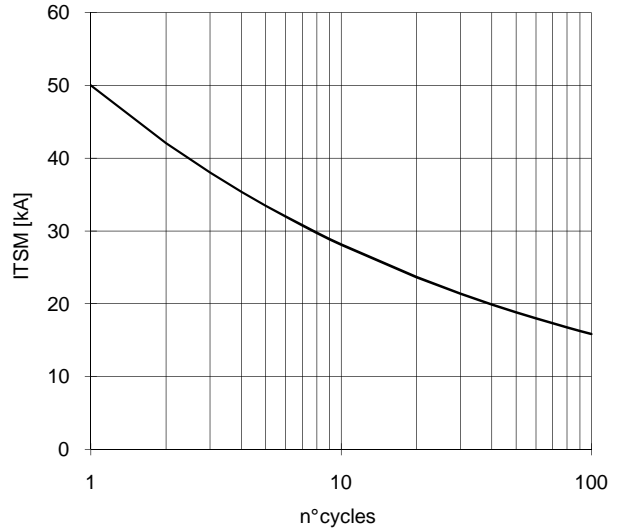
AT980 PHASE CONTROL THYRISTOR

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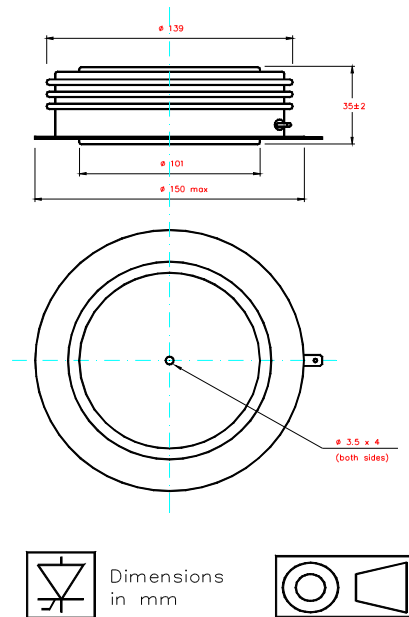
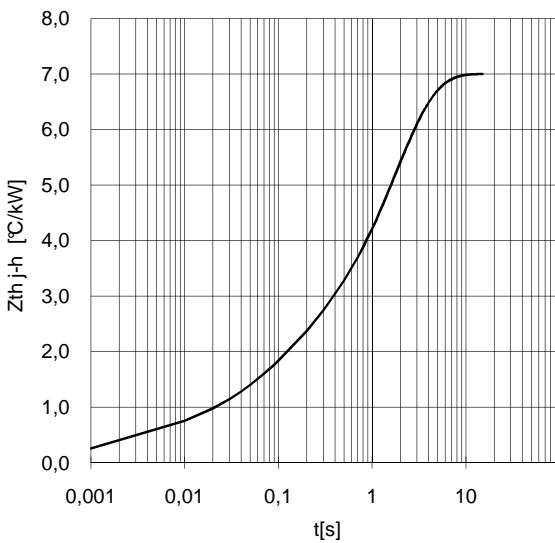
ON-STATE CHARACTERISTIC
 $T_j = 120\text{ }^\circ\text{C}$



SURGE CHARACTERISTIC
 $T_j = 120\text{ }^\circ\text{C}$



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm .
In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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