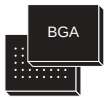
M69AW024B

16 Mbit (1M x16) 3V Asynchronous PSRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE: 2.7 to 3.3V
- ACCESS TIME: 60ns, 70ns
- LOW STANDBY CURRENT: 70µA
- DEEP POWER DOWN CURRENT: 10µA
- LOW V_{CC} DATA RETENTION: 2.3V
- COMPATIBLE WITH STANDARD LPSRAM

Figure 1. Package



TFBGA48 (ZB)
6x8 mm

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SUMMARY DESCRIPTION

The M69AW024B is a 16 Mbit (16,777,216 bit) CMOS memory, organized as 1,048,576 words by 16 bits, and is supplied by a single 2.7V to 3.3V supply voltage range.

M69AW024B is a member of STMicroelectronics PSRAM memory family, based on the one-transistor per-cell architecture. These devices are manufactured using dynamic random access memory cells, to minimize the cell size, and maximize the amount of memory that can be implemented in a given area.

However, through the use of internal control logic, the device is fully static in its operation, requiring no external clocks or timing strobes, and has a standard Asynchronous SRAM Interface.

The internal control logic of the M69AW024B handles the periodic refresh cycle, automatically, and without user involvement.

Write cycles can be performed on a single byte by using Upper Byte Enable ($\overline{UB}$) and Lower Byte Enable ($\overline{LB}$).

The device can be put into standby mode using Chip Enable ($\overline{E1}$) or in deep power down mode by using Chip Enable (E2).

Power-Down mode achieves a very low current consumption by halting all the internal activities. Since the refresh circuitry is halted, the duration of the power-down should be less than the maximum period for refresh, if the user has not finished with the data contents of the memory.

Figure 2. Logic Diagram

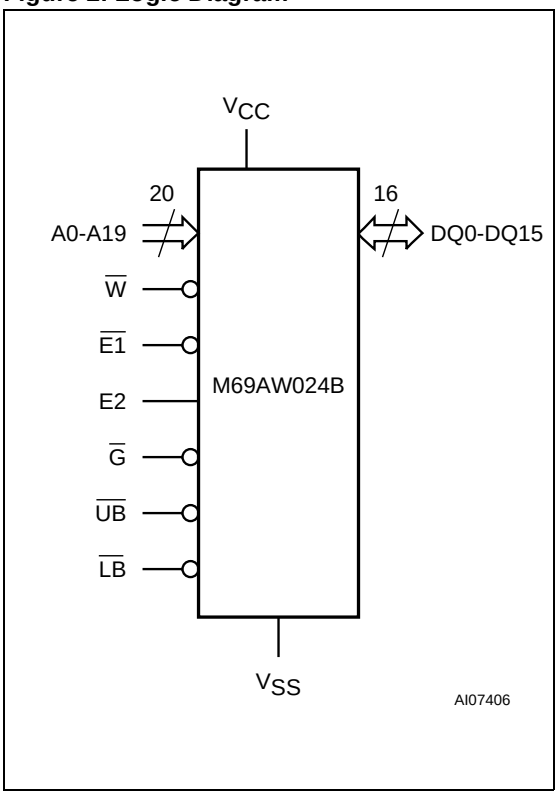
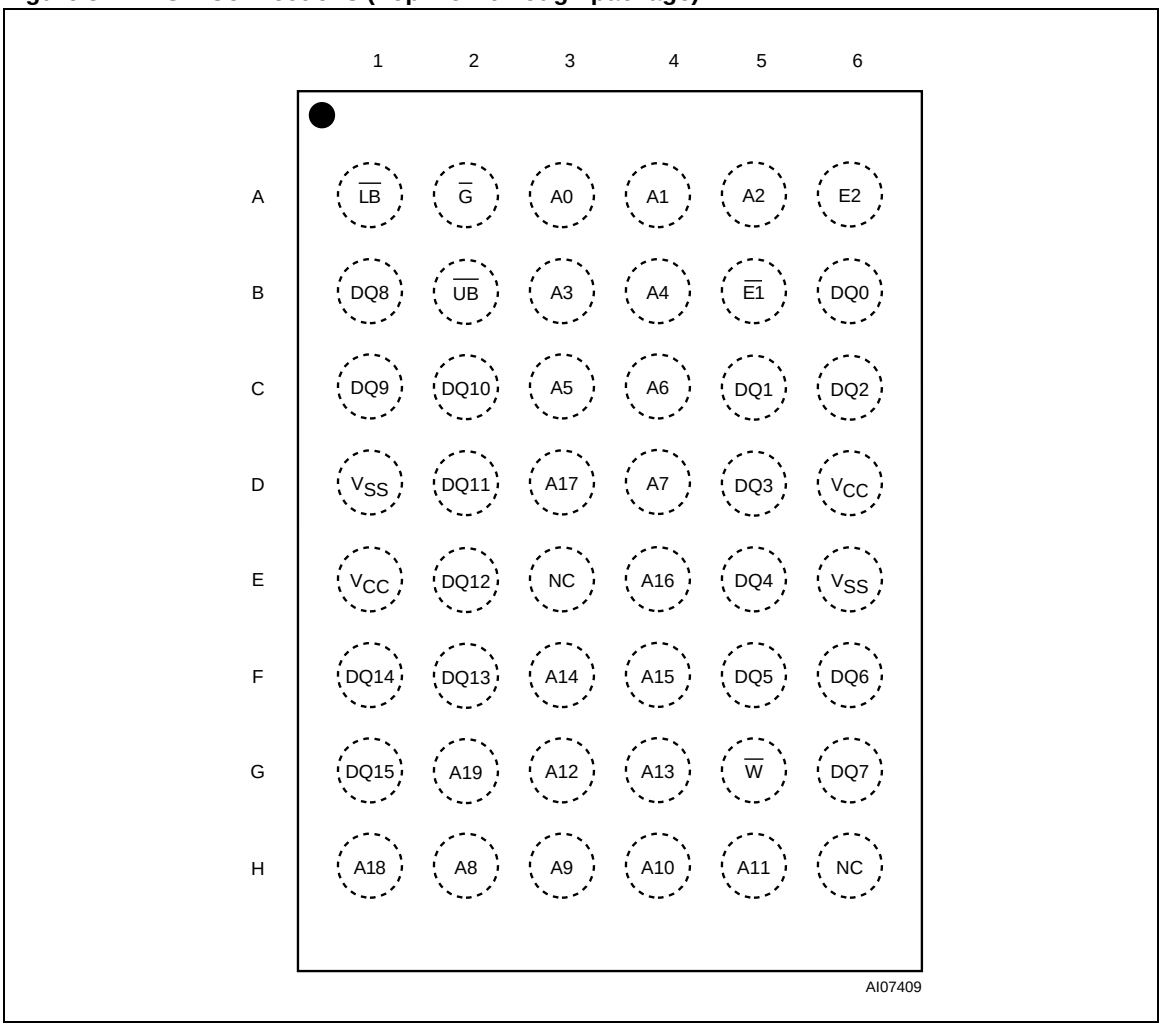


Table 1. Signal Names

A0-A19	Address Input
DQ0-DQ15	Data Input/Output
$\overline{E1}$, E2	Chip Enable, Power Down
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable
$\overline{LB}$	Lower Byte Enable
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected (no internal connection)

Figure 3. TFBGA Connections (Top view through package)



SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram, and Table 1., Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A19). The Address Inputs select the cells in the memory array to access during Read and Write operations.

Data Inputs/Outputs (DQ8-DQ15). The Upper Byte Data Inputs/Outputs carry the data to or from the upper part of the selected address during a Write or Read operation, when Upper Byte Enable ($\overline{UB}$) is driven Low.

Data Inputs/Outputs (DQ0-DQ7). The Lower Byte Data Inputs/Outputs carry the data to or from the lower part of the selected address during a Write or Read operation, when Lower Byte Enable ($\overline{LB}$) is driven Low.

Chip Enable ($\overline{E1}$). When asserted (Low), the Chip Enable, $\overline{E1}$, activates the memory state machine, address buffers and decoders, allowing Read and Write operations to be performed. When de-asserted (High), all other pins are ignored, and the device is put, automatically, in low-power Standby mode.

Chip Enable (E2). The Chip Enable, E2, puts the device in Deep Power-down mode when it is driven Low. This is the lowest power mode.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory.

Upper Byte Enable ($\overline{UB}$). The Upper Byte Enable, $\overline{UB}$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

Lower Byte Enable ($\overline{LB}$). The Lower Byte Enable, $\overline{LB}$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

V_{CC} Supply Voltage. The V_{CC} Supply Voltage supplies the power for all operations (Read or Write) and for driving the refresh logic, even when the device is not being accessed.

V_{SS} Ground. The V_{SS} Ground is the reference for all voltage measurements.

Figure 4. Block Diagram

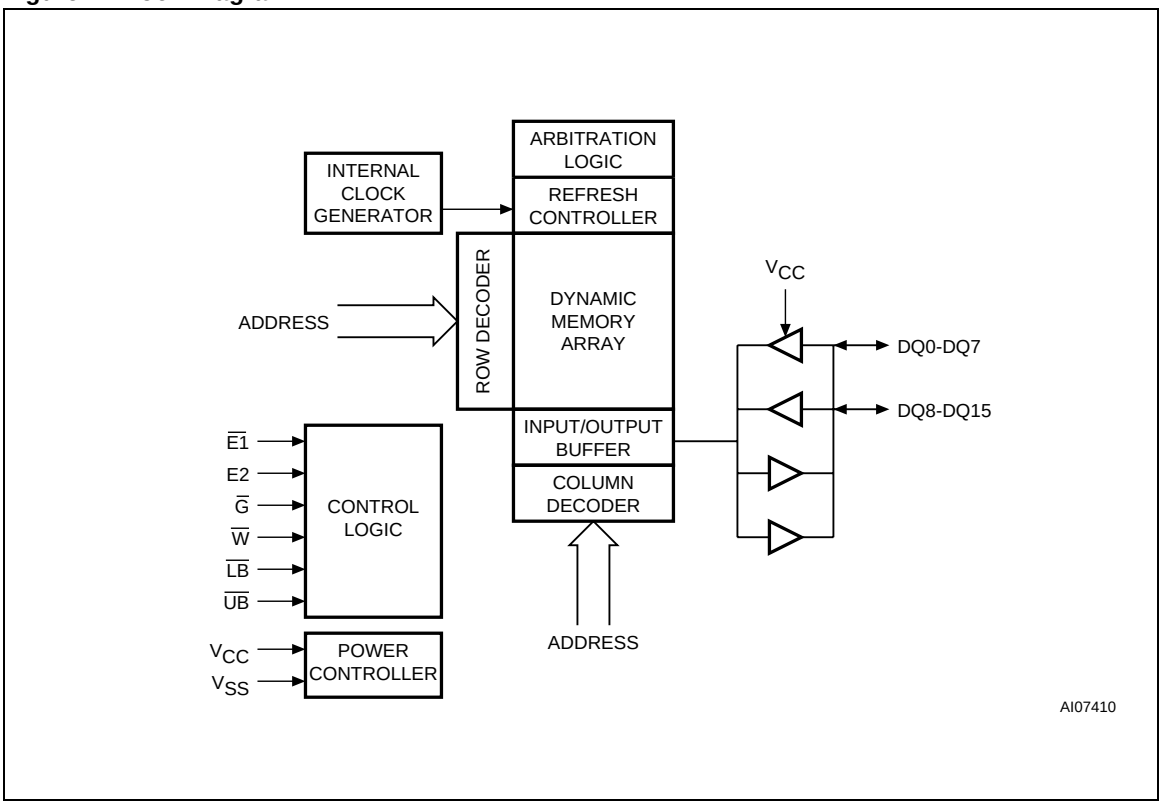


Table 2. Operating Modes

Operation	E2	$\overline{E1}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	A0-A19	DQ0-DQ7	DQ8-DQ15	I_{CC}	Data Retention
Standby (Deselect)	V_{IH}	V_{IH}	X (1)	X (1)	X (1)	X (1)	X (1)	Hi-Z	Hi-Z	I_{SB}	Yes
Output Disabled (2)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X (1)	X (1)	Note (4)	Hi-Z	Hi-Z	I_{CC}	Yes
Output Disabled (No Read)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Valid	Hi-Z	Hi-Z	I_{CC}	Yes
Word Read(5)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	$V_{IL(6)}$		Valid	Output Valid		I_{CC}	Yes
Word Read	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Valid	Output Valid		I_{CC}	Yes
Upper Byte Write	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Valid	Invalid	Input Valid	I_{CC}	Yes
Lower Byte Write	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Valid	Input Valid	Invalid	I_{CC}	Yes
Word Write	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Valid	Input Valid	Input Valid	I_{CC}	Yes
Power-down (3)	V_{IL}	X (1)	X (1)	X (1)	X (1)	X (1)	X (1)	Hi-Z	Hi-Z	I_{PD}	No

Note: 1. X = V_{IH} or V_{IL}.
2. Output Disable mode should not be kept longer than 1µs.
3. Power-down mode can be entered from Stand-by state, and all DQ pins are in Hi-Z state.
4. Can be either VIL or VIH but must be valid before Read or Write.
5. Byte Read is not supported.
6. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low, V_{IL}, for Read operations.

OPERATION

Operational modes are determined by device control inputs $\overline{W}$, $\overline{E1}$, E2, $\overline{LB}$ and $\overline{UB}$ as summarized in the Operating Modes table (see Table 2.).

Power On Sequence

Because the internal control logic of the M69AW024B needs to be initialized, the following power-on procedure must be followed before the memory is used:

- Apply power and wait for V_{CC} to stabilize
- Wait 400µs while driving both Chip Enable signals ($\overline{E1}$ and E2) High
- Activate the memory by driving Chip Enable ($\overline{E1}$) Low.

Read Mode

The device is in Read mode when:

- Write Enable ($\overline{W}$) is High and
- Output Enable ($\overline{G}$) Low and
- the two Chip Enable signals are asserted ($\overline{E1}$ is Low, and E2 is High).

The time taken to enter Read mode (t_{ELQV}, t_{GLQV} or t_{BLQV}) depends on which of the above signals was the last to reach the appropriate level.
Data out (DQ15-DQ0) may be indeterminate during t_{ELQX}, t_{GLQX} and t_{BLQX}, but data will always be valid during t_{AVQV}.

Write Mode

The device is in Write mode when

- Write Enable ($\overline{W}$) is Low and
- Chip Enable ($\overline{E1}$) is Low and
- the two Chip Enable signals are asserted ($\overline{E1}$ is Low, and E2 is High)
- one of Upper Byte Enable ($\overline{UB}$) or Lower Byte Enable ($\overline{LB}$) is Low, while the other is High.

The Write cycle begins just after the event (the falling edge) that causes the last of these conditions to become true (t_{AVWL} or t_{AVEL} or t_{AVBL}).
The Write cycle is terminated by the earlier of a rising edge on Write Enable ($\overline{W}$) or Chip Enable ($\overline{E1}$). If the device is in Write mode (Chip Enable ($\overline{E1}$) is Low, Output Enable ($\overline{G}$) is Low, Upper Byte Enable ($\overline{UB}$) or Lower Byte Enable ($\overline{LB}$) is Low), then Write Enable ($\overline{W}$) will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable ($\overline{W}$), or for t_{DVEH} before the rising edge of Chip Enable ($\overline{E1}$), whichever occurs first, and remain valid for t_{WHDX}, t_{EHDX}

Standby Mode

The device is in Standby mode when:

- Chip Enable ($\overline{E1}$) is High and
- Chip Enable (E2) is High.

The input/output buffers and the decoding/control logic are switched off, but the dynamic array continues to be refreshed. In this mode, the memory current consumption, I_{SB}, is reduced, and the data remains valid.

Deep Power-down Mode

The device is in Deep Power-down mode when:

- Chip Enable (E2 is Low).

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
I_O	Output Current	–50	50	mA
T_A	Ambient Operating Temperature	–30	85	°C
T_{STG}	Storage Temperature	–55	125	°C
V_{CC}	Core Supply Voltage	–0.5	3.6	V
V_{IO}	Input or Output Voltage	–0.5	3.6	V

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 4., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter	M69AW024B		Unit
	–60, –70		
	Min	Max	
V_{CC} Supply Voltage[1]	2.7	3.3	V
Ambient Operating Temperature	–30	85	°C
Load Capacitance (C_L)	50		pF
Output Circuit Protection Resistance (R_1)	50		Ω
Input Rise and Fall Times		4	ns
Input Pulse Voltages	0 to V_{CC}		V
Input and Output Timing Ref. Voltages	$V_{CC}/2$		V
Output Transition Timing Ref. Voltages	$V_{RL} = 0.3V_{CC}$; $V_{RH} = 0.7V_{CC}$		V
Input Transition Time[2] (tτ) between V_{IL} and V_{IH}	5		ns

Note: 1. All voltages are referenced to V_{SS}.
2. The Input Transition Time used in AC measurements is 5ns. For other input transition times, see Table 9.

Figure 5. AC Measurement Load Circuit

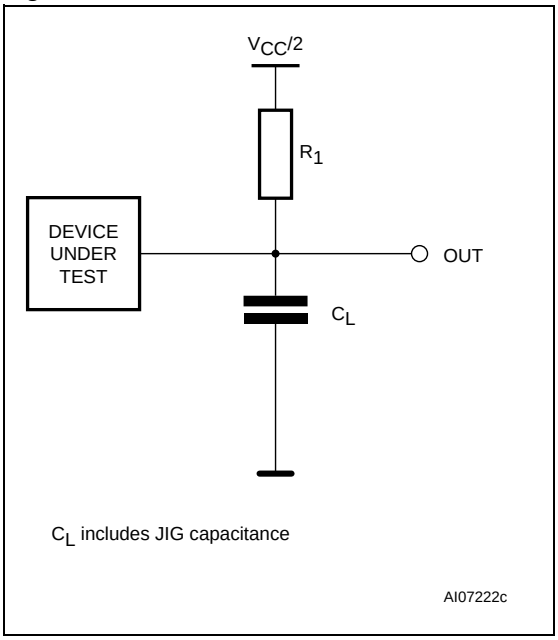


Figure 6. AC Measurement I/O Waveform

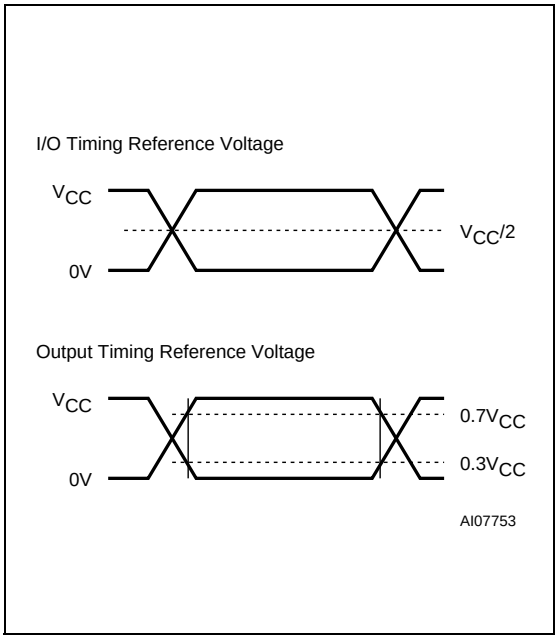


Table 5. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		5	pF
C_{OUT} (1)	Output Capacitance	V_{OUT} = 0V		8	pF

Note: 1. Outputs deselected.

Table 6. DC Characteristics

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{CC1} (1)	Operating Supply Current	V_{CC} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{E1} = V_{IL}$, E2 = V_{IH}, I_{OUT} = 0mA	t_{RC}/t_{WC} = Min		20	mA
			t_{RC}/t_{WC} = 1µs		3.0	mA
I_{LI}	Input Leakage Current	0V ≤V_{IN} ≤V_{CC}		–1	1	µA
I_{LO}	Output Leakage Current	0V ≤V_{OUT} ≤V_{CC}		–1	1	µA
I_{PD}	Deep Power Down Current	V_{CC} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}, E2 ≤0.2V			10	µA
I_{SB}	Standby Supply Current CMOS	3.1V ≤V_{CC} ≤3.3V, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{E1} = V_{IH}$ and E2 = V_{IH}, I_{OUT} = 0mA			1.5	mA
		2.7V ≤V_{CC} ≤3.1V, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{E1} = V_{IH}$ and E2 = V_{IH}, I_{OUT} = 0mA			1	mA
		3.1V ≤V_{CC} ≤3.3V, V_{IN} ≤0.2V or ≥ V_{CC} –0.2V, $\overline{E1}$ ≥ V_{CC} –0.2V and E2 ≥ V_{CC} –0.2V), I_{OUT} = 0mA			100	µA
		2.7V ≤V_{CC} ≤3.1V, V_{IN} ≤0.2V or ≥ V_{CC} –0.2V, $\overline{E1}$ ≥ V_{CC} –0.2V and E2 ≥ V_{CC} –0.2V), I_{OUT} = 0mA			70	µA
V_{IH} (2)	Input High Voltage	3.1V ≤V_{CC} ≤3.3V		2.6	V_{CC} + 0.3	V
		2.7V ≤V_{CC} ≤3.1V		2.2	V_{CC} + 0.3	V
V_{IL} (3)	Input Low Voltage	3.1V ≤V_{CC} ≤3.3V		–0.3	0.6	V
		2.7V ≤V_{CC} ≤3.1V		–0.3	0.5	V
V_{OH}	Output High Voltage	3.1V ≤V_{CC} ≤3.3V, I_{OH} = –0.5mA		2.5		V
		2.7V ≤V_{CC} ≤3.1V, I_{OH} = –0.5mA		2.2		V
V_{OL}	Output Low Voltage	V_{CC} = 3V, I_{OL} = 1mA			0.4	V

Note: 1. Average AC current, Outputs open, cycling at t_{AVAX} (min).
2. Maximum DC voltage on input and I/O pins is V_{CC} + 0.3V.
During voltage transitions, input may positive overshoot to V_{CC} + 1.0V for a period of up to 5ns.
3. Minimum DC voltage on input or I/O pins is –0.3V.
During voltage transitions, input may positive overshoot to V_{SS} + 1.0V for a period of up to 5ns.

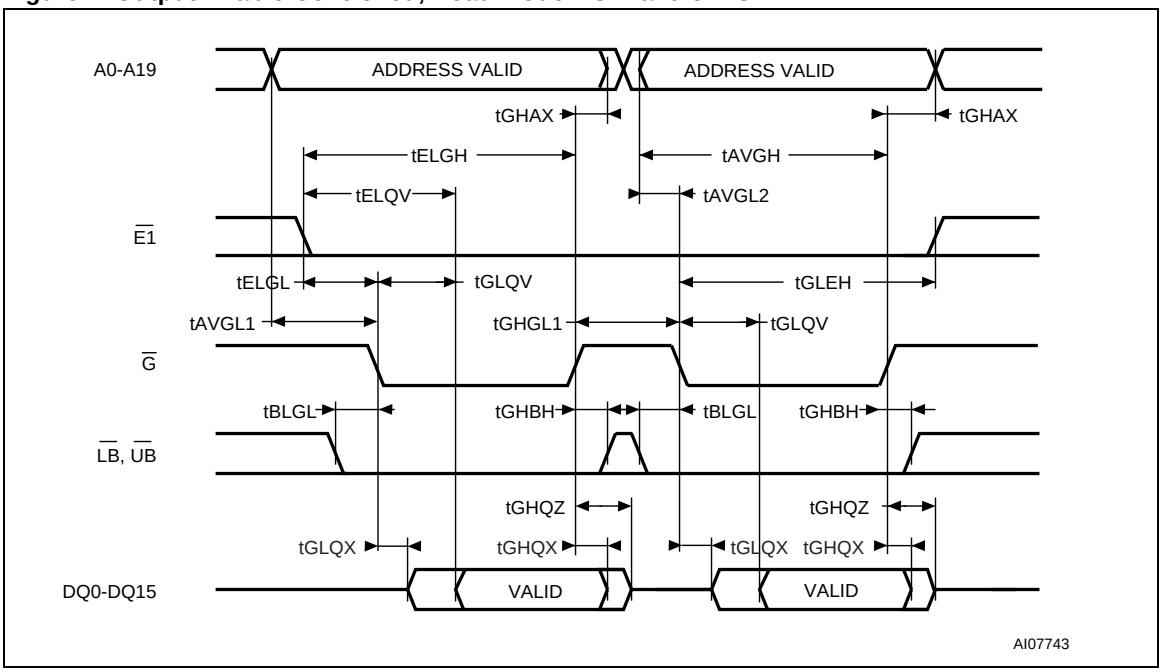
Table 7. Read and Standby Modes AC Characteristics

Symbol	Alt.	Parameter	M69AW024B				Unit
			–60		–70		
			Min	Max	Min	Max	
t_{AVAX}	t_{RC}	Read Cycle Time	80		90		ns
t_{AVEH}	t_{RC}	Address Valid to Chip Enable High (Read Cycle Time)	80		90		ns
t_{AVEL} (5)	t_{ASC}	Address Set-up Time to Chip Enable Low	–5		–5		ns
t_{AVGH}	t_{RC}	Address Valid to Output Enable High (Read Cycle Time)	80		90		ns
t_{AVGL1} (3,6)	t_{ASO}	Address Valid to Output Enable Low	25		30		ns
t_{AVGL2} (7)	t_{ASO}(ABS)	Address Valid to Output Enable Low (absolute)	5		5		ns
t_{AVQV} (1,4)	t_{AA}	Address Access Time		60		70	ns
t_{AXAV} (4,8)	t_{AX}	Address Invalid Time		5		5	ns
t_{AXQX} (1)	t_{OH}	Output Hold Time after Address Transition	5		5		ns
t_{BLEL} (5)	t_{BSC}	$\overline{LB}$, $\overline{UB}$ Set-up Time to Chip Enable Low	–5		–5		ns
t_{BLGL}	t_{BSO}	$\overline{LB}$, $\overline{UB}$ Set-up Time to Output Enable Low	0		0		ns
t_{EHAX}	t_{CHAH}	Chip Enable High to Address Hold Time	–5		–5		ns
t_{EHBH}	t_{CHBH}	Chip Enable High to $\overline{LB}$, $\overline{UB}$ High	–5		–5		ns
t_{EHEL}	t_{CP}	Chip Enable High Pulse Width	10		12		ns
t_{EHQX} (1)	t_{OH}	Output Hold Time after Chip Enable Low	5		5		ns
t_{EHQZ} (2)	t_{CHZ}	Chip Enable High to Output Hi-Z		20		25	ns
t_{ELAX} (4)	t_{CLAH}	Chip Enable Low to Address Hold Time	80		90		ns
t_{ELEH}	t_{RC}	Chip Enable Low to Chip Enable High (Read Cycle Time)	80		90		ns
t_{ELGH}	t_{RC}	Chip Enable Low to Output Enable High (Read Cycle Time)	80		90		ns
t_{ELGL} (3,6,9,10)	t_{CLOL}	Chip Enable Low to Output Enable Low Delay Time	25	1000	30	1000	ns
t_{ELQV} (1,3)	t_{CE}	Chip Enable Access Time		60		70	ns
t_{ELQX} (2)	t_{CLZ}	Chip Enable Low to Output Lo-Z	5		5		ns
t_{GHAX}	t_{OHAH}	Output Enable High to Address Hold Time	–5		–5		ns
t_{GHBH}	t_{OHBH}	Output Enable High to $\overline{LB}$, $\overline{UB}$ High	–5		–5		ns
t_{GHGL1} (6,9,10)	t_{OP}	Output Enable High Pulse Width	25	1000	30	1000	ns
t_{GHGL2} (7)	t_{OP}(ABS)	Output Enable High Pulse Width (absolute)	10		10		ns
t_{GHQX} (1)	t_{OH}	Output Hold Time after Output Enable Low	5		5		ns
t_{GHQZ} (2)	t_{OHZ}	Output Enable High to Output Hi-Z		20		25	ns
t_{GLAX} (4,9)	t_{OLAH}	Output Enable Low to Address Hold Time	45		50		ns
t_{GLEH} (9)	t_{OLCH}	Output Enable Low to Chip Enable High Delay Time	45		50		ns

Symbol	Alt.	Parameter	M69AW024B				Unit
			–60		–70		
			Min	Max	Min	Max	
t_{GLQV}(1)	t_{OE}	Output Enable Access Time		35		40	ns
t_{GLQX}(2)	t_{OLZ}	Output Enable Low to Output Lo-Z	0		0		ns

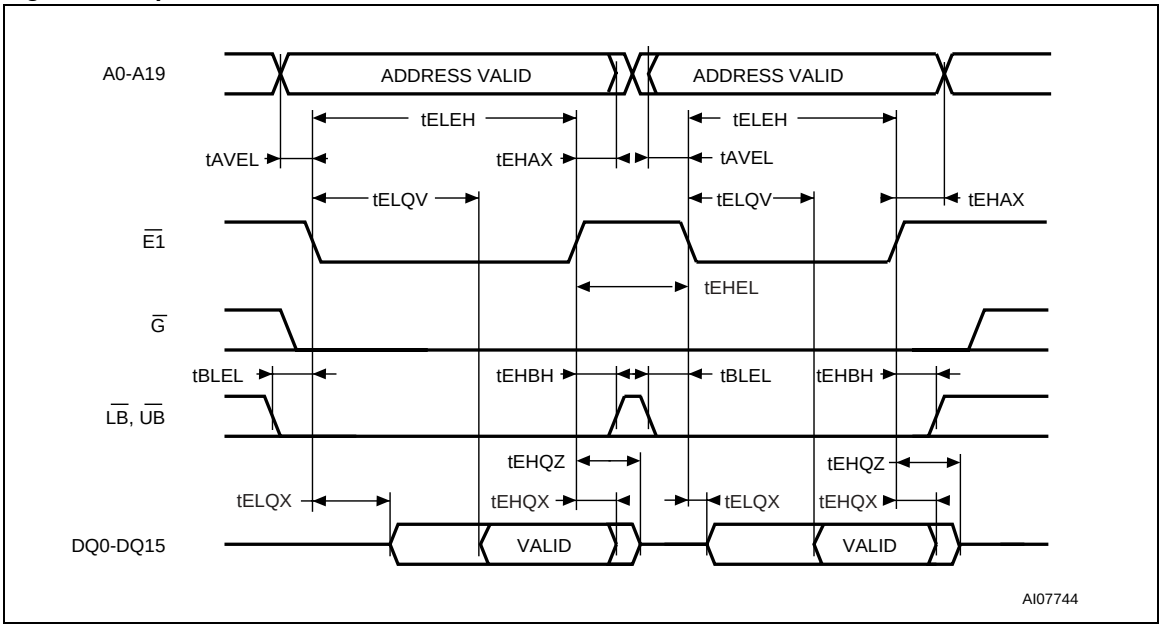
Note: 1. C_L = 50pF with 1 TTL and R1=50Ω
2. C_L = 5pF
3. t_{ELQV} is applicable if $\overline{G}$ is brought to Low before $\overline{E1}$ goes Low and if actual value of either t_{AVGL1} or t_{ELGL}, or both, is shorter than the specified value.
4. Only applicable to A0, A1 and A2 when both and $\overline{G}$ and $\overline{E1}$ are kept Low for Address access.
5. Applicable if $\overline{G}$ is brought to Low before $\overline{E1}$ goes Low.
6. t_{AVGL1}, t_{ELGL}(Min) and t_{GHGL1}(Min) are reference values when the access time is determined by t_{GLQV}. If the actual value of each parameter is lower than the specified minimum values, t_{GLQV} is increased by the difference between the actual value and the specified minimum value.
7. t_{AVGL2} and t_{GHGL2} correspond to absolute minimum values during $\overline{G}$ controlled access.
8. t_{AXAV} is applicable when two or more addresses from A0 to A2 are switched from the previous state.
9. If the actual value of t_{ELGL} or t_{GHGL1} is lower than the specified minimum value, t_{GLAX} and t_{GLEH} will be equal to t_{AVAX}(Min) – t_{ELGL} (Actual) and t_{AVAX} (Min) –t_{GHGL1} (Actual), respectively.
10. The maximum value is applicable if $\overline{E1}$ is kept Low.

Figure 7. Output Enable Controlled, Read Mode AC Waveforms



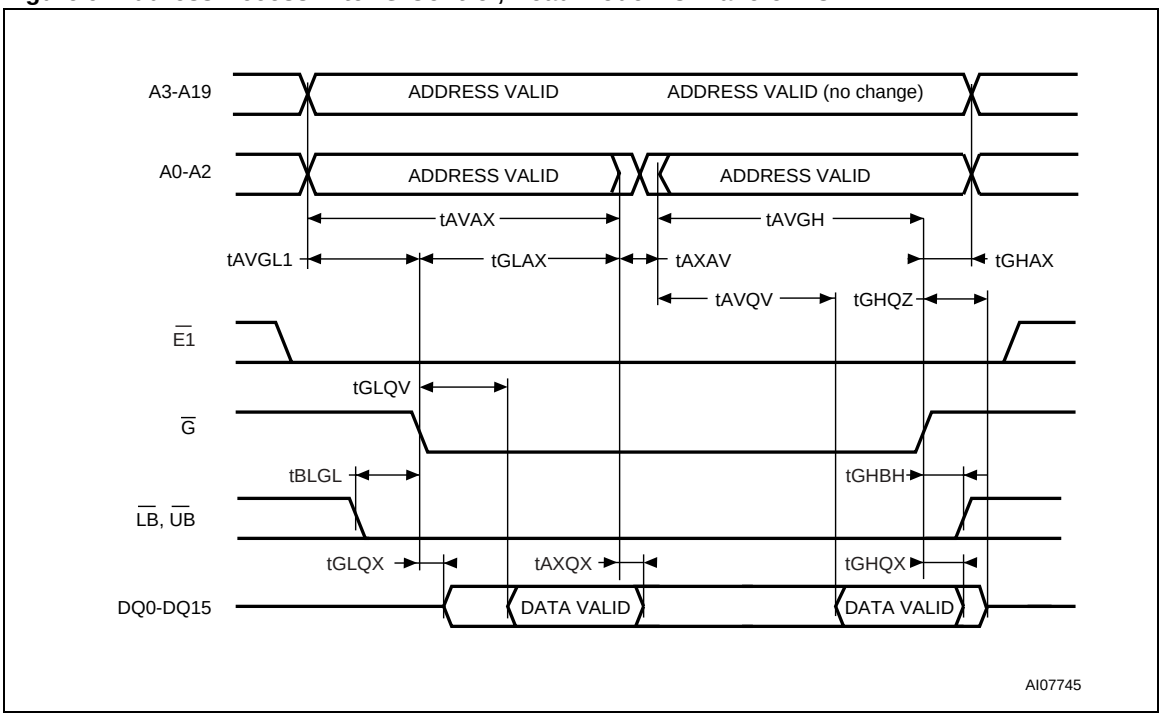
Note: 1. E2 = High and $\overline{W}$ = High.
2. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{E1}$ and $\overline{G}$ are Low.

Figure 8. Chip Enable Controlled, Read Mode AC Waveforms



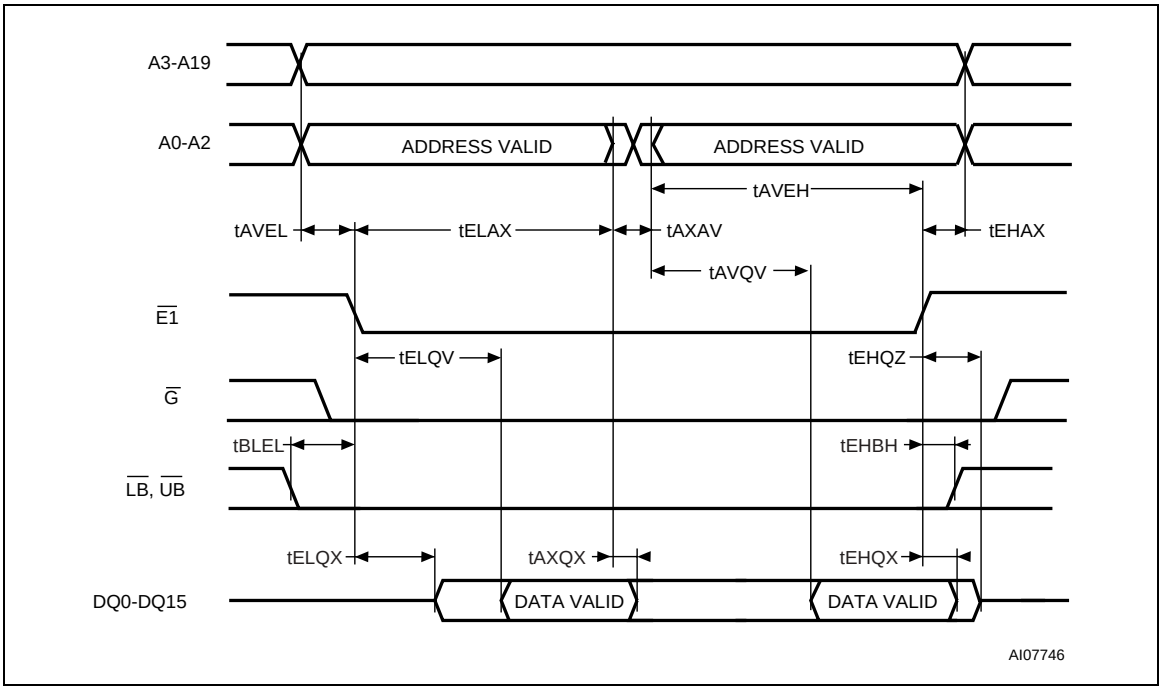
Note: 1. E2 = High and $\overline{W}$ = High.
2. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{E1}$ and $\overline{G}$ are Low.

Figure 9. Address Access After $\overline{G}$ Control, Read Mode AC Waveforms



Note: 1. E2 = High and $\overline{W}$ = High.
2. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{E1}$ and $\overline{G}$ are Low.

Figure 10. Address Access After $\overline{E1}$ Control, Read Mode AC Waveforms



Note: 1. E2 = High and $\overline{W}$ = High.
2. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{E1}$ and $\overline{G}$ are Low.

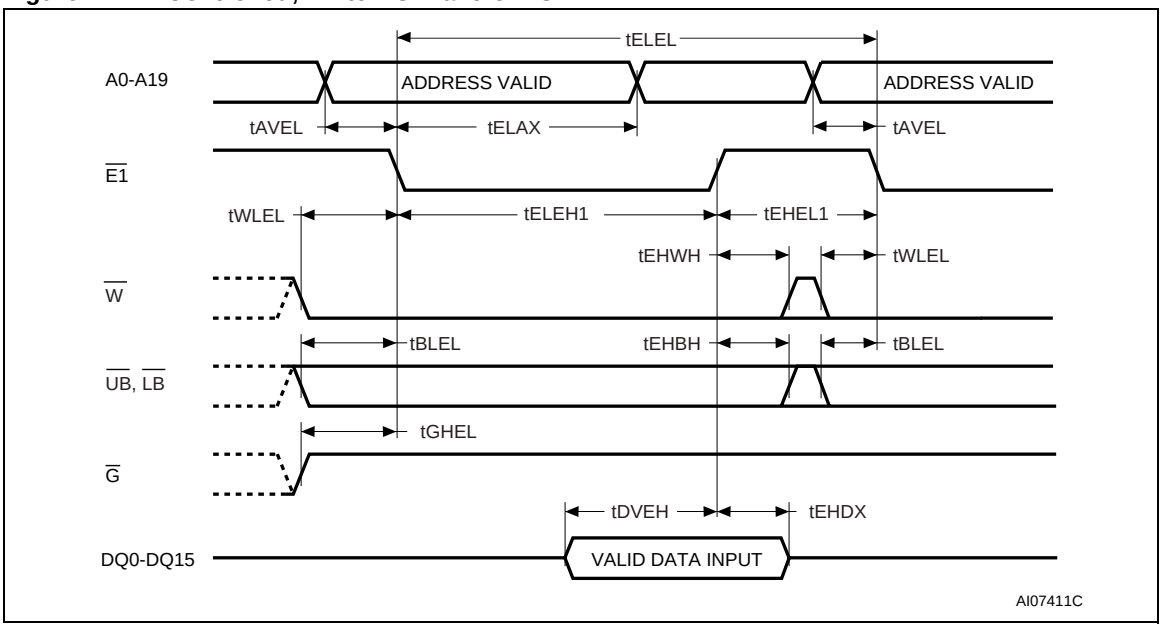
Table 8. Write Mode AC Characteristics

Symbol	Alt.	Parameter	M69AW024B				Unit
			–60		–70		
			Min	Max	Min	Max	
t_{AVEL} (2)	t_{AS}	Address Set-up Time to Chip Enable Low	0		0		ns
t_{AVWL}	t_{AS}	Address Set-up Time to Write Enable Low	0		0		ns
t_{AXGL1} (3,4)	t_{OEH}	Address Invalid to Output Enable Low	25	1000	35	1000	ns
t_{AXGL2} (5)	t_{OEH}(ABS)	Address Invalid to Output Enable Low (absolute)	12		15		ns
t_{BLEL}	t_{BS}	$\overline{LB}$, $\overline{UB}$ Set-up Time to Chip Enable Low	–5		–5		ns
t_{BLWL}	t_{BS}	$\overline{LB}$, $\overline{UB}$ Set-up Time to Write Enable Low	–5		–5		ns
t_{DVEH}	t_{DS}	Data Set-up Time to Chip Enable High	15		20		ns
t_{DVWH}	t_{DS}	Data Set-up Time to Write Enable High	15		20		ns
t_{EHBH}	t_{BH}	$\overline{LB}$, $\overline{UB}$ Hold Time from Chip Enable High	–5		–5		ns
t_{EHDX}	t_{DH}	Input Data Hold Time from Chip Enable High	0		0		ns
t_{EHEL1} (9,10)	t_{WRC}	Chip Enable High Pulse Width to Chip Enable Low	20		20		ns
t_{EHEL2} (10)	t_{CP}	Chip Enable High Pulse Width to Chip Enable Low	10		12		ns
t_{EHWH}	t_{WH}	Write Enable Low Hold Time	0		0		ns
t_{EHWL}	t_{WH}	Write Enable High Hold Time	0		0		ns
t_{ELAX} (2)	t_{AH}	Address Hold Time from Chip Enable Low	35		40		ns
t_{ELEH1} (1,8)	t_{CW}	Chip Enable Write Pulse Width	45		50		ns
t_{ELEH2} (1,9,10)	t_{WRC}	Chip Enable Write Recovery Time	20		20		ns
t_{ELEL}	t_{WC}	Chip Enable Write Cycle Time	80		90		ns
t_{ELWL}	t_{CS}	Chip Enable Write Set-up Time	0	1000	0	1000	ns
t_{GHAX} (7)	t_{OHAH}	Address Hold Time from Output Enable High	–5		–5		ns
t_{GHBH}	t_{BH}	$\overline{LB}$, $\overline{UB}$ Hold Time from Output Enable High	–5		–5		ns
t_{GHEL} (6)	t_{OHCL}	Output Enable High to Chip Enable Low Set-up Time	–5		–5		ns
t_{GHWL} (3)	t_{OES}	Output Enable Set-up Time	0	1000	0	1000	ns
t_{WHAV} (1,3,9,10)	t_{WR}	Write Enable High to Address Valid	20	1000	20	1000	ns
t_{WHBH}	t_{BH}	$\overline{LB}$, $\overline{UB}$ Hold Time from Write Enable High	–5		–5		ns
t_{WHDX}	t_{DH}	Input Data Hold Time from Write Enable High	0		0		ns
t_{WHEH}	t_{CH}	Chip Enable Write Hold Time	0	1000	0	1000	ns
t_{WHEL}	t_{WS}	Write Enable High Set-up Time	0		0		ns
t_{WHWL} (1,3,9,10)	t_{WR}	Write Enable Write Recovery Time to Write Enable Low	20	1000	20	1000	ns
t_{WLAV}	t_{WC}	Write Enable Low to Address Valid Write Cycle Time	80		90		ns
t_{WLAX} (2)	t_{AH}	Address Hold Time from Write Enable Low	35		40		ns

Symbol	Alt.	Parameter	M69AW024B				Unit
			–60		–70		
			Min	Max	Min	Max	
t_{WLEL}	t_{WS}	Write Enable Low Set-up Time	0		0		ns
t_{WLWH}(1,8)	t_{WP}	Write Enable Write Pulse Width	45		50		ns
t_{WLWL}	t_{WC}	Write Enable Write Cycle Time	80		90		ns

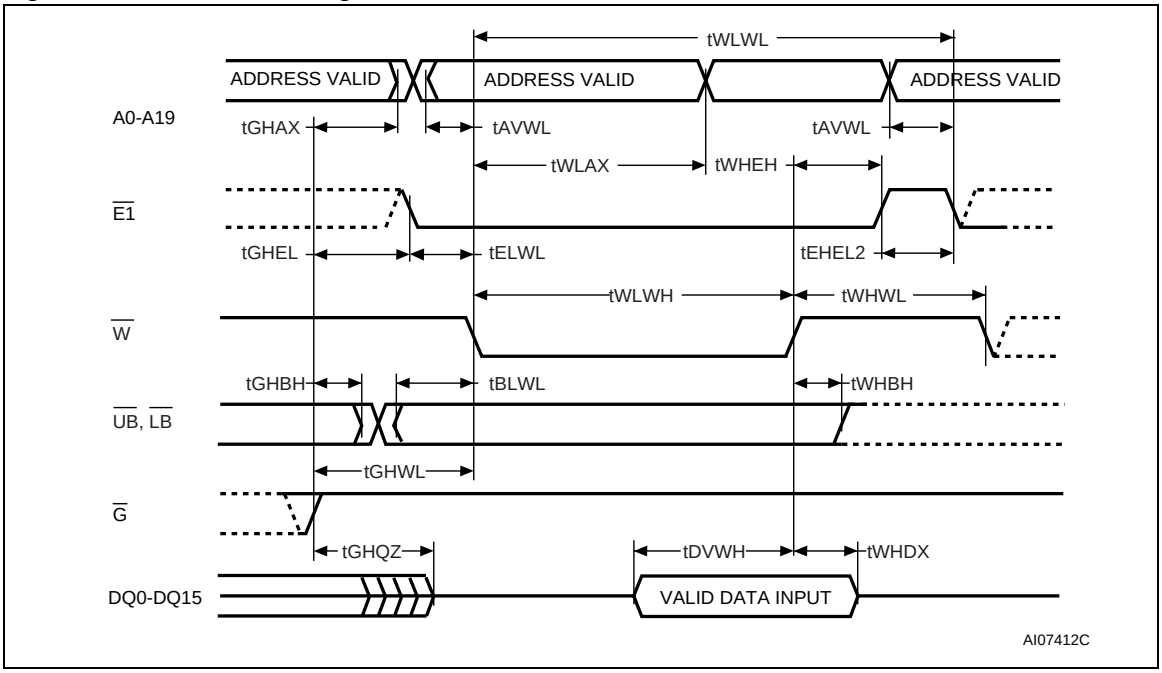
Note: 1. The minimum value must be equal to or greater than the sum of actual t_{ELEH} (or t_{WLWH}).
2. The new write address is valid from either $\overline{E1}$ High or $\overline{W}$ High.
3. t_{AXGL1} is specified from end of t_{AVAX} (Min) and is a reference value when access time is determined by t_{AXGL1}. If actual value is lower than specified minimum value, t_{AXGL1} is increased by the difference between the actual value and the specified minimum value.
4. t_{AXGL1} maximum is applicable if $\overline{E1}$ is kept Low and both $\overline{W}$ and $\overline{G}$ are kept High.
5. t_{AXGL2} is the absolute minimum value if the Write cycle terminates with $\overline{W}$ and $\overline{E1}$ Low.
6. t_{GHEL} (Min) must be kept if the Read cycle is not performed prior to the Write cycle. In case $\overline{G}$ is disabled after a time t_{GHEL}(Min), $\overline{W}$ must go Low t_{ELEH2} (Min) after $\overline{E1}$ goes Low. In other words, the Read cycle is initiated if t_{GHEL} (Min) is not kept.
7. Applicable if $\overline{E1}$ stays Low after the Read cycle.
8. t_{ELEH} or t_{WLWH} is applicable if the Write operation is initiated by $\overline{E1}$ or $\overline{W}$, respectively.
9. If the write operation is terminated by $\overline{W}$ followed by $\overline{E1}$ High, the sum of actual t_{ELWL} and t_{WLWH} and the sum of actual t_{AVWL} and t_{WLWH} must be equal or greater than 60ns.
10. t_{EHEL1} or t_{WHWL} is applicable if the Write operation is terminated by $\overline{E1}$ or $\overline{W}$, respectively. If $\overline{E1}$ goes High before t_{WHWL} (Min), then t_{EHEL1} (Min) must apply.
11. t_{EHEL1} and t_{EHEL2} is applicable if write operation is terminated by $\overline{E1}$ and $\overline{W}$, respectively. In case $\overline{E1}$ is brought to High before satisfaction of t_{EHEL2} (min), the t_{EHEL1} (min) is also applied.
12. For other timings please refer to Table 7., Read and Standby Modes AC Characteristics.

Figure 11. $\overline{E1}$ Controlled, Write AC Waveforms



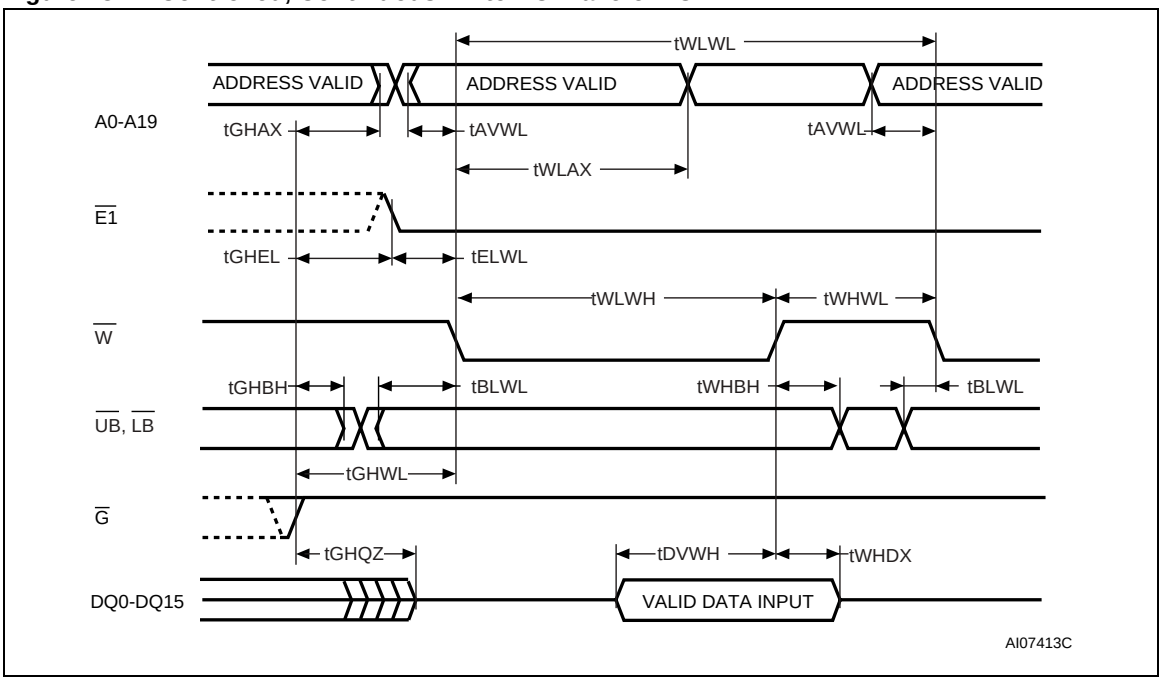
Note: 1. E2 must be High during the Write cycle.

Figure 12. $\overline{W}$ Controlled, Single Write AC Waveforms



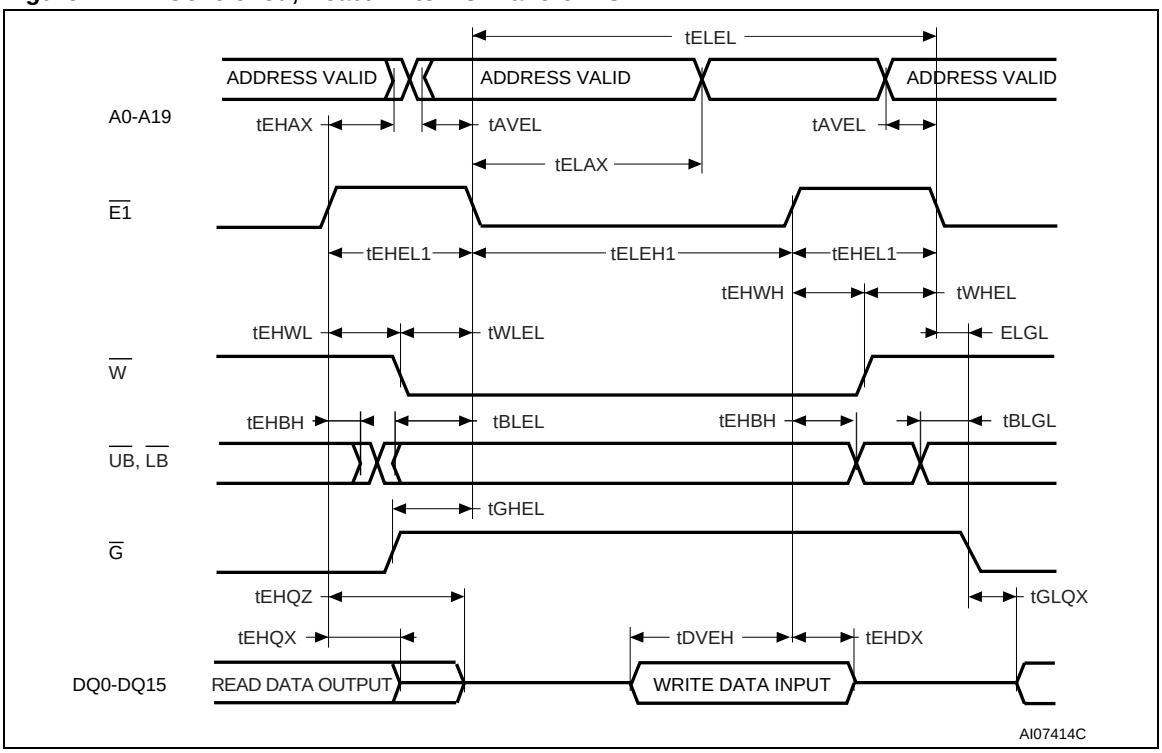
Note: 1. E2 must be High during the Write cycle.

Figure 13. $\overline{W}$ Controlled, Continuous Write AC Waveforms



Note: 1. E2 must be High during the Write cycle.

Figure 14. $\overline{E1}$ Controlled, Read/Write AC Waveforms



Note: 1. Write address is valid from the falling edge of either $\overline{E1}$ or $\overline{W}$, whichever occurs later.

Figure 15. $\overline{E1}$ Controlled, Read/Write AC Waveforms 2

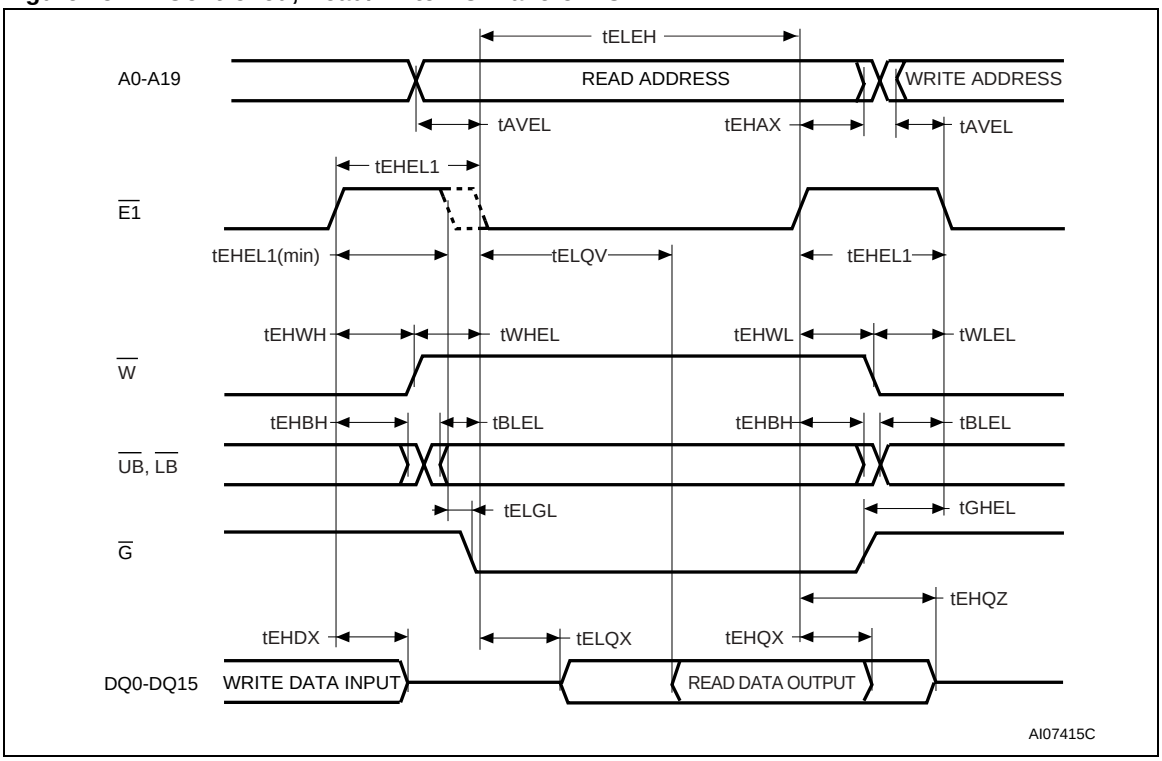
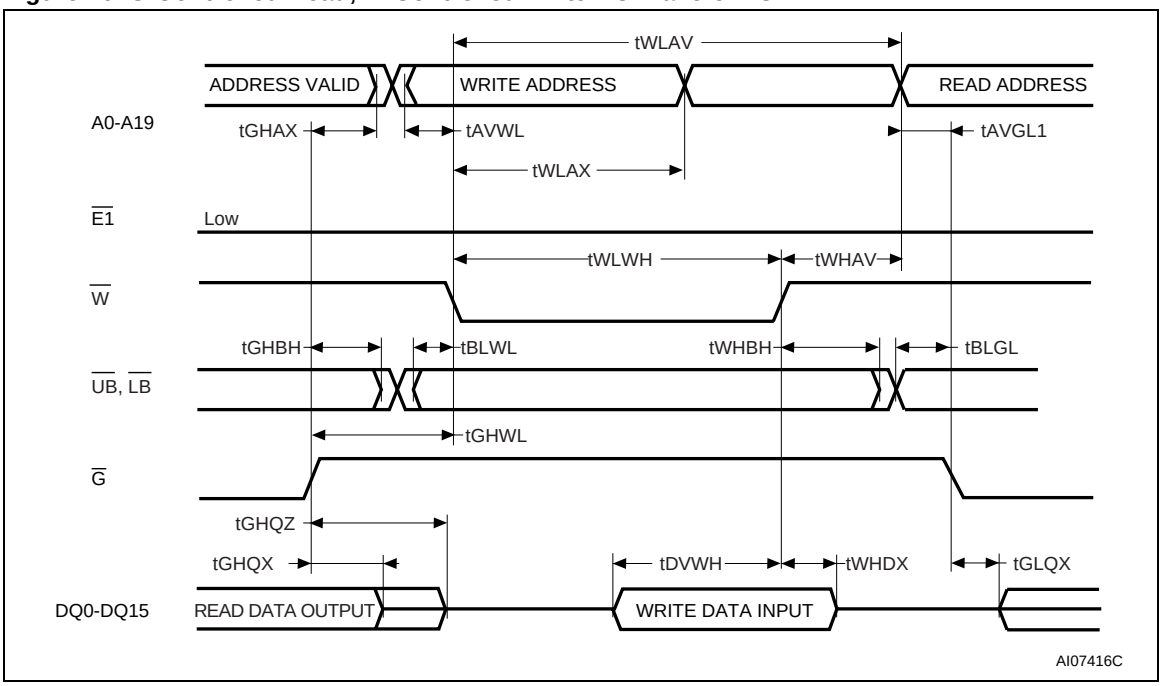
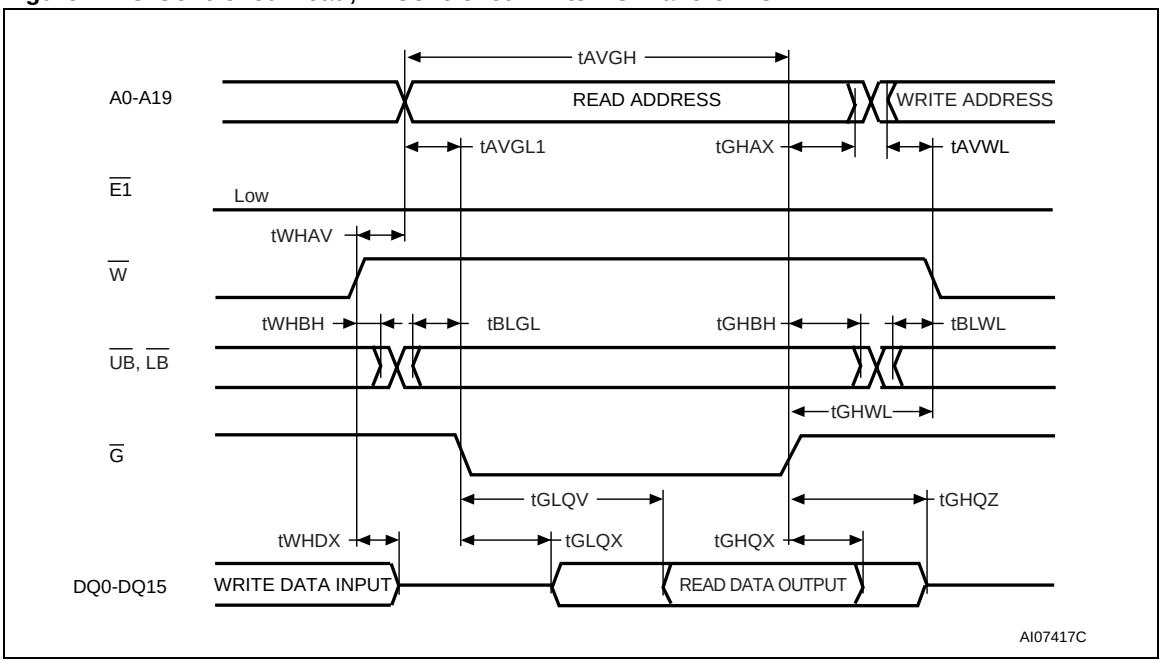


Figure 16. $\overline{G}$ Controlled Read, $\overline{W}$ Controlled Write AC Waveforms



Note: 1. $\overline{E1}$ can be tied to Low for $\overline{W}$ and $\overline{G}$ controlled operation. When $\overline{E1}$ is tied to Low, output is exclusively controlled by $\overline{G}$.

Figure 17. $\overline{G}$ Controlled Read, $\overline{W}$ Controlled Write AC Waveforms 2



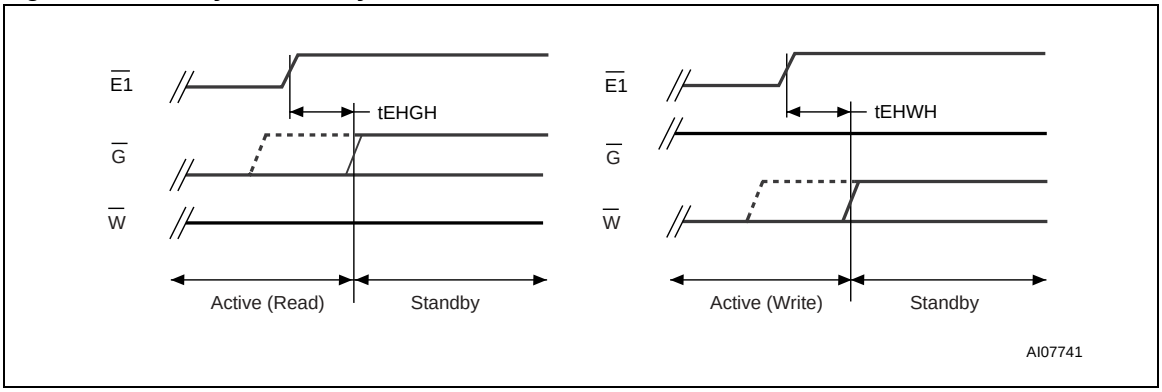
Note: 1. $\overline{E1}$ can be tied to Low for $\overline{W}$ and $\overline{G}$ controlled operation. When $\overline{E1}$ is tied to Low, output is exclusively controlled by $\overline{G}$.

Table 9. Power Down and Power-Up AC Parameters

Symbol	Alt.	Parameter	M69AW024B				Unit
			–60		–70		
			Min	Max	Min	Max	
t_{CLEL}	t_{CSP}	E2 Low Setup Time for Power Down Entry	10		10		ns
t_{ELCH}	t_{C2LP}	E2 Low Hold Time after Power Down Entry	80		90		ns
t_{CHEL}	t_{CHH}	$\overline{E1}$ High Hold Time following E2 High after Power-Down Exit (Sleep Mode only)	350		350		µs
t_{EHEL}	t_{CHHP}	$\overline{E1}$ High Hold Time following E2 High after Power-Down Exit (not in Sleep Mode)	400		400		µs
t_{EHCH1}	t_{CHS}	$\overline{E1}$ High Setup Time following E2 High after Power-Down Exit	10		10		ns
t_{EHCH2}	t_{C2LH}	Power-up Time 1	50		50		µs
t_{CHCL1}[2] t_{CHCL2}[2]	t_{C2HL}	Power-up Time 2	50		50		µs
t_{EHGH}	t_{CHOX}	$\overline{E1}$ High to $\overline{G}$ Invalid Time for Standby Entry	10		10		ns
t_{EHWH}	t_{CHWX}	$\overline{E1}$ High to $\overline{W}$ Invalid Time for Standby Entry	10		10		ns
t_T	t_T	Input Transition Time	1	25	1	25	ns

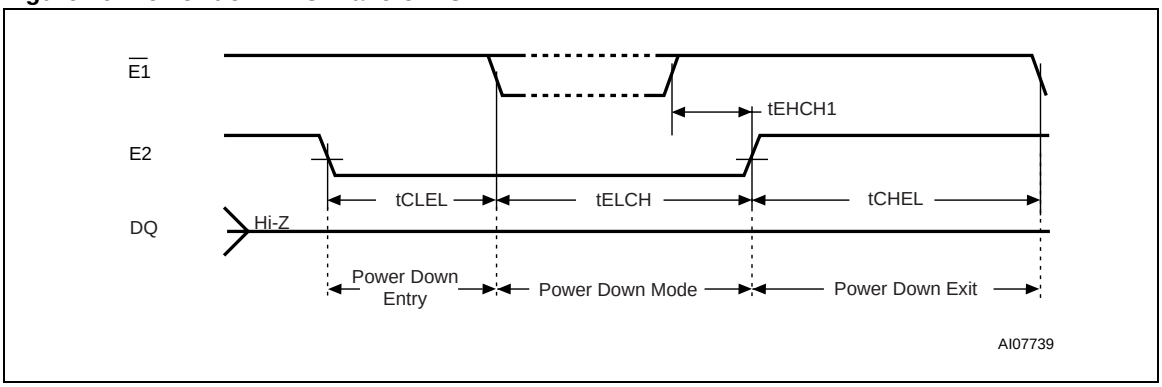
Note: 1. Some data may be written to any address location if t_{EHWH} is less than the minimum required time.
2. The device has to enter and exit Power Down mode after t_{CHCL}.
3. The Input Transition Time used in AC measurements is 5ns.

Figure 18. Standby Mode Entry AC Waveforms, After Read or Write



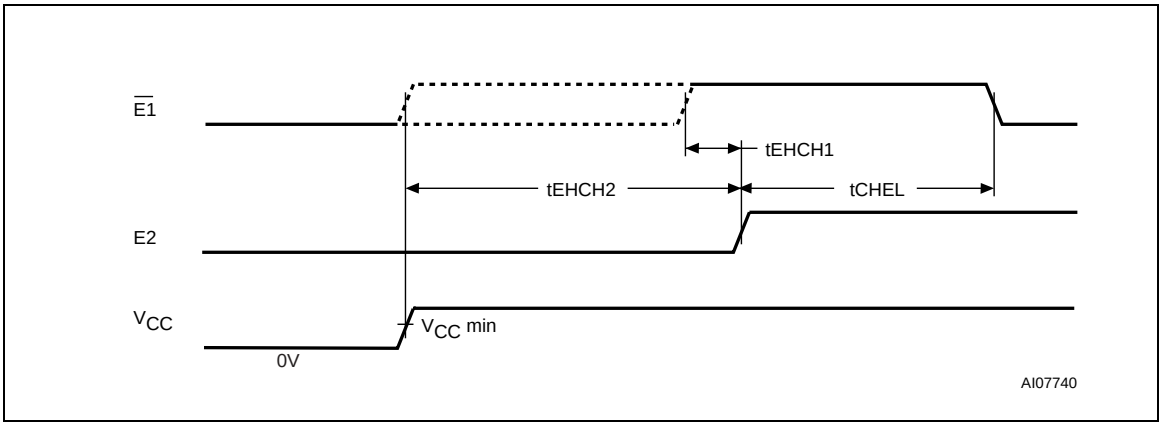
Note: Both t_{EHGH} and t_{EHWH} define the earliest entry timing for Stand-by mode. If either of timing is not satisfied, it takes the t_{AVAX}(min) period from either the last address transition of A0, A1 and A2, or $\overline{E1}$ rising edge.

Figure 19. Power-down AC Waveforms



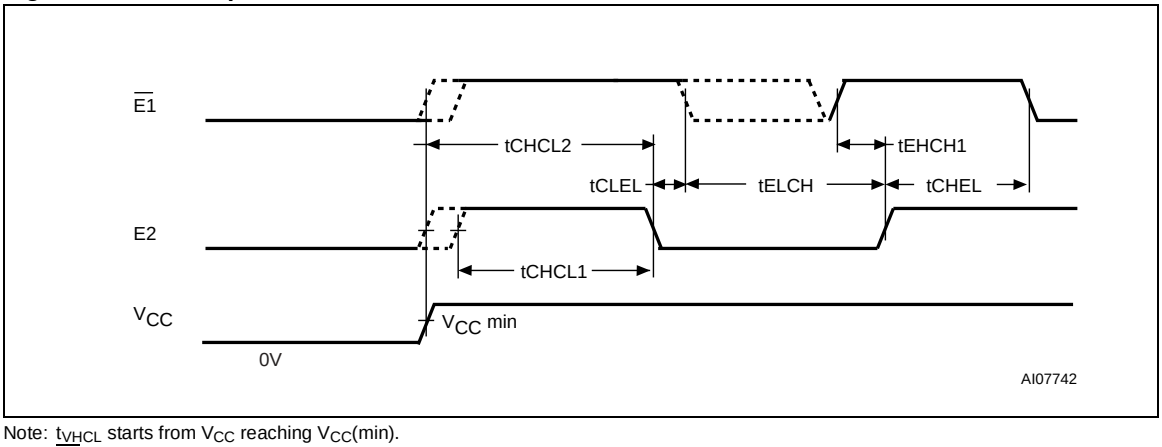
Note: This Power Down mode can be also be used in “Power-up Mode AC Waveforms - 2”.

Figure 20. Power-up Mode AC Waveforms - 1



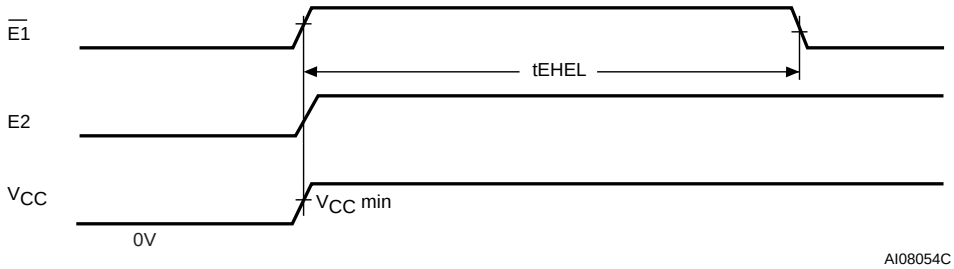
Note: t_{VHCH} starts from V_{CC} reaching V_{CC}(min).

Figure 21. Power-up Mode AC Waveforms - 2



Note: t_{VHCL} starts from V_{CC} reaching V_{CC}(min).
$\overline{E1}$ must be taken High prior to, or together with, the rising edge on E2.

Figure 22. Power-up Mode AC Waveforms - 3



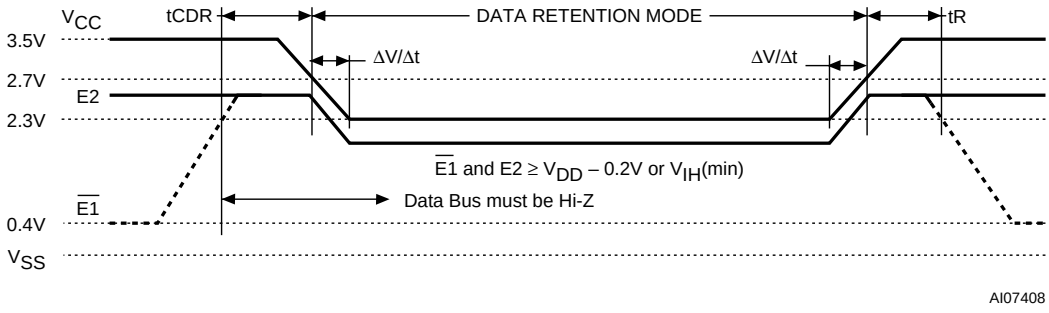
Note: Both $\overline{E1}$ and E2 must go High as V_{CC} reaches V_{CC}(min). If not, the timings provided in Power-Up Mode AC Waveforms 1 (Figure 20.) or Power-Up Mode AC Waveforms 2 (Figure 21.) should be used to ensure proper operation.

Table 10. Low V_{CC} Data Retention Characteristics

Symbol	Parameter	Test Condition[1]	Min	Max	Unit
V_{DR} (2)	Supply Voltage (Data Retention)	$\overline{E1}$ = E2 ≥ V_{CC} –0.2V, or $\overline{E1}$ = V_{IH} and E2 = V_{IH}	2.3	3.5	V
I_{CCDR}	Supply Current (Data Retention)	V_{CC} = V_{DR}, V_{IN} ≤0.2V or ≥ V_{CC} –0.2V, $\overline{E1}$ = ≥ V_{CC} –0.2V and E2 ≥ V_{CC} –0.2V, I_{OUT} = 0mA		70	µA
t_{CDR} (2,3)	Chip deselected to Data Retention Time	V_{CC} = 2.7V	0		ns
t_R (3)	Operation Recovery Time	V_{CC} = 2.7V	100		ns
$\Delta V/\Delta t$ (3)	VCC Voltage Transition Time		0.2		V/µs

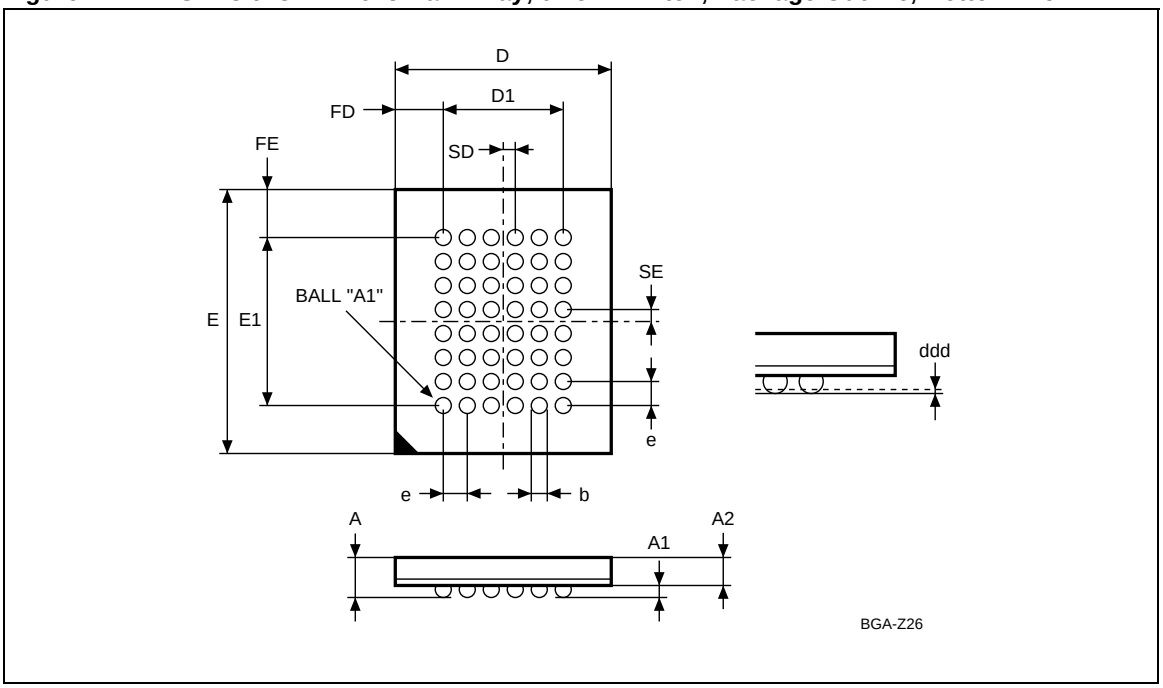
Note: 1. T_A = –30 to 85°C
2. All other Inputs at V_{IH} ≥ V_{CC} –0.2V or V_{IL} ≤0.2V.
3. See Figure 23. for measurement points.

Figure 23. Low V_{CC} Data Retention AC Waveforms



PACKAGE MECHANICAL

Figure 24. TFBGA48 6x8mm - 6x8 Ball Array, 0.75mm Pitch, Package Outline, Bottom View



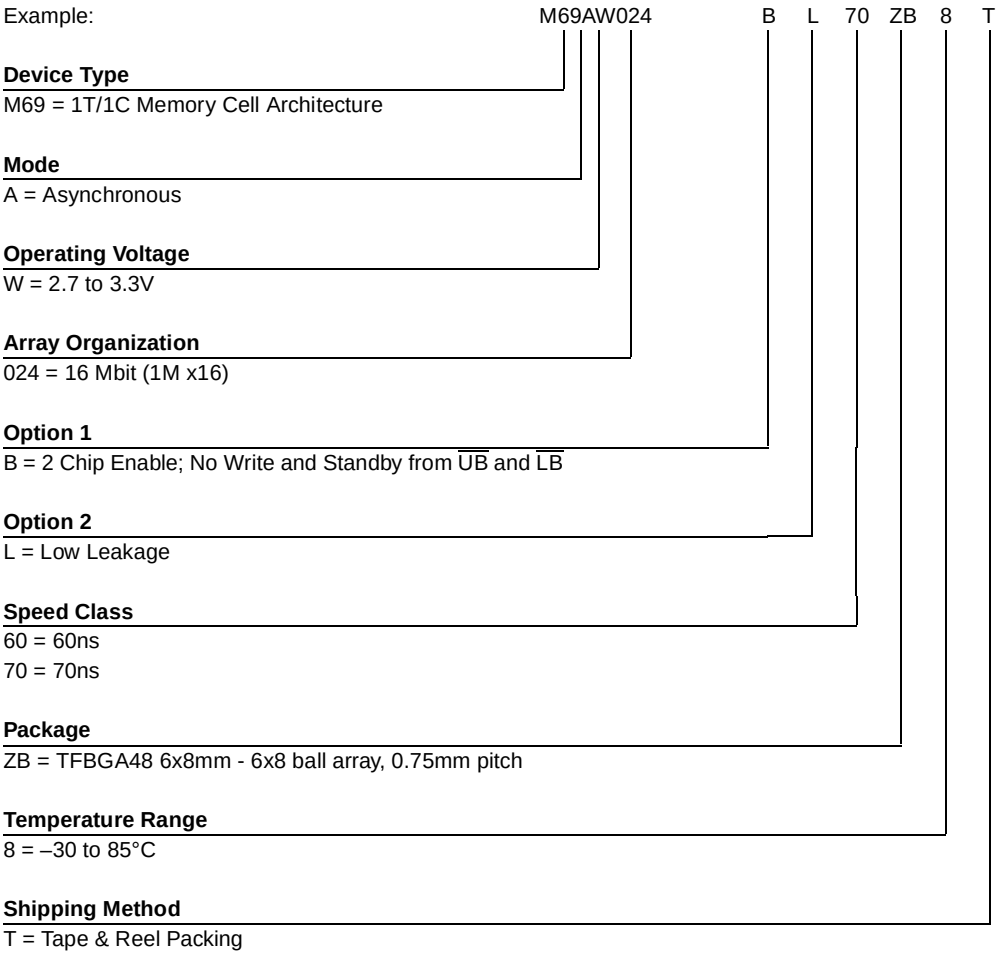
Note: Drawing is not to scale.

Table 11. TFBGA48 6x8mm - 6x8 Ball Array, 0.75mm Pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	3.750	–	–	0.1476	–	–
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.250	–	–	0.2067	–	–
e	0.750	–	–	0.0295	–	–
FD	1.125	–	–	0.0443	–	–
FE	1.375	–	–	0.0541	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

PART NUMBERING

Table 12. Ordering Information Scheme



The notation used for the device number is as shown in Table 12. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest STMicroelectronics Sales Office.

REVISION HISTORY

Table 13. Document Revision History

Date	Rev.	Revision Details
01-Jun-2002	1.0	First Issue
04-Feb-2003	2.0	Document completely revised
14-Mar-2003	2.1	AC Testing Load Circuit revised; 60ns access time device added
29-Apr-2003	2.2	Timing parameter names changed in tables and illustrations
25-Jul-2003	2.3	Chip enable signals $\overline{E1}$ and E2 must change together during Power-on sequence
07-May-2004	3.0	Datasheet title updated. Table 2., Operating Modes updated for read operations.
29-Sep-2004	4.0	Minor modification in first paragraph of Summary Description.