RFMD

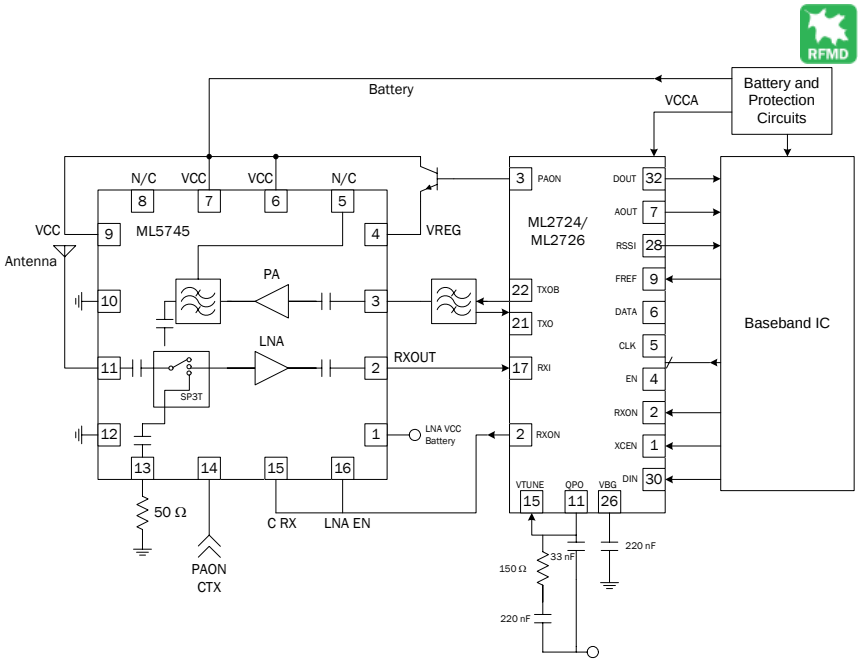
rfmd.com

Proposed

SRF-2724CS

2.4GHZ LOW-IF 1.5MBPS FSK TRANSCEIVER

Package: 7mmx7mmx1mm



Functional Block Diagram

Features

- Complete 2.4GHz Transceiver
  - High Data Rate (1.5Mbps)
  - 81dBm Sensitivity at 0.1% BER (Typ.)
  - 3dBm Output Power (Differential, Typ.)
- Closed Loop TX Modulation
- Low IF Receiver: No External IF Filters Required
- Fully Integrated Frequency Synthesizer:
  - No External Resonator Required
- Sigma-Delta Fractional-N Two-Port Modulator
- Automatic Filter Alignment
  - No Manufacturing Adjustments Required
- No External Data Slicer Components Required
- Control Outputs Correctly Sequence and Control PA
- Three-Wire Control Interface
- Analog RSSI Output

Applications

- 2.4GHz FSK Data Transceivers
  - Digital Cordless Telephones
  - Wireless PC Peripherals
  - Wireless Game Controllers
  - Wireless Streaming Media

Product Description

The SRF-2724CS is a fully integrated 1.5Mbps frequency shift keyed (FSK) transceiver that operates in the unlicensed 2.4GHz ISM frequency band. The device has been optimized for digital cordless telephone application and includes all the frequency generation, receive, and transmit functions. Automatically adjusted filters eliminate mechanical tuning. Closed loop modulation eliminates frequency drift and permits practically unlimited TX duration. The transmitter generates a 3dBm FSK output signal.

The 1.5Mbps data rate permits data spreading, such as Direct Sequence Spread Spectrum (DSSS) modulation, which improves range. The dual conversion Low-IF receiver has all of the sensitivity and selectivity advantages of a traditional superheterodyne without advantages of a traditional super heterodyne without requiring costly, bulky external filters, while providing the integration advantages of direct conversion.

The phase locked loop (PLL) synthesizer is completely integrated, including the voltage controlled oscillator (VCO), tuning circuits, and VCO resonator. This allows the SRF-2724CS to be used in frequency hopped spread spectrum (FHSS) applications.

The SRF-2724CS contains internal voltage regulation. It also contains PLL and transmitter configuration registers. The device can be placed in a low power standby mode for current sensitive applications.

Optimum Technology Matching® Applied

☐ GaAs HBT	☑ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Absolute Maximum Ratings

Parameter	Rating	Unit
VCCA, VDD	5.5	V
Junction Temperature	150	°C
Storage Temperature Range	-65 to +150	°C
Lead Temperature (Soldering, 10s)	260	°C
Normal Temperature Range	-10 to +60	°C
VCCA Range	2.7 to 4.5	V
VDD Range	2.7 to 3.3	V
Thermal Resistance	70	°C/W

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

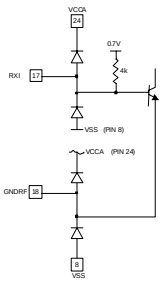
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					VCCA=VDD=3.3V, T_A=25°C, f_{REF}=6.144MHz, Data Rate=1.536Mbps, 13kHz Loop Filter as shown in Figure 1
Power Consumption					
Analog Supply (VCCA)	2.7	3.3	4.5	V	
Digital Supply Voltage	2.7		3.3	V	VDD pin (VCCA ≥ VDD always)
Bandgap Voltage		1.23		V	VBG pin 26, I_O=0µA
Supply current, STANDBY Mode		10	120	µA	DC supply connected, XCEN low
Supply current, RECEIVE Mode		55	76	mA	RX chain active, data being received
Supply current, TRANSMIT Mode		50	76	mA	P_{OUT}=3dBm
Gain Variation					
Carrier frequency range	2.4		2.485	GHz	
Channel Spacing		2048		kHz	
Charge Pump sink/source current		±5.5		mA	
Phase noise at TXO					Closed loop, loop fitter bandwidth 13kHz (See Figure 1)
1.2MHz		-95		dBc/Hz	
3MHz		-115		dBc/Hz	
>7MHz		-125		dBc/Hz	
Lock time for channel switch					From EN asserted to RX valid data (RX), or PAON high (TX)
1 Channel		110	125	µS	
5 Channels		185	220	µS	
Full Range		250	300	µS	
Lock time for TX/RX		70	120	µS	RXON High to Valid RX data
Lock time for RX/TX		63	75	µS	RXON Low to PAON high
Lock up time from standby		240	325	µS	XCEN high to Valid RX data, XCEN low period>120 seconds
Reference signal frequency		6.144		MHz	
		12.288		MHz	
Reference signal input level	2.0		VCC	VPP	6.144MHz or 12.288MHz sine wave, capacitively coupled

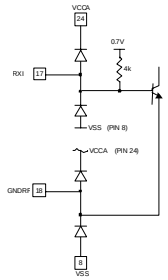
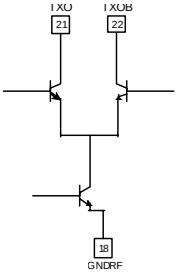
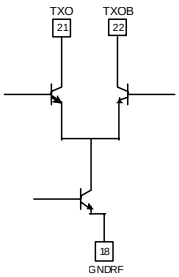
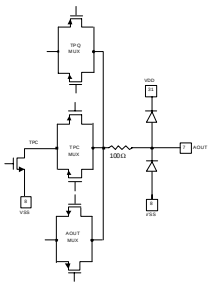
7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					VCCA=VDD=3.3V, T_A=25°C, f_{REF}=6.144MHz, Data Rate=1.536Mbps, 13kHz Loop Filter as shown in Figure 1
Receiver					
Receiver input impedance		2.2 + j0		Ω	f_C=2445MHz
Receiver noise figure		16.5		dB	f_C=2445MHz
Data Rate		1.536		Mbps	FSK modulation, f_{DEV}=±512kHz
Input Sensitivity	-82	-90		dBm	<12.5% CER at 1.536Mchip/s
		-81		dBm	<0.1% BER at 1.536Mbps
Bandwidth		770		kHz	3dB Bandwidth
Maximum RX RF input	+5			dBm	<12.5% CER at 1.536Mchip/s
	-4			dBm	<0.1% BER at 1.536Mb/s
Receiver Input IP3		-15		dBm	Test tones 2 and 4 channels away
LO leakage at RX1		-60		dBm	
Mixer Image Rejection Ratio		35		dB	Measured at 3.5MHz offset
Adjacent channel rejection					-80dBm wanted signal <10_{-3} BER. Single 2GFSK modulated interferer with a 1.5MHz - 20dBc bandwidth
		6		dB	1 channel away
		31		dB	2 channels away
		36		dB	3 or more channels away
IF Filters					
IF filter center frequency		1.024		MHz	After Automatic Filter Alignment
IF filter 3dB bandwidth		1405		kHz	After Automatic Filter Alignment
Limiter, AGC, and FMD Demodulator					
Recovery from overload		5	12	µs	From +15dBm at input
Eb/No		10.5		dB	For 0.1% BER
Co-Channel, 0.1% BER		10.5		dB	-80dBm, modulated with 1.536Mbps GFSK, BT=0.5, PRBS data
Quiescent voltage at AOUT		1.1		V	
Output voltage swing AOUT	0.55		1.1	V_{PP}	
AOUT open-drain voltage			0.4	V	I_O=100µA, TPD mode
RSSI Performance					
RSSI rise time. No Signal to -15dBm into the IF mixer		4.5		µs	20pF load, 20% to 80%
RSSI fall time, <-15dBm to No Signal into the IF mixer		3.0		µs	20pF load, 20% to 80%
RSSI sensitivity	28	36	42	mV/dB	(V_{-40dBm} - V_{-60dBm})/20dB
RSSI maximum voltage	1.8	2.3		V	See Figure 3
RSSI midrange voltage	1.4	1.7	20	V	-40dBm into RXI
RSSI minimum voltage		75		mV	No signal into RXI
RSSI maximum voltage (clipped)	1.6	1.95		V	-10dBm into RX1
Transmit RF Mixer					
Output power, single ended	-3	1	5	dBm	TRXO or TRXOB, f_C=2.445GHz
Output power, differential	-1	3	6	dBm	$P_{(TRXO, TRXOB)}$, f_C=2.445GHz
Output impedance		12 + j0		Ω	TRXO or TRXOB, f_C=2.445GHz

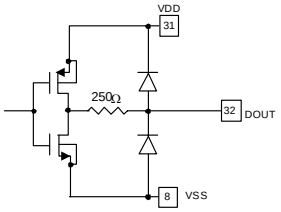
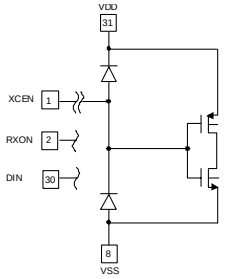
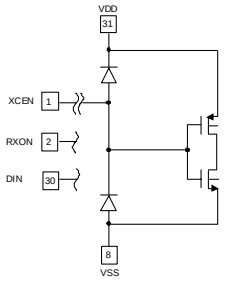
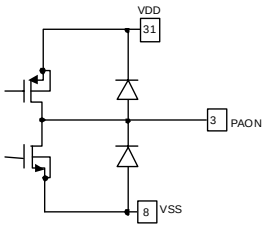
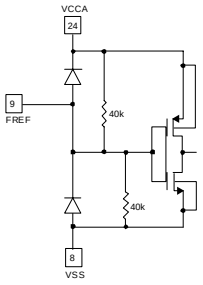
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					VCCA=VDD=3.3V, T_A=25°C, f_{REF}=6.144MHz, Data Rate=1.536Mbps, 13kHz Loop Filter as shown in Figure 1
Transmit Modulation					
Modulation Deviation at 2.4GHz	500	512	524	kHz	200uS of consecutive '1's of '0's
Modulation center frequency offset	-50		+50	kHz	50us after RXON low
Transmit Data Filter					
Transmit Data Filter Bandwidth		1.4		kHz	3dB Bandwidth
TX spurious		-25		dBc	
TX spurious image		-20		dBc	
Interface Logic Levels					
Input (DIN, XCEN, RXON, DATA, CLK, EN)					
Input high voltage	0.75*VDD		VDD	V	never exceed VDD
Input low voltage	0		0.25*VDD	V	
Input bias current	-5	0	5	µA	
Input capacitance		4		pF	measured at 1MHz
Outputs (DOUT, PAON)					
DOUT high voltage	VDD-0.4			V	I_O=0.1mA
DOUT low voltage			0.4	V	I_O=0.1mA
DOUT sink/source current	0.1			mA	
PAON output high voltage	VDD-0.4			V	Sourcing 0.5mA
PAON output low voltage			0.4	V	Sinking 0.5mA
PAON source/sink current	0.5			mA	
Three-Wire Serial Bus Timing					See Figure 4
CLK input rise time			15	ns	
CLK input fall time			15	ns	
CLK period	50			ns	
CLK pulse width	100			ns	
Delay from last CLK falling edge	15			ns	
EN setup tome to ignore next rising CLK	15			ns	
DATA-to-CLK setup time	15			ns	
DATA-to-CLK hold time	15			ns	

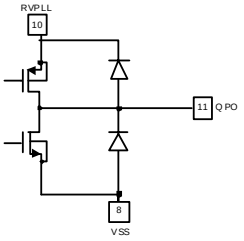
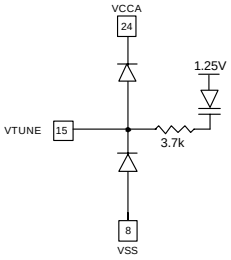
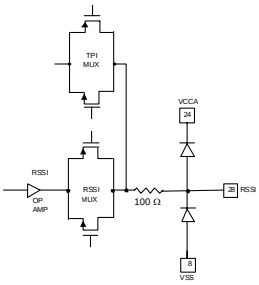
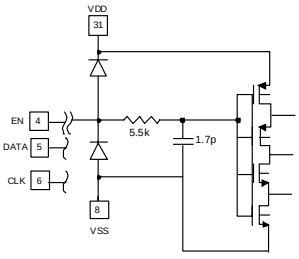
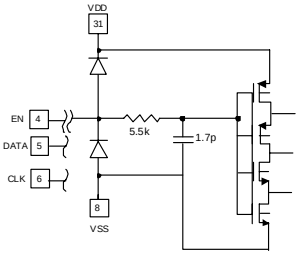
7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Pin	Function	Description	Interface Schematic
		Power and Ground	
8	VSS	Digital Ground. Ground for digital I/O circuits and control logic	
10	RVPLL	PLL Supply. DC power supply decoupling point for the PLL dividers, phase detector, and charge pump. This pin is connected to the output of the regulator and to the PLL supplies. There must be a 220nF capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator.	See Pin 11 below.
12	GNDPLL	Ground for the PLL dividers, phase detector, and charge pump.	
13	VVREG	DC Power Supply Input to the VCO voltage regulator. Must be connected to RVQMIF (pin 27) or RVDMD (pin 29) via decoupling network.	
14	RVVCO	DC power supply decoupling point for the VCO. Connected to the output of the VCO regulator. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
16	GND	DC ground for VCO and LO circuits.	
18	GNDRF	Ground return for the Receive RF input and the Transmit RF output.	
19	GDNRXMX	Signal ground for the Receive mixers.	
20	GNDRXMX2	Signal ground for the Receive mixers.	
23	RVLO	DC power supply decoupling point for the LO Chain. Connected to the output of a regulator. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
24	VCCA	DC power supply Input to Voltage Regulators and unregulated loads: 2.7 to 3.8V. VCCA is the main (or master) analog VCC pin. There must be capacitors to ground from this pin to decouple (bypass) supply noise.	
25	GNDDMD	DG ground to IF, Demodulator, and Data Slicer circuits.	
27	RVQMIF	DC power supply decoupling point for Quadrature Mixer and IF filter circuits. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
29	RVDMD	DC power supply decoupling point for IF, Demodulator, and Data Slicer circuits. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
31	VDD	DC power supply input to the interface logic and control registers. This supply is not connected internally to any other supply pin, but its voltage must be less than or equal to the VCCA supply and greater than 2.7V. A capacitor must be tied between this pin and ground to decouple (bypass) noise.	

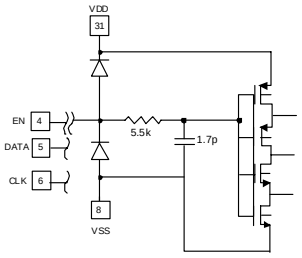
Pin	Function	Description	Interface Schematic
		Transmit/Receive	
17	RX1	Receive RF Input. Nominal impedance at 2445MHz is 2.6-j2.6 with a simple matching network required for optimum noise figure. This input connects to the base of an NPN transistor and should be AC coupled.	
21	TXO	TX RF open-collector output. This output requires a DC path to VCCA.	
22	TXOB	Complementary TX RF open-collector output. This output requires a DC path to VCCA. For single-ended output applications, this pin should be connected to a dummy load that includes a DC path to VCCA.	
		Data	
7	AOUT	Multi-function Output. In Analog output mode this is output drives an off chip data slicer. In Transmit power control mode this is an open drain output, which is pulled low when the TPC bit is serial register #1, is clear. Transitions on TPC are synchronized to the falling edge of RXON. In analog test modes this pin and the RSSI output become test access points controlled by the serial control bus.	
30	DIN	Transmit Data Input. Drives the transmit pulse shaping circuits. Serial digital data on this pin becomes FSK modulation on the Transmit RF output. The logic timing on this pin controls data timing. Internal circuits determine the modulation deviation. This is a standard CMOS input referenced to VDD and VSS.	See Pin 1 below.

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

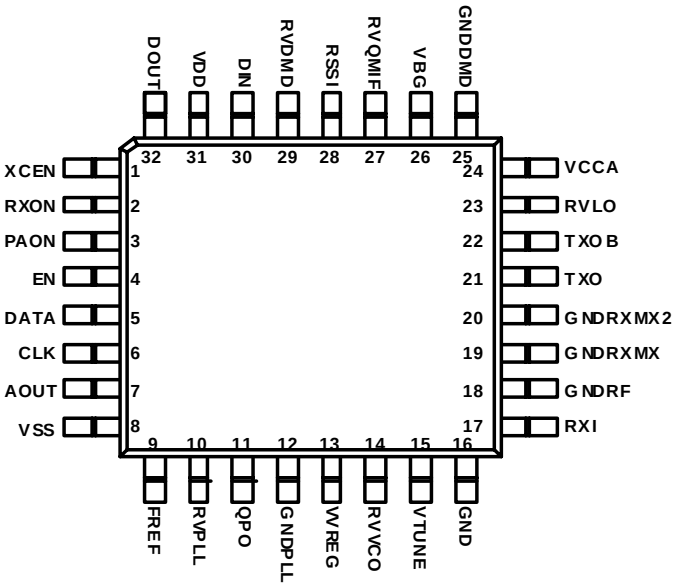
Pin	Function	Description	Interface Schematic
		Data, cont.	
32	DOUT	Serial digital output after demodulation, chip rate filtering and center data slicing. A CMOS level output (VSS to VDD) with controlled slew rates. A low drive output designed to drive a PCB trace and a CMOS logic input while generating minimal RFI. In digital test modes this pin becomes a test access port controlled by the serial control bus.	
		Mode Control and Interface Lines	
1	XCEN	Enables the bandgap reference and voltage regulators when high. Consumes only leakage current in STANDBY mode when low. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
2	RXON	TX/RX Control Input. Switches the transceiver between TRANSMIT and RECEIVE modes. Circuits are powered up and signal paths reconfigured according to the operating mode. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
3	PAON	PA Control Output. Enables the off-chip PA at the correct times in a Transmit slot. Goes high when transmit RF is present at TXO; goes low 5µs before transmit RF is removed from TXO. Has interlock logic to shut down the PA if the PLL does not lock.	
9	FREF	Input for the 12.288MHz or 6.144MHz reference frequency. This input is used as the reference frequency for the PLL and as a calibration frequency for the on-chip filters. An AC-coupled sine or square wave source drives this self-biased input.	

Pin	Function	Description	Interface Schematic
		Mode Control and Interface Lines, cont.	
11	QPO	Charge Pump Output of the phase detector. This is connected to the external PLL loop filter.	
15	VTUNE	VCO Tuning Voltage input from the PLL loop filter. This pin is very sensitive to noise coupling and leakage currents.	
26	VBG	Bandgap Decouple Voltage. Decoupled to ground with 220nF capacitor.	
28	RSSI	Buffered Analog RSSI output with a nominal sensitivity of 35mV/dB. In analog test modes, this pin and the AOUT output become test access points controlled by the serial control bus.	
		Serial Bus Signals	
4	EN	Control Bus Enable. Enable pin for the three-wire serial control bus that sets the operating frequency and programmable options. The control registers are loaded on a low-to-high transition of the signal. Serial control bus data is ignored when this signal is high. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
5	DATA	Serial Control Bus Data. 16-bit words, which include programming data and the two-bit address of a control, register. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Pin	Function	Description	Interface Schematic
		Serial Bus Signals, cont.	
6	CLK	Serial control bus data is clocked in on the rising edge when EN is low. This is a CMOS input; the thresholds are referenced to VDD and VSS.	

Pin Diagram



Simplified Application Diagram

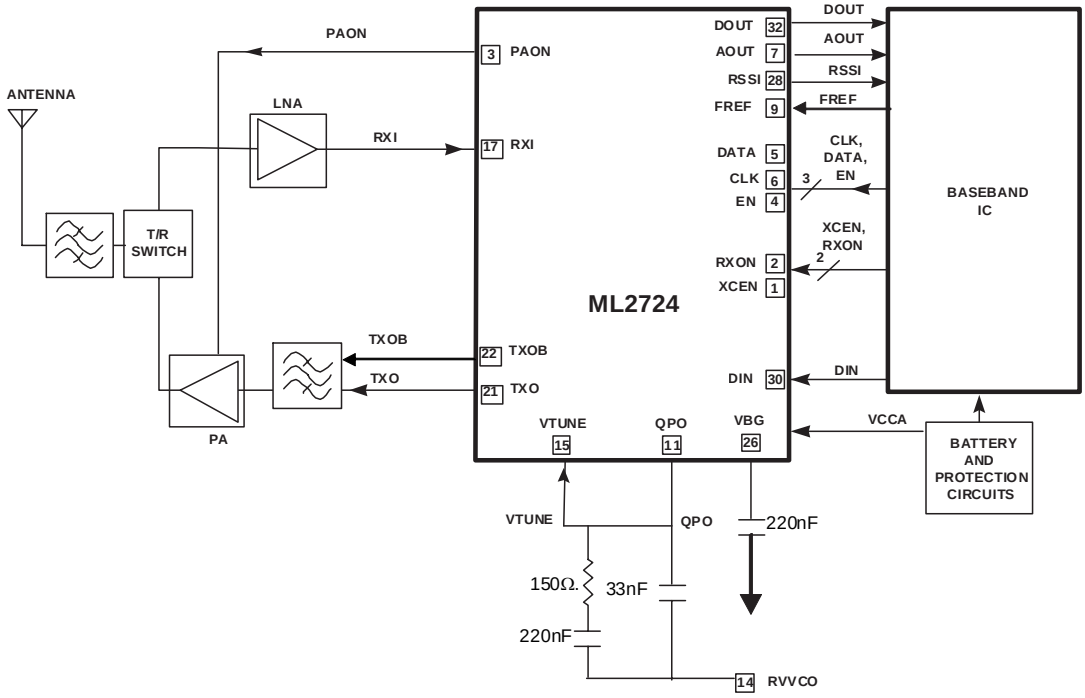


Figure 1: Typical SRF-274CS Application Diagram

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Functional Description

The SRF-2724CS is a fully integrated 1.5 Mbps frequency shift keyed (FSK) transceiver that operates in the unlicensed 2.4 GHz ISM frequency band. The device has been optimized for digital cordless telephone applications and includes all the frequency generation, receive and transmit functions for a raw data rate of 1.5 Mbps. This high data rate allows for data spreading, such as Direct Sequence Spread Spectrum (DSSS) modulation, which improves range. The SRF-2724CS receiver architecture is a dual conversion Low IF, which has all of the sensitivity and selectivity advantages of a traditional super-heterodyne receiver without requiring costly, bulky external filters.

The RF mixer down-converts the 2.4 GHz RF input signal to the first intermediate frequency (IF), where it is filtered to remove adjacent channel signals. An active image reject mixer converts this signal down to a Low IF frequency, where the data is limited, filtered, and demodulated. This architecture provides all the benefits of direct conversion to baseband while maintaining the stability and robustness of a traditional super-heterodyne.

A single synthesizer is used for both the receiver and the FSK transmitter. The phase locked loop (PLL) is completely integrated, including the voltage controlled oscillator (VCO), tuning circuits, and VCO resonator.

In RECEIVE MODE, the SRF-2724CS is a dual conversion Low IF receiver. No external SAW filters are required. The integrated image reject mixer gives sufficient rejection in this channel. All channel filtering and demodulation is performed using active filters, which are automatically aligned. A matched bit rate filter and a data slicer follow the demodulator. The sliced data is provided at the DOUT pin, and the analog data is available at AOUT.

In TRANSMIT MODE, the SRF-2724CS generates a 2.4 GHz output using the transmit mixer. An auto-aligned transmit data filter and modulation compensation circuit results in an adjustment-free transmitter. The VCO is modulated by the transmit data, which is put through a sigma-delta fractional-N PLL ensuring modulation accuracy. This modulation occurs while the phase locked loop is closed, thus allowing practically infinite transmit or receive times with excellent frequency accuracy and stability. A 3 dBm FSK-modulated differential signal is output at the TXO/TXOB pins at the 2.4 GHz carrier frequency.

The integrated PLL frequency synthesizer includes a fully integrated VCO, prescaler, phase detector and charge pump. The reference frequency is generated from the incoming signal at the FREF pin, which can be either 6.144 MHz or 12.288 MHz. The loop filter is external to allow customers to optimize their loop bandwidth to their system's lock time and in-band phase noise requirements. This frequency-agile synthesizer allows the SRF-2724CS to be used in frequency hopped spread spectrum (FHSS) applications with nominal channel spacing of 2.048 MHz. Carrier frequency is programmed via the configuration registers and 3-wire serial interface. The VCO tank circuit (inductor and varactor) is fully integrated.

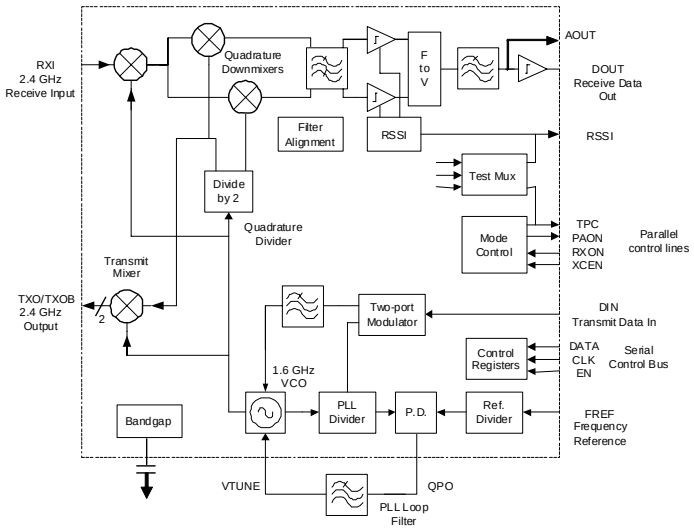
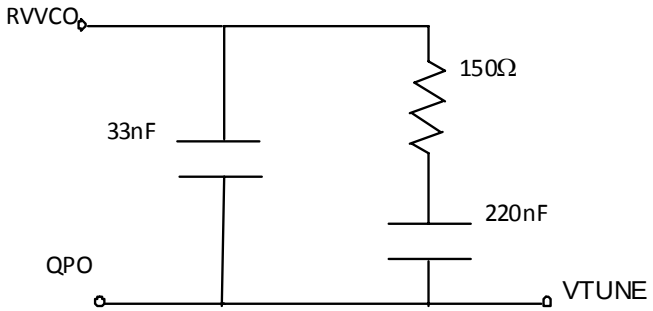


Figure 2: SRF-2724CS Internal Block Diagram

Example: 13kHz Loop Filter



Modes of Operation

There are three key modes of operation:

- STANDBY:All circuits powered down, except the control interface (Static CMOS)
- RECEIVE:Receiver circuits active
- TRANSMIT:Modulated RF output from IC

The two operational modes are RECEIVE and TRANSMIT, controlled by RXON. XCEN is the chip enable/disable control pin, which sets the part in operational or STANDBY modes. The relationship between the parallel control lines and the mode of operation of the IC is given in Table 1:

Table 1

XCEN	RXON	Mode	Function
0	X	STANDBY	Control interfaces active, all other circuits powered down
1	1	RECEIVE	Receiver time slot
1	0	TRANSMIT	Transmit time slot

Mode Control

The SRF-2724CS is intended for use in TDD and TDMA radios in battery-powered equipment. To minimize power consumption it is designed to switch rapidly from a low power mode (STANDBY) to an active mode. The SRF-2724CS can also make a quick transition from receive to transmit for TDD operation. Prior to transmitting or receiving, time should be allowed for the PLL to lock and for the filters to align. When the SRF-2724CS is operated in single-carrier TDD mode, the LO is automatically shifted by the second (low) IF frequency when the device is switched between RECEIVE and TRANSMIT modes.

SRF-2724CS carrier frequency can be changed (hopped) at any time, but is usually changed between transmissions. Carrier frequency (channel) is modified in the SRF-2724CS by writing a corresponding new value to the PLL frequency register (Register 1)

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Receive

The SRF-2724CS uses a double-conversion super-heterodyne receiver with a nominal second IF of 1.024MHz. The signal flow in RECEIVE mode is from the RF input, through an RF down-conversion mixer and integrated IF filter, image reject quadrature mixer, integrated Low IF filter, hard limiter, frequency to voltage converter, and data filter to the AOUT pin and data slicer where the digital NRZ data is available at the DOUT pin. A 20dB step AGC extends the dynamic range of the receiver. The SRF-2724CS receive chain is a Low IF receiver using advanced integrated radio techniques to eliminate external IF filters and minimize external RF filter requirements. The precision filtering and demodulation circuits give improved performance over conventional radio designs using external filters while providing integration comparable to advanced direct conversion radio designs.

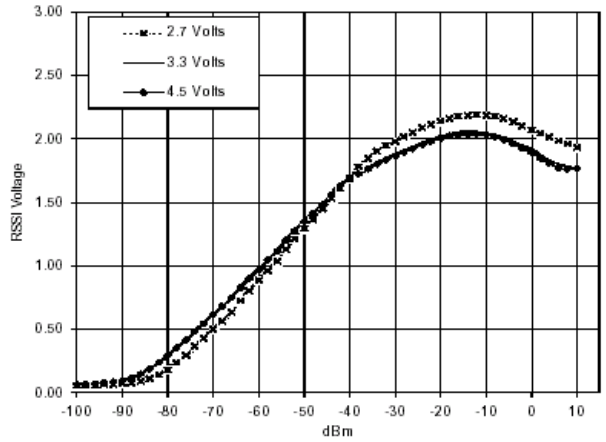


Figure 2. RSSI Output Voltage vs Input Signal Level (Clipped, 25°C, Various Input Voltage Levels)

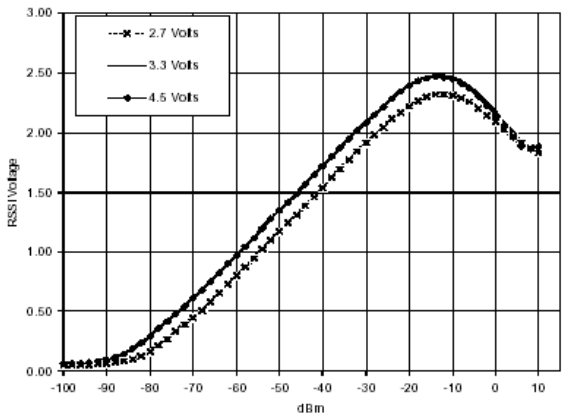


Figure 2a. RSSI Output Voltage vs Input Signal Level (Unclipped, 25°C, Various Input Voltage Levels)

Figure 3: RSSI Voltage versus Input Signal Level

Automatic Filter Alignment

When the SRF-2724CS is placed in RECEIVE mode, it automatically tunes all the internal filters using the reference frequency from the FREF pin. When the chip is powered up (VDD first applied), the tuning information is reset to mid-range. This self-calibration sets:

- Discriminator center frequency
- IF filter center frequency and bandwidth
- Receiver data low-pass filter bandwidth
- Transmit data low-pass filter bandwidth

Transmit Mode

In TRANSMIT mode, the PLL is closed to eliminate frequency drift. A two-port modulator modulates both the VCO and the fractional-N PLL. The VCO is directly modulated with filtered FSK transmit data. The PLL is driven by a sigma-delta modulator, which ensures that the PLL follows the mean frequency of the modulated VCO.

The transmit modulation filter is automatically tuned during every RECEIVE time, alleviating the need for production alignment. Asserting RXON enables the SRF-2724CS. The rising edge of XCEN triggers a complete calibration of all the on-chip filters, which takes up to 256μs, which ensures the modulation filters are aligned to prevent unwanted spurious emissions.

PLL Programming and Channel Selection

The SRF-2724CS PLL is programmed via control register 2 to the set RF center frequency of operation of the radio. The PLL does not need to be (though it can be) reprogrammed between RECEIVE and TRANSMIT modes. Nominal channel separation is 2.048MHz, allowing for over 40 non-overlapping channels in any given location. With careful planning, channels can be programmed in 1024kHz steps as long as care is exercised to insure that two radio links will not share spectrum at any one time. The equation to determine channel center frequency from the SRF-2724CS control register word is:

fC = CHQ<0:11>*1.024MHz

Standby Mode

In STANDBY mode, the SRF-2724CS transceiver is powered down. The only circuits active are the control interfaces, which are digital CMOS to minimize power consumption. The serial control interface and control registers remain powered up and will accept and retain programming data as long as the digital supply is present. When exiting STANDBY mode, the device may need to be kept in RECEIVE mode for up to 256µs to allow for filter self-calibration.

DATA INTERFACE

There are two control interfaces: CONTROL and SERIAL.

CONTROL Interface

The control interface provides immediate control and monitoring of the SRF-2724CS. Input signals include:

- XCEN:Transceiver enable. Places the SRF-2724CS in Standby or Active (when asserted) modes.
- RXON:Receive On. Places an Active SRF-2724CS in Receive mode when asserted.
- FREF:Reference frequency input

Output signals include:

- RSSI:Received Signal Strength Indicator: indicates the power of the received signal
- PAON:External Power Amplifier Control Pin

SERIAL Interface

A 3-wire serial interface (EN, DATA, CLK) is used for programming the SRF-2724CS configuration registers, which control device mode, pin functions, PLL and reference dividers, internal test modes, and filter alignment. Data words are entered beginning with the MSB (“big-endian”). The word is divided into a leading 14-bit data field followed by a 2-bit address field. When the address field has been decoded the destination register is loaded on the rising edge of EN. Providing less than 16 bits of data will result in unpredictable behavior when EN goes high.

Data and clock signals are ignored when EN is high. When EN is low, data on the DATA pin is clocked into a shift register on the rising edge of the CLK pin. This information is loaded into the target control register when EN goes high. This serial interface bus is similar to that commonly found on PLL devices. It can be efficiently programmed by either byte or 16-bit word oriented serial bus hardware. The data latches are implemented in CMOS and use minimal power when the bus is inactive. Refer to Figure 4 and Table 2: 3-Wire Bus Timing Characteristics for timing and register programming illustrations.

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Table 2: Three-Wire Bus Timing Characteristics

Symbol	Parameter	MIN	TYP	MAX	Unit
Bus Clock (CLK)					
t_r	CLK input rise time			15	ns
t_f	CLK input fall time			15	ns
t_{ck}	CLK period	50			ns
Enable (EN)					
t_{ew}	Minimum pulse width	100			ns
t_r	Delay from last CLK rising edge	15			ns
t_{se}	Set up time to ignore next rising CLK	15			ns
Bus Data (DATA)					
t_s	Data to clock set up time	15			Ns
t_h	Data to clock hold time	15			Ns

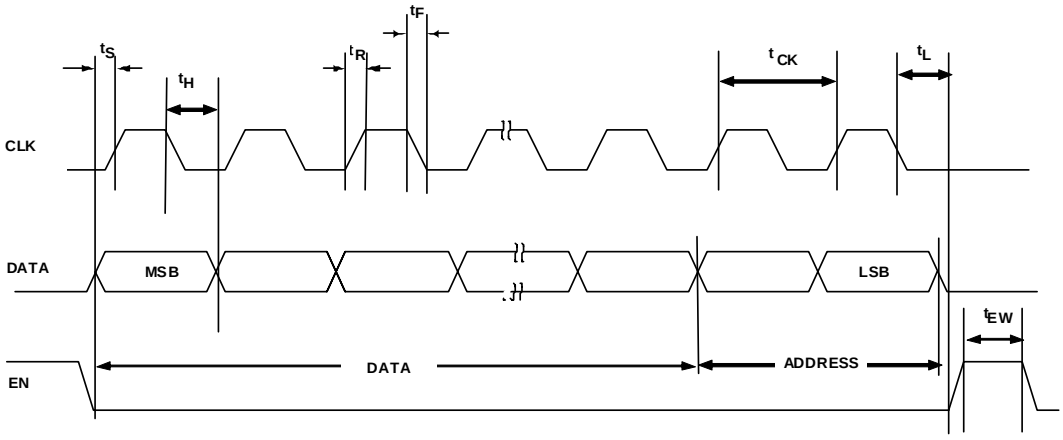


Figure 4: Serial Bus Timing for Address and Data Programming

CONTROL INTERFACES AND RESGISTERED DESCRIPTIONS

Register Information

A 3-wire serial data input bus sets the SRF-2724CS's transceiver parameters and programs the PLL circuits. Entering 16-bit words into the SRF-2724CS serial interface performs programming. Three 16-bit registers are partitioned such that 14 bits are dedicated for data to program the operation and two bits identify the register address. The contents of these registers cannot be read back via this bus.

The three registers are:

- Register 0: PLL Configuration
- Register 1: Channel Frequency Data
- Register 2: Internal Test Access

Figure 5 shows a register map. Table 3 through Table 5 provide detailed diagrams of the register organization: Table 3 and Table 4 outline the PLL configuration and channel frequency registers, and Table 5 displays the filter tuning and test mode register.

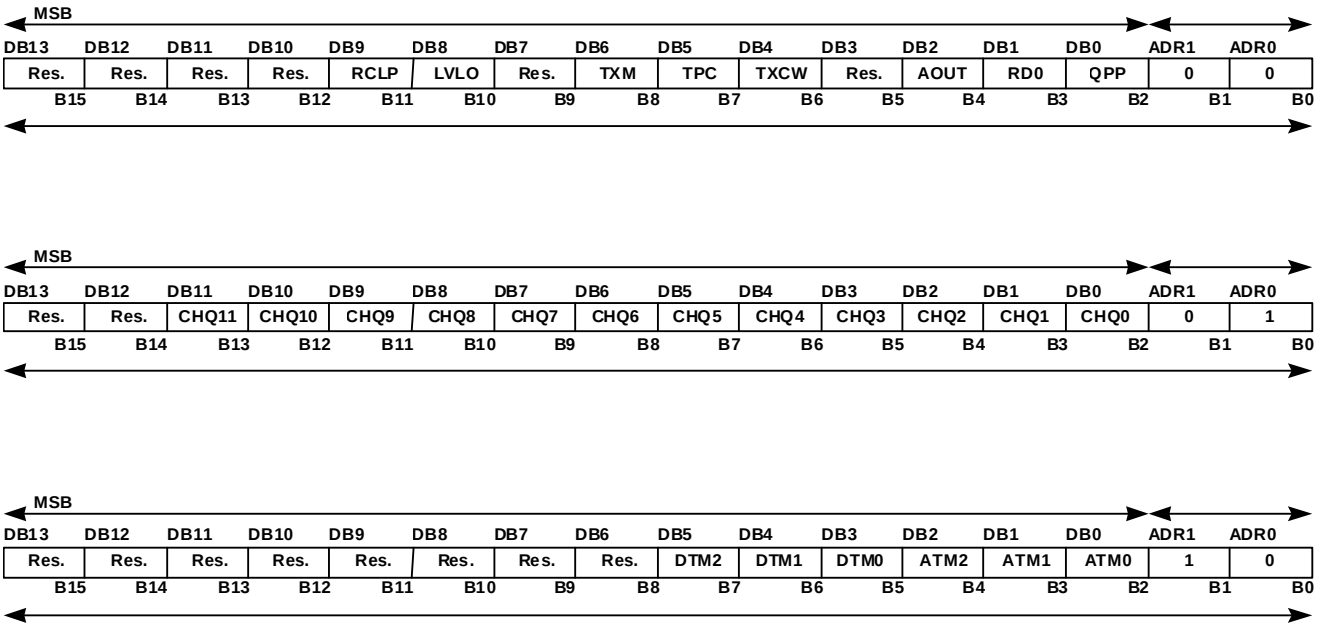


Figure 5: Configuration Register Map

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Table 3: Register 0 - PLL Configuration Register

Name	Description	Definition
Reserved	Reserved	Set all bits to 0 (zero)
Reserved	Reserved	
Reserved	Reserved	
Reserved	Reserved	
RCLP	RSSI Clip Disable	0: RSSI clipped to 1.9V at -15dBm 1: RSSI not clipped
LVLO	Low Voltage Lockout	0: PAON Undisturbed 1: PAON De-asserted for VCCA < 2.65V. Reset on RXON high
Reserved	Reserved	Set to 0
TXM	TX RF Output Mode	0: TX RF Output always on TX mode 1: TX RF Output follows PAON signal
TPC	Transmit Power Control	0: AOUT pin pulled to ground 1: AOUT pin high impedance
TXCW	Transmit Test Mode	0: FSK modulation Transmit mode 1: CW (no modulation in Transmit mode)
Reserved	Reserved	Set to 0
AOUT	Analog Output	0: AOUT pin is Transmit Power Control 1: AOUT pin is Analog Data Out
RD0	Reference Frequency Select	0: 6.144MHz nominal reference frequency 1:12.288MHz nominal reference frequency (preferred)
QPP	PLL Charge Pump Polarity	0: For fc<fref, charge pump sources current 1: For fc<fref, charge pump sinks current
ADR1	MSB Address Bit	ADR1=0
ADR0	LSB Address Bit	ADR0=0

Table 4: Register 1 - Channel Frequency Register

Name	Description	Definition
Reserved	Channel Frequency select bits	Set all bits to 0 (zero)
Reserved		
CHQ11		Divide ratio= f_C/1.024
CHQ10		
CHQ9		
CHQ8		
CHQ7		
CHQ6		
CHQ5		
CHQ4		
CHQ3		
CHQ2		
CHQ1		
CHQ0		
ADR1	MSB Address Bit	ADR1=0
ADR0	LSB Address Bit	ADR0=1

Table 5: Register 2 - Test Mode Register

Name	Description	Definition
Reserved	Reserved	Set all bits to 0 (zero)
Reserved		
Reserved		
Reserved		
Reserved		
Reserved		
Reserved		
Reserved		
DTM2	Digital Test Control Bits	See Table 16
DTM1		
DTM0		
ATM2	Analog Test Control Bits	See Table 15
ATM1		
ATM0		
ADR1	MSB Address Bit	ADR1=0
ADR0	LSB Address Bit	ADR0=1

Power-On State

On Power up, all register bits are cleared to the default value of 0 (zero). Power up is defined as occurring when VDD ≥2.0V. The register default values are valid upon power up.

CONTROL REGISTER BIT DESCRIPTIONS

ADR <1:0>, All Registers, Bits 0-1

Address Bits: The ADR<1:0> bits are the least-significant bits of each register. Each register is divided into a data field and an address field. The data field is the leading field, while the last two bits clocked into the register are always the address field. When EN goes high, the address field is decoded and the addressed destination register is loaded. The last 16 bits clocked into the serial bus are loaded into the register. Clocking in less than 16 bits results in a potentially incorrect entry into the register.

RES (Reserved), All Registers

Reserved Bits: These bits are reserved. These bits must be cleared to 0s (zeros) for normal operation. When power is reset, all of the registers' data fields are cleared to 0s (zeros).

QPP - Register 0, Bit 2

Charge Pump Polarity: This bit sets the charge pump polarity to sink or source current. For a majority of applications, this bit is cleared (QPP=0). For applications where an external inverting amplifier is used in the loop filter, this bit is set to change the charge pump polarity (see Table 6).

Table 6: PLL Charge Pump Polarity

QPP	PLL Charge Pump Polarity
0	$f_c > f_{ref}$=Charge pump sinks current
1	$f_c > f_{ref}$=Charge pump sources current

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

RD0 - Register 0, Bit 3
Reference Divide: This bit sets the reference divider from the FREF pin to the reference input of the PLL phase/frequency detector to either 9 or 18 (see Table 7).

Table 7: Reference Frequency Select

RD0	Reference Division	FREF XTAL Freq	PLL REF Freq
0	9	6.144MHz	682.67kHz
1	18	12.288MHz	682.67kHz

AOUT - Register 0, Bit 4
Analog Output Mode: This bit changes the function of the AOUT pin between an analog data output to transmit power control (see Table 8).

Table 8: AOUT Function Select

AOUT	AOUT Pin Function
0	Transmit Power Control
1	Data Filter Analog Output

TXCW - Register 0, Bit 6
Transmit Continuous Wave: This bit produces a continuous wave (CW) transmitter output for product test when RXON is low (see Table 9).

Table 9: Transmit Modulation Mode

TXCW	Transmit Modulation
0	FSK Modulation
1	CW - No Modulation

TPC - Register 0, Bit 7
Transmit Power Control: When the AOUT bit is low, this bit controls the state of the open-drain output pin. Although this bit can be changed at any time, the AOUT pin only changes state at the falling edge of RXON (see Table 10).

Table 10: TPC Pin State

TPC	TPC Pin State
0	High Impedance
1	Pulled to Ground

TXM - Register 0, Bit 8
Transmit Mode: This bit controls the TX RF buffer state timing mode. It must be reset to 0 for normal operation (see Table 11).

Table 11: TXM Mode

TXM	TXRF Buffer Behavior
0	RF Output Always On in TX Mode
1	RF Output Follows PAON

LVLO - Register 0, Bit 10
.Low Voltage Lock Out: The LVLO bit enables a transmit low voltage lockout latch, which shuts off the transmitter by de-asserting the PAON output. This latch is set if the supply voltage drops below 2.65V and is reset when the RXON control input goes high (see Table 12).

Table 12: LVLO Operation

LVLO	PAON Behavior
0	PAON Undisturbed
1	PAON de-asserted when VCCA<2.65V, Reset by RXON high

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

RCLP - Register 0, Bit 11
RSSI Clip Enable: The RCLP bit disables the RSSI clipping circuitry. With RCLP low, the RSSI output voltage is clipped to a maximum of about 2.0V at –10dBm. With RCLP high, the RSSI is not clipped. (see Table 13).

Table 13: RCLP Operation

RCLP	RSSI Behavior
0	RSSI output clipped to a maximum of ~1.9V at -15dBm
1	RSSI output not clipped

CHQ <11:0> - Register 1, Bits 2-13
Channel Frequency Selection: These bits set the RF carrier frequency for the transceiver (see Table 14). With a 6.144MHz or 12.288MHz clock at the FREF pin, the channel frequency value is calculated by multiplying the CHQ value by 1.024. The recommended operating range value of the CHQ is from 2,346 to 2,424. These bits must be programmed to a valid channel frequency before XCEN is asserted.

Table 14: Main Divider

B15	B14	B13 to B2	B1	B0
0	0	CHQ - PLL Divide Ratio	0	1

The divide ratio is calculated as fC /1.024 where fC is the channel frequency in MHz.

f_C=1.024 * CHQ

CHQ <11:0> - Register 1, Bits 2-13
Channel Frequency Selection: These bits set the RF carrier frequency for the transceiver (see Table 14). With a 6.144MHz or 12.288MHz clock at the FREF pin, the channel frequency value is calculated by multiplying the CHQ value by 1.024. The recommended operating range value of the CHQ is from 2,346 to 2,424. These bits must be programmed to a valid channel frequency before XCEN is asserted.

Table 14: Main Divider

B15	B14	B13 to B2	B1	B0
0	0	CHQ - PLL Divide Ratio	0	1

ATM <2:0> - Register 2, Bits 2-4

Analog Test Mode: The test mode selected is described in Table 15. The performance of the SRF-2724CS is not specified in these test modes. Although primarily intended for IC test and debug, they also can help in debugging the radio system. The default (power-up) state of these bits is ATM<2:0>=<0,0,0>. When a non-zero value is written to the field, the RSSI and AOUT pins become analog test access ports, giving access to the outputs of key signal processing stages in the transceiver. During normal operation, ATM<2:0> must be set to all zeros.

Table 15: Analog Test Control Bits

ATM2	ATM1	ATM0	RSSI	AOUT
0	0	0	RSSI	Set AOUT bit
0	0	1	No connect	No connect
0	1	0	IF Filter Output	Q IF Filter Output
0	1	1	Q IF Filter - ve Output	Q IF + ve Output
1	0	0	IF Filter - ve Output	IF Filter + ve Output
1	0	1	IF Limiter Outputs	Q IF Limiter Outputs
1	1	0	I IF Limiter Outputs	Q IF Limiter Outputs
1	1	1	1.67V Voltage Reference	VCO Modulation Port Input

DTM <2:0> - Register 2, Bits 5-7

Digital Test Mode: The DTM<2:0> bit functions are described in Table 16. The performance of the SRF-2724CS is not specified in these test modes. Although primarily intended for IC test and debug, they also can help in debugging the radio system. The default (power up) state of these bits is DTM<2:0>=<0,0,0>. When a non-zero value is written to these fields, the DOUT and PAON pins become a digital test access port for key digital signals in the transceiver. During normal operation, DTM<2:0> must be set to all zeros.

Table 16: Digital Test Control Bits

DTM2	DTM1	DTM0	PAON	DOUT
0	0	0	PA Control	Data Out
0	0	1	PA Control	AGC Switch State
0	1	0	PA Control	PLL Main Divider Output
0	1	1	PA Control	PLL Reference Divider Output
1	0	0	S - D Modulation LSB	Sigma - Delta Modulation MSB

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

DATA INTERFACES

Baseband Interface: DIN and DOUT

The DIN and DOUT pins are digital CMOS signals that correspond to FSK modulation of the carrier frequency. The SRF-2724CS is designed to operate as an FSK transceiver in the 2.4GHz ISM band. The frequency deviation and transmit filtering is determined in the transceiver.

Data on the DIN pin is filtered and presented to the transmit two-port modulator. There is no re-timing of the bits, so the transmitted FSK data takes its timing from the input data. In the receive chain, FSK demodulation, data filtering, and data slicing take place in the SRF-2724CS, and the digital data is output on the DOUT pin. Bit and word rate timing recovery are performed off chip. The data filter output is available on the AOUT pin for use with an optional external data slicer.

RSSI and FREF

FREF (pin 9) is the master reference frequency for the transceiver. It supplies the frequency reference for the RF channel frequency and the filter tuning. The FREF pin is a CMOS input with internal biasing resistors. It can be AC coupled to sine or square wave source. The FREF input can also be driven by a CMOS logic output. The frequency of the FREF input is limited to one of: 6.144MHz or 12.288MHz.

The Received Signal Strength Indicator (RSSI) pin supplies a voltage proportional to the logarithm of the received power level. It is normally connected to the input of a low speed ADC and is used during channel scanning to detect clear channels on which the radio may transmit. It can also be used to set transmit power to optimize power consumption while maintaining an acceptable bit error rate (BER).

PA Control Outputs (PAON and AOUT)

The PAON (PA control) is a CMOS output that controls an optional off-chip RF PA. It outputs a logic high when the PA should be enabled and a logic low at all other times. This output is inhibited when the PLL fails to lock.

AOUT (pin 7) normally supplies the analog (not data-sliced) data output, but it can also be configured as an open-drain output for transmit power control. This mode is controlled by the TPC bit in Register 0. This bit can be changed at any time, but the AOUT pin will not change mode until the beginning of the next transmit slot, triggered by a falling edge on RXON (see Figure 6 and Table 17 for details).

In analog test modes the RSSI and AOUT pins become analog test access ports that allow the user to observe internal signals in the SRF-2724CS.

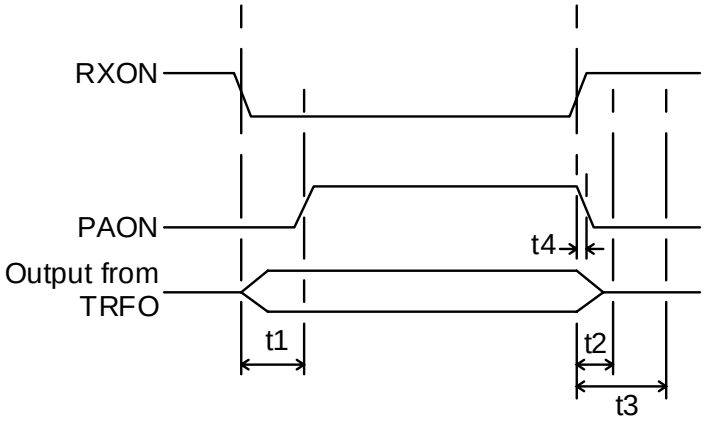


Figure 6: Power Amplifier Interface

Table 17: Power Amplifier Timing

Symbol	Parameter	Time/μS
T1	RXON falling edge to PAON rising edge	62.5
T2	RXON rising edge to PLL frequency shift	6.5
T3	RXON rising edge to RECEIVE mode	70
T4	RXON rising edge to PAON falling edge	<0.1

RF Interface: RXI and TXO/TXOB

The RXI receive input (pin 17) and the TXO/TXOB differential transmit outputs (pins 21 and 22) are the only RF I/O pins. The RXI pin requires a simple impedance matching network for optimum input noise figure. The TXO/TXOB pins require a matching network for maximum power output into the RF power amp. If a single ended output is preferred, the signal from the TXO pin can be matched to the power amp and the TXOB output can be shunted to a power supply through a dummy load. The RF input and output ground (pin 18) must have a direct connection to the RF ground plane, and the RF power supply pins must be decoupled to the same ground plane as close to the device as possible.

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Performance Graphs

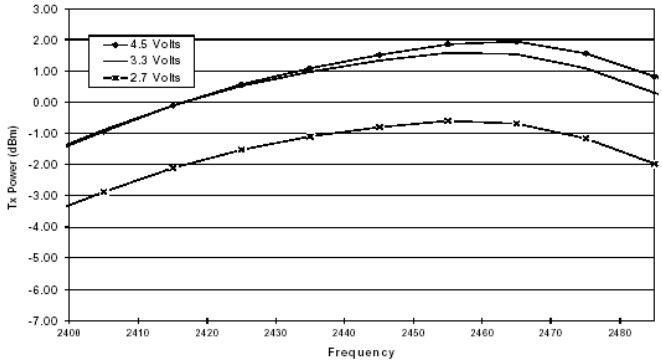


Figure 7: Output Power (Single Ended) versus Frequency

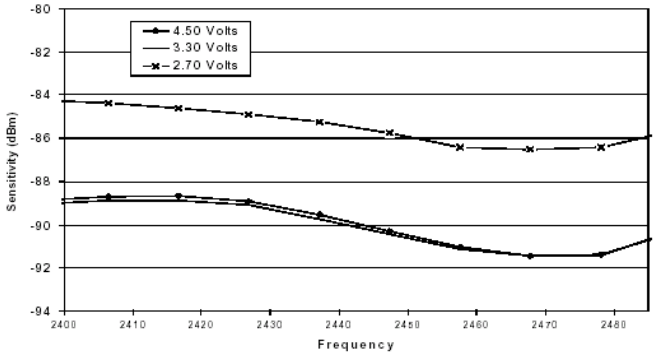


Figure 8: RX Sensitivity (12.5% BER) versus Frequency

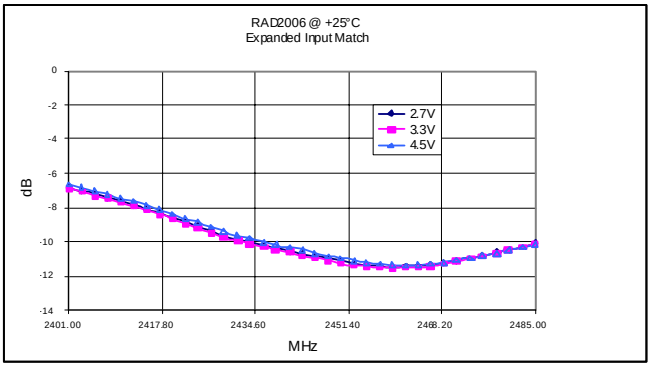


Figure 9: Input Return Loss versus Frequency and Voltage

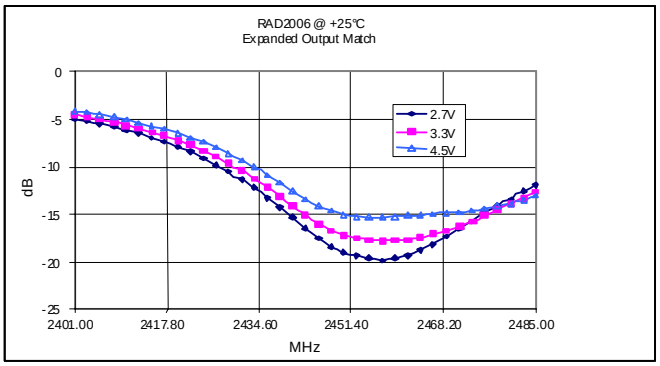


Figure 10: Output Match (SE) versus Frequency and Voltage

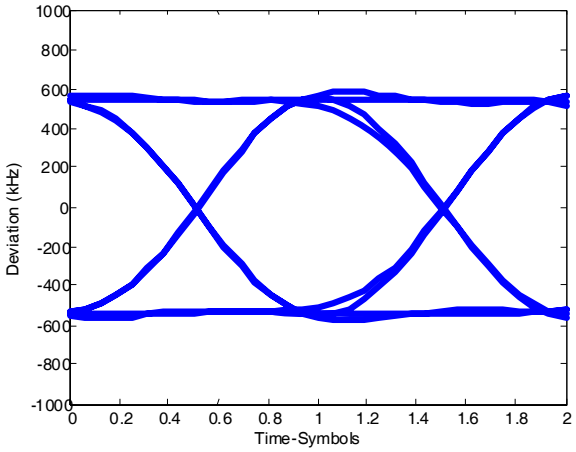


Figure 11: TX Eye Diagram

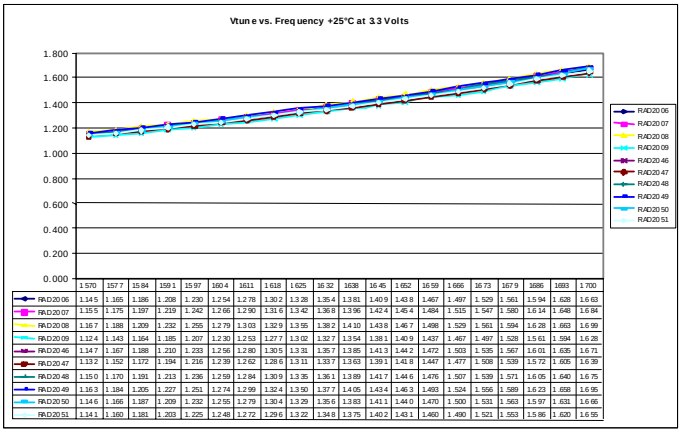
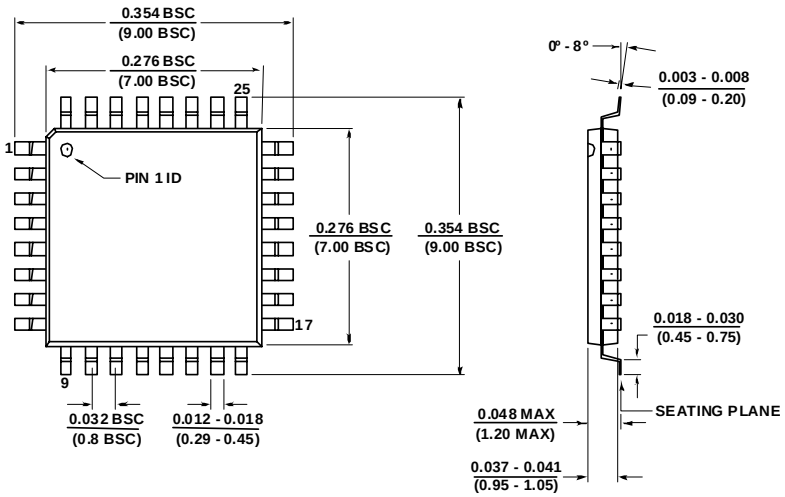


Figure 12: VCO Tuning Voltage versus Frequency

PHYSICAL DIMENSIONS (INCHES/MILIMETERS)

Package: H32-7
32-Pin (7 x 7 x 1mm) TQFP



Note: This package meets "Green" Pb-Free requirements and is compliant with the European Union directives WEEE (Waste Electrical and Electronic Equipment) and RoHS (Restriction of the use of certain Hazardous Substances in electrical and electronic equipment). The package pins are finished with 100% matte tin.

Ordering Information

Part Number	Temp Range	Package	Pack (Qty)
ML2724DH	-10°C to +60°C	32TQFP 7x7x1mm	Antistatic Tray (250)
ML2724DH-T	-10°C to +60°C	32TQFP 7x7x1mm	Tape and Reel(2500)

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.