W86L488

Winbond Host Interface SD/SDIO/MMC Memory Card Bridge

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REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.50	08/2002		First published.
0.60	12/2002		Add QFN package.
0.70	03/2003	P6, P8, P10, P11, P24, P25, P26, P41, P42, P43, P44, P45, P46	1. Modify pin function of CLK, ACLK, BCLK, XASN, XDRQN, 2. Revise function description of Data Access Request & Interrupt. 3. Revise reference schematic
0.80	05/2003	P30	Revise access time to 70ns
0.81	06/2003	P36	Revise 48-QFN package dimension
0.82	05/2004	P36, P37	Revise 48, 64 –QFN package dimension
1.00	04/2005	P42	Add Important Notice
1.10	08/2005	P1, P4-11, P32	1. Revise features and pin descriptions. 2. Revise the top mark description.
1.20	04/2006	P35-40	Revise the reference schematics.
1.21	06/2006	P1	Revise the ordering information.

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1. GENERAL DESCRIPTION

The W86L488 is a SD/SDIO/MMC interface bridge between microprocessor and SD/SDIO/MMC applications. The data width of microprocessor should be 16-bits. W86L488 supports synchronous or asynchronous type of host interface. It also supports interrupt or DMA mode to improve data transfer performance. By W86L488 internal register controlled and monitored, you can easily trace the signal between microprocessor and application I/F. There are two host interface are supported by W86L488Y/AY. Type 1 utilizes with microprocessors like Intel XScale, ARM/Strong ARM series, Hitachi SHx series and Toshiba Micro-controllers. Type 2 utilizes with microprocessors like Fujitsu SparcLite series. W86L488Y/AY can meet the most of IA devices requirement, such as PDA, Cellular Phone, DSC, and MP3 player applications and reserve the flexibility of your design.

2. FEATURES

- Compliant with SD and SDIO spec. Version 1.01.
- Compliant with MMC spec. Version 3.X.
- Support SD/MMC card commands in SPI mode
- Simultaneously access two ports of SD/SDIO/MMC supported. (W86L488AY only)
- Support physical layer commands of SD/SDIO/MMC interface.
- Support SD/MMC and SPI mode for SD/SDIO/MMC interface.
- Support SDIO interrupt and bus suspend/resume operation.
- Built-in 128 bytes data buffer for data transmit (send/receive).
- Support two types of Host microprocessor Interface access – synchronous and asynchronous.
- DMA and Interrupt transfer mode supported.
- Host microprocessor Interface support (Such as: Motorola's Dragon Ball series;Intel's Strong ARM, ARM series; Hitachi's SHx series; Fujisui's FR30)
- Support 8/16 bits data bus of Microprocessor I/F.
- Built-in 3.58 to 25MHz crystal driver circuit, support external oscillator or crystal clock.
- Operation voltage: 2.7~3.6V for SD/SDIO/MMC, 2.5/3.3V for Host CPU interface.
- 48/64-pin QFN package.

Ordering Information

PART NUMBER	DESCRIPTION	PACKAGE TYPE	PB FREE	PRODUCTION FLOW
W86L488Y	1Port SD/SDIO/MMC	48-PIN QFN	Yes	Commercial, 0°C to +70°C
W86L488AY	2Port SD/SDIO/MMC	64-PIN QFN	Yes	Commercial, 0°C to +70°C

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3. PIN CONFIGURATIONS

3.1 W86L488Y Pin Configuration

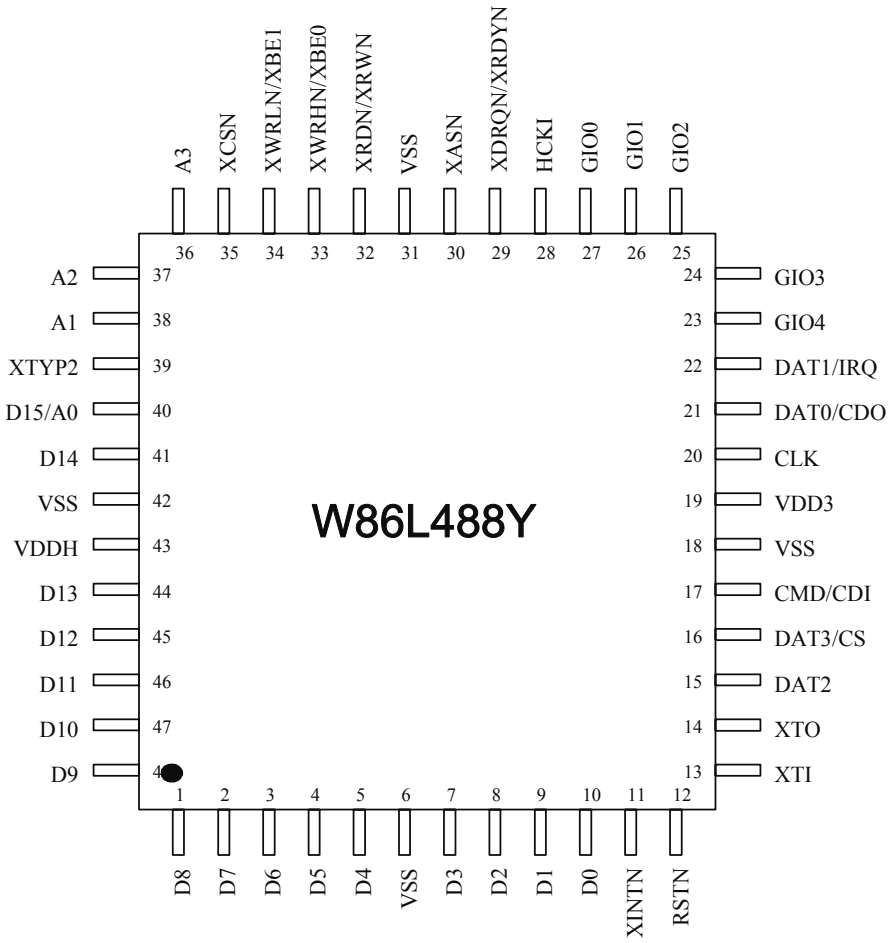

Fig. 3-1 W86L488Y Pin Assignment (48-pin QFN).

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3.2 W86L488AY Pin Configuration

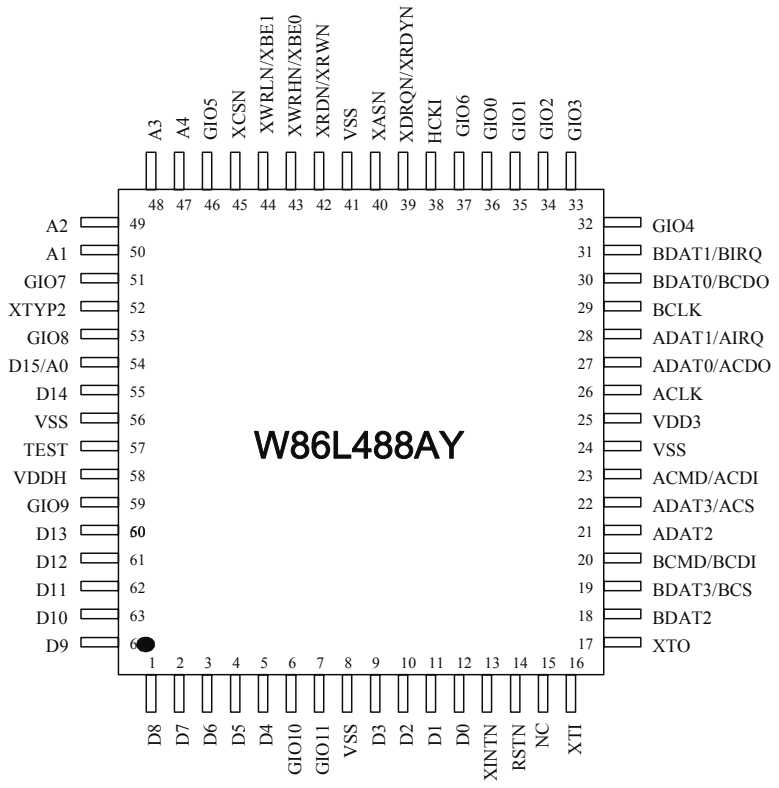

Fig. 3-2 W86L488AY Pin Assignment (64-pin QFN).

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4. PIN DESCRIPTIONS

4.1 W86L488Y Pin Descriptions

Type:

DP : Power,

DI : Digital Input,

DO : Digital Output.

DIO : Digital Input/Output

Note*1: When Host I/F voltage is 2.5V, VDDH connects to 2.5V.
When Host I/F voltage is 3.3V, VDDH connects to 3.3V.

PIN	NAME	TYPE	DESCRIPTION
SD/SDIO/MMC Interface (VDD3 powered):			
21	DAT0 CDO	DIO	**SD/MMC mode:** Data line bit [0] for SD and data signal for MMC. **SDIO mode:** Data line bit [0]. **SPI mode:** Card data output in SPI mode.
22	DAT1 IRQ	DIO	**SD/MMC mode:** Data line bit [1] for SDI and no use for MMC. **SPI mode:** No use. **SDIO mode:** Data line bit [1] or Interrupt (Optional).
15	DAT2	DIO	**SD/MMC mode:** Data line bit [2] I for SD and no use for MMC. **SDIO mode:** Data line bit [2] or Read Wait (Optional). **SPI mode:** No use.

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W86L488Y Pin Descriptions, continued

PIN	NAME	TYPE	DESCRIPTION
16	DAT3 CS	DIO	**SD/MMC mode:** Data line bit [3] or Card detect. **SDIO mode:** Data line bit [3] or Card detect. **SPI mode:** Card select.
17	CMD CDI	DIO	**SD/MMC mode:** Command line. **SDIO mode:** Command line. **SPI mode:** Card data input. This pin will be tri-state when the command is not driven.
20	CLK	DO	Clock output. This pin will stay at high or low when card clock is not needed depends on the configuration of Control Register (A[3:1] = 001) setting.
Crystal Driver (VDD3 powered):			
13	XTI	DI	Crystal clock input or External clock input,
14	XTO	DO	Crystal clock output. Left this pin open when use external input.
Host Interface Signal (VDDH powered):			
28	HCKI	DI	Host clock input.
35	XCSN	DI	Chip select input, host asserts to enable.
36:38	A[3:1]	DI	Address input.
40	D15 A0	DIO	**16-bit Mode:** Data bus D15. **Test Mode:** A0 = 1 : Internal register accesses data bus [7:0] to D[15:8]. A0 = 0 : Internal register accesses data bus [7:0] to D[7:0].
41	D14	DIO	Data bus D14.
44:48	D[13:9]	DIO	Data bus D[13:9].
1:5	D[8:4]	DIO	Data bus D[8:4], D[7:0] is the low byte of the data bus.
7:10	D[3:0]	DIO	Data bus D[3:0].

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W86L488Y Pin Descriptions, continued

PIN	NAME	TYPE	DESCRIPTION
33	XWRHN XBE0	DI	**Type 1:** High byte D[15:D8] write strobe, Host asserts to enable. **Type 2:** High byte D[15:D8] data valid, host asserts to enable.
34	XWRLN XBE1	DI	**Type 1:** Low byte D[7:0] write strobe, host asserts to enable. **Type 2:** Low byte D[7:0] data valid, host asserts to enable.
11	XINTN	DO	Interrupt request, host asserts low to enable.
32	XRDN XRWN	DI	Type 1: Read strobe, host asserts to enable. Type 2: Read or Write strobe, host asserts to enable. 1: Read transaction 0: Write transaction
30	XASN	DI	Type 1: None. Type 2: Bus access cycle start, host asserts to enable.
29	XDRQN XRDYN	DO	Type 1: Data Access request, controller asserts to request. Type 2: Bus cycle complete, controller asserts to inform host.
39	XTYP2	DI	Host interface type select, 0: Type 1 mode. 1: Type 2 mode.
General I/O Port Signal (VDD3 powered):			
23:27	GIO[4:0]	DIO	General input/output port signals. GIO0 pin can be used as dedicate card insert detect. Input mode and active low in default.(Powered by VCC3)
Other Signal (VDDH powered):			
12	RSTN	DI	Hardware Reset, Level low sensitive.

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W86L488Y Pin Descriptions, continued

PIN	NAME	TYPE	DESCRIPTION
Power:			
19	VDD3	DP	Power supply 3.3V.
43	VDDH	DP	Power supply 2.5V or 3.3V for Host I/F.
6, 18, 31, 42	VSS	DP	Ground supply.

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4.2 W86L488AY Pin Descriptions

Type:

DP : Power,

DI : Digital Input,

DO : Digital Output.

DIO : Digital Input/Output

Note*1: When Host I/F voltage is 2.5V, VDDH connects to 2.5V.
When Host I/F voltage is 3.3V, VDDH connects to 3.3V.

PIN	NAME	TYPE	DESCRIPTION
SD/SDIO/MMC Interface (VDD3 powered):			
27 30	ADAT0 BDAT0 ACDO BCDO	DIO	**SD/MMC mode:** Data line bit [0] for SD and data signal for MMC. **SDIO mode:** Data line bit [0]. **SPI mode:** Card data output in SPI mode.
28 31	ADAT1 BDAT1 AIRQ BIRQ	DIO	**SD/MMC mode:** Data line bit [1] for SDI and no use for MMC. **SPI mode:** No use. **SDIO mode:** Data line bit[1] or Interrupt (Optional).
21 18	ADAT2 BDAT2	DIO	**SD/MMC mode:** Data line bit [2] I for SD and no use for MMC. **SDIO mode:** Data line bit [2] or Read Wait (Optional). **SPI mode:** No use.

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W86L488AY Pin Descriptions, continued

PIN	NAME	TYPE	DESCRIPTION
22 19	ADAT3 BDAT3 ACS BCS	DIO	**SD/MMC mode:** Data line bit [3] or Card detect. **SDIO mode:** Data line bit [3] or Card detect. **SPI mode:** Card select.
23 20	ACMD BCMD ACDI BCDI	DIO	**SD/MMC mode:** Command line. **SDIO mode:** Command line. **SPI mode:** Card data input. This pin will be tri-state when the command is not driven.
26 29	ACLK BCLK	DO	Clock output . This pin will stay at high or low when card clock is not needed depends on the configuration of Control Register (A[3:1] = 001) setting.
Crystal Driver (VDD3 powered):			
16	XTI	DI	Crystal clock input or External clock input,
17	XTO	DO	Crystal clock output. Left this pin open when use external input.
Host Interface Signal (VDDH powered):			
38	HCKI	DI	Host clock input.
45	XCSN	DI	Chip select input, host asserts low to enable.
47:50	A[4:1]	DI	Address input.
54	D15/A0	DIO	**16-bit Mode:** Data bus D15. **Test Mode:** A0 = 1 : Internal register accesses data bus [7:0] to D[15:8]. A0 = 0 : Internal register accesses data bus [7:0] to D[7:0].
55	D14	DIO	Data bus D14.
60:64	D[13:9]	DIO	Data bus D[13:9].
1:5	D[8:4]	DIO	Data bus D[8:4], D[7:0] is the low byte of the data bus.
9:12	D[3:0]	DIO	Data bus D[3:0].

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W86L488AY Pin Descriptions, continued

PIN	NAME	TYPE	DESCRIPTION
43	XWRHN XBE0	DI	**Type 1:** High byte D[15:D8] write strobe, host asserts low to enable. **Type 2:** High byte D[15:D8] data valid, host asserts low to enable.
44	XWRLN XBE1	DI	**Type 1:** Low byte D[7:0] write strobe, host asserts low to enable. **Type 2:** Low byte D[7:0] data valid, host asserts low to enable.
13	XINTN	DO	Interrupt request, host asserts low to enable.
42	XRDN XRWN	DI	**Type 1:** Read strobe, host asserts low to enable. **Type 2:** Read or Write strobe, host asserts low to enable. 1: Read transaction 0: Write transaction
40	XASN	DI	**Type 1:** None. **Type 2:** Bus access cycle start, host asserts low to enable.
39	XDRQN XRDYN	DO	**Type 1:** Data Access request, controller asserts low to request. **Type 2:** Bus cycle complete, controller asserts low to inform host.
52	XTYP2	DI	Host interface type select, 0: Type 1 mode. 1: Type 2 mode.
General I/O Port Signal:			
46, 32:36	GIO[5:0]	DIO	General input/output port signals of first port GIO0 pin can be used as dedicate card insert detection of first port. Input mode and active low in default (GIO[4:0] powered by VDD3, GIO5 powered by VDDH).
7, 6, 59, 53, 51,37	GIO[11:6]	DIO	General input/output port signals of second port GIO6 pin can be used as dedicate card insert detection of second port. Input mode and active low in default (GIO6 powered by VDD3, GIO[11:7] powered by VDDH).

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W86L488AY Pin Descriptions, continued

PIN	NAME	TYPE	DESCRIPTION
Other Signal (VDDH powered):			
14	RSTN	DI	Hardware Reset, Level low sensitive.
57	TEST	DI	Reserved for internal test, must be connected to Vss.
Power:			
25	VDD3	DP	Power supply 3.3V.
58	VDDH	DP	Power supply 2.5V or 3.3V for Host I/F.
8, 24, 41, 56	VSS	DP	Ground supply.

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5. BLOCK DIAGRAM

5.1 W86L488Y Block Diagram

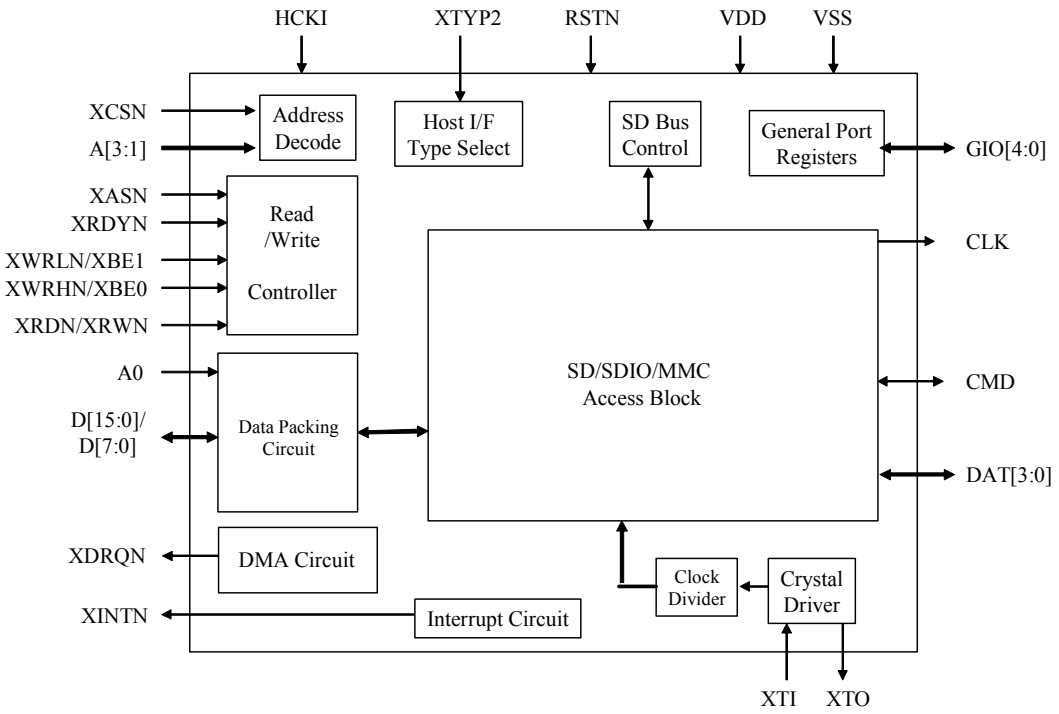

Fig. 5-1 Block Diagram of W86L488Y.

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5.2 W86L488AY Block Diagram

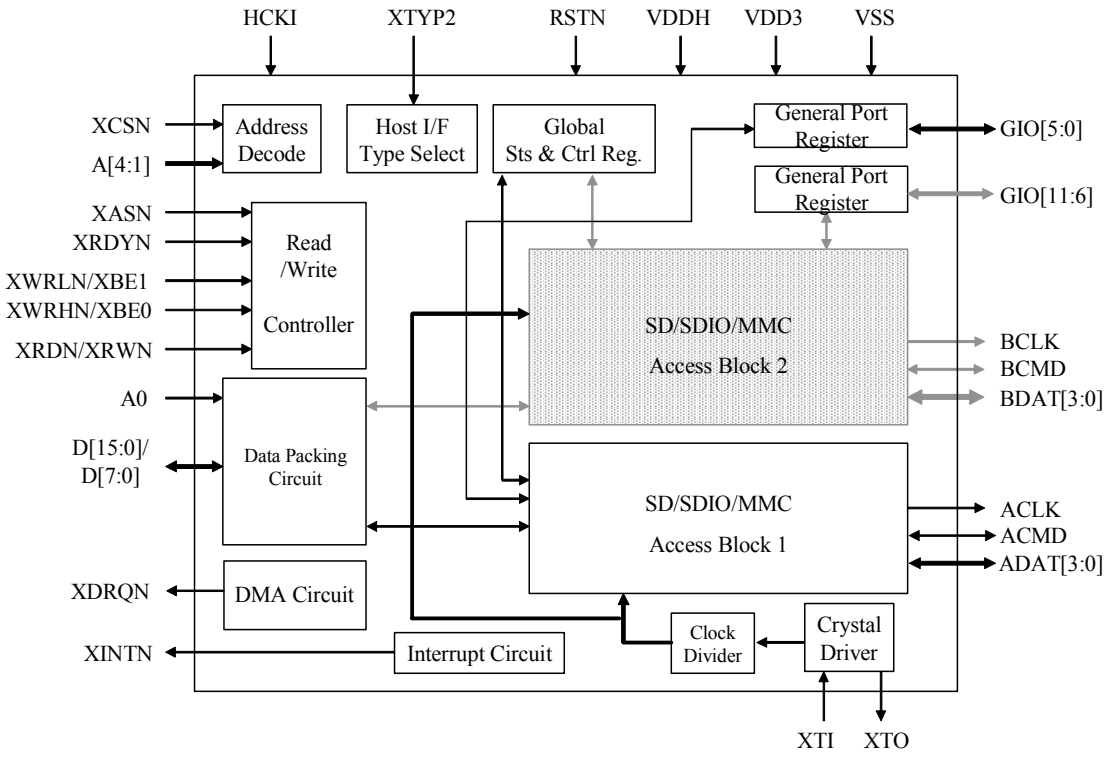

Fig. 5-2 Block Diagram of W86L488AY.

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6. REGISTER

The registers in the W86L488Y/AY are direct access registers and indirect access registers. The direct access registers and indirect access registers are listed as follows:

6.1 W86L488Y Register

Access Mode:

RO : Read Only

RC : Read Only and Read Clear

WO : Write Only

RW : Read/ Write

ADDRESS A[3:1]	ACCESS MODE	15	14	13	12	11	12	10	9	8	7	6	5	4	3	2	1	0
Direct Access Registers																		
000b	WO	Command Pipe Reg.																
000b	RO	Response Reg.																
001b	RO	Status Reg.									0	0	0	0	0	0	0	0
001b	RW*1	0	0	0	0	0	0	0	0	Control Reg.								
010b	RO	Receive Data Buffer																
010b	WO	Transmit Data Buffer																
011b	RO	Interrupt Status Reg.									0	0	0	0	0	0	0	0
011b	RW	0	0	0	0	0	0	0	0	0	Interrupt Enable Reg.							
100b	RW	General I/O Data Reg.																
100b	RW	0	0	0	0	0	0	0	0	0	General I/O Control Reg.							
101b	RC	General I/O Interrupt Status Reg.									0	0	0	0	0	0	0	0
101b	RW	0	0	0	0	0	0	0	0	0	General I/O Interrupt Enable Reg.							
110b	RW	0	0	0	0	0	0	0	0	0	Index Address Reg.							
111b	RW	Index Data Reg.																
Indirect Access Registers																		
0000b	RO	Extend Status Reg.						0	0	0	0	0	0	0	0	0	0	0
0000b	RW							Setting Reg.										
0001b	RO	SDIO Bus Function Reg.								0	0	0	0	0	0	0	0	
0001b	RW*2	0	0	0	0	0	0	0	0	SDIO Bus Control Reg.								

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W86L488Y Register, continued

ADDRESS A[3:1]	ACCESS MODE	15	14	13	12	11	12	10	9	8	7	6	5	4	3	2	1	0
0010b	RW	Master Data Format Reg.																
0011b	RW	0	0	0	0	0	0	0	0	Master Block Count Reg.								
0100b	RW	Slave Data Format Reg.																
0101b	RW	0	0	0	0	0	0	0	0	Slave Block Count Reg.								
0110b	RW	Nac Time-Out Reg.																
0111b	RO	Error Status Reg.											0	0	0	0	0	0
1000b	RO	Buffer Service Length Reg.								0	0	0	0	0	0	0	0	0
1000b	RW	0	0	0	0	0	0	0	0	Ready & Data Size Reg.								
1001b	RW	Test Reg.																
1010b	RO	ID Code Reg.																

*1 : Bit 8 is WO and others are RW.

*2 : Bit [7:6] are RO and others are RW.

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6.2 W86L488AY Register

Access Mode:

RO : Read Only

RC : Read Only and Read Clear

WO : Write Only

RW : Read/ Write

ADDRESS A[4:1]	ACCESS MODE	15	14	13	12	11	12	10	9	8	7	6	5	4	3	2	1	0
Global Registers																		
1000b	RO	Global Status Reg.																
1001b	RW*3	Global Control Reg.																
1010b	RW	Ready & Data Size Reg.																
Direct Access Registers																		
0000b	WO	Command Pipe Reg.																
0000b	RO	Response Reg.																
0001b	RO	Status Reg.									0	0	0	0	0	0	0	0
0001b	RW*4	0	0	0	0	0	0	0	0	Control Reg.								
0010b	RO	Receive Data Buffer																
0010b	WO	Transmit Data Buffer																
0011b	RO	Interrupt Status Reg.									0	0	0	0	0	0	0	0
0011b	RW	0	0	0	0	0	0	0	0	0	Interrupt Enable Reg.							
0100b	RW	General I/O Data Reg.																
0100b	RW	0	0	0	0	0	0	0	0	0	General I/O Control Reg.							
0101b	RC	General I/O Interrupt Status Reg.									0	0	0	0	0	0	0	0
0101b	RW	0	0	0	0	0	0	0	0	0	General I/O Interrupt Enable Reg.							
0110b	RW	0	0	0	0	0	0	0	0	0	Index Address Reg.							
0111b	RW	Index Data Reg.																

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W86L488AY Register, continued

ADDRESS A[4:1]	ACCESS MODE	15	14	13	12	11	12	10	9	8	7	6	5	4	3	2	1	0
Indirect Access Registers																		
0000b	RO	Extend Status Reg.						0	0	0	0	0	0	0	0	0	0	0
0000b	RW							Setting Reg.										
0001b	RO	SDIO Bus Function Reg.								0	0	0	0	0	0	0	0	
0001b	RW*5	0	0	0	0	0	0	0	0	SDIO Bus Control Reg.								
0010b	RW	Master Data Format Reg.																
0011b	RW	0	0	0	0	0	0	0	0	Master Block Count Reg.								
0100b	RW	Slave Data Format Reg.																
0101b	RW	0	0	0	0	0	0	0	0	Slave Block Count Reg.								
0110b	RW	Nac Time-Out Reg.																
0111b	RO	Error Status Reg.											0	0	0	0	0	0
1000b	RO	Buffer Service Length Reg.								0	0	0	0	0	0	0	0	0
1000b	RW	0	0	0	0	0	0	0	0	Ready & Data Size Reg.								
1001b	RW	Test Reg.																
1010b	RO	ID Code Reg.																

*3 : Bit [9:8] are RO.

*4 : Bit 8 is WO and others are RW.

*5 : Bit [7:6] are RO and others are RW.

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7. FUCNTIONAL DESCRIPTION

7.1 Host Interface

The Host interface can support Type 1 or Type 2 that depends on different microprocessors. The data bus width should be configured as 16-bit.

Host Interface Type 1:

Figure 7-1 shows the transaction of specified 16-bit microprocessors. Figure 7-2 is the timing of 16-bit microprocessors writes high and low byte.

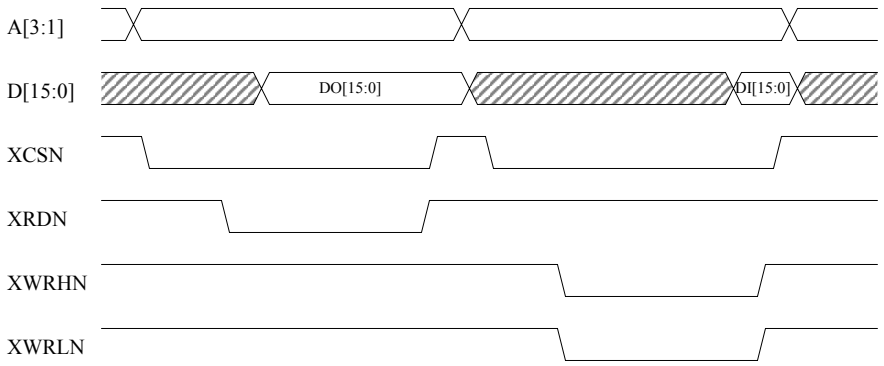

Fig. 7-1 16-bit Read and Write Access in Host I/F Type 1.

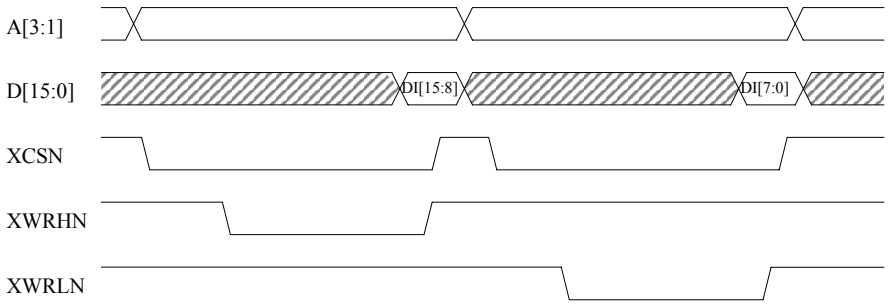

Fig. 7-2 High Byte and Low Byte Write Access in Host I/F Type 1.

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Host Interface Type 2:

The data size of the microprocessors data bus should be 16-bit and the access cycle may be in 3-cycle or 2-cycle. Figure 7-3 shows the timing of microprocessors read write in type 2 and the access cycle is 3-cycle access, figure 7-4 shows the timing of microprocessors read write in type 2 and the access cycle is 2-cycle access.

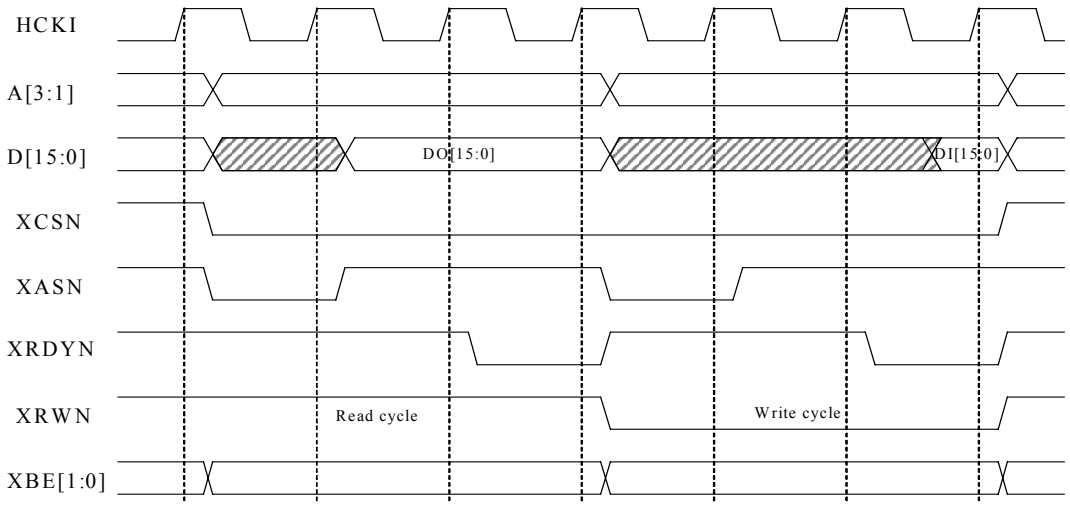

Fig. 7-3 Read and Write Timing in Host I/F Type 2, 3-Cycle Access.

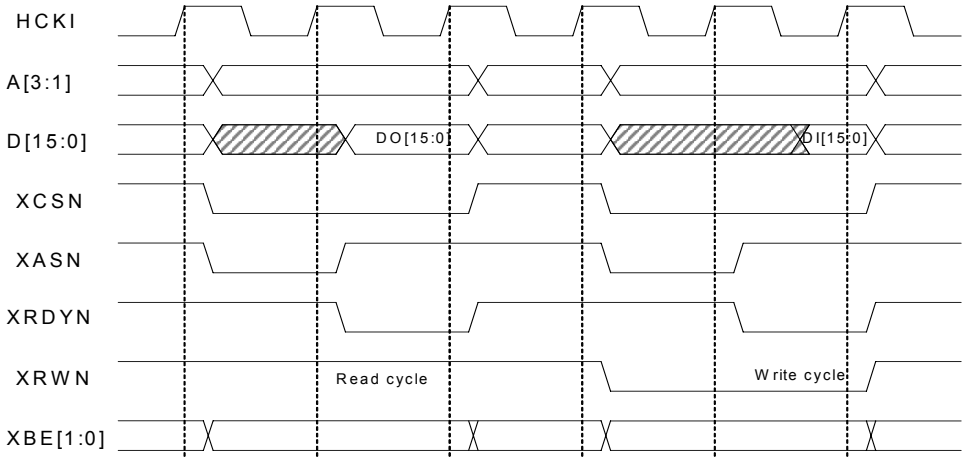

Fig. 7-4 Read and Write Timing in Host I/F Type 2, 2-Cycle Access.

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Data Access Request (XDRQN):

Data Aaccess Request is used to notify the Host to access transmit or receive buffers. The Data Access Request can be activated both in Type 1 and Type 2.

During host transmits data to the card, the XDRQN will be asserted if the data write command has been transfer to the card and the transmit data buffer have not enough data to transmit to the card. The XDRQN will not be asserted if the transmit data buffer have enough data to transmit to the card. The last byte of the data should be placed at bit [15:8] if the data length is odd byte and CPU data size is 16-bit.

During host receives data from the card, the XDRQN will be asserted if the data read command has been transferred to the card and the data have been received in the receive data buffer. The XDRQN will not be asserted if the data read command has been executed completely and the receive data buffer is read out. The last byte of the data is located at bit [7:0] if the data length is odd byte and CPU data size is 16-bit.

There are two types of data access request waveform, Single and Burst Access Mode.

Single Access Mode is configured if DABST = low, XDRQN will be de-asserted after each access receive or transmit data buffer, the XDRQN will be activated again after four clock period later. Figure 7-5 shows the waveform of Host access receive data buffer in single access mode (DABST = low).

Burst Access Mode is configured if DABST = high, XDRQN will hold at active state until the data has been transferred completely. The Host can access receive or transmit data buffer with higher speed continuously and regardless of the system clock. Figure 7-6 is the waveform of Host access transmit data buffer in burst mode (DABST = high).

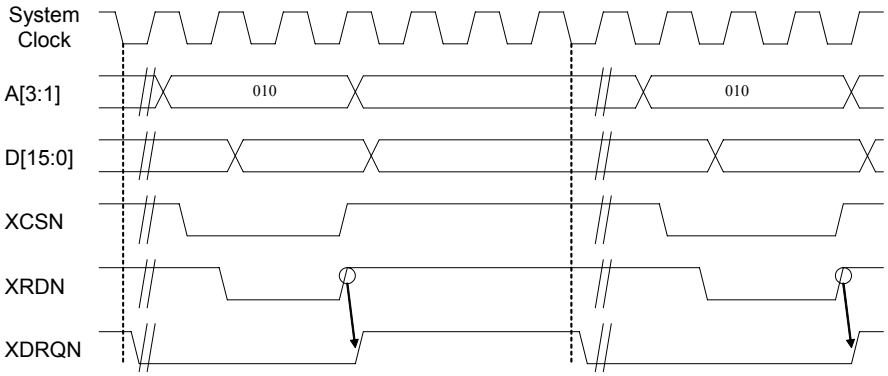

Fig. 7-5 Host Read Receive Data Buffer in Single Access Mode (DABST = low).

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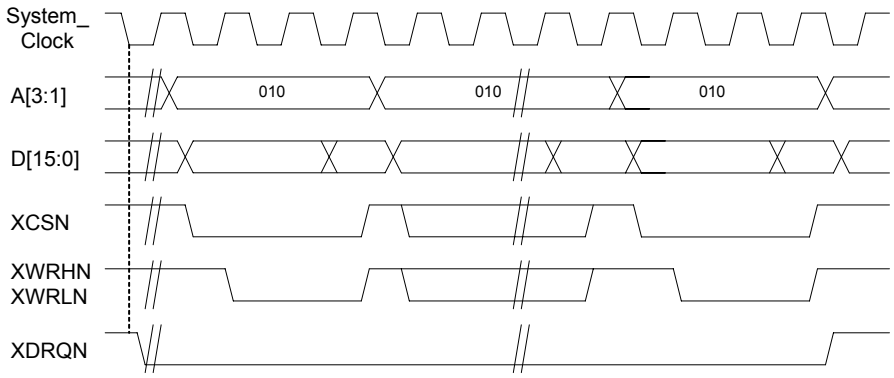

Fig. 7-6 Host Write Transmit Data Buffer in Burst Access Mode (DABST = high).

Interrupt (XINTN):

Interrupt is used to notify Host that this device needs its service. The status can be read and check repeatedly if the Host cannot serve regard interrupt. XINTN will be asserted (low level) at the falling edge of system clock if any bit in the Interrupt Reg. is set, XINTN pin will de-asserted (high level) when related bit of Interrupt Status Reg. is set. But DRQ interrupt has the higher priority than configuration of Interrupt Status Reg.. XINTN will be asserted again at four system clocks period later if any other interrupt event is still pending.

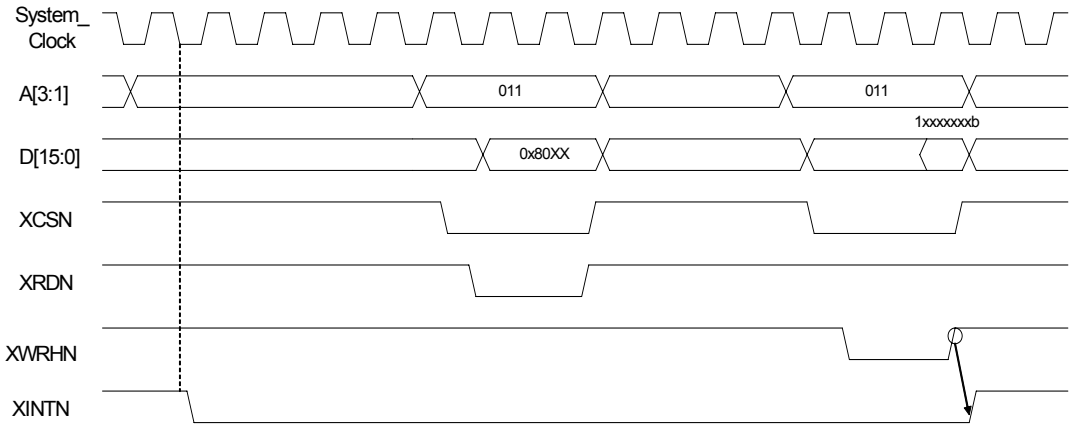

Fig. 7-7 Timing of Interrupt in.

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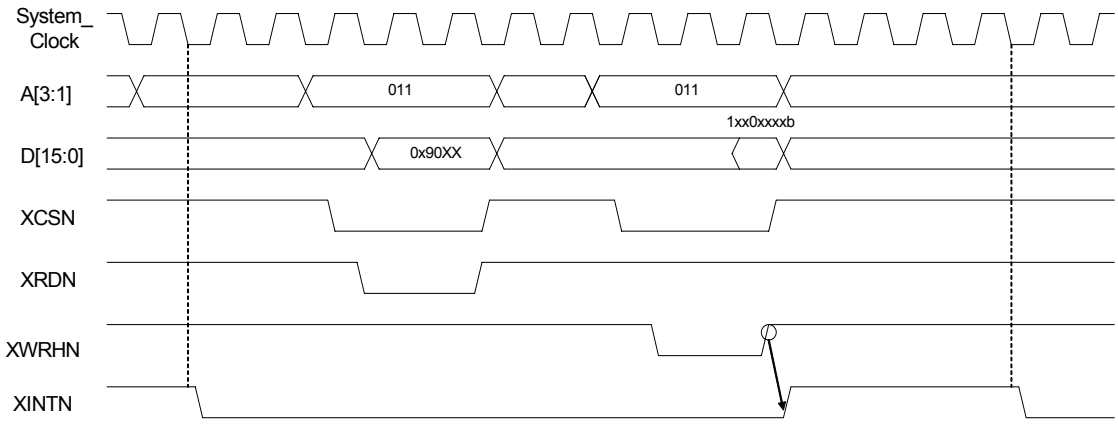

Fig. 7-8 Timing of Interrupt in (XINTN is asserted again).

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7.2 Card Inserting and Removing

There are two different approaches for Host to detect SD/SDIO card is inserted or ejected through W86L488Y/AY. For MMC card is just suitable for second one. First approach is detected by CD/DAT3 pin, and second is a dedicated mechanical switch on the SD/MMC slot can be connected to the GIO0 pin and set GIO0 to input direction. These two methods can be performed even if the W86L488 is in power down state. Second approach is recommended to implement.

Approach 1, CD/DAT3 as card detection:

The CD/DAT3 of SD bus can be used as card detection after power up. This method will not be effective when 4-bit mode activated on the SD bus is transferring. MMC card may not be utilized this method. Some MMC cards will be configured as SPI mode after GO_IDLE_STATE (CMD0) command is issued due to external or dedicated pulled-down resister.

Approach 2, GIO0, GIP6 as card detection (Recommended):

Some SD/MMC slots support external switch for card existing detection, the switch will be stuck on specified state when SD/SDIO or MMC card is exist. GIO0 and GIP6 with a pull-up resister can be used as card detection of port A and port B. SD/SDIO or MMC card inserting or removing changes the switch state of GIO0 pin and then generates interrupt to the Host. Host may check the card state by General I/O Port Data Reg.. The card inserted status of port A and port B also regards to Global Status and Control Reg..

Figure 7-9 shows the waveform of GIO0 and GIOx when card is inserted and removed if GIO0 as card insert and GIOx as write protect detection.

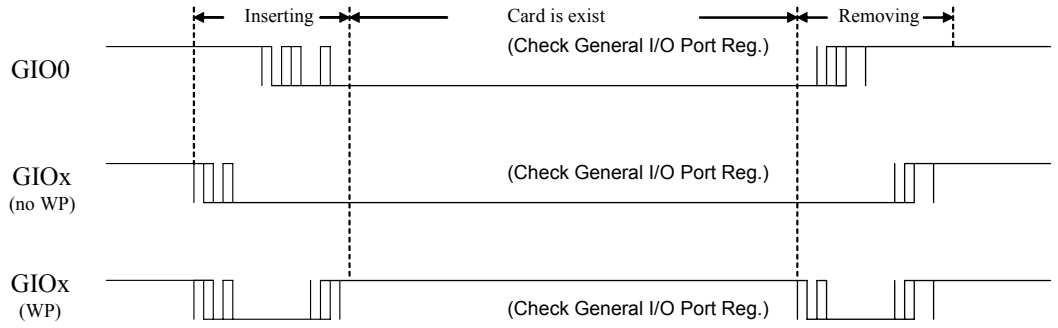

Fig. 7-9 Card Insert use GIO0 and Write Protect use GIOx.

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7.3 Reset Action

Hardware Reset:

Hardware reset results from asserting RSTN pin for more than 1uS.

(1) Clear Receive and Transmit data buffer.

(2) All the internal logic will be reset to initial state.

(3) The content of all registers are restored to default values.

Software Reset:

Software reset is executed by configuring Control Reg..

(1) Clear Receive and Transmit data buffer.

(2) All the internal logic will be reset to initial state.

(3) The content of all registers are not affected.

In W86L488AY, the port A and port B will reset at the same time if global software reset in the Global Control Reg. is set.

Data Buffer Reset:

Data buffer reset is executed by configuring Control Reg..

(1) Clear receive data buffer and transmit data buffer simultaneously.

(2) The serial interface command will affected if the data receive or transmit command is progressing.

(3) Internal logic state and the content of registers are not affected.

7.4 Clock Source

The internal clock source of W86L488Y/AY is fed on XTO pin and XTI pin may be used as clock input by crystal or oscillator. The operation frequency is required from 3.58MHz to 25MHz. In W86L488AY, the clock driver will be disabled when port A and port B are into power down or Global Control Reg. is configured.

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8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings*

	PARAMETER	SYMBOL	RATING	UNITS
1	Supply Voltage with respect to V_{VSS}	V_{VDD}	-0.3 to 6	V
2	Current at any pin other than supplies		0 to 10	mA
3	Storage Temperature	T_{st}	-65 to 150	°C

* Exceeding these values may cause permanent damage.

8.2 Recommended Operating Conditions

	CHARACTERISTICS	SYMBOL	RATING	UNIT
1	Host I/F Operation Voltage (referenced to Vss pin).	V_{VDDH}	2.5 to 3.6	V
2	Operation Voltage (referenced to Vss pin).	V_{VDD3}	3.0 to 3.6	V
3	Operation Voltage (referenced to Vss pin) (Note)	V_{VDD3}	2.7to 3.0	V
4	Clock Frequency at XTI pin	f_{XTL}	25	MHz
5	Operation Temperature	T_{op}	0 to 70	°C

Note: Clock frequency not guaranteed up to 25 MHz.

8.3 Power Supply Characteristics

(Measurement VDD3+ VDDH at VDD3 = VDDH)

	PARAMETER	CONDITION	SYM.	MIN	TYP‡	MAX	UNITS	TEST
1	Standby Supply Current	Power Supply	I_Q		2	20	μA	Test 1
2	Operating Supply Current (Single port)	(V_{VDD} = 3.3V)	I_{VDD}		14	22	mA	Test 2
3	Operating Supply Current (Dual port)		I_{VDD}		24	36	mA	Test 2
4	Operating Supply Current (Single port)	(V_{VDD} = 3.3V)	I_{VDD}		13		mA	Test 3
5	Operating Supply Current (Dual port)		I_{VDD}		23		mA	Test 3

‡: Typical figure are at V_{DIVDD} = 3.3V and temperature = 25 °C and are for design aid only, not guaranteed and not subject to production testing.

Test 1: All input pins are V_{VDD} or V_{VSS}, configured as power down mode, output without loading and no clock input on the XTI and HCKI pins.

Test 2: 25 MHz external clock input on the XTI pin, output without loading.

Test 3: 25 MHz crystal connected at XTI and XTO pins, output without loading.

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8.4 Digital Characteristics

	PARAMETER	CONDITION	SYMBOL	MIN.	TYP‡	MAX.	UNITS	NOTES
1	Output High Voltage	2mA load	V_{OH}	0.9			VDD	1
2	Output Low Voltage	2mA sink	V_{OL}			0.1	VDD	1
3	Output High Voltage at SD4 output	3mA load	V_{OH}	0.9			VDD	
4	Output Low Voltage at SD4 output	3mA sink	V_{OL}			0.1	VDD	
5	High Level Input Voltage		V_{IH}	0.7			VDD	
6	Low Level Input Voltage		V_{IL}			0.3	VDD	
7	Input Current		Iin			1	μA	
8	Input Capacitance		Cin		10		pF	

‡: Typical figure are at V_{DVDD} = 3.3V and temperature = 25 °C and are for design aid only, not guaranteed and not subject to production testing.

Notes:

1: All output pins except SD4 output.

8.5 Timing Characteristics

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock (figure 8-1)							
1	XTI	fXTI	1	-	20	MHz	1
2	XTI high pulse width	$tXTI_{wh}$	10	-	-	nS	1
3	XTI low pulse width	$tXTI_{wl}$	10	-	-	nS	1
4	XTI rise time	$tXTI_r$	-	-	5	nS	1
5	XTI fall time	$tXTI_f$	-	-	5	nS	1
6	XTO delay time	$tXTO_d$	-	-	5	nS	2
7	XTI crystal driver	fXTI	3.58	-	25	MHz	3
8	HCLK frequency	fHCLK	1	-	40	MHz	
9	HCLK high pulse width	$tHCLK_{wh}$	10	-	-	nS	
10	HCLK low pulse width	$tHCLK_{wl}$	10	-	-	nS	
11	HCLK rise time	$tHCLK_l$	-	-	5	nS	
12	HCLK fall time	$tHCLK_f$	-	-	5	nS	
Reset							
1	RSTN	tRST	4	-	-	cycle	

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Timing Characteristics, continued

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Host Interface at Type 1 (figure 8-2, 8-3)							
1	Access time	t_{acc}	70	-	-	nS	4
2	Address setup time	tA_{su}	10	-	-	nS	
3	Address hold time	tA_h	5	-	-	nS	
4	D[15:0] output delay time	tD_{od}	-	-	30	nS	5,6
5	D[15:0] output hold time	tD_{oh}	10	-	-	nS	5,7
6	D[15:0] input setup time	tD_{su}	10	-	-	nS	8
7	D[15:0] input hold time	tD_h	5	-	-	nS	9
8	DMA request delay time	$tDRQ_d$	-	-	20	nS	2
9	DMA request hold time	$tDRQ_h$	5	-	20	nS	2
Host Interface at Type 2 (figure 8-5)							
1	Input signals setup time	$tIF2_{su}$	10	-	-	nS	10
2	Input signals hold time	$tIF2_h$	5	-	-	nS	10
3	Address setup time	$tA2_{su}$	10	-	-	nS	
4	Address hold time	$tA2_h$	5	-	-	nS	
5	XRDYN delay time	$tRDY_d$	-	-	20	nS	2
6	XRDYN hold time	$tRDY_h$	5	-	-	nS	2
7	D[15:0] output delay time	tD_{od}	-	-	30	nS	5
8	D[15:0] output hold time	tD_{oh}	10	-	-	nS	5
9	D[15:0] input setup time	tD_{su}	10	-	-	nS	
10	D[15:0] input hold time	tD_h	5	-	-	nS	
Interrupt (figure 8-4)							
1	Interrupt delay time	$tINT_d$	-	-	20	nS	
2	Interrupt hold time	$TINT_h$	5	-	20	nS	
Serial Interface Signals (figure 8-6, 8-7, 8-8, 8-9)							
1	SD3 output delay	$tSD3_d$	5	-	15	nS	2
2	SD3 input setup time	$tSD3D_{su}$	10	-	-	nS	
3	SD3 input hold time	$tSD3_h$	5	-	-	nS	
4	SD1, SD2, SD5, SD6 output delay time	$tSDn_d^*$	-	-	30	nS	2
5	SD1, SD2, SD5, SD6 input setup time	$tSDn_{su}$	10	-	-	nS	
6	SD1, SD2, SD5, SD6 input hold time	$tSDn_h$	5	-	-	nS	

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Note 1: External clock input.

Note 2: 20 pF output loading.

Note 3: Crystal driver.

Note 4: Minimum active pulse width of (XCSN and XRDN) or (XCSN and XWRHN and XWRLN).

Note 5: 40 pF output loading.

Note 6: From the last active signal of XCSN or XRDN.

Note 7: From the first in-active signal of XCSN or XRDN.

Note 8: To the first in-active signal of XCSN, XWRHN or XWRLN, XWRHN or XWRLN related to the D[15:8] or D[7:0].

Note 9: From the first in-active signal of XCSN, XWRHN or XWRLN, XWRHN or XWRLN related to the D[15:8] or D[7:0].

Note 10: XCSN, XASN, XRWN and XBE[1:0] signals.

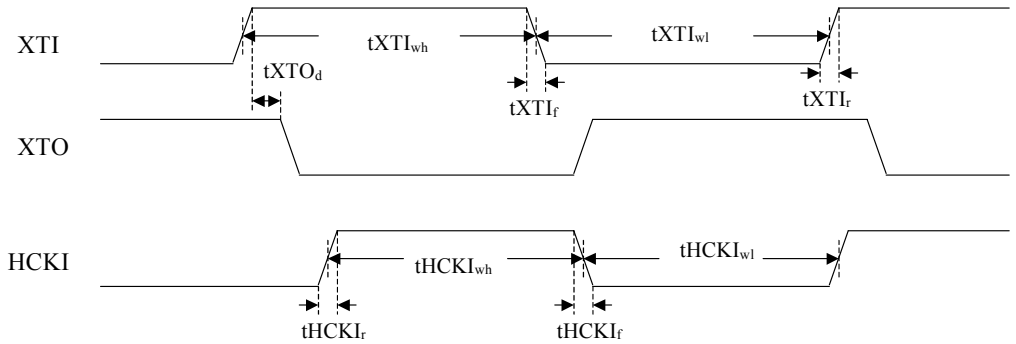

Fig. 8-1 Timing Characteristic of XTI, XTO and HCKI.

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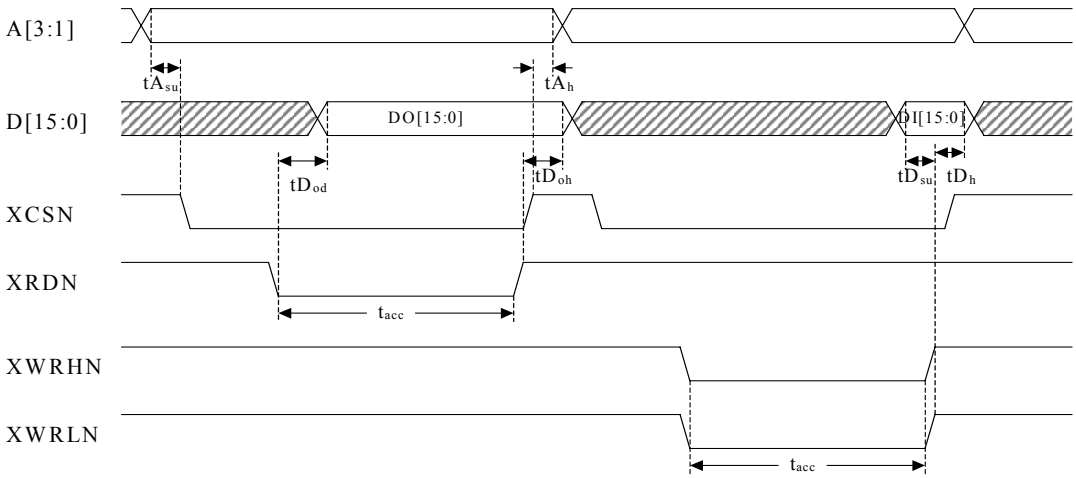

Fig. 8-2 Host Access Timing Characteristic in Host I/F Type 1.

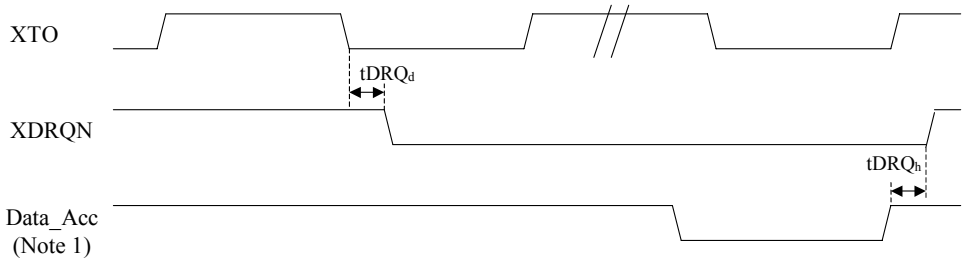

Fig. 8-3 Data Access Request Timing Characteristic.

Note 1: May be XRDN or XWRHN or XWRLN signals when DABST = low.

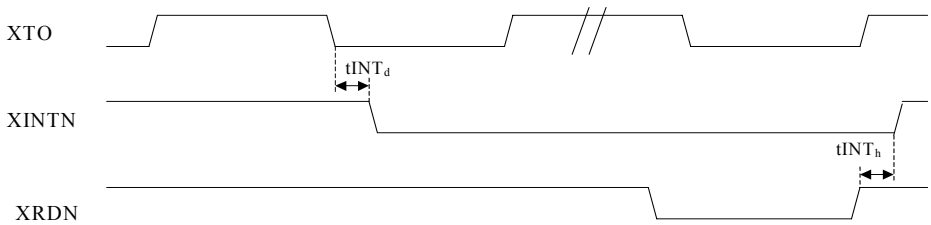

Fig. 8-4 Interrupt Timing Characteristic.

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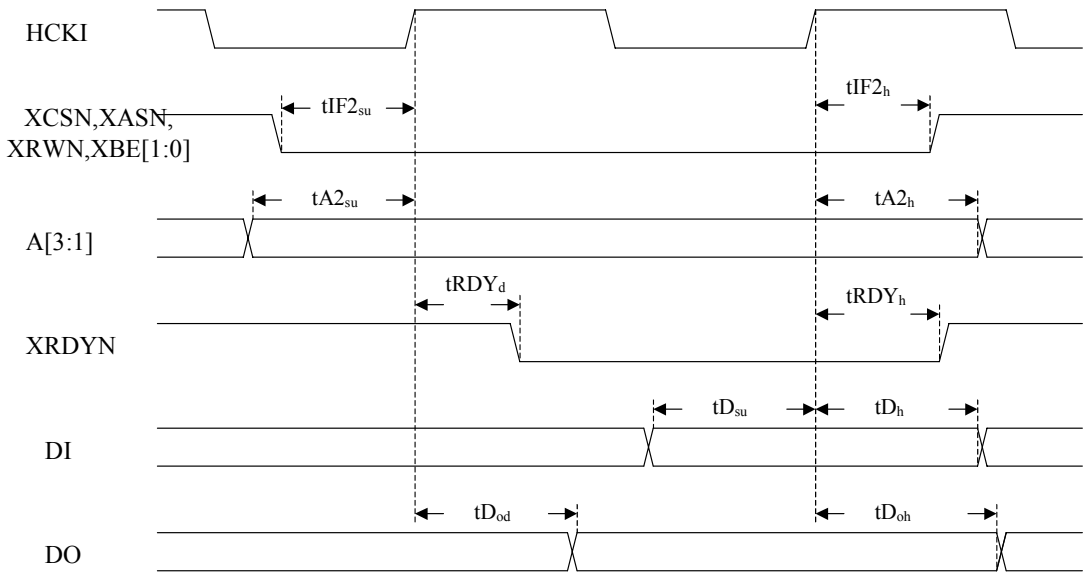

Fig. 8-5 Host Interface Type 2 Timing Characteristic.

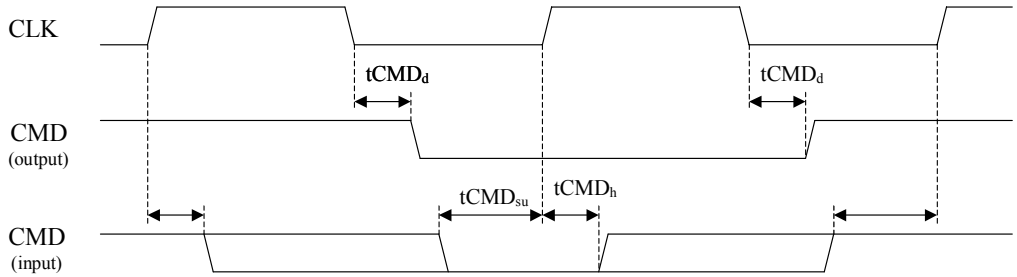

Fig. 8-6 Serial Interface CMD Timing Characteristic (SD Mode).

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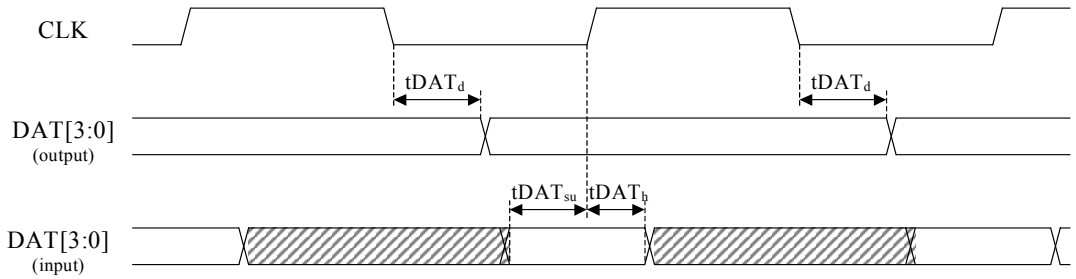

Fig. 8-7 Serial Interface DAT[3:0] Timing Characteristic (SD Mode).

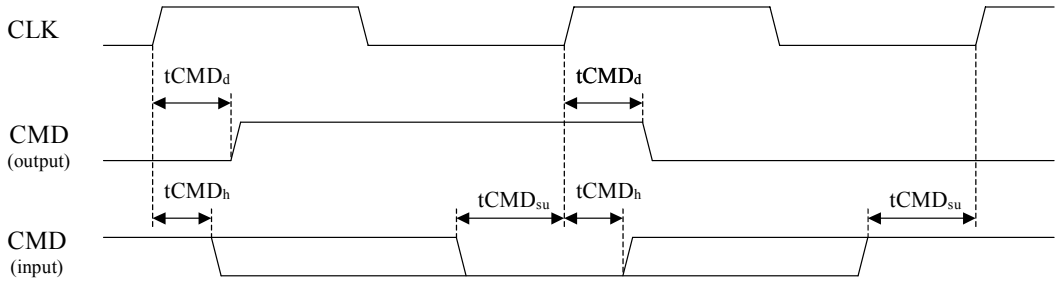

Fig. 8-8 Serial Interface CMD Timing Characteristic (MMC Mode).

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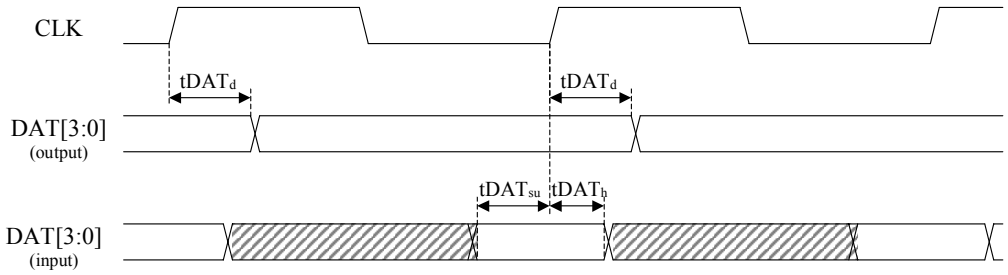
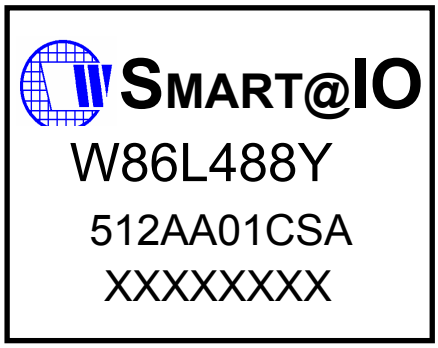


Fig. 8-9 Serial Interface DAT[3:0] Timing Characteristic (MMC Mode).

9. HOW TO READ THE TOP MARKING

The top marking of W86L488Y



1st line: Winbond logo and SMART@IO Mark

2nd line: Part number

- W86L488Y (1 port of SD/SDIO/MMC bridge)
- W86L488AY (2 ports of SD/SDIO/MMC bridge)

3rd line: Tracking code 512 AA 01 CSA

512: packages made in '05, week 12

AA: Assembly house ID code

01: For internal use

C: IC revision; A means version A, B means version B and C means version C.

SA: For internal use

4th line: For intermal use

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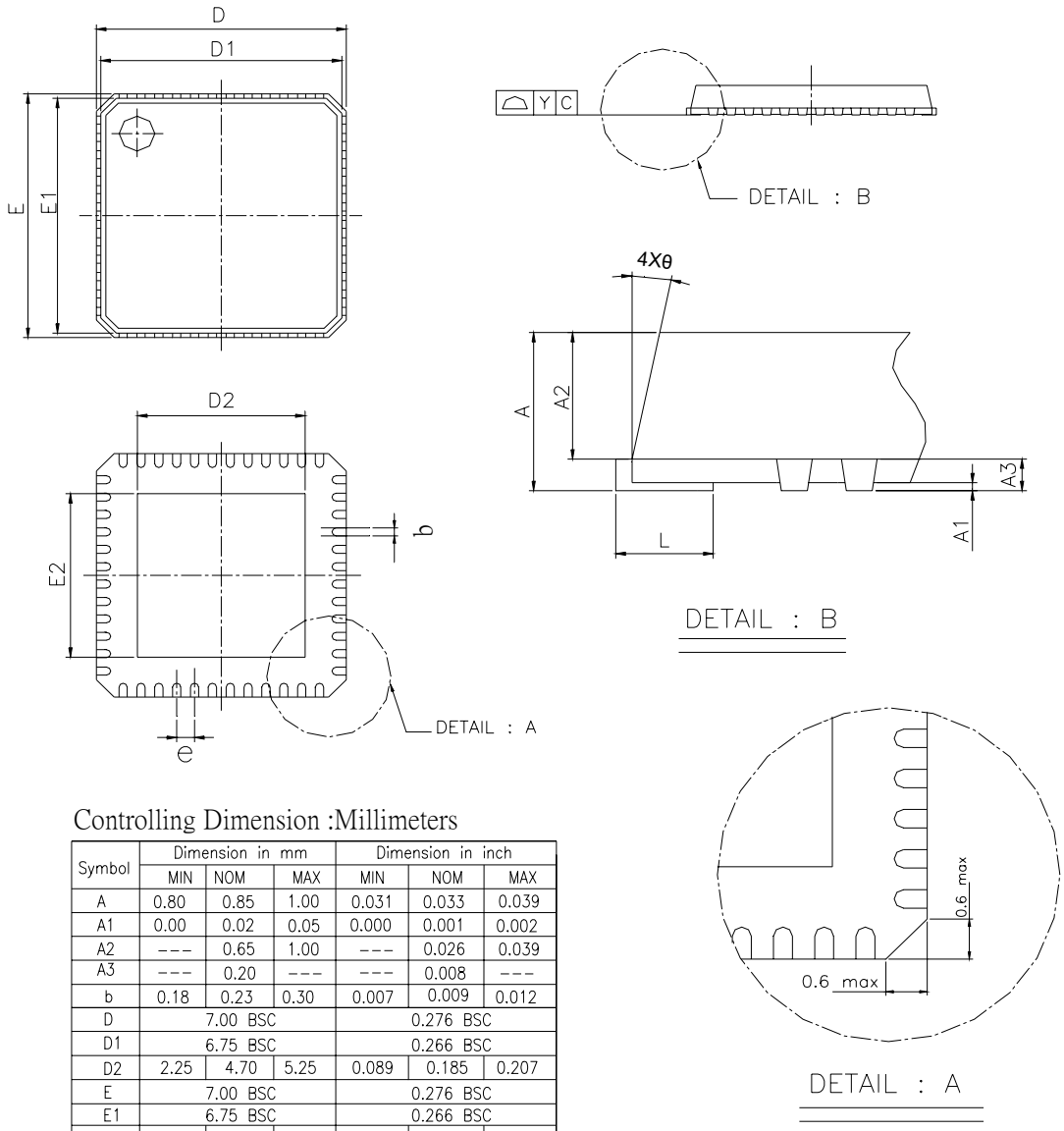
10. PACKAGE DIMENSIONS

10.1 W86L488Y Package Dimensions

48- QFN 7x7 MM^2, Thickness: 1.0MM



Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3	---	0.20	---	---	0.008	---
b	0.18	0.23	0.30	0.007	0.009	0.012
D	7.00 BSC			0.276 BSC		
D1	6.75 BSC			0.266 BSC		
D2	2.25	4.70	5.25	0.089	0.185	0.207
E	7.00 BSC			0.276 BSC		
E1	6.75 BSC			0.266 BSC		
E2	2.25	4.70	5.25	0.089	0.185	0.207
e	0.5 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	12°	0°	---	12°
Y	---	---	0.08	---	---	0.003

*D2,*E2 :By die size difference

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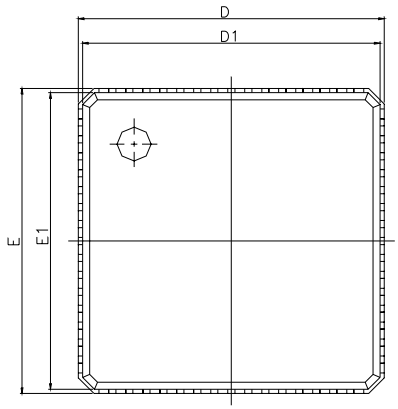
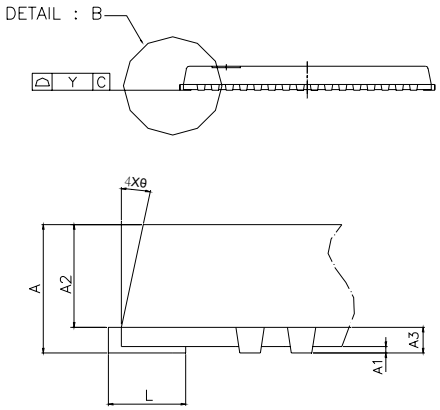
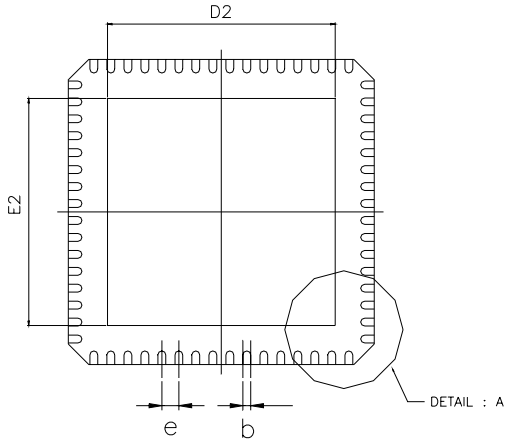
10.2 W86L488AY Package Dimensions

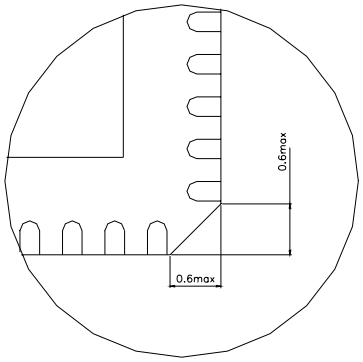
64- QFN 9x9 MM^2, Thickness: 1.0MM





DETAIL : B





DETAIL : A

Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3	0.20 REF			0.008 REF		
b	0.18	0.23	0.30	0.007	0.009	0.012
D	9.00 BSC			0.354 BSC		
D1	8.75 BSC			0.344 BSC		
E	9.00 BSC			0.354 BSC		
E1	8.75 BSC			0.344 BSC		
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	12°	0°	---	12°
D2	6.90	7.05	7.20	0.272	0.276	0.283
E2	6.90	7.05	7.20	0.272	0.276	0.283
Y	---	---	0.08	---	---	0.003

*D2,*E2 :By die size difference

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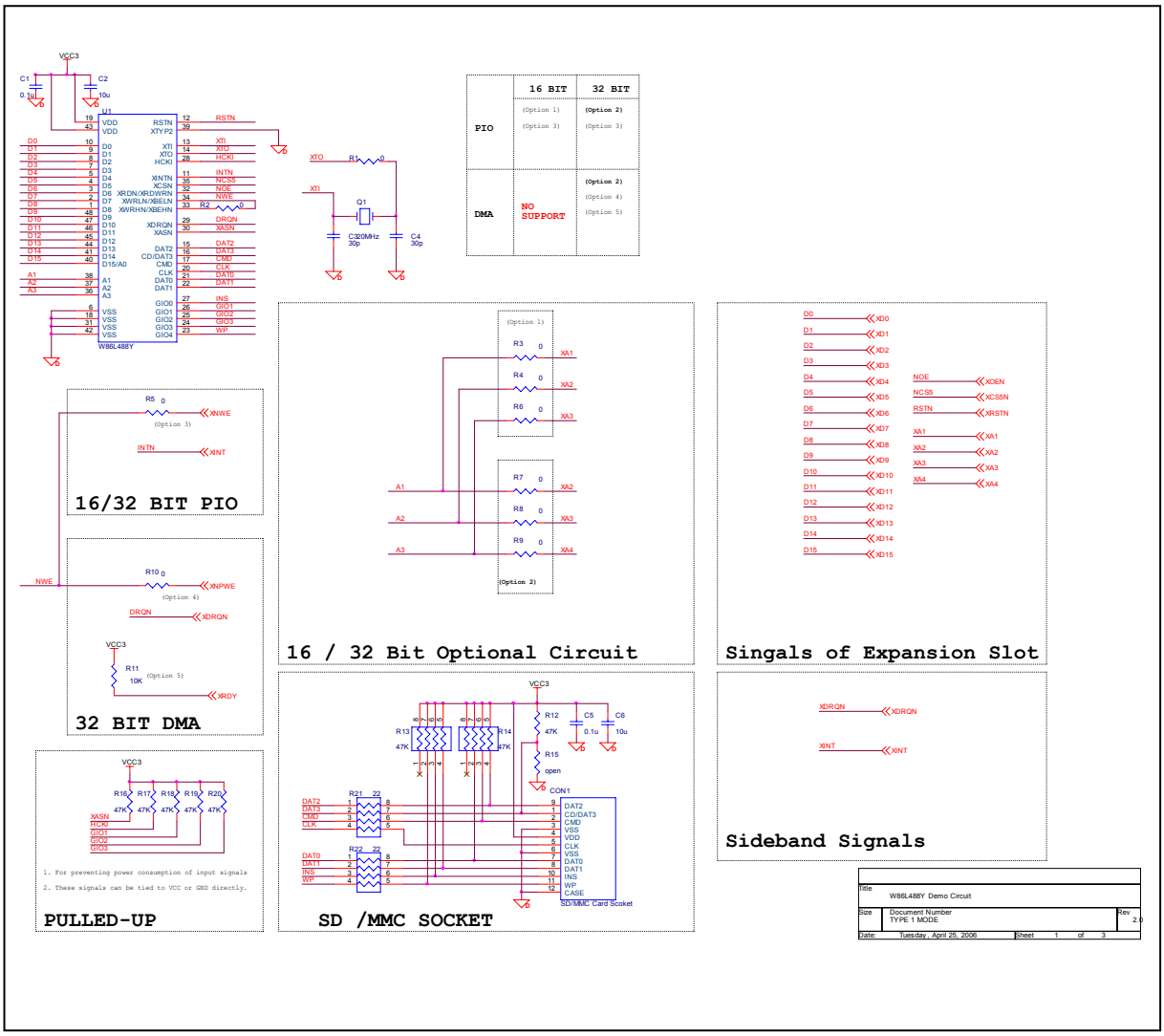
11. REFERENCE SCHEMATIC

11.1 W86L488Y Reference Schematic

16/32bit PIO/DMA mode with PXA255/PXA27X expansion connector



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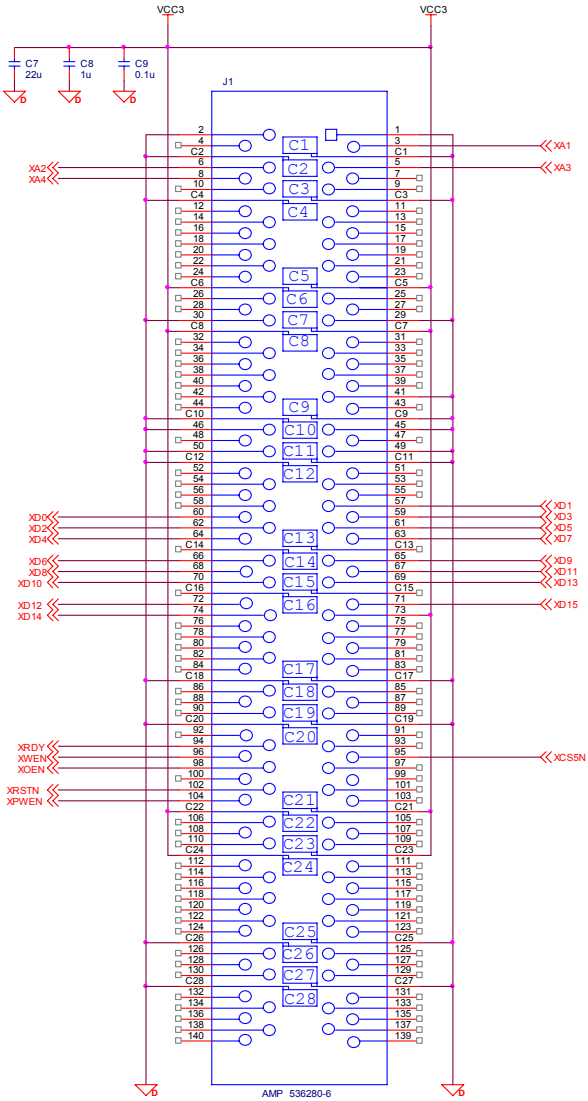

Host interface (PXA25X)

Title	Intel PXA25X Connector		
Size Custom	Document Number <Doc>		Rev 2.0
Date: Tuesday, April 25, 2006		Sheet 2 of 3	

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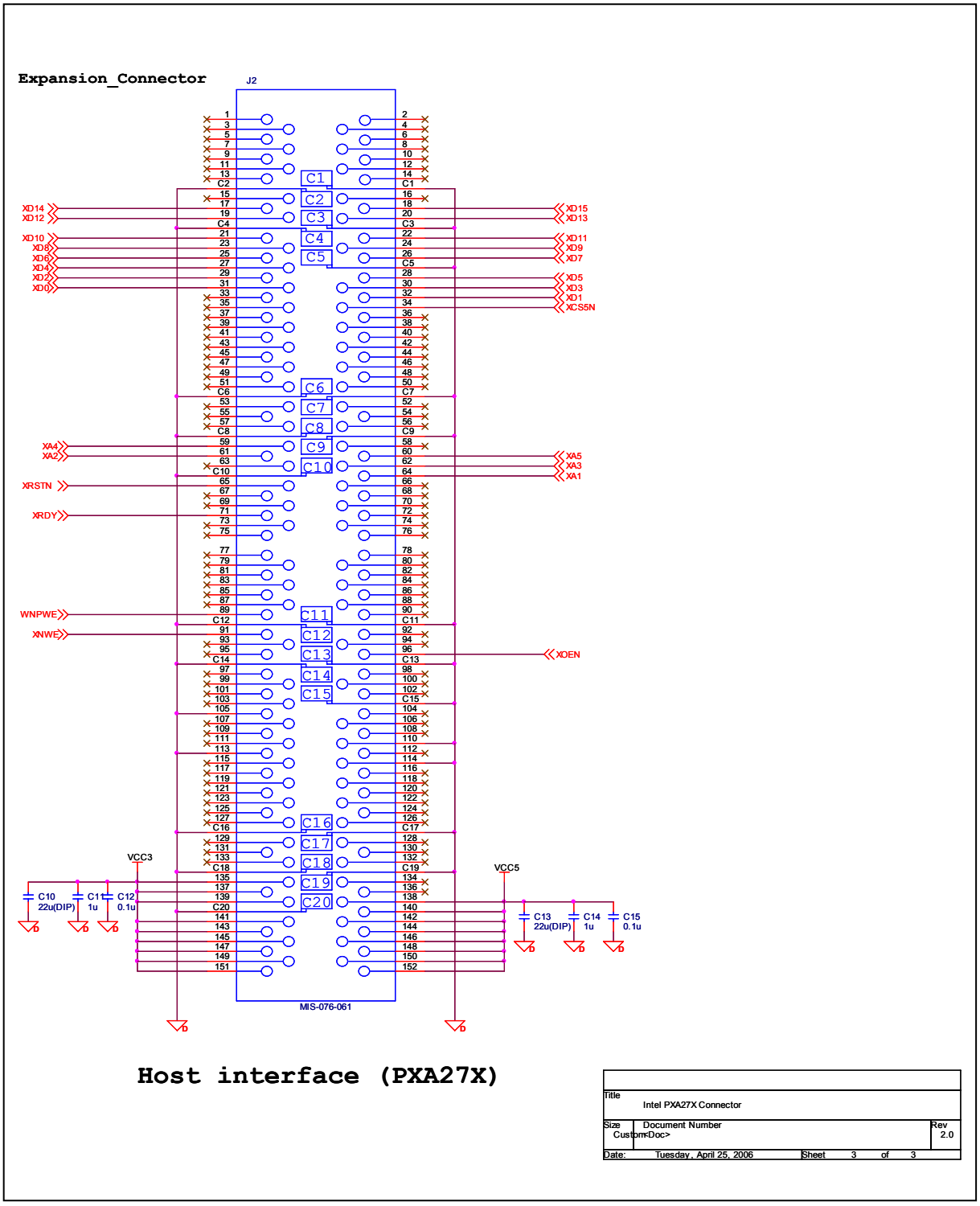

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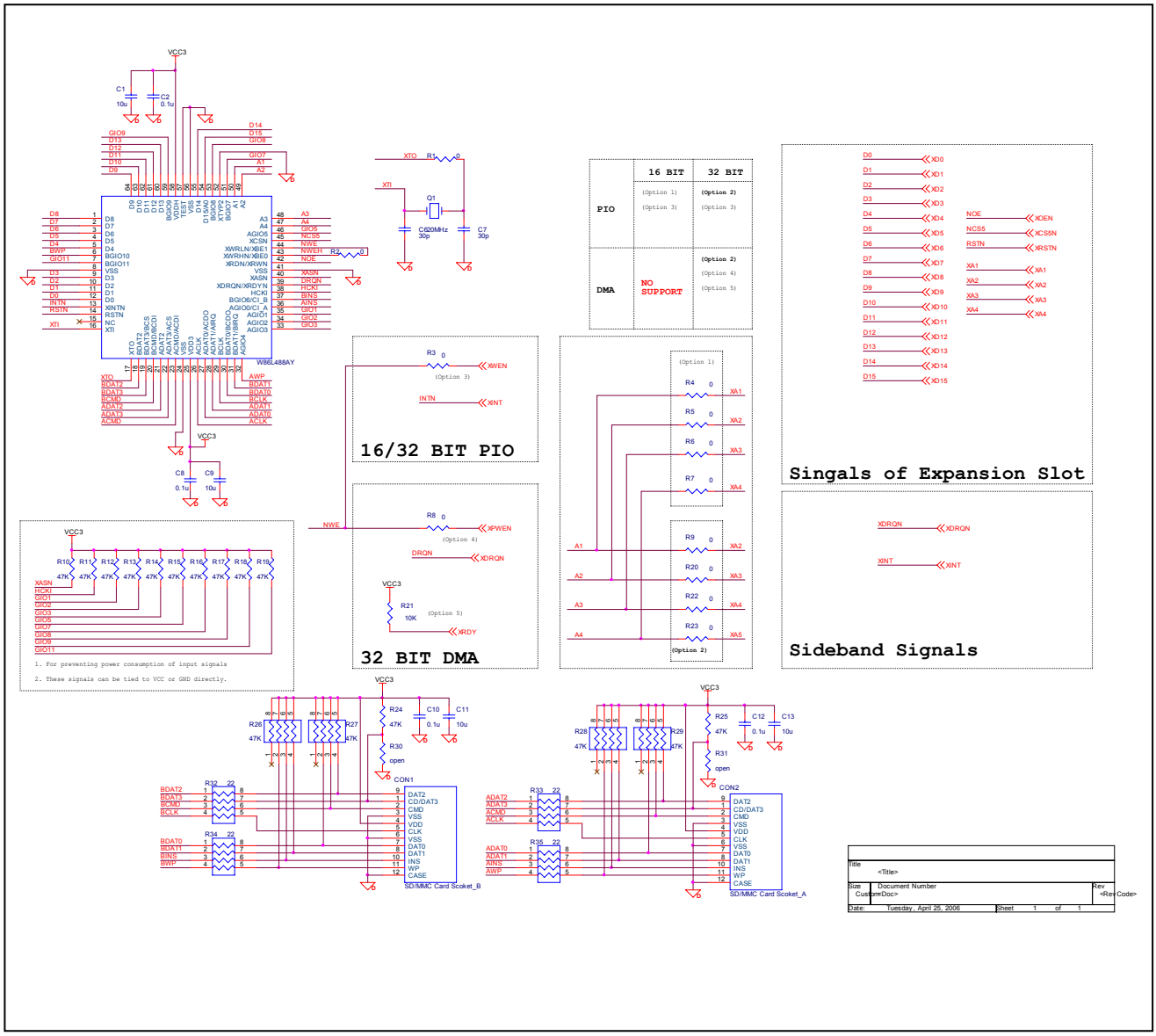
11.2 W86L488AY Reference Schematic

16/32bit PIO/DMA mode with PXA255/PXA27X expansion connector



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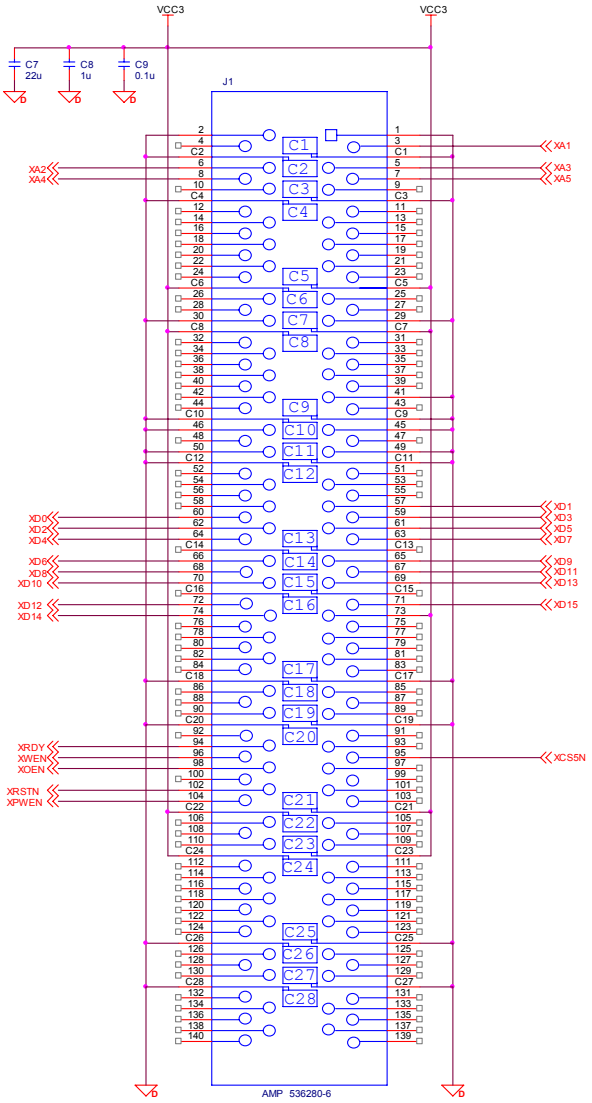

Host interface (PXA25X)

Title	Intel PXA25X Connector		
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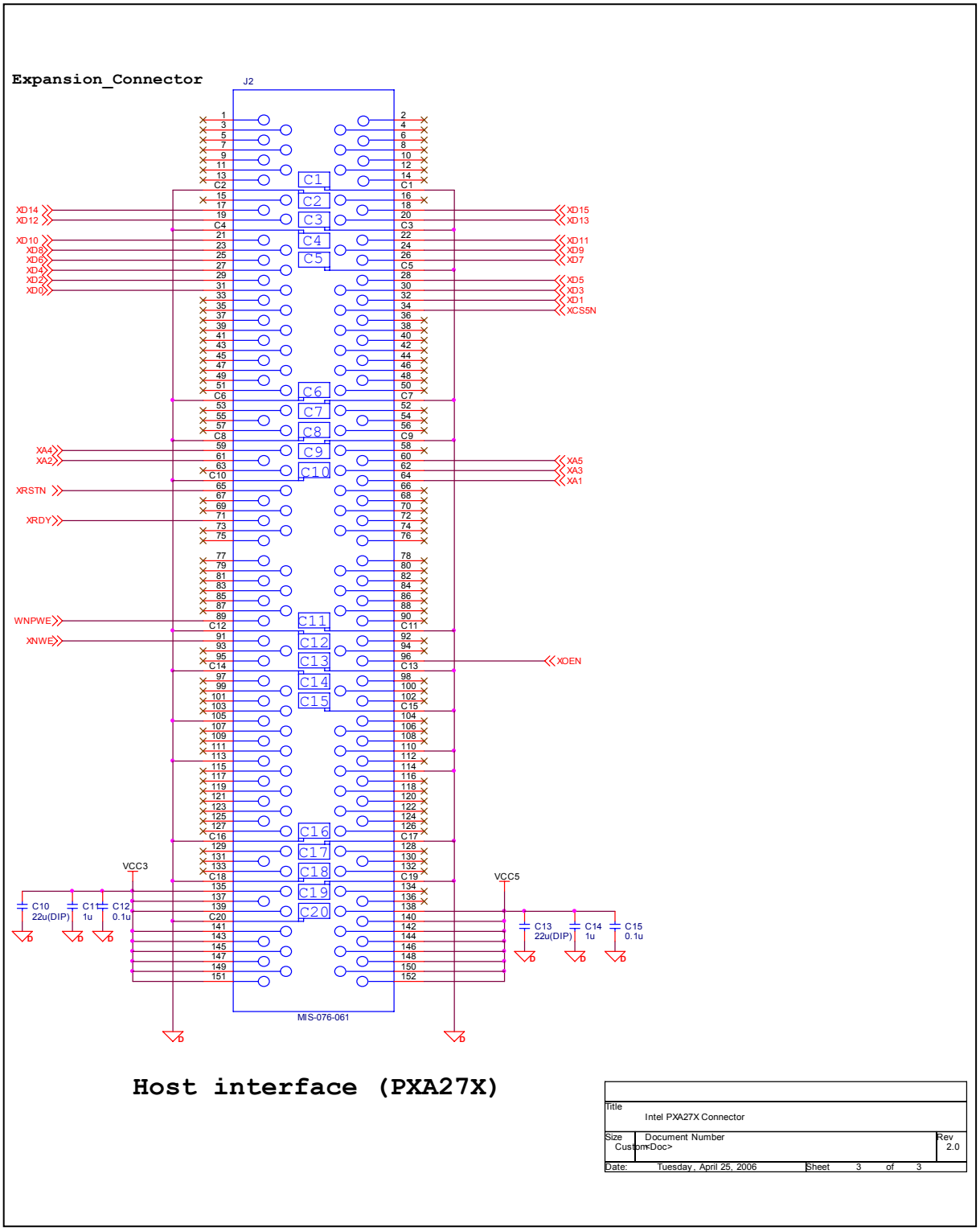

Host interface (PXA27X)

Title	Intel PXA27X Connector		
Size Custom	Document Number <Doc>		Rev 2.0
Date: Tuesday, April 25, 2006	Sheet 3 of 3		

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