256Mb J-die SDRAM Specification

54 TSOP-II with Lead-Free & Halogen-Free

(RoHS compliant)

Table of Contents

\Revision History

Revision	Month	Year	History
1.0	June	2007	- Release 1.0 version SPEC
1.1	October	2007	- Changed IDD current SPEC - Revised typo of package dimension - Added the comment of Halogen-free supporting
1.2	January	2008	- Added 200Mhz speed
1.21	March	2008	- Added Package pin out lead width - Added 200MHz current SPEC

16M x 4Bit x 4 Banks / 8M x 8Bit x 4 Banks / 4M x 16Bit x 4 Banks SDRAM

1.0 Features

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM (x4,x8) & L(U)DQM (x16) for masking
- Auto & self refresh
- 64ms refresh period (8K Cycle)
- Lead-Free & Halogen-Free Package
- RoHS compliant

2.0 General Description

The K4S560432J / K4S560832J / K4S561632J is 268,435,456 bits synchronous high data rate Dynamic RAM organized as 4 x 16,777,216 words by 4 bits / 4 x 8,388,608 words by 8bits / 4 x 4,194,304 words by 16bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

3.0 Ordering Information

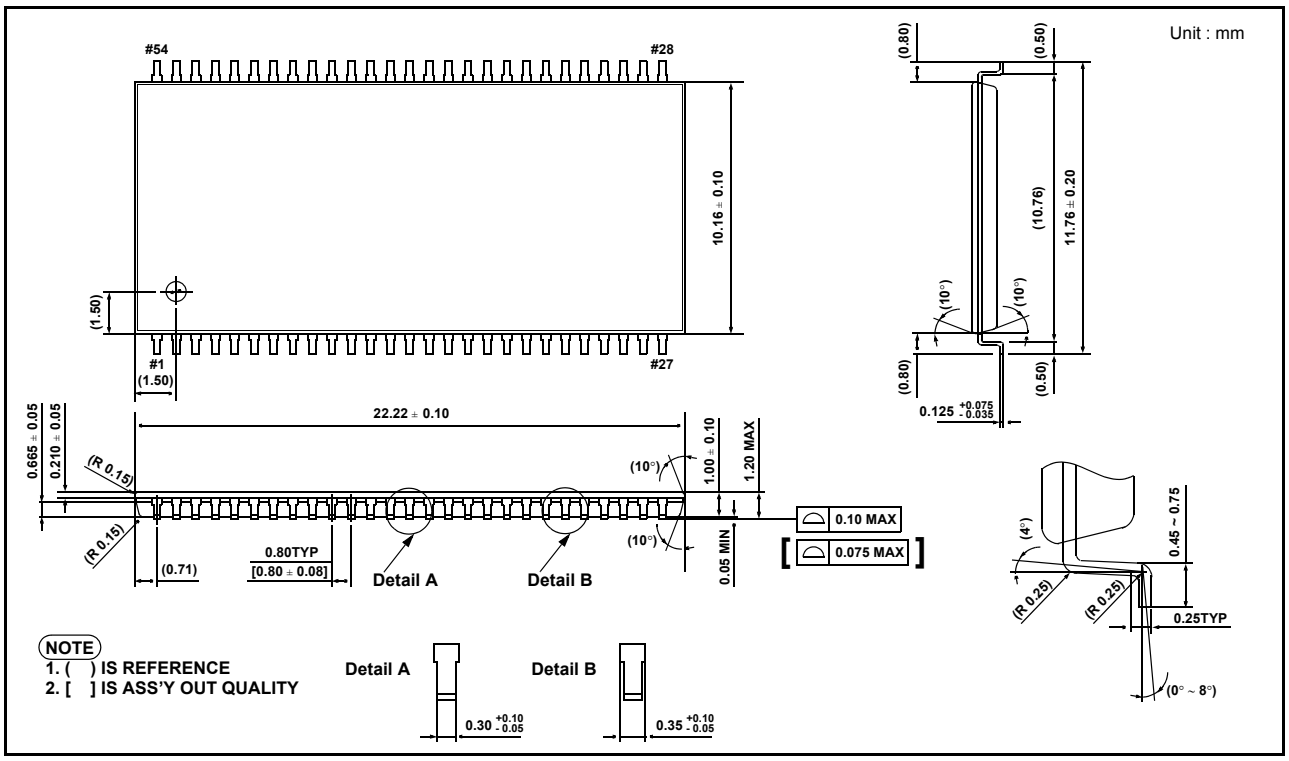
Part No.	Orgainization	Max Freq.	Interface	Package
K4S560432J-U*1C/L75	64M x 4	133MHz (CL=3)	LVTTL	54pin TSOP(II) Lead-Free & Halogen-Free*1
K4S560832J-UC/L75	32M x 8	133MHz (CL=3)		
K4S561632J-UC/L50	16M x 16	200MHz (CL=3)		
K4S561632J-UC/L60		166MHz (CL=3)		
K4S561632J-UC/L75		133MHz (CL=3)		

Note 1 : 256Mb J-die SDR DRAMs support Lead-Free & Halogen-Free package with Lead-Free package code(-U).

Organization	Row Address	Column Address
64Mx4	A0~A12	A0-A9, A11
32Mx8	A0~A12	A0-A9
16Mx16	A0~A12	A0-A8

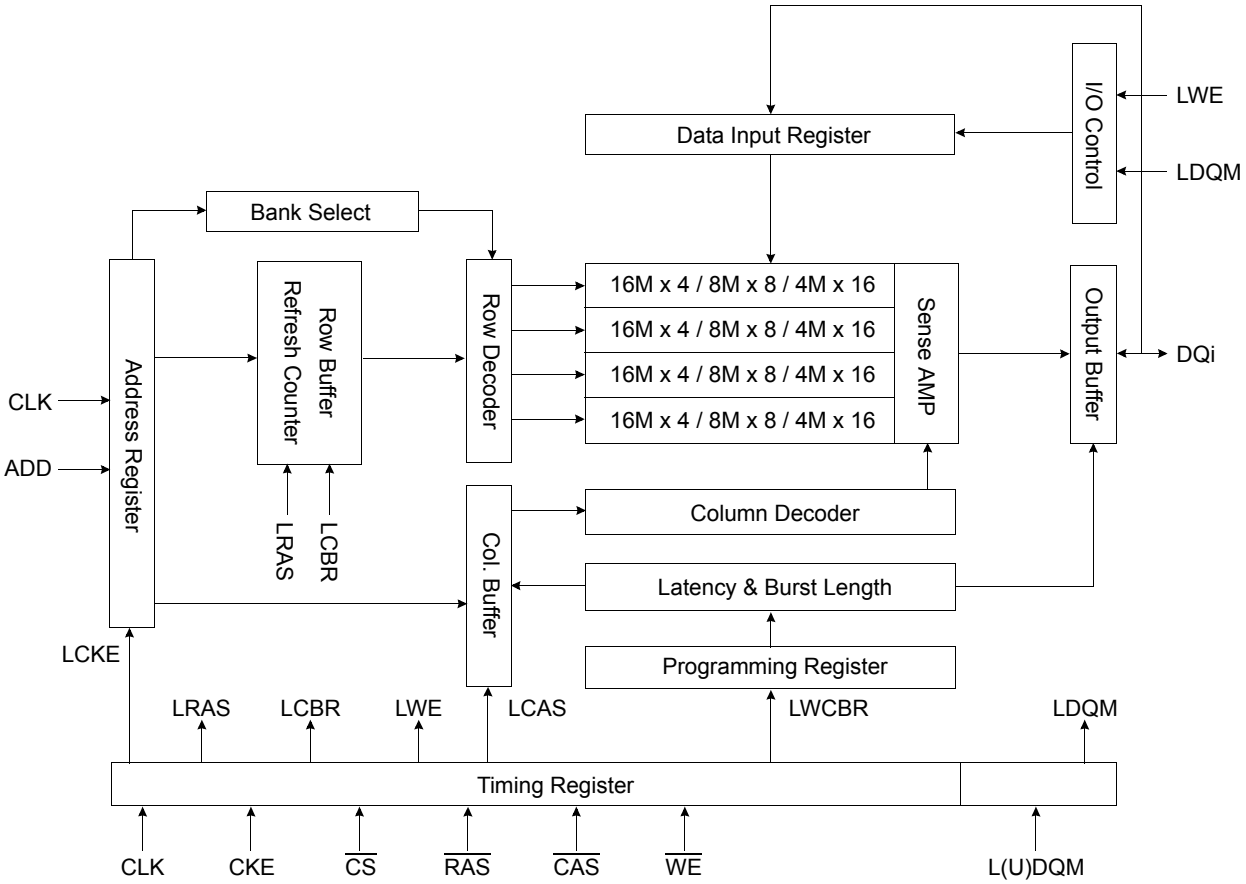
Row & Column address configuration

4.0 Package Physical Dimension



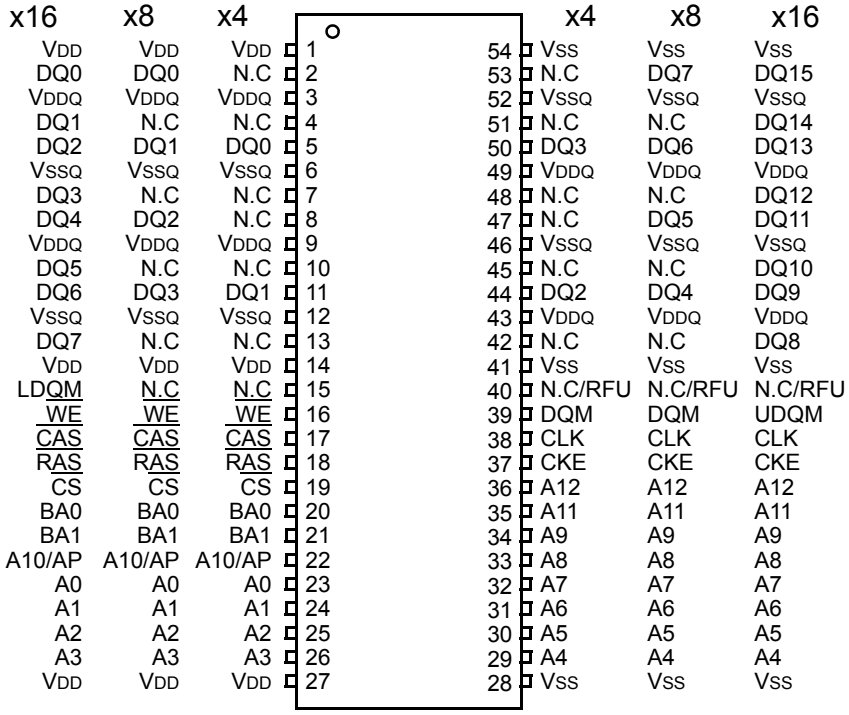
54Pin TSOP(II) Package Dimension

5.0 Functional Block Diagram



* Samsung Electronics reserves the right to change products or specification without notice.

6.0 Pin Configuration (Top view)



54Pin TSOP
(400mil x 875mil)
(0.8 mm Pin pitch)

7.0 Pin Function Description

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{12}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{12}, Column address : (x4 : CA_0 ~ CA_9,CA_{11}), (x8 : CA_0 ~ CA_9), (x16 : CA_0 ~ CA_8)
BA_0 ~ BA_1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ_0 ~ N	*Data input/output*	Data inputs/outputs are multiplexed on the same pins. (x4 : DQ_0 ~ 3), (x8 : DQ_0 ~ 7), (x16 : DQ_0 ~ 15)
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

8.0 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

9.0 DC Operating Conditions

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

10.0 Capacitance

(V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Clock	C_{CLK}	2.5	3.5	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.5	3.8	pF
Address	C_{ADD}	2.5	3.8	pF
(x4 : DQ_0 ~ DQ_3), (x8 : DQ_0 ~ DQ_7), (x16 : DQ_0 ~ DQ_{15})	C_{OUT}	4.0	6.0	pF

11.0 DC Characteristics (x4, x8)

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version 75	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		70	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		2	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		15	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		10		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		5	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		5		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		28	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		20	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4banks Activated. t_{CCD} = 2CLKs		110	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		160	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	3	mA	3
			L	1.5	mA	4

Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S5604(08)32J-UC
4. K4S5604(08)32J-UL
5. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

12.0 DC Characteristics (x16)

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

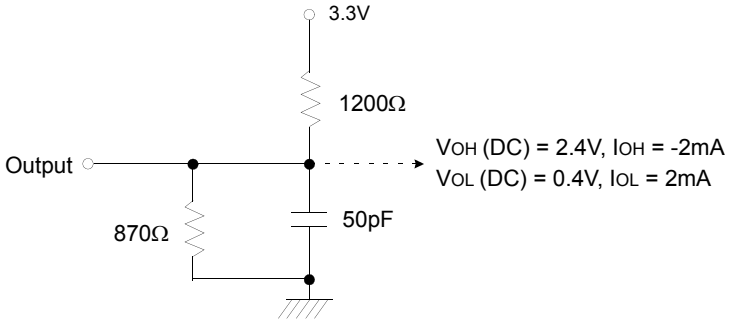
Parameter	Symbol	Test Condition		Version			Unit	Note
				50	60	75		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		110	90	70	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		2			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		15			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		10				
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		5			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		5				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		28			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		20			mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4banks Activated. t_{CCD} = 2CLKs		140	120	110	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		200	180	160	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	3			mA	3
			L	1.5			mA	4

Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S561632J-UC
4. K4S561632J-UL
5. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

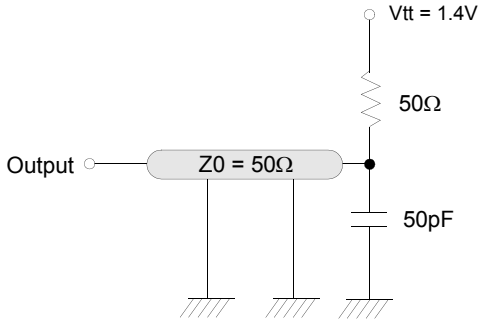
13.0 AC Operating Test Conditions

(V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

14.0 Operating AC Parameter

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			50 (x16 only)	60 (x16 only)	75		
Row active to row active delay		tRRD(min)	10	12	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	15	18	20	ns	1
Row precharge time		tRP(min)	15	18	20	ns	1
Row active time		tRAS(min)	37.5	42	45	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	55	60	65	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + tRP			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. In 100MHz and below 100MHz operating conditions, tRDL=1CLK and tDAL=1CLK + 20ns is also supported. SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.
6. tRC =tRFC, tRDL = tWR.

15.0 AC Characteristics

(AC operating conditions unless otherwise noted)

Parameter		Symbol	50 (x16 only)		60(x16 only)		75		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	5	1000	6	1000	7.5	1000	ns	1
	CAS latency=2		-		-		10			
CLK to valid output delay	CAS latency=3	tSAC	-	4.5		5		5.4	ns	1,2
	CAS latency=2		-	-		-		6		
Output data hold time	CAS latency=3	tOH	2	-	2.5		3		ns	2
	CAS latency=2		-	-	-		3			
CLK high pulse width		tCH	2	-	2.5		2.5		ns	3
CLK low pulse width		tCL	2	-	2.5		2.5		ns	3
Input setup time		tSS	1.5	-	1.5		1.5		ns	3
Input hold time		tSH	1	-	1		0.8		ns	3
CLK to output in Low-Z		tSLZ	1	-	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	4.5		5		5.4	ns	
	CAS latency=2		-	-		-		6		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.
4. tSS applies for address setup time, clock enable setup time. commend setup time and data setup time
tSH applies for address holde time, clock enable hold time. commend hold time and data hold time

16.0 DQ Buffer Output Drive Characteristics

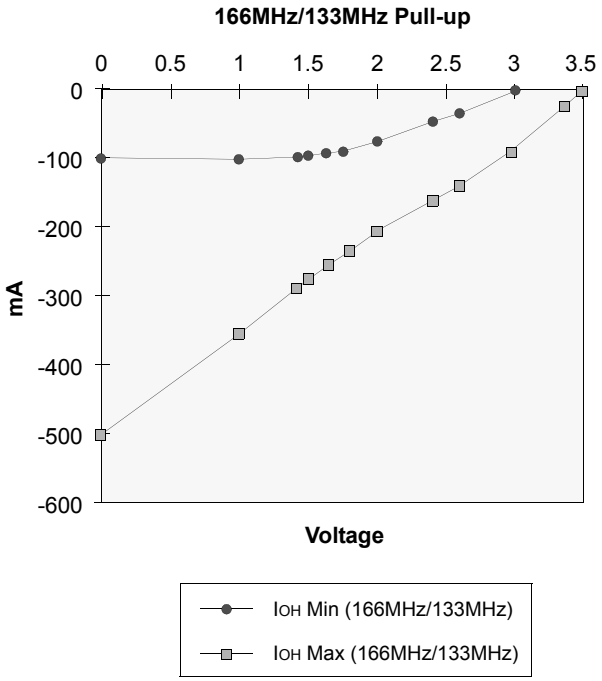
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

Notes : 1. Rise time specification based on 0pF + 50 Ω to VSS, use these values to design to.
2. Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
3. Measured into 50pF only, use these values to characterize to.
4. All measurements done with respect to VSS.

17.0 IBIS SPECIFICATION

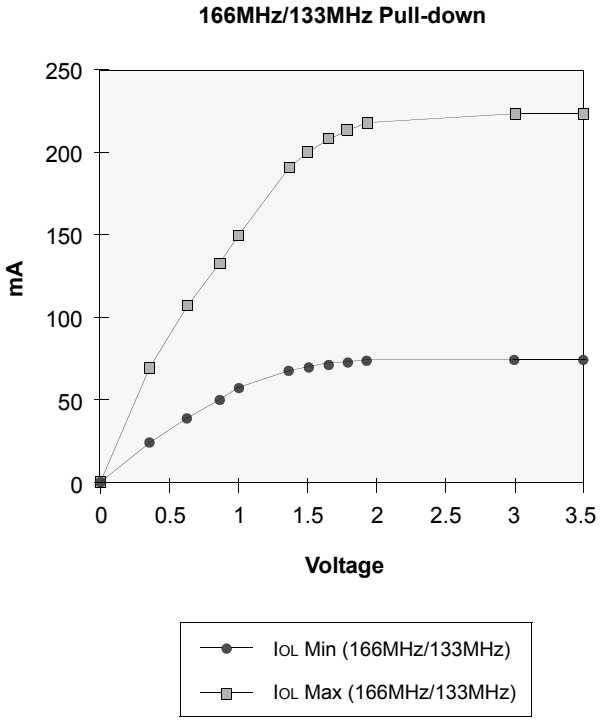
IOH Characteristics (Pull-up)

Voltage	166MHz 133MHz Min	166MHz 133MHz Max
(V)	I (mA)	I (mA)
3.45		-2.4
3.3		-27.3
3.0	0.0	-74.1
2.6	-21.1	-129.2
2.4	-34.1	-153.3
2.0	-58.7	-197.0
1.8	-67.3	-226.2
1.65	-73.0	-248.0
1.5	-77.9	-269.7
1.4	-80.8	-284.3
1.0	-88.6	-344.5
0.0	-93.0	-502.4



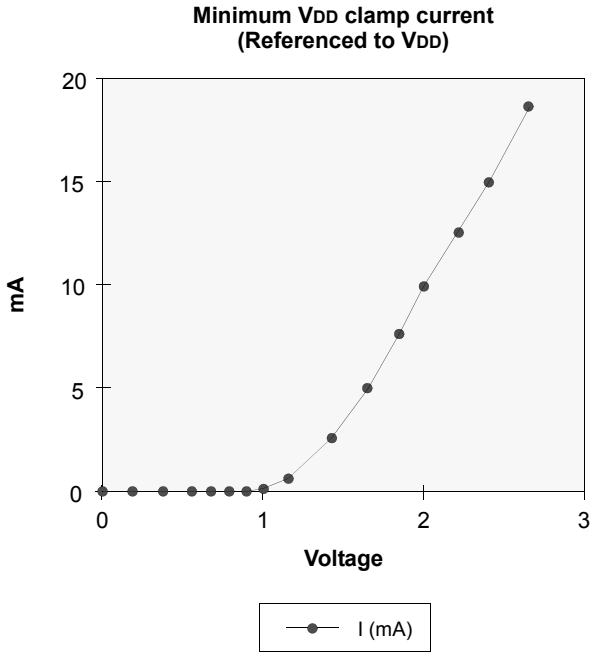
IOL Characteristics (Pull-down)

Voltage	166MHz 133MHz Min	166MHz 133MHz Max
(V)	I (mA)	I (mA)
0.0	0.0	0.0
0.4	27.5	70.2
0.65	41.8	107.5
0.85	51.6	133.8
1.0	58.0	151.2
1.4	70.7	187.7
1.5	72.9	194.4
1.65	75.4	202.5
1.8	77.0	208.6
1.95	77.6	212.0
3.0	80.3	219.6
3.45	81.4	222.6



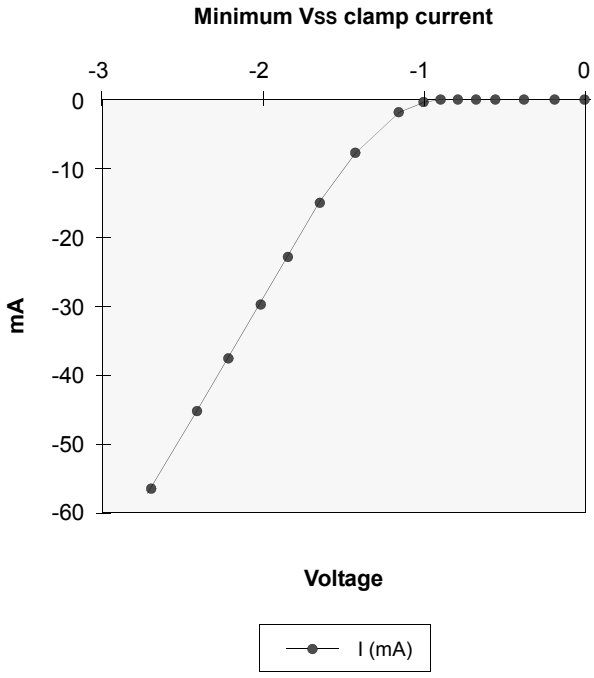
V_{DD} Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

V_{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31



V_{SS} Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

V_{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



18.0 Simplified Truth Table

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	$A_0 \sim A_9$, A_{11}, A_{12}	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

Notes : 1. OP Code : Operand code
$A_0 \sim A_{12}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)