

# 128Mbit GDDR SDRAM

***1M x 32Bit x 4 Banks  
Graphic Double Data Rate  
Synchronous DRAM  
with Bi-directional Data Strobe and DLL  
(144-Ball FBGA)***

**Revision 1.7**

**November 2003**

Samsung Electronics reserves the right to change products or specification without notice.

## **Revision History**

### **Revision 1.7 (November 14, 2003)**

- Typo corrected

### **Revision 1.6 (August 14, 2003)**

- Added a note for the input reference voltage of clock in case of differential clocks

### **Revision 1.5 (August 11, 2003)**

- Typo corrected

### **Revision 1.4 (April 30, 2003)**

- Added Lead free package part number in the datasheet

### **Revision 1.3 (April 14, 2003)**

- K4D263238E-GC2A/33/36 support wide voltage range from 2.375V to 2.94V

### **Revision 1.2 (April 7, 2003)**

- Removed K4D263238E-GL36 from the spec.

### **Revision 1.1 (March 17, 2003)**

- Typo corrected

### **Revision 1.0 (February 13, 2003)**

- Defined DC spec
- Added K4D263238E-GC25 and K4D263238E-GL36 in the spec.

## K4D263238E-GC

## 128M GDDR SDRAM

### ***1M x 32Bit x 4 Banks Graphic Double Data Rate Synchronous DRAM with Bi-directional Data Strobe and DLL***

#### FEATURES

- VDD/VDDQ = 2.8V  $\pm$  5% for -GC25
- VDD/VDDQ = 2.5V  $\pm$  5% for -GC2A/33/36/40/45
- SSTL\_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
  - Read latency 3, 4, 5 (clock)
  - Burst length (2, 4, 8 and Full page)
  - Burst type (sequential & interleave)
- Full page burst length for sequential burst type only
- Start address of the full page burst should be even
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- No Write-Interrupted by Read Function
- 4 DQS's ( 1DQS / Byte )
- Data I/O transactions on both edges of Data strobe
- DLL aligns DQ and DQS transitions with Clock transition
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 32ms refresh period (4K cycle)
- 144-Ball FBGA
- Maximum clock frequency up to 400MHz
- Maximum data rate up to 800Mbps/pin

#### ORDERING INFORMATION

| Part NO.        | Max Freq. | Max Data Rate | Interface                 | Package       |
|-----------------|-----------|---------------|---------------------------|---------------|
| K4D263238E-GC25 | 400MHz    | 800Mbps/pin   | SSTL_2<br>(VDD/VDDQ=2.8V) | 144-Ball FBGA |
| K4D263238E-GC2A | 350MHz    | 700Mbps/pin   | SSTL_2<br>(VDD/VDDQ=2.5V) |               |
| K4D263238E-GC33 | 300MHz    | 600Mbps/pin   |                           |               |
| K4D263238E-GC36 | 275MHz    | 550Mbps/pin   |                           |               |
| K4D263238E-GC40 | 250MHz    | 500Mbps/pin   |                           |               |
| K4D263238E-GC45 | 222MHz    | 444Mbps/pin   |                           |               |

**K4D263238E-VC is the Lead Free package part number.**

#### GENERAL DESCRIPTION

##### **FOR 1M x 32Bit x 4 Bank DDR SDRAM**

The K4D263238E is 134,217,728 bits of hyper synchronous data rate Dynamic RAM organized as 4 x1,048,576 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 3.2GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

## PIN CONFIGURATION (Top View)

|   | 2                       | 3                      | 4    | 5    | 6           | 7           | 8           | 9                | 10               | 11    | 12                     | 13   |
|---|-------------------------|------------------------|------|------|-------------|-------------|-------------|------------------|------------------|-------|------------------------|------|
| B | DQS0                    | DM0                    | VSSQ | DQ3  | DQ2         | DQ0         | DQ31        | DQ29             | DQ28             | VSSQ  | DM3                    | DQS3 |
| C | DQ4                     | VDDQ                   | NC   | VDDQ | DQ1         | VDDQ        | VDDQ        | DQ30             | VDDQ             | NC    | VDDQ                   | DQ27 |
| D | DQ6                     | DQ5                    | VSSQ | VSSQ | VSSQ        | VDD         | VDD         | VSSQ             | VSSQ             | VSSQ  | DQ26                   | DQ25 |
| E | DQ7                     | VDDQ                   | VDD  | VSS  | VSSQ        | VSS         | VSS         | VSSQ             | VSS              | VDD   | VDDQ                   | DQ24 |
| F | DQ17                    | DQ16                   | VDDQ | VSSQ | VSS Thermal | VSS Thermal | VSS Thermal | VSS Thermal      | VSSQ             | VDDQ  | DQ15                   | DQ14 |
| G | DQ19                    | DQ18                   | VDDQ | VSSQ | VSS Thermal | VSS Thermal | VSS Thermal | VSS Thermal      | VSSQ             | VDDQ  | DQ13                   | DQ12 |
| H | DQS2                    | DM2                    | NC   | VSSQ | VSS Thermal | VSS Thermal | VSS Thermal | VSS Thermal      | VSSQ             | NC    | DM1                    | DQS1 |
| J | DQ21                    | DQ20                   | VDDQ | VSSQ | VSS Thermal | VSS Thermal | VSS Thermal | VSS Thermal      | VSSQ             | VDDQ  | DQ11                   | DQ10 |
| K | DQ22                    | DQ23                   | VDDQ | VSSQ | VSS         | VSS         | VSS         | VSS              | VSSQ             | VDDQ  | DQ9                    | DQ8  |
| L | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | VDD  | VSS  | A10         | VDD         | VDD         | RFU <sub>1</sub> | VSS              | VDD   | NC                     | NC   |
| M | $\overline{\text{RAS}}$ | NC                     | NC   | BA1  | A2          | A11         | A9          | A5               | RFU <sub>2</sub> | CK    | $\overline{\text{CK}}$ | MCL  |
| N | $\overline{\text{CS}}$  | NC                     | BA0  | A0   | A1          | A3          | A4          | A6               | A7               | A8/AP | CKE                    | VREF |

## NOTE:

1. RFU1 is reserved for A12
2. RFU2 is reserved for BA2
3. VSS Thermal balls are optional

## PIN DESCRIPTION

|                            |                          |            |                     |
|----------------------------|--------------------------|------------|---------------------|
| CK, $\overline{\text{CK}}$ | Differential Clock Input | BA0, BA1   | Bank Select Address |
| CKE                        | Clock Enable             | A0 ~ A11   | Address Input       |
| $\overline{\text{CS}}$     | Chip Select              | DQ0 ~ DQ31 | Data Input/Output   |
| $\overline{\text{RAS}}$    | Row Address Strobe       | VDD        | Power               |
| $\overline{\text{CAS}}$    | Column Address Strobe    | VSS        | Ground              |
| WE                         | Write Enable             | VDDQ       | Power for DQ's      |
| DQS                        | Data Strobe              | VSSQ       | Ground for DQ's     |
| DM                         | Data Mask                | NC         | No Connection       |
| RFU                        | Reserved for Future Use  | MCL        | Must Connect Low    |

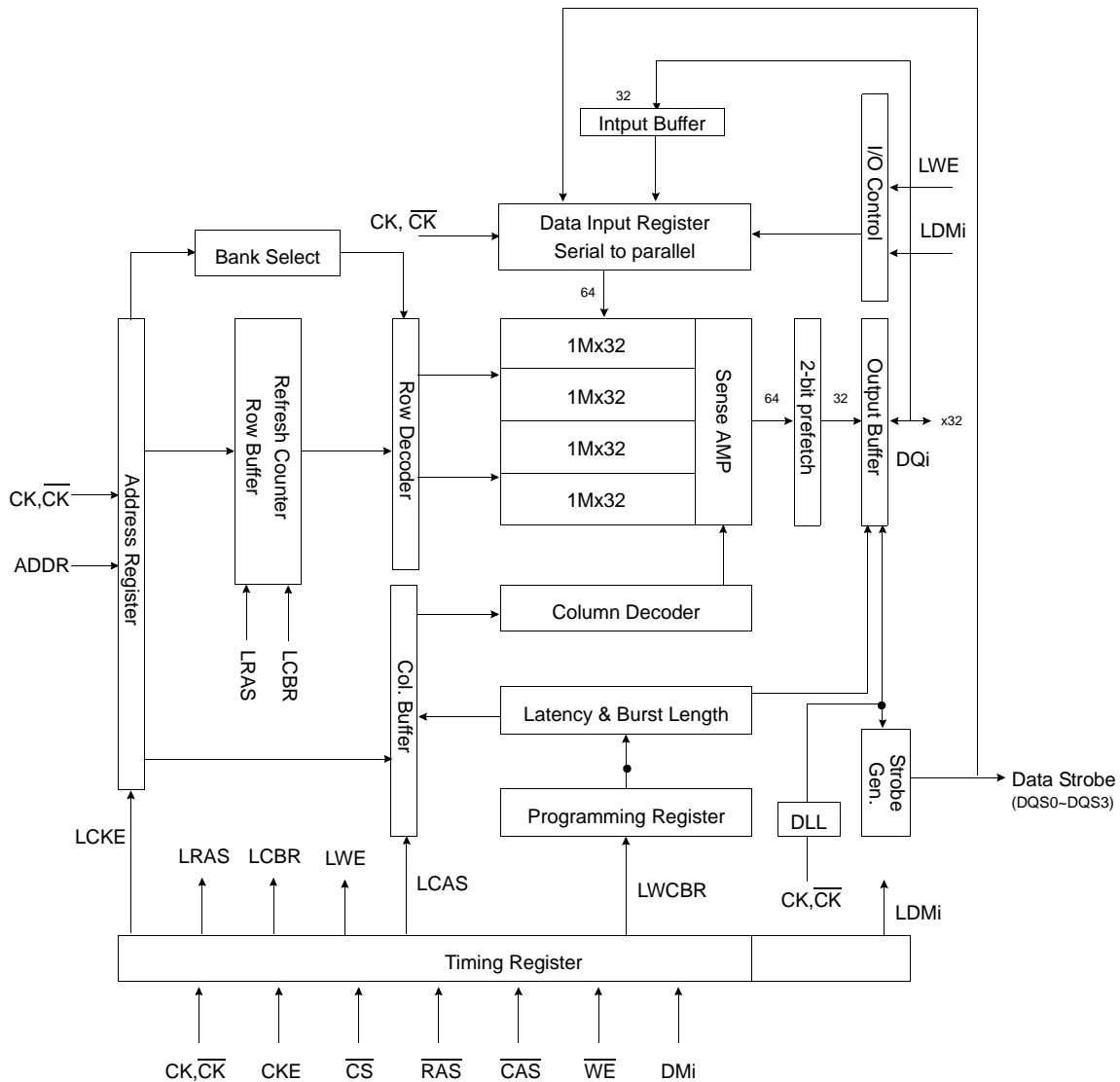
## INPUT/OUTPUT FUNCTIONAL DESCRIPTION

| Symbol                              | Type                                      | Function   |
|-------------------------------------|---|--|
| CK, $\overline{\text{CK}}^{*1}$     | Input                                     | The differential system clock Input.<br>All of the inputs are sampled on the rising edge of the clock except DQ's and DM's that are sampled on both edges of the DQS.  |
| CKE                                 | Input                                     | Activates the CK signal when high and deactivates the $\overline{\text{CK}}$ signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode.   |
| $\overline{\text{CS}}$              | Input                                     | $\overline{\text{CS}}$ enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.   |
| $\overline{\text{RAS}}$             | Input                                     | Latches row addresses on the positive going edge of the CK with $\overline{\text{RAS}}$ low. Enables row access & precharge.   |
| $\overline{\text{CAS}}$             | Input                                     | Latches column addresses on the positive going edge of the CK with $\overline{\text{CAS}}$ low. Enables column access.   |
| $\overline{\text{WE}}$              | Input                                     | Enables write operation and row precharge.<br>Latches data in starting from $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ active.   |
| DQS <sub>0</sub> ~ DQS <sub>3</sub> | Input/Output                              | Data input and output are synchronized with both edge of DQS.<br>DQS <sub>0</sub> for DQ <sub>0</sub> ~ DQ <sub>7</sub> , DQS <sub>1</sub> for DQ <sub>8</sub> ~ DQ <sub>15</sub> , DQS <sub>2</sub> for DQ <sub>16</sub> ~ DQ <sub>23</sub> , DQS <sub>3</sub> for DQ <sub>24</sub> ~ DQ <sub>31</sub> .            |
| DM <sub>0</sub> ~ DM <sub>3</sub>   | Input                                     | Data In mask. Data In is masked by DM Latency=0 when DM is high in burst write. DM <sub>0</sub> for DQ <sub>0</sub> ~ DQ <sub>7</sub> , DM <sub>1</sub> for DQ <sub>8</sub> ~ DQ <sub>15</sub> , DM <sub>2</sub> for DQ <sub>16</sub> ~ DQ <sub>23</sub> , DM <sub>3</sub> for DQ <sub>24</sub> ~ DQ <sub>31</sub> . |
| DQ <sub>0</sub> ~ DQ <sub>31</sub>  | Input/Output                              | Data inputs/Outputs are multiplexed on the same pins.  |
| BA <sub>0</sub> , BA <sub>1</sub>   | Input                                     | Selects which bank is to be active.  |
| A <sub>0</sub> ~ A <sub>11</sub>    | Input                                     | Row/Column addresses are multiplexed on the same pins.<br>Row addresses : RA <sub>0</sub> ~ RA <sub>11</sub> , Column addresses : CA <sub>0</sub> ~ CA <sub>7</sub> .<br>Column address CA <sub>8</sub> is used for auto precharge.  |
| VDD/VSS                             | Power Supply                              | Power and ground for the input buffers and core logic.   |
| VDDQ/VSSQ                           | Power Supply                              | Isolated power supply and ground for the output buffers to provide improved noise immunity.  |
| VREF                                | Power Supply                              | Reference voltage for inputs, used for SSTL interface.   |
| NC/RFU                              | No connection/<br>Reserved for future use | This pin is recommended to be left "No connection" on the device   |
| MCL                                 | Must Connect Low                          | Must connect low   |

\*1 : The timing reference point for the differential clocking is the cross point of CK and  $\overline{\text{CK}}$ .

For any applications using the single ended clocking, apply VREF to  $\overline{\text{CK}}$  pin.

## BLOCK DIAGRAM (1Mbit x 32I/O x 4 Bank)



## FUNCTIONAL DESCRIPTION

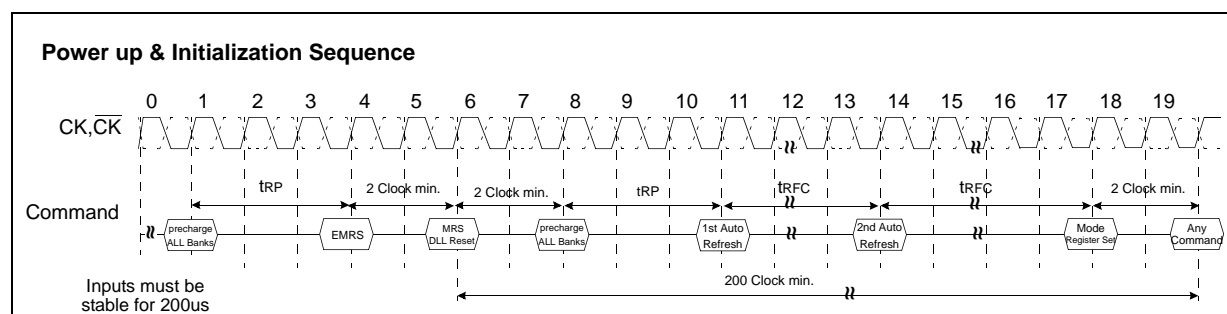
### • Power-Up Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and keep CKE at low state (All other inputs may be undefined)
  - Apply VDD before VDDQ .
  - Apply VDDQ before VREF & VTT
2. Start clock and maintain stable condition for minimum 200us.
3. The minimum of 200us after stable power and clock(CK,  $\overline{CK}$ ), apply NOP and take CKE to be high .
4. Issue precharge command for all banks of the device.
5. Issue a EMRS command to enable DLL
- \*1 6. Issue a MRS command to reset DLL. The additional 200 clock cycles are required to lock the DLL.
- \*1,2 7. Issue precharge command for all banks of the device.
8. Issue at least 2 or more auto-refresh commands.
9. Issue a mode register set command with A8 to low to initialize the mode register.

\*1 The additional 200cycles of clock input is required to lock the DLL after enabling DLL.

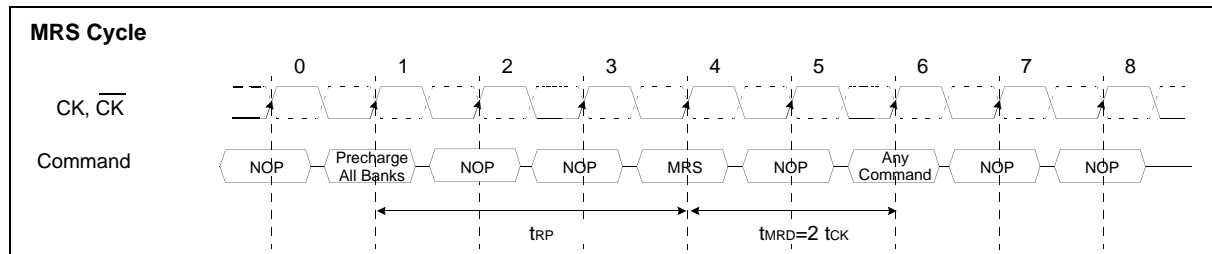
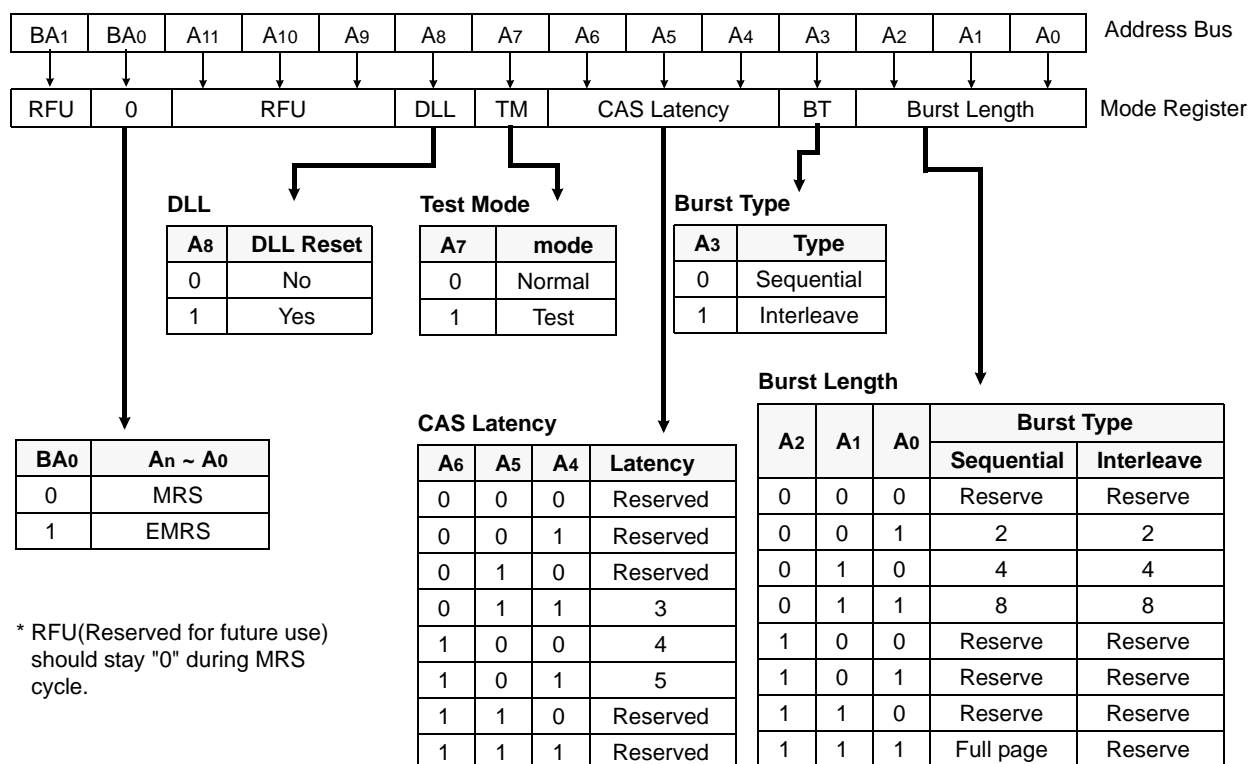
\*2 Sequence of 6&7 is regardless of the order



\* When the operating frequency is changed, DLL reset should be required again.  
After DLL reset again, the minimum 200 cycles of clock input is needed to lock the DLL.

## MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$  and  $\overline{WE}$  (The DDR SDRAM should be in active mode with  $\overline{CKE}$  already high prior to writing into the mode register). The state of address pins  $A_0 \sim A_{11}$  and  $BA_0, BA_1$  in the same cycle as  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$  and  $\overline{WE}$  going low is written in the mode register. Minimum two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses  $A_0 \sim A_2$ , addressing mode uses  $A_3$ , CAS latency (read latency from column address) uses  $A_4 \sim A_6$ .  $A_7$  is used for test mode.  $A_8$  is used for DLL reset.  $A_7, A_8, BA_0$  and  $BA_1$  must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.



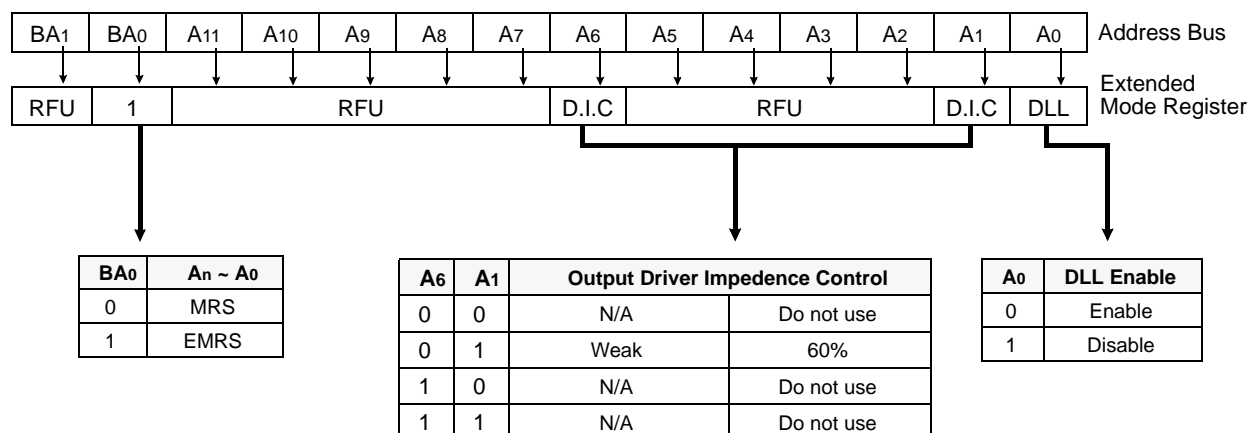
\*1 : MRS can be issued only at all banks precharge state.

\*2 : Minimum  $t_{RP}$  is required to issue MRS command.



## EXTENDED MODE REGISTER SET(EMRS)

The extended mode register stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$  and high on  $BA_0$  (The DDR SDRAM should be in all bank precharge with  $\overline{CKE}$  already high prior to writing into the extended mode register). The state of address pins  $A_0$ ,  $A_2 \sim A_5$ ,  $A_7 \sim A_{11}$  and  $BA_1$  in the same cycle as  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$  and  $\overline{WE}$  going low are written in the extended mode register.  $A_1$  and  $A_6$  are used for setting driver strength to normal, weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state.  $A_0$  is used for DLL enable or disable. "High" on  $BA_0$  is used for EMRS. All the other address pins except  $A_0, A_1, A_6$  and  $BA_0$  must be set to low for proper EMRS operation. Refer to the table for specific codes.



\*1 : RFU(Reserved for future use) should stay "0" during EMRS cycle.

Figure 7. Extended Mode Register set

**ABSOLUTE MAXIMUM RATINGS**

| Parameter                              | Symbol                             | Value      | Unit |
|--|------------------------------------|------------|------|
| Voltage on any pin relative to Vss     | V <sub>IN</sub> , V <sub>OUT</sub> | -0.5 ~ 3.6 | V    |
| Voltage on VDD supply relative to Vss  | VDD                                | -1.0 ~ 3.6 | V    |
| Voltage on VDDQ supply relative to Vss | VDDQ                               | -0.5 ~ 3.6 | V    |
| Storage temperature                    | T <sub>STG</sub>                   | -55 ~ +150 | °C   |
| Power dissipation                      | P <sub>D</sub>                     | 3.3        | W    |
| Short circuit current                  | I <sub>OS</sub>                    | 50         | mA   |

**Note :** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**POWER & DC OPERATING CONDITIONS(SSTL\_2 In/Out)**

Recommended operating conditions(Voltage referenced to Vss=0V, T<sub>A</sub>=0 to 65°C)

| Parameter                 | Symbol               | Min                   | Typ  | Max                   | Unit | Note                        |
|---------------------------|----------------------|-----------------------|------|-----------------------|------|-----------------------------|
| Device Supply voltage     | VDD                  | 2.66                  | 2.8  | 2.94                  | V    | 1, 8                        |
|                           |                      | 2.375                 | 2.5  | 2.625                 | V    | 1, 9                        |
| Output Supply voltage     | VDDQ                 | 2.66                  | 2.8  | 2.94                  | V    | 1, 8                        |
|                           |                      | 2.375                 | 2.5  | 2.625                 | V    | 1, 9                        |
| Reference voltage         | VREF                 | 0.49*VDDQ             | -    | 0.51*VDDQ             | V    | 2                           |
| Termination voltage       | V <sub>tt</sub>      | VREF-0.04             | VREF | VREF+0.04             | V    | 3                           |
| Input logic high voltage  | V <sub>IH</sub> (DC) | VREF+0.15             | -    | VDDQ+0.30             | V    | 4                           |
| Input logic low voltage   | V <sub>IL</sub> (DC) | -0.30                 | -    | VREF-0.15             | V    | 5                           |
| Output logic high voltage | V <sub>OH</sub>      | V <sub>tt</sub> +0.76 | -    | -                     | V    | I <sub>OH</sub> =-15.2mA, 7 |
| Output logic low voltage  | V <sub>OL</sub>      | -                     | -    | V <sub>tt</sub> -0.76 | V    | I <sub>OL</sub> =+15.2mA, 7 |
| Input leakage current     | I <sub>IL</sub>      | -5                    | -    | 5                     | uA   | 6                           |
| Output leakage current    | I <sub>OL</sub>      | -5                    | -    | 5                     | uA   | 6                           |

**Note :** 1. Under all conditions VDDQ must be less than or equal to VDD.

2. VREF is expected to equal 0.50\*VDDQ of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the VREF may not exceed + 2% of the DC value.

3. V<sub>tt</sub> of the transmitting device must track VREF of the receiving device.

4. V<sub>IH</sub>(max.)= VDDQ +1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.

5. V<sub>IL</sub>(min.)= -1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.

6. For any pin under test input of 0V ≤ V<sub>IN</sub> ≤ VDD is acceptable. For all other pins that are not under test V<sub>IN</sub>=0V.

7. Output logic high voltage and low voltage is depend on output channel condition.

8. VDD/VDDQ = 2.8V ± 5% for K4D263238E-GC25

9. VDD/VDDQ = 2.5V ± 5% for K4D263238E-GC2A/33/36/40/45

**10 . K4D263238E-GC2A/33/36 support wide voltage range from 2.375V to 2.94V.**

**DC CHARACTERISTICS**

Recommended operating conditions Unless Otherwise Noted, TA=0 to 65°C)

| Parameter   | Symbol | Test Condition  | Version |     |     |     |     |     | Unit | Note |
|---|--------|---|---------|-----|-----|-----|-----|-----|------|------|
|   |        |   | -25     | -2A | -33 | -36 | -40 | -45 |      |      |
| Operating Current<br>(One Bank Active)              | ICC1   | Burst Lenth=2 trc ≥ trc(min)<br>IOL=0mA, tcc= tcc(min)      | 530     | 455 | 400 | 375 | 350 | 350 | mA   | 1    |
| Precharge Standby Current<br>in Power-down mode     | ICC2P  | CKE ≤ VIL(max), tcc= tcc(min)                               | 110     | 95  | 80  | 80  | 75  | 70  | mA   |      |
| Precharge Standby Current<br>in Non Power-down mode | ICC2N  | CKE ≥ VIH(min), CS ≥ VIH(min),<br>tcc= tcc(min)             | 185     | 150 | 130 | 125 | 115 | 110 | mA   |      |
| Active Standby Current<br>power-down mode           | ICC3P  | CKE ≤ VIL(max), tcc= tcc(min)                               | 200     | 160 | 140 | 130 | 120 | 120 | mA   |      |
| Active Standby Current<br>in Non Power-down mode    | ICC3N  | CKE ≥ VIH(min), CS ≥ VIH(min),<br>tcc= tcc(min)             | 410     | 300 | 260 | 250 | 240 | 230 | mA   |      |
| Operating Current<br>( Burst Mode)                  | ICC4   | IOL=0mA ,tcc= tcc(min),<br>Page Burst, All Banks activated. | 1090    | 830 | 735 | 680 | 625 | 570 | mA   |      |
| Refresh Current                                     | ICC5   | trc ≥ trfc(min)   | 415     | 350 | 310 | 310 | 300 | 290 | mA   | 2    |
| Self Refresh Current                                | ICC6   | CKE ≤ 0.2V  | 3       |     |     |     |     |     | mA   |      |
| Operating Current<br>(4Bank interleaving)           | ICC7   | Burst Length=4 trc ≥ trc(min)<br>IOL=0mA, tcc= tcc(min)     | 1210    | 935 | 830 | 770 | 710 | 655 | mA   |      |

**Note** : 1. Measured with outputs open.  
2. Refresh period is 32ms.

**AC INPUT OPERATING CONDITIONS**

Recommended operating conditions(Voltage referenced to VSS=0V, TA=0 to 65°C)

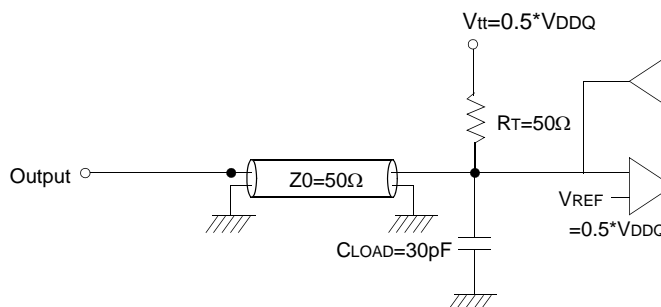
| Parameter  | Symbol | Min          | Typ | Max          | Unit | Note |
|--|--------|--------------|-----|--------------|------|------|
| Input High (Logic 1) Voltage ;DQ                           | VIH    | VREF+0.35    | -   | -            | V    |      |
|  |        | VREF+0.4     | -   | -            | V    | 3    |
| Input Low (Logic 0) Voltage; DQ                            | VIL    | -            | -   | VREF-0.35    | V    |      |
|  |        | -            | -   | VREF-0.4     | V    | 3    |
| Clock Input Differential Voltage; CK and $\overline{CK}$   | VID    | 0.7          | -   | VDDQ+0.6     | V    | 1    |
|  |        | 0.8          | -   | VDDQ+0.6     | V    | 1, 3 |
| Clock Input Crossing Point Voltage; CK and $\overline{CK}$ | VIX    | 0.5*VDDQ-0.2 | -   | 0.5*VDDQ+0.2 | V    | 2    |

**Note** : 1. VID is the magnitude of the difference between the input level on CK and the input level on  $\overline{CK}$   
2. The value of Vix is expected to equal 0.5\*VDDQ of the transmitting device and must track variations in the DC level of the same  
3. 400MHz only

**AC OPERATING TEST CONDITIONS** ( $T_A = 0$  to  $65^\circ\text{C}$ )

| Parameter   | Value                     | Unit | Note |
|---|---------------------------|------|------|
| Input reference voltage for CK(for single ended)        | $0.50 \cdot V_{DDQ}$      | V    | 1    |
| CK and $\overline{\text{CK}}$ signal maximum peak swing | 1.5                       | V    |      |
| CK signal minimum slew rate                             | 1.0                       | V/ns |      |
| Input Levels( $V_{IH}/V_{IL}$ )                         | $V_{REF}+0.4/V_{REF}-0.4$ | V    |      |
| Input timing measurement reference level                | $V_{REF}$                 | V    |      |
| Output timing measurement reference level               | $V_{tt}$                  | V    |      |
| Output load condition                                   | See Fig.1                 |      |      |

Note 1 : In case of differential clocks(CK and  $\overline{\text{CK}}$ ), input reference voltage for clock is a CK and  $\overline{\text{CK}}$  's crossing point  
Accordingly, clock duty should be measured at a CK and  $\overline{\text{CK}}$  's crossing point.



(Fig. 1) Output Load Circuit

**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

| Parameter  | Symbol    | Min | Max | Unit |
|--|-----------|-----|-----|------|
| Input capacitance(CK, $\overline{\text{CK}}$ )   | $C_{IN1}$ | 1.0 | 5.0 | pF   |
| Input capacitance( $A_0 \sim A_{11}$ , $BA_0 \sim BA_1$ )  | $C_{IN2}$ | 1.0 | 4.0 | pF   |
| Input capacitance( $\overline{\text{CKE}}$ , $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ ) | $C_{IN3}$ | 1.0 | 4.0 | pF   |
| Data & DQS input/output capacitance( $DQ_0 \sim DQ_{31}$ )   | $C_{OUT}$ | 1.0 | 6.5 | pF   |
| Input capacitance( $DM_0 \sim DM_3$ )  | $C_{IN4}$ | 1.0 | 6.5 | pF   |

**DECOUPLING CAPACITANCE GUIDE LINE**

Recommended decoupling capacitance added to power line at board.

| Parameter  | Symbol    | Value        | Unit          |
|--|-----------|--------------|---------------|
| Decoupling Capacitance between $V_{DD}$ and $V_{SS}$   | $C_{DC1}$ | $0.1 + 0.01$ | $\mu\text{F}$ |
| Decoupling Capacitance between $V_{DDQ}$ and $V_{SSQ}$ | $C_{DC2}$ | $0.1 + 0.01$ | $\mu\text{F}$ |

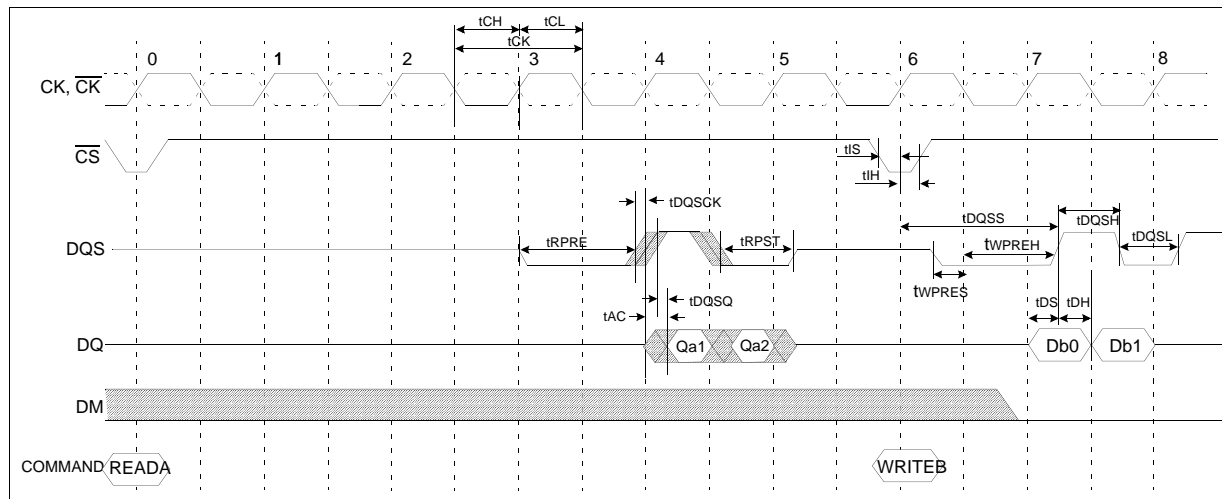
**Note** : 1.  $V_{DD}$  and  $V_{DDQ}$  pins are separated each other.  
All  $V_{DD}$  pins are connected in chip. All  $V_{DDQ}$  pins are connected in chip.  
2.  $V_{SS}$  and  $V_{SSQ}$  pins are separated each other  
All  $V_{SS}$  pins are connected in chip. All  $V_{SSQ}$  pins are connected in chip.

## AC CHARACTERISTICS

| Parameter                         | Symbol                       | -25                    |      | -2A                    |      | -33                    |      | -36                    |      | -40                    |      | -45                    |      | Unit | Note |
|-----------------------------------|------------------------------|------------------------|------|------------------------|------|------------------------|------|------------------------|------|------------------------|------|------------------------|------|------|------|
|                                   |                              | Min                    | Max  | Min                    | Max  | Min                    | Max  | Min                    | Max  | Min                    | Max  | Min                    | Max  |      |      |
| CK cycle time                     | CL=3                         | -                      | -    | -                      | -    | -                      | -    | -                      | -    | -                      | -    | 4.5                    | -    | ns   |      |
|                                   | CL=4                         | -                      | 4    | 2.86                   | 4    | 3.3                    | 10   | 3.6                    | 10   | 4.0                    | 10   | -                      | 10   | ns   |      |
|                                   | CL=5                         | 2.5                    | -    | -                      | -    | -                      | -    | -                      | -    | -                      | -    | -                      | -    | ns   |      |
| CK high level width               | tCH                          | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | tCK  |      |
| CK low level width                | tCL                          | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | tCK  |      |
| DQS out access time from CK       | tDQSK                        | -0.55                  | 0.55 | -0.55                  | 0.55 | -0.55                  | 0.55 | -0.6                   | 0.6  | -0.6                   | 0.6  | -0.7                   | 0.7  | ns   |      |
| Output access time from CK        | tAC                          | -0.55                  | 0.55 | -0.55                  | 0.55 | -0.55                  | 0.55 | -0.6                   | 0.6  | -0.6                   | 0.6  | -0.7                   | 0.7  | ns   |      |
| Data strobe edge to Dout edge     | tDQSQ                        | -                      | 0.35 | -                      | 0.35 | -                      | 0.35 | -                      | 0.40 | -                      | 0.40 | -                      | 0.45 | ns   | 1    |
| Read preamble                     | tRPRE                        | 0.9                    | 1.1  | 0.9                    | 1.1  | 0.9                    | 1.1  | 0.9                    | 1.1  | 0.9                    | 1.1  | 0.9                    | 1.1  | tCK  |      |
| Read postamble                    | tRPST                        | 0.4                    | 0.6  | 0.4                    | 0.6  | 0.4                    | 0.6  | 0.4                    | 0.6  | 0.4                    | 0.6  | 0.4                    | 0.6  | tCK  |      |
| CK to valid DQS-in                | tDQSS                        | 0.85                   | 1.15 | 0.85                   | 1.15 | 0.85                   | 1.15 | 0.85                   | 1.15 | 0.8                    | 1.2  | 0.8                    | 1.2  | tCK  |      |
| DQS-In setup time                 | tWPRES                       | 0                      | -    | 0                      | -    | 0                      | -    | 0                      | -    | 0                      | -    | 0                      | -    | ns   |      |
| DQS-in hold time                  | tWPREH                       | 0.35                   | -    | 0.35                   | -    | 0.35                   | -    | 0.35                   | -    | 0.35                   | -    | 0.3                    | -    | tCK  |      |
| DQS write postamble               | tWPST                        | 0.4                    | 0.6  | 0.4                    | 0.6  | 0.4                    | 0.6  | 0.4                    | 0.6  | 0.4                    | 0.6  | 0.4                    | 0.6  | tCK  |      |
| DQS-In high level width           | tDQSH                        | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | tCK  |      |
| DQS-In low level width            | tDQSL                        | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | 0.45                   | 0.55 | tCK  |      |
| Address and Control input setup   | tIS                          | 0.8                    | -    | 0.8                    | -    | 0.8                    | -    | 0.9                    | -    | 0.9                    | -    | 1.0                    | -    | ns   |      |
| Address and Control input hold    | tIH                          | 0.8                    | -    | 0.8                    | -    | 0.8                    | -    | 0.9                    | -    | 0.9                    | -    | 1.0                    | -    | ns   |      |
| DQ and DM setup time to DQS       | tDS                          | 0.35                   | -    | 0.35                   | -    | 0.35                   | -    | 0.40                   | -    | 0.40                   | -    | 0.45                   | -    | ns   |      |
| DQ and DM hold time to DQS        | tDH                          | 0.35                   | -    | 0.35                   | -    | 0.35                   | -    | 0.40                   | -    | 0.40                   | -    | 0.45                   | -    | ns   |      |
| Clock half period                 | tHP                          | tCLmin<br>or<br>tCHmin | -    | tCLmin<br>or<br>tCHmin | -    | tCLmin<br>or<br>tCHmin | -    | tCLmin<br>or<br>tCHmin | -    | tCLmin<br>or<br>tCHmin | -    | tCLmin<br>or<br>tCHmin | -    | ns   | 1    |
| Data Hold skew factor             | tQHS                         | -                      | 0.4  | -                      | 0.4  | -                      | 0.4  | -                      | 0.45 | -                      | 0.45 | -                      | 0.5  | ns   |      |
| Data output hold time from DQS    | tQH                          | tHP-<br>tQHS           | -    | tHP-<br>tQHS           | -    | tHP-<br>tQHS           | -    | tHP-<br>tQHS           | -    | tHP-<br>tQHS           | -    | tHP-<br>tQHS           | -    | ns   | 1    |
| Jitter over 1~6 clock cycle error | t <sub>J</sub> <sup>*1</sup> | -                      | 75   | -                      | 75   | -                      | 85   | -                      | 95   | -                      | 100  | -                      | 105  | ps   |      |
| Cycle to cycle duty cycle error   | tDCERR                       | -                      | 75   | -                      | 75   | -                      | 85   | -                      | 95   | -                      | 100  | -                      | 105  | ps   |      |
| Rise and fall times of CK         | tR, tF                       | -                      | 600  | -                      | 600  | -                      | 700  | -                      | 700  | -                      | 700  | -                      | 700  | ps   |      |

\*1. The cycle to cycle jitter over 1~6 cycle short term jitter.

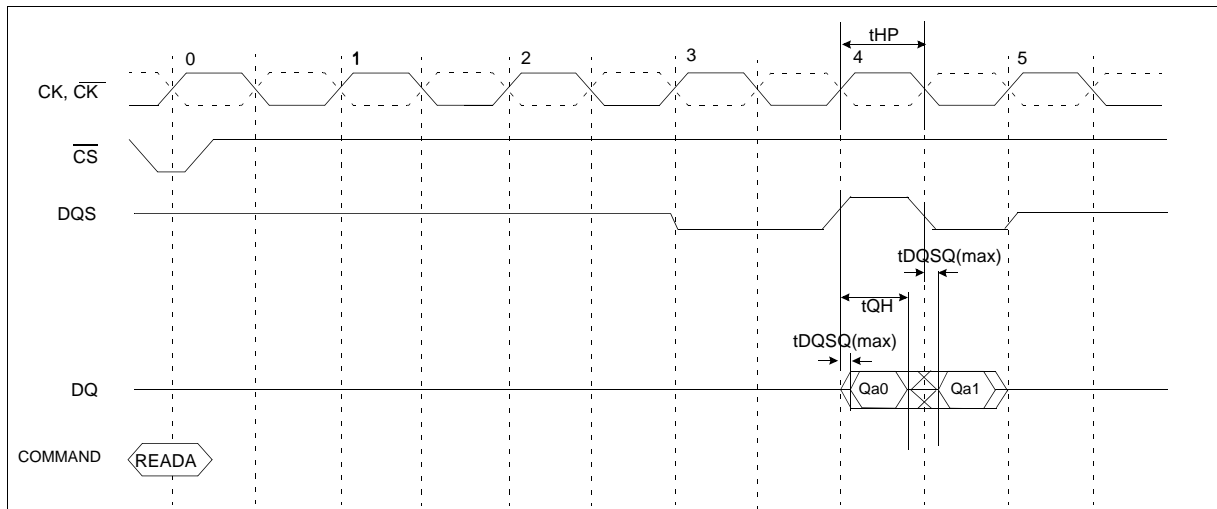
## Simplified Timing @ BL=2, CL=4



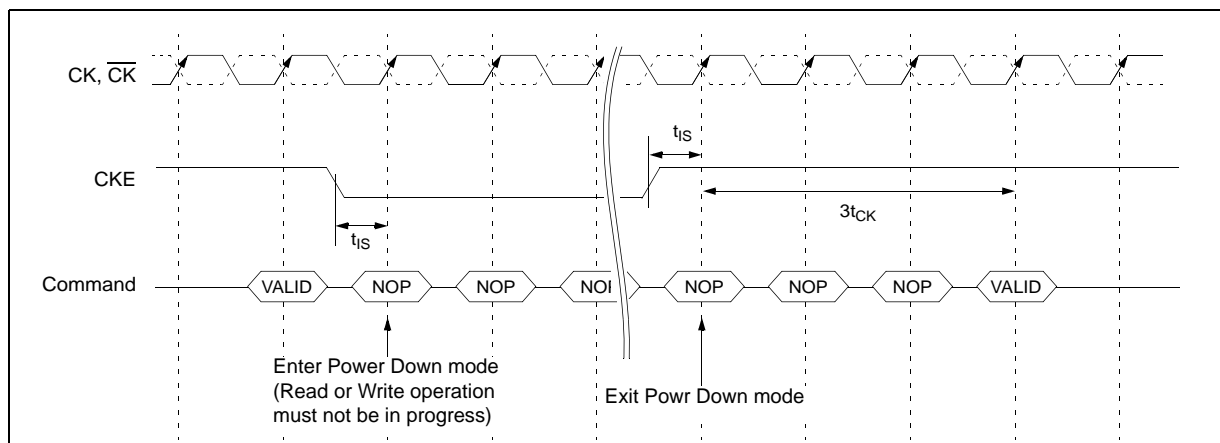
Note 1 :

- The JEDEC DDR specification currently defines the output data valid window( $t_{DV}$ ) as the time period when the data strobe and all data associated with that data strobe are coincidentally valid.
- The previously used definition of  $t_{DV}(=0.35t_{CK})$  artificially penalizes system timing budgets by assuming the worst case output valid window even then the clock duty cycle applied to the device is better than 45/55%
- A new AC timing term,  $t_{QH}$  which stands for data output hold time from DQS is defined to account for clock duty cycle variation and replaces  $t_{DV}$
- $t_{QHmin} = t_{HP}-X$  where
  - .  $t_{HP}$ =Minimum half clock period for any given cycle and is defined by clock high or clock low time( $t_{CH}, t_{CL}$ )
  - .  $X$ =A frequency dependent timing allowance account for  $t_{DQSQmax}$

**$t_{QH}$  Timing (CL4, BL2)**



**Power Down Timing**



## AC CHARACTERISTICS (I)

| Parameter                                       | Symbol             | -25          |      | -2A          |      | -33          |      | -36          |      | -40          |      | -45          |      | Unit | Note |
|---|--------------------|--------------|------|--------------|------|--------------|------|--------------|------|--------------|------|--------------|------|------|------|
|   |                    | Min          | Max  | Min          | Max  | Min          | Max  | Min          | Max  | Min          | Max  | Min          | Max  |      |      |
| Row cycle time                                  | t <sub>RC</sub>    | 17           | -    | 15           | -    | 13           | -    | 13           | -    | 13           | -    | 12           | -    | tCK  |      |
| Refresh row cycle time                          | t <sub>RFC</sub>   | 19           | -    | 17           | -    | 15           | -    | 15           | -    | 15           | -    | 14           | -    | tCK  |      |
| Row active time                                 | t <sub>RAS</sub>   | 12           | 100K | 10           | 100K | 9            | 100K | 9            | 100K | 9            | 100K | 8            | 100K | tCK  |      |
| RAS to CAS delay for Read                       | t <sub>RCDRD</sub> | 6            | -    | 5            | -    | 4            | -    | 4            | -    | 4            | -    | 4            | -    | tCK  |      |
| RAS to CAS delay for Write                      | t <sub>RCDWR</sub> | 4            | -    | 3            | -    | 2            | -    | 2            | -    | 2            | -    | 2            | -    | tCK  |      |
| Row precharge time                              | t <sub>RP</sub>    | 5            | -    | 5            | -    | 4            | -    | 4            | -    | 4            | -    | 4            | -    | tCK  |      |
| Row active to Row active                        | t <sub>RRD</sub>   | 4            | -    | 4            | -    | 3            | -    | 3            | -    | 3            | -    | 3            | -    | tCK  |      |
| Last data in to Row precharge @Normal Precharge | t <sub>WR</sub>    | 3            | -    | 3            | -    | 3            | -    | 3            | -    | 3            | -    | 3            | -    | tCK  | 1    |
| Last data in to Row precharge @Auto Precharge   | t <sub>WR_A</sub>  | 3            | -    | 3            | -    | 3            | -    | 3            | -    | 3            | -    | 3            | -    | tCK  | 1    |
| Last data in to Read command                    | t <sub>CDLR</sub>  | 2            | -    | 2            | -    | 2            | -    | 2            | -    | 2            | -    | 2            | -    | tCK  | 1    |
| Col. address to Col. address                    | t <sub>CCD</sub>   | 1            | -    | 1            | -    | 1            | -    | 1            | -    | 1            | -    | 1            | -    | tCK  |      |
| Mode register set cycle time                    | t <sub>MRD</sub>   | 2            | -    | 2            | -    | 2            | -    | 2            | -    | 2            | -    | 2            | -    | tCK  |      |
| Auto precharge write recovery + Pre-charge      | t <sub>DAL</sub>   | 8            | -    | 8            | -    | 7            | -    | 7            | -    | 7            | -    | 7            | -    | tCK  |      |
| Exit self refresh to read command               | t <sub>XSRL</sub>  | 200          | -    | 200          | -    | 200          | -    | 200          | -    | 200          | -    | 200          | -    | tCK  |      |
| Power down exit time                            | t <sub>PDEX</sub>  | 3tCK+<br>tIS | -    | 3tCK+<br>tIS | -    | 3tCK+<br>tIS | -    | 3tCK+<br>tIS | -    | 3tCK+<br>tIS | -    | 3tCK+<br>tIS | -    | ns   |      |
| Refresh interval time                           | t <sub>REF</sub>   | 7.8          | -    | 7.8          | -    | 7.8          | -    | 7.8          | -    | 7.8          | -    | 7.8          | -    | us   |      |

Note : 1. For normal write operation, even numbers of Din are to be written inside DRAM

(Unit : Number of Clock)

## AC CHARACTERISTICS (II)

## K4D263238E-GC25

| Frequency        | Cas Latency | t <sub>RC</sub> | t <sub>RFC</sub> | t <sub>RAS</sub> | t <sub>RCDRD</sub> | t <sub>RCDWR</sub> | t <sub>RP</sub> | t <sub>RRD</sub> | t <sub>DAL</sub> | Unit |
|------------------|-------------|-----------------|------------------|------------------|--------------------|--------------------|-----------------|------------------|------------------|------|
| 400MHz ( 2.5ns ) | 5           | 17              | 19               | 12               | 6                  | 4                  | 5               | 4                | 8                | tCK  |

## K4D263238E-GC2A

| Frequency         | Cas Latency | t <sub>RC</sub> | t <sub>RFC</sub> | t <sub>RAS</sub> | t <sub>RCDRD</sub> | t <sub>RCDWR</sub> | t <sub>RP</sub> | t <sub>RRD</sub> | t <sub>DAL</sub> | Unit |
|-------------------|-------------|-----------------|------------------|------------------|--------------------|--------------------|-----------------|------------------|------------------|------|
| 350MHz ( 2.86ns ) | 4           | 15              | 17               | 10               | 5                  | 3                  | 5               | 4                | 8                | tCK  |
| 300MHz ( 3.3ns )  | 4           | 13              | 15               | 9                | 4                  | 2                  | 4               | 3                | 7                | tCK  |
| 275MHz ( 3.6ns )  | 4           | 13              | 15               | 9                | 4                  | 2                  | 4               | 3                | 7                | tCK  |
| 250MHz ( 4.0ns )  | 4           | 13              | 15               | 9                | 4                  | 2                  | 4               | 3                | 7                | tCK  |
| 222MHz ( 4.5ns )  | 3           | 12              | 14               | 8                | 4                  | 2                  | 4               | 3                | 7                | tCK  |

## K4D263238E-GC33

| Frequency        | Cas Latency | t <sub>RC</sub> | t <sub>RFC</sub> | t <sub>RAS</sub> | t <sub>RCDRD</sub> | t <sub>RCDWR</sub> | t <sub>RP</sub> | t <sub>RRD</sub> | t <sub>DAL</sub> | Unit |
|------------------|-------------|-----------------|------------------|------------------|--------------------|--------------------|-----------------|------------------|------------------|------|
| 300MHz ( 3.3ns ) | 4           | 13              | 15               | 9                | 4                  | 2                  | 4               | 3                | 7                | tCK  |
| 275MHz ( 3.6ns ) | 4           | 13              | 15               | 9                | 4                  | 2                  | 4               | 3                | 7                | tCK  |
| 250MHz ( 4.0ns ) | 4           | 13              | 15               | 9                | 4                  | 2                  | 4               | 3                | 7                | tCK  |
| 222MHz ( 4.5ns ) | 3           | 12              | 14               | 8                | 4                  | 2                  | 4               | 3                | 7                | tCK  |

# K4D263238E-GC

# 128M GDDR SDRAM

## K4D263238E-GC36

| Frequency        | Cas Latency | tRC | tRFC | tRAS | tRCDRD | tRCDWR | tRP | tRRD | tDAL | Unit |
|------------------|-------------|-----|------|------|--------|--------|-----|------|------|------|
| 275MHz ( 3.6ns ) | 4           | 13  | 15   | 9    | 4      | 2      | 4   | 3    | 7    | tCK  |
| 250MHz ( 4.0ns ) | 4           | 13  | 15   | 9    | 4      | 2      | 4   | 3    | 7    | tCK  |
| 222MHz ( 4.5ns ) | 3           | 12  | 14   | 8    | 4      | 2      | 4   | 3    | 7    | tCK  |

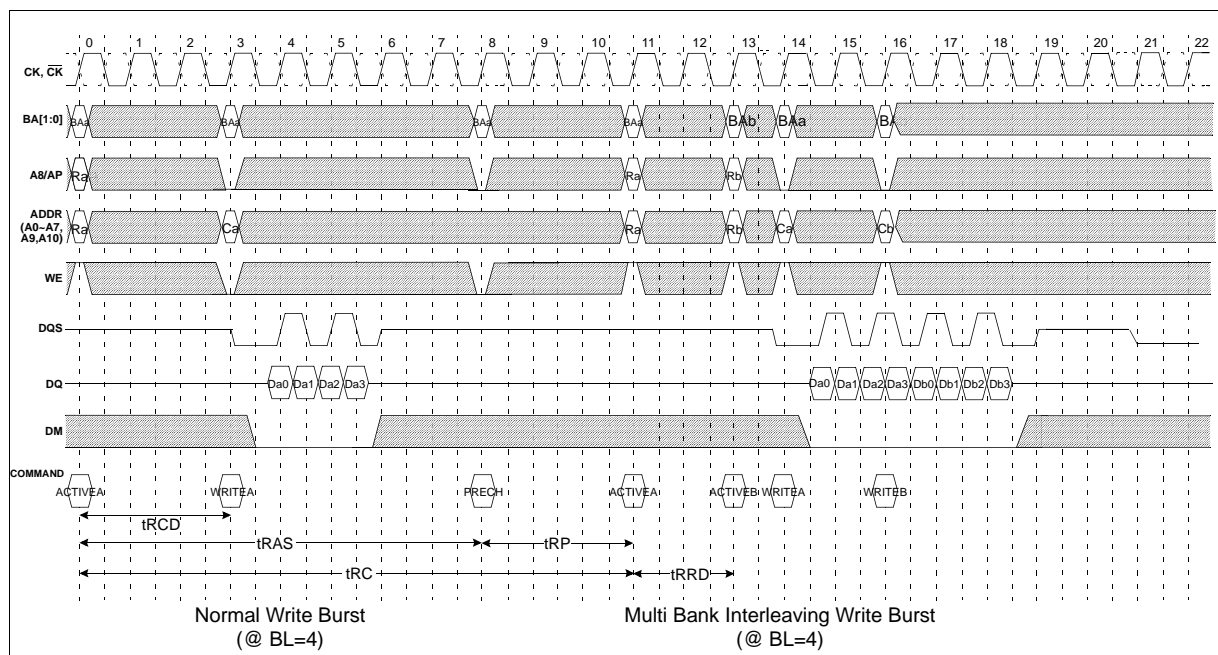
## K4D263238E-GC40

| Frequency        | Cas Latency | tRC | tRFC | tRAS | tRCDRD | tRCDWR | tRP | tRRD | tDAL | Unit |
|------------------|-------------|-----|------|------|--------|--------|-----|------|------|------|
| 250MHz ( 4.0ns ) | 4           | 13  | 15   | 9    | 4      | 2      | 4   | 3    | 7    | tCK  |
| 222MHz ( 4.5ns ) | 3           | 12  | 14   | 8    | 4      | 2      | 4   | 3    | 7    | tCK  |

## K4D263238E-GC45

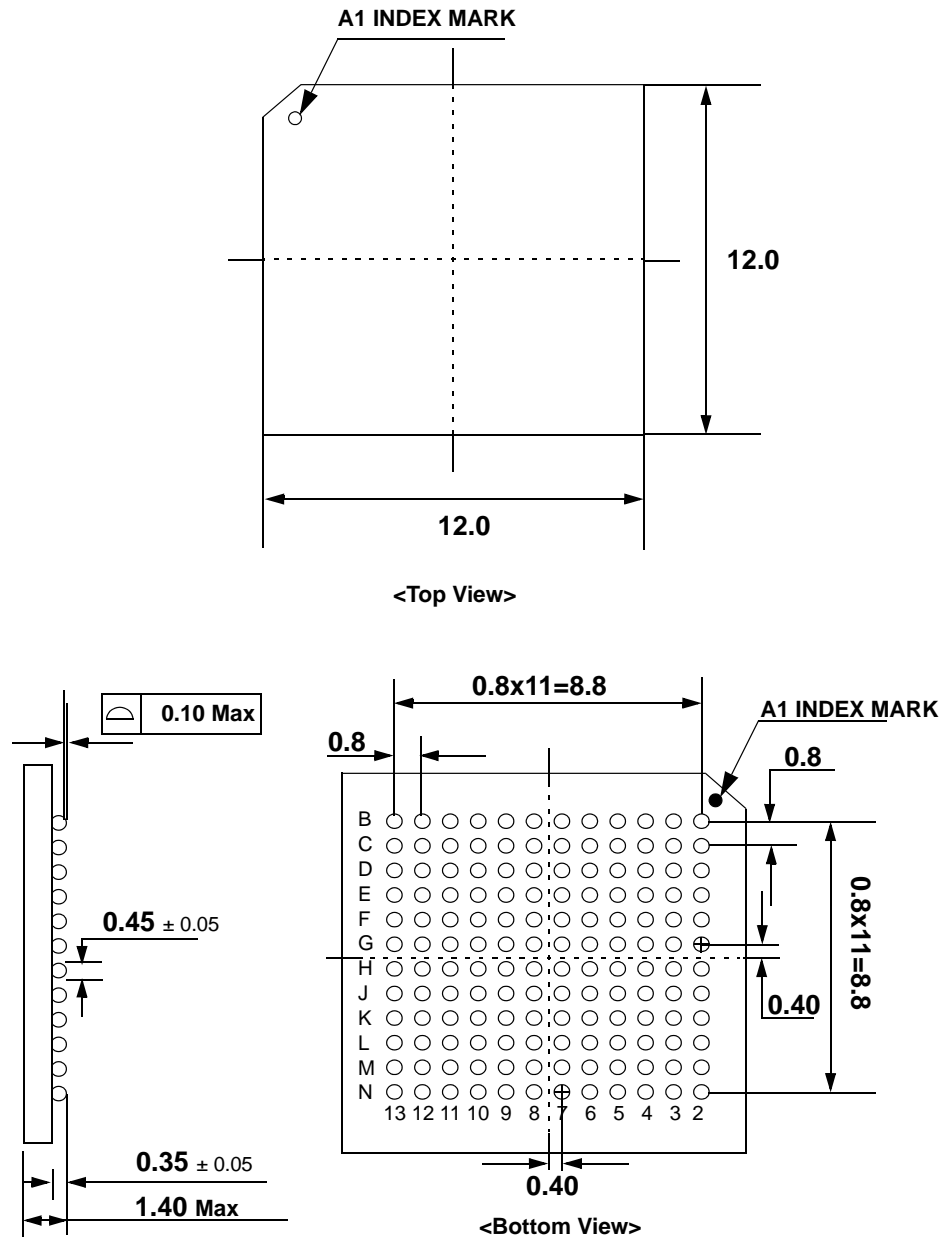
| Frequency        | Cas Latency | tRC | tRFC | tRAS | tRCDRD | tRCDWR | tRP | tRRD | tDAL | Unit |
|------------------|-------------|-----|------|------|--------|--------|-----|------|------|------|
| 222MHz ( 4.5ns ) | 3           | 12  | 14   | 8    | 4      | 2      | 4   | 3    | 7    | tCK  |

## Simplified Timing(2) @ BL=4





## PACKAGE DIMENSIONS (144-Ball FBGA)



Unit : mm