

LRS1830

Stacked Chip

256M (x16) Boot Block Flash and 32M (x16) SCRAM

(Model No.: LRS1830)

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SPECIFICATIONS

Product Type 128M (x16) Flash Memory +128M (x16) Flash Memory
32M (x16) Smartcombo RAM

LRS1830

Model No. (LRS1830)

*This specifications contains 73 pages including the cover and appendix.

*Refer to LH28F320BF, LH28F640BF, LH28F128BF Series Appendix (FUM00701).

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1. Description

The LRS1830 is a combination memory organized as 8,388,608 x16 bit flash memory, 8,388,608 x16 bit flash memory and 2,097,152 x16 bit Smartcombo RAM in one package.

Features

- Power supply • • • • 2.7V to 3.1V
- Operating temperature • • • • -30°C to +85°C
- Not designed or rated as radiation hardened
- 115 pin (LCSP115-P-0914) plastic package
- Flash memory has P-type bulk silicon, and Smartcombo RAM has P-type bulk silicon
- For specifications of Flash memory and Smartcombo RAM, refer to specification of each chip

Flash Memory 1 (F₁: 128M (x16) bit Flash Memory)

- Access Time (t_{AVQV}) • • • • 70 ns (Max.)
- Power supply current (The current for F₁-V_{CC} pin)
 - Read • • • • 30 mA (Max. t_{CYCLE} = 200ns, CMOS Input)
 - Word write • • • • 120 mA (Max.)
 - Block erase • • • • 60 mA (Max.)
 - Standby • • • • 40 μA (Max.)

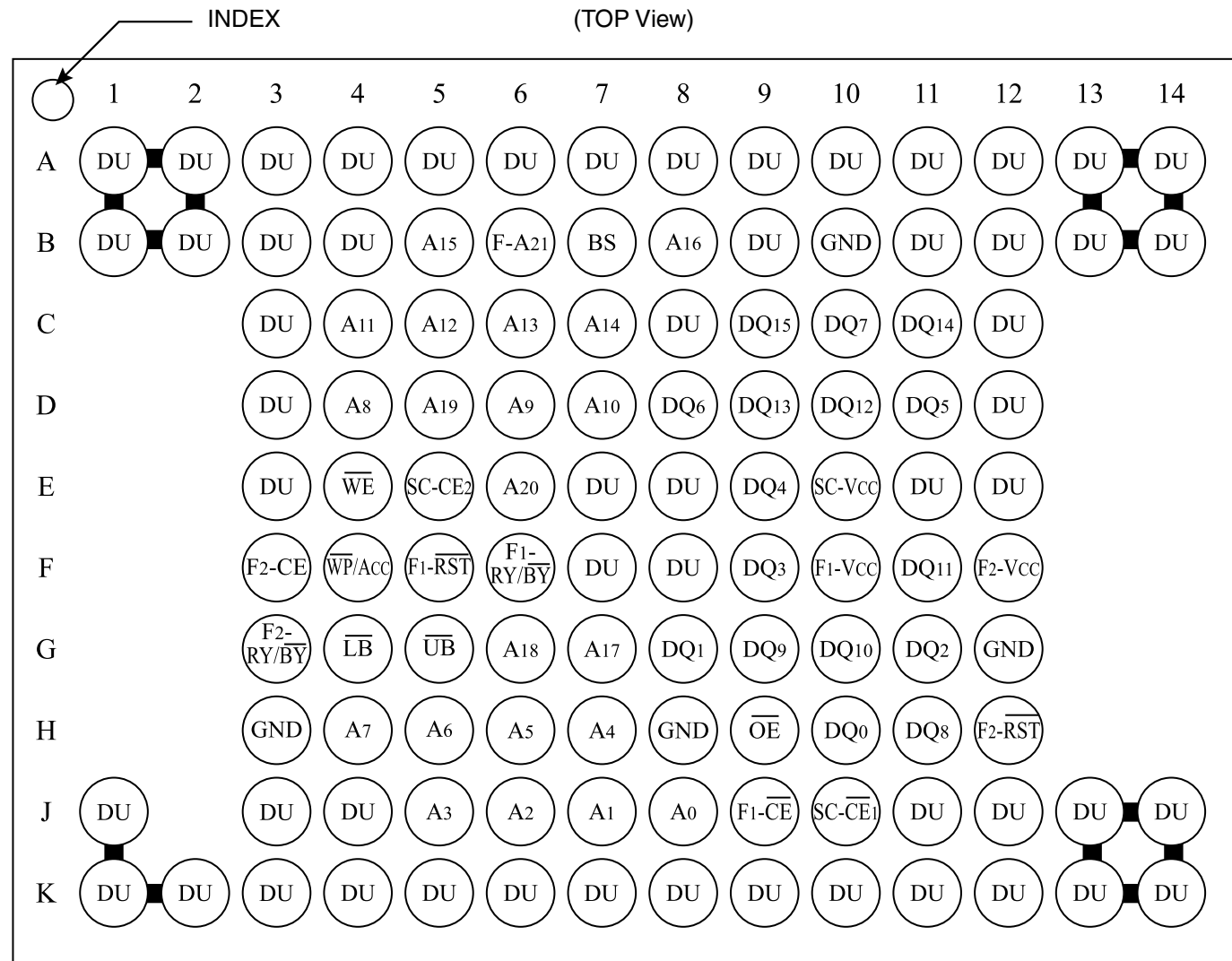
Flash Memory 2 (F₂: 128M (x16) bit Flash Memory)

- Access Time (t_{AVQV}) • • • • 70 ns (Max.)
- Power supply current (The current for F₂-V_{CC} pin)
 - Read • • • • 30 mA (Max. t_{CYCLE} = 200ns, CMOS Input)
 - Word write • • • • 120 mA (Max.)
 - Block erase • • • • 60 mA (Max.)
 - Standby • • • • 40 μA (Max. F₂- $\overline{\text{CE}}$ = F₂- $\overline{\text{RST}}$ = F₂-V_{CC} ± 0.2V)

Smartcombo RAM (32M (x16) bit Smartcombo RAM)

- Access Time (t_{AA}) • • • • 70 ns (Max.)
- Cycle time • • • • 70 ns (Min.)
- Power Supply current
 - Operating current • • • • 50 mA (Max. t_{RC}, t_{WC} = Min.)

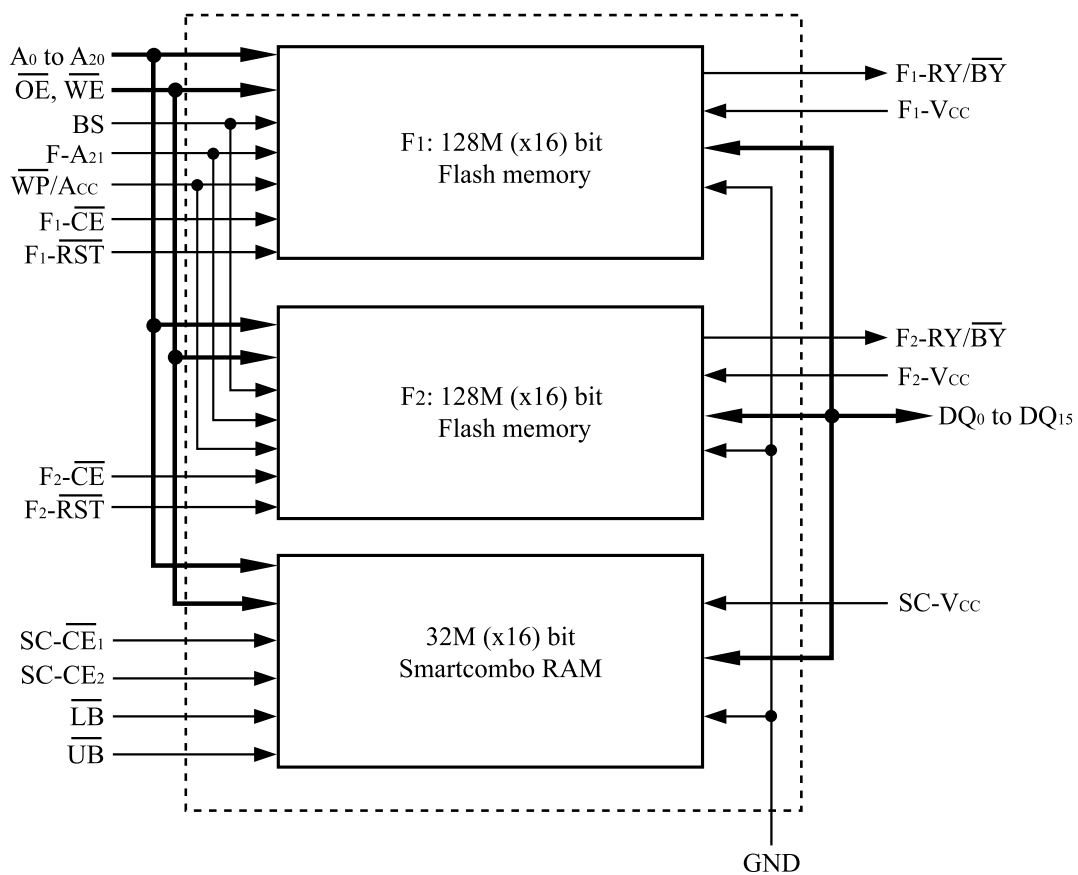
2. Pin Configuration



Note) Do not float any GND pins.

Pin	Description	Type
A ₀ to A ₂₀	Address Inputs (Common)	Input
F-A ₂₁	Address Input (Flash)	Input
BS (A ₂₂)	Bank Select (Flash) Bank 0 is selected by BS = "0". Bank 1 is selected by BS = "1". This pin can be used for A ₂₂ pin. Refer to AC Characteristics for timings.	Input
F ₁ - \overline{CE}	Chip Enable Input (Flash - F ₁ Selected)	Input
F ₂ - \overline{CE}	Chip Enable Input (Flash - F ₂ Selected)	Input
SC- \overline{CE} ₁	Chip Enable Input (Smartcombo RAM)	Input
SC-CE ₂	Sleep State Input (Smartcombo RAM) * See Chapter B-1	Input
\overline{WE}	Write Enable Input (Common)	Input
\overline{OE}	Output Enable Input (Common)	Input
\overline{LB}	Byte Enable Input : DQ ₀ to DQ ₇ (Smartcombo RAM)	Input
\overline{UB}	Byte Enable Input : DQ ₈ to DQ ₁₅ (Smartcombo RAM)	Input
F ₁ - \overline{RST}	Reset Power Down Input (Flash - F ₁ Selected) Block erase and Write : V _{IH} Read : V _{IH} Reset Power Down : V _{IL}	Input
F ₂ - \overline{RST}	Reset Power Down Input (Flash - F ₂ Selected) Block erase and Write : V _{IH} Read : V _{IH} Reset Power Down : V _{IL}	Input
\overline{WP}/A_{CC}	Write Protect Input (Flash) When \overline{WP}/A_{CC} is V _{IL} , locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and locked-down. When \overline{WP}/A_{CC} is V _{IH} , lock-down is disabled. Moreover, High Speed Erase and High Speed Program can be operated by applying 12V ±0.3V to \overline{WP}/A_{CC} . In this case, \overline{WP}/A_{CC} becomes the power supply pin.	Input / Power
F ₁ -RY/ \overline{BY}	Ready/Busy Output (Flash - F ₁ Selected) During an Erase or Write operation : V _{OL} Block Erase and Write Suspend : High-Z (High impedance)	Open Drain Output
F ₂ -RY/ \overline{BY}	Ready/Busy Output (Flash - F ₂ Selected) During an Erase or Write operation : V _{OL} Block Erase and Write Suspend : High-Z (High impedance)	Open Drain Output
DQ ₀ to DQ ₁₅	Data Inputs and Outputs (Common)	Input / Output
F ₁ -V _{CC}	Power Supply (Flash - F ₁ Selected)	Power
F ₂ -V _{CC}	Power Supply (Flash - F ₂ Selected)	Power
SC-V _{CC}	Power Supply (Smartcombo RAM)	Power
GND	GND (Common)	Power
DU	Don't Use	-

3. Block Diagram



Note: Only one among $F1-\overline{CE}$, $F2-\overline{CE}$ and $SC-\overline{CE}_1$ can be "low".
Two or more should not be "low".

4. Absolute Maximum Ratings

Symbol	Parameter	Notes	Ratings	Unit
V_{CC}	Supply Voltage	1	-0.2 to +3.6	V
V_{IN}	Input Voltage	1,2,3,4	-0.4 to $V_{CC} + 0.3$	V
T_A	Operating Temperature		-30 to +85	°C
T_{STG}	Storage Temperature		-55 to +125	°C
\overline{WP}/A_{CC}	\overline{WP}/A_{CC} Voltage	1,3,5	-0.2 to +12.6	V

Notes:

1. The maximum applicable voltage on any pins with respect to GND.
2. Except \overline{WP}/A_{CC} .
3. -1.0V undershoot is allowed when the pulse width is less than 5 nsec.
4. V_{IN} should not be over $V_{CC} + 0.3V$.
5. Applying $12V \pm 0.3V$ to \overline{WP}/A_{CC} during erase/write can only be done for a maximum of 1000 cycles on each block. \overline{WP}/A_{CC} may be connected to $12V \pm 0.3V$ for total of 80 hours maximum. +13.0V overshoot is allowed when the pulse width is less than 20 nsec.

5. Recommended DC Operating Conditions

 $(T_A = -30^\circ\text{C to } +85^\circ\text{C})$

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	2	2.7		3.1	V
\overline{WP}/A_{CC}	\overline{WP}/A_{CC} Voltage when Used as a Logic Control	V_{IL}	-0.4		0.4	V
		V_{IH}	2.4		$V_{CC} + 0.4^{(1)}$	V
	Supply Voltage		11.7	12	12.3	V
V_{IL}	Input Voltage		-0.4		0.4	V
V_{IH}	Input Voltage		2.4		$V_{CC} + 0.4^{(1)}$	V

Notes:

1. V_{CC} is the lower of F_1-V_{CC} , F_2-V_{CC} or $SC-V_{CC}$.
2. V_{CC} includes both F_1-V_{CC} , F_2-V_{CC} and $SC-V_{CC}$.

6. Flash Memory 1, 2

6.1 Truth Table

6.1.1 Bus Operation ⁽¹⁾

Flash	Notes	F- $\overline{\text{CE}}$	F- $\overline{\text{RST}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	DQ ₀ to DQ ₁₅
Read	3,5	L	H	L	H	(8)
Output Disable	5			H		High - Z
Write	2,3,4,5			L	D _{IN}	
Standby	5	H	H	X	X	High - Z
Reset Power Down	5,6	X	L			

Notes:

1. L = V_{IL}, H = V_{IH}, X = H or L, High-Z = High impedance. Refer to the DC Characteristics.
2. Command writes involving block erase, (page buffer) program are reliably executed when $\overline{\text{WP}}/\text{ACC} = V_{\text{ACCH1/2}}$ and V_{CC} = 2.7V to 3.1V.
Command writes involving bank erase is reliably executed when $\overline{\text{WP}}/\text{ACC} = V_{\text{ACCH1}}$ and V_{CC} = 2.7V to 3.1V.
Block erase, bank erase, (page buffer) program with $\overline{\text{WP}}/\text{ACC} < V_{\text{ACCH1/2}}$ (Min.) produce spurious results and should not be attempted.
3. Never hold $\overline{\text{OE}}$ low and $\overline{\text{WE}}$ low at the same timing.
4. Refer to Section 6.2 Command Definitions for Flash Memory valid D_{IN} during a write operation.
5. $\overline{\text{WP}}/\text{ACC}$ set to V_{IL} or V_{IH}.
6. Electricity consumption of Flash Memory is lowest when F- $\overline{\text{RST}} = \text{GND} \pm 0.2\text{V}$.
7. Never hold F₁- $\overline{\text{CE}}$ low and F₂- $\overline{\text{CE}}$ low at the same timing.
8. Flash Read Mode

Mode	Address	DQ ₀ to DQ ₁₅
Read Array	X	D _{OUT}
Read Identifier Codes	See 6.2.2	See 6.2.2
Read Query	Refer to the Appendix	Refer to the Appendix

6.1.2 Simultaneous Operation Modes Allowed with Four Planes ^(1, 2, 3, 4)

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:									
	Read Array	Read ID	Read Status	Read Query	Word Program	Page Buffer Program	Block Erase	Bank Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X	X		X	X
Read ID	X	X	X	X	X	X	X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X	X		X	X
Word Program	X	X	X	X						X
Page Buffer Program	X	X	X	X						X
Block Erase	X	X	X	X						
Bank Erase			X							
Program Suspend	X	X	X	X						X
Block Erase Suspend	X	X	X	X	X	X			X	

Notes:

1. "X" denotes the operation available.
2. Configurative Partition Dual Work Restrictions:
Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition.
Only one partition can be erased or programmed at a time - no command queuing.
Commands must be written to an address within the block targeted by that command.
3. This table shows operation which can be performed by only the selected chip, not during 2 chips of F₁ and F₂.
4. It is inhibited to execute the dual work operation between the memory area selected by BS="0" and the memory area selected by BS="1"

6.2 Command Definitions for Flash Memory ⁽¹¹⁾

6.2.1 Command Definitions

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper ⁽¹⁾	Address ⁽²⁾	Data	Oper ⁽¹⁾	Address ⁽²⁾	Data ⁽³⁾
Read Array	1		Write	PA	FFH			
Read Identifier Codes	≥ 2	4	Write	PA	90H	Read	IA	ID
Read Query	≥ 2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	PA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Bank Erase	2	5, 9	Write	X	30H	Write	X	D0H
Program	2	5, 6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5, 7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8, 9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	8, 9	Write	PA	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
Set Partition Configuration Register	2	12	Write	PCRC	60H	Write	PCRC	04H

Notes:

- Bus operations are defined in 6.1.1 Bus Operation.
- All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.
X=Any valid address within the device. Bank erase is executed to the bank selected by BS.
PA=Address within the selected partition.
IA=Identifier codes address (See 6.2.2 Identifier Codes for Read Operation).
QA=Query codes address. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.
BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
PCRC=Partition configuration register code presented on the address A₀-A₁₅.
- ID=Data read from identifier codes (See 6.2.2 Identifier Codes for Read Operation).
QD=Data read from query database. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.
SRD=Data read from status register. See 6.3 Register Definition for a description of the status register bits.
WD=Data to be programmed at location WA. Data is latched on the rising edge of \overline{WE} or \overline{CE} (whichever goes high first) during command write cycles.
N-1=N is the number of the words to be loaded into a page buffer.
- Following the Read Identifier Codes command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code (See 6.2.2 Identifier Codes for Read Operation).
The Read Query command is available for reading CFI (Common Flash Interface) information.
- Block erase, bank erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when F-RST is V_{IH}.
- Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
- Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H). Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.

8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Bank erase operation can not be suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when \overline{WP}/ACC is V_{IL} .
When \overline{WP}/ACC is V_{IH} , lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.
12. The partition setting for the memory area which consists of Plane0-Plane3 can be configured by writing the Set Partition Configuration Register command with BS="0".
The partition setting for the memory area which consists of Plane4-Plane7 can be configured by writing the Set Partition Configuration Register command with BS="1".

6.2.2 Identifier Codes for Read Operation

	Code	Address [A ₁₅ -A ₀]	Data [DQ ₁₅ -DQ ₀]	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	3
Device Code	Device Code	0001H	0008H	3
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	DQ ₀ = 0	1
	Block is Locked		DQ ₀ = 1	1
	Block is not Locked-Down		DQ ₁ = 0	1
	Block is Locked-Down		DQ ₁ = 1	1
Device Configuration Code	Partition Configuration Register	0006H	PCRC	2, 3

Notes:

1. Block Address = The beginning location of a block address within the partition to which the Read Identifier Codes command (90H) has been written.
DQ₁₅-DQ₂ is reserved for future implementation.
2. PCRC = Partition Configuration Register Code.
3. The address A₂₁-A₁₆ are shown in below table for reading the manufacturer, device, device configuration code.
The address to read the identifier codes is dependent on the partition which is selected when writing the Read Identifier Codes command (90H).
See Partition Configuration Register Definition (P.18) for the partition configuration register.

Identifier Codes for Read Operation on Partition Configuration (128M (x16)-bit device)

Partition Configuration Register			Address (128M (x16)-bit device)	
			BS="0" [A ₂₁ -A ₁₆]	BS="1" [A ₂₁ -A ₁₆]
PCR.10	PCR.9	PCR.8		
0	0	0	00H	00H
0	0	1	00H or 10H	00H or 10H
0	1	0	00H or 20H	00H or 20H
1	0	0	00H or 30H	00H or 30H
0	1	1	00H or 10H or 20H	00H or 10H or 20H
1	1	0	00H or 20H or 30H	00H or 20H or 30H
1	0	1	00H or 10H or 30H	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H	00H or 10H or 20H or 30H

6.2.3 Functions of Block Lock and Block Lock-Down

Current State					Erase/Program Allowed ⁽²⁾
State	\overline{WP}/A_{CC}	$DQ_1^{(1)}$	$DQ_0^{(1)}$	State Name	
[000]	0	0	0	Unlocked	Yes
[001] ⁽³⁾	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101] ⁽³⁾	1	0	1	Locked	No
[110] ⁽⁴⁾	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

Notes:

- $DQ_0 = 1$: a block is locked; $DQ_0 = 0$: a block is unlocked.
 $DQ_1 = 1$: a block is locked-down; $DQ_1 = 0$: a block is not locked-down.
- Erase and program are general terms, respectively, to express: block erase, bank erase and (page buffer) program operations.
- At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] ($\overline{WP}/A_{CC} = "0"$) or [101] ($\overline{WP}/A_{CC} = "1"$), regardless of the states before power-off or reset operation.
- When \overline{WP}/A_{CC} is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.

6.2.4 Block Locking State Transitions upon Command Write ⁽⁴⁾

Current State				Result after Lock Command Written (Next State)		
State	\overline{WP}/A_{CC}	DQ_1	DQ_0	Set Lock ⁽¹⁾	Clear Lock ⁽¹⁾	Set Lock-down ⁽¹⁾
[000]	0	0	0	[001]	No Change	[011] ⁽²⁾
[001]	0	0	1	No Change ⁽³⁾	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111] ⁽²⁾
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111] ⁽²⁾
[111]	1	1	1	No Change	[110]	No Change

Notes:

- “Set Lock” means Set Block Lock Bit command, “Clear Lock” means Clear Block Lock Bit command and “Set Lock-down” means Set Block Lock-Down Bit command.
- When the Set Block Lock-Down Bit command is written to the unlocked block ($DQ_0 = 0$), the corresponding block is locked-down and automatically locked at the same time.
- “No Change” means that the state remains unchanged after the command written.
- In this state transitions table, assumes that \overline{WP}/A_{CC} is not changed and fixed V_{IL} or V_{IH} .

6.2.5 Block Locking State Transitions upon \overline{WP}/A_{CC} Transition ⁽⁴⁾

Previous State	Current State				Result after \overline{WP}/A_{CC} Transition (Next State)	
	State	\overline{WP}/A_{CC}	DQ ₁	DQ ₀	$\overline{WP}/A_{CC} = 0 \rightarrow 1$ ⁽¹⁾	$\overline{WP}/A_{CC} = 1 \rightarrow 0$ ⁽¹⁾
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110] ⁽²⁾	[011]	0	1	1	[110]	-
Other than [110] ⁽²⁾					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011] ⁽³⁾
-	[111]	1	1	1	-	[011]

Notes:

1. " $\overline{WP}/A_{CC} = 0 \rightarrow 1$ " means that \overline{WP}/A_{CC} is driven to V_{IH} and " $\overline{WP}/A_{CC} = 1 \rightarrow 0$ " means that \overline{WP}/A_{CC} is driven to V_{IL} .
2. State transition from the current state [011] to the next state depends on the previous state.
3. When \overline{WP}/A_{CC} is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

6.3 Register Definition

Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPS	WPACCS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

<p>SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> <p>SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy</p> <p>SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed</p> <p>SR.5 = BLOCK ERASE AND BANK ERASE STATUS (BEFCES) 1 = Error in Block Erase or Bank Erase 0 = Successful Block Erase or Bank Erase</p> <p>SR.4 = (PAGE BUFFER) PROGRAM STATUS (PBPS) 1 = Error in (Page Buffer) Program 0 = Successful (Page Buffer) Program</p> <p>SR.3 = \overline{WP}/A_{CC} STATUS (WPACCS) 1 = $3.1V < \overline{WP}/ACC < 11.7V$ Detect, Operation Abort 0 = \overline{WP}/A_{CC} OK</p> <p>SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS) 1 = (Page Buffer) Program Suspended 0 = (Page Buffer) Program in Progress/Completed</p> <p>SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Erase or Program Attempted on a Locked Block, Operation Abort 0 = Unlocked</p> <p>SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p>	<p>Notes:</p> <p>Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.</p> <p>Check SR.7 or $F-RY/\overline{BY}$ to determine block erase, bank erase, (page buffer) program completion. SR.6 - SR.1 are invalid while SR.7 = "0".</p> <p>If both SR.5 and SR.4 are "1"s after a block erase, bank erase, (page buffer) program, set/clear block lock bit, set block lock-down bit or set partition configuration register attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of \overline{WP}/A_{CC} level. The WSM interrogates and indicates the \overline{WP}/A_{CC} level only after Block Erase, Bank Erase, (Page Buffer) Program command sequences. SR.3 is not guaranteed to report accurate feedback when $\overline{WP}/A_{CC} \neq V_{ACCH1/2}$.</p> <p>SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Bank Erase, (Page Buffer) Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock bit status.</p> <p>SR.15 - SR.8, SR.3 and SR.0 are reserved for future use and should be masked out when polling the status register.</p>
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Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

<p>XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> <p>XSR.7 = STATE MACHINE STATUS (SMS) 1 = Page Buffer Program available 0 = Page Buffer Program not available</p> <p>XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p>	<p>Notes:</p> <p>After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.</p> <p>XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.</p>
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Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2-0)

000 = No partitioning. Dual Work is not allowed.

001 = Plane1-3 are merged into one partition. (default in Bank 0 selected by BS="0")

010 = Plane 0-1 and Plane2-3 are merged into one partition respectively.

100 = Plane 0-2 are merged into one partition. (default in Bank 1 selected by BS="1")

011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:
After power-up or device reset, PCR10-8 (PC2-0) is set to "001" in Bank 0 and "100" in Bank 1.

See the table below for more details.

PCR.15-11 and PCR.7-0 are reserved for future use and should be masked out when checking the partition configuration register.

Partition Configuration

PC2 PC1 PC0	PARTITIONING FOR DUAL WORK	PC2 PC1 PC0	PARTITIONING FOR DUAL WORK
0 0 0	<p>PARTITION0</p>	0 1 1	<p>PARTITION2 PARTITION1 PARTITION0</p>
0 0 1	<p>PARTITION1 PARTITION0</p>	1 1 0	<p>PARTITION2 PARTITION1 PARTITION0</p>
0 1 0	<p>PARTITION1 PARTITION0</p>	1 0 1	<p>PARTITION2 PARTITION1 PARTITION0</p>
1 0 0	<p>PARTITION1 PARTITION0</p>	1 1 1	<p>PARTITION3 PARTITION2 PARTITION1 PARTITION0</p>

6.4 Memory Map for Flash Memory

6.4.1 Memory Map - F₁ Selected

Memory Area selected by BS="0"

Selected by BS="0" (Bank0)

BLOCK NUMBER	ADDRESS RANGE
134	32K-WORD 3F8000H - 3FFFFFFH
133	32K-WORD 3F0000H - 3F7FFFH
132	32K-WORD 3E8000H - 3E7FFFH
131	32K-WORD 3E0000H - 3E7FFFH
130	32K-WORD 3D8000H - 3D7FFFH
129	32K-WORD 3D0000H - 3D7FFFH
128	32K-WORD 3C8000H - 3C7FFFH
127	32K-WORD 3C0000H - 3C7FFFH
126	32K-WORD 3B8000H - 3B7FFFH
125	32K-WORD 3B0000H - 3B7FFFH
124	32K-WORD 3A8000H - 3A7FFFH
123	32K-WORD 3A0000H - 3A7FFFH
122	32K-WORD 398000H - 397FFFH
121	32K-WORD 390000H - 397FFFH
120	32K-WORD 388000H - 387FFFH
119	32K-WORD 380000H - 387FFFH
118	32K-WORD 378000H - 377FFFH
117	32K-WORD 370000H - 377FFFH
116	32K-WORD 368000H - 367FFFH
115	32K-WORD 360000H - 367FFFH
114	32K-WORD 358000H - 357FFFH
113	32K-WORD 350000H - 357FFFH
112	32K-WORD 348000H - 347FFFH
111	32K-WORD 340000H - 347FFFH
110	32K-WORD 338000H - 337FFFH
109	32K-WORD 330000H - 337FFFH
108	32K-WORD 328000H - 327FFFH
107	32K-WORD 320000H - 327FFFH
106	32K-WORD 318000H - 317FFFH
105	32K-WORD 310000H - 317FFFH
104	32K-WORD 308000H - 307FFFH
103	32K-WORD 300000H - 307FFFH

BLOCK NUMBER	ADDRESS RANGE
102	32K-WORD 2F8000H - 2FFFFFFH
101	32K-WORD 2F0000H - 2F7FFFH
100	32K-WORD 2E8000H - 2E7FFFH
99	32K-WORD 2E0000H - 2E7FFFH
98	32K-WORD 2D8000H - 2D7FFFH
97	32K-WORD 2D0000H - 2D7FFFH
96	32K-WORD 2C8000H - 2C7FFFH
95	32K-WORD 2C0000H - 2C7FFFH
94	32K-WORD 2B8000H - 2B7FFFH
93	32K-WORD 2B0000H - 2B7FFFH
92	32K-WORD 2A8000H - 2A7FFFH
91	32K-WORD 2A0000H - 2A7FFFH
90	32K-WORD 298000H - 297FFFH
89	32K-WORD 290000H - 297FFFH
88	32K-WORD 288000H - 287FFFH
87	32K-WORD 280000H - 287FFFH
86	32K-WORD 278000H - 277FFFH
85	32K-WORD 270000H - 277FFFH
84	32K-WORD 268000H - 267FFFH
83	32K-WORD 260000H - 267FFFH
82	32K-WORD 258000H - 257FFFH
81	32K-WORD 250000H - 257FFFH
80	32K-WORD 248000H - 247FFFH
79	32K-WORD 240000H - 247FFFH
78	32K-WORD 238000H - 237FFFH
77	32K-WORD 230000H - 237FFFH
76	32K-WORD 228000H - 227FFFH
75	32K-WORD 220000H - 227FFFH
74	32K-WORD 218000H - 217FFFH
73	32K-WORD 210000H - 217FFFH
72	32K-WORD 208000H - 207FFFH
71	32K-WORD 200000H - 207FFFH

BLOCK NUMBER ADDRESS RANGE

BLOCK NUMBER	ADDRESS RANGE
70	32K-WORD 1F8000H - 1FFFFFFH
69	32K-WORD 1F0000H - 1F7FFFH
68	32K-WORD 1E8000H - 1E7FFFH
67	32K-WORD 1E0000H - 1E7FFFH
66	32K-WORD 1D8000H - 1D7FFFH
65	32K-WORD 1D0000H - 1D7FFFH
64	32K-WORD 1C8000H - 1C7FFFH
63	32K-WORD 1C0000H - 1C7FFFH
62	32K-WORD 1B8000H - 1B7FFFH
61	32K-WORD 1B0000H - 1B7FFFH
60	32K-WORD 1A8000H - 1A7FFFH
59	32K-WORD 1A0000H - 1A7FFFH
58	32K-WORD 198000H - 197FFFH
57	32K-WORD 190000H - 197FFFH
56	32K-WORD 188000H - 187FFFH
55	32K-WORD 180000H - 187FFFH
54	32K-WORD 178000H - 177FFFH
53	32K-WORD 170000H - 177FFFH
52	32K-WORD 168000H - 167FFFH
51	32K-WORD 160000H - 167FFFH
50	32K-WORD 158000H - 157FFFH
49	32K-WORD 150000H - 157FFFH
48	32K-WORD 148000H - 147FFFH
47	32K-WORD 140000H - 147FFFH
46	32K-WORD 138000H - 137FFFH
45	32K-WORD 130000H - 137FFFH
44	32K-WORD 128000H - 127FFFH
43	32K-WORD 120000H - 127FFFH
42	32K-WORD 118000H - 117FFFH
41	32K-WORD 110000H - 117FFFH
40	32K-WORD 108000H - 107FFFH
39	32K-WORD 100000H - 107FFFH

BLOCK NUMBER	ADDRESS RANGE
38	32K-WORD 0F8000H - 0FFFFFFH
37	32K-WORD 0F0000H - 0F7FFFH
36	32K-WORD 0E8000H - 0E7FFFH
35	32K-WORD 0E0000H - 0E7FFFH
34	32K-WORD 0D8000H - 0D7FFFH
33	32K-WORD 0D0000H - 0D7FFFH
32	32K-WORD 0C8000H - 0C7FFFH
31	32K-WORD 0C0000H - 0C7FFFH
30	32K-WORD 0B8000H - 0B7FFFH
29	32K-WORD 0B0000H - 0B7FFFH
28	32K-WORD 0A8000H - 0A7FFFH
27	32K-WORD 0A0000H - 0A7FFFH
26	32K-WORD 098000H - 097FFFH
25	32K-WORD 090000H - 097FFFH
24	32K-WORD 088000H - 087FFFH
23	32K-WORD 080000H - 087FFFH
22	32K-WORD 078000H - 077FFFH
21	32K-WORD 070000H - 077FFFH
20	32K-WORD 068000H - 067FFFH
19	32K-WORD 060000H - 067FFFH
18	32K-WORD 058000H - 057FFFH
17	32K-WORD 050000H - 057FFFH
16	32K-WORD 048000H - 047FFFH
15	32K-WORD 040000H - 047FFFH
14	32K-WORD 038000H - 037FFFH
13	32K-WORD 030000H - 037FFFH
12	32K-WORD 028000H - 027FFFH
11	32K-WORD 020000H - 027FFFH
10	32K-WORD 018000H - 017FFFH
9	32K-WORD 010000H - 017FFFH
8	32K-WORD 008000H - 007FFFH
7	4K-WORD 007000H - 007FFFH
6	4K-WORD 006000H - 006FFFH
5	4K-WORD 005000H - 005FFFH
4	4K-WORD 004000H - 004FFFH
3	4K-WORD 003000H - 003FFFH
2	4K-WORD 002000H - 002FFFH
1	4K-WORD 001000H - 001FFFH
0	4K-WORD 000000H - 000FFFH

Memory Area selected by BS="1"

		BLOCK NUMBER	ADDRESS RANGE		
PLANE3 (PARAMETER PLANE)	134	4K-WORD	3FF000H - 3FFFFFFH	Selected by BS="1" (Bank1)	
	133	4K-WORD	3FE000H - 3FEFFFFH		
	132	4K-WORD	3FD000H - 3FDFFFFH		
	131	4K-WORD	3FC000H - 3FCFFFFH		
	130	4K-WORD	3FB000H - 3FBFFFFH		
	129	4K-WORD	3FA000H - 3FAFFFFH		
	128	4K-WORD	3F9000H - 3F9FFFFH		
	127	4K-WORD	3F8000H - 3F8FFFFH		
	126	32K-WORD	3F0000H - 3F7FFFFH		
	125	32K-WORD	3E8000H - 3EFFFFH		
	124	32K-WORD	3E0000H - 3E7FFFFH		
	123	32K-WORD	3D8000H - 3DFFFFH		
	122	32K-WORD	3D0000H - 3D7FFFFH		
	121	32K-WORD	3C8000H - 3CFFFFH		
	120	32K-WORD	3C0000H - 3C7FFFFH		
	119	32K-WORD	3B8000H - 3BFFFFH		
	118	32K-WORD	3B0000H - 3B7FFFFH		
	117	32K-WORD	3A8000H - 3AFFFFH		
	116	32K-WORD	3A0000H - 3A7FFFFH		
	115	32K-WORD	398000H - 39FFFFH		
	114	32K-WORD	390000H - 397FFFFH		
	113	32K-WORD	388000H - 38FFFFH		
	112	32K-WORD	380000H - 387FFFFH		
	111	32K-WORD	378000H - 37FFFFH		
	110	32K-WORD	370000H - 377FFFFH		
	109	32K-WORD	368000H - 36FFFFH		
	108	32K-WORD	360000H - 367FFFFH		
	107	32K-WORD	358000H - 35FFFFH		
	106	32K-WORD	350000H - 357FFFFH		
	105	32K-WORD	348000H - 34FFFFH		
	104	32K-WORD	340000H - 347FFFFH		
	103	32K-WORD	338000H - 33FFFFH		
	102	32K-WORD	330000H - 337FFFFH		
101	32K-WORD	328000H - 32FFFFH			
100	32K-WORD	320000H - 327FFFFH			
99	32K-WORD	318000H - 31FFFFH			
98	32K-WORD	310000H - 317FFFFH			
97	32K-WORD	308000H - 30FFFFH			
96	32K-WORD	300000H - 307FFFFH			
PLANE1 (UNIFORM PLANE)	63	32K-WORD	1F8000H - 1FFFFFFH	Selected by BS="1" (Bank1)	
	62	32K-WORD	1F0000H - 1F7FFFFH		
	61	32K-WORD	1E8000H - 1EFFFFH		
	60	32K-WORD	1E0000H - 1E7FFFFH		
	59	32K-WORD	1D8000H - 1DFFFFH		
	58	32K-WORD	1D0000H - 1D7FFFFH		
	57	32K-WORD	1C8000H - 1CFFFFH		
	56	32K-WORD	1C0000H - 1C7FFFFH		
	55	32K-WORD	1B8000H - 1BFFFFH		
	54	32K-WORD	1B0000H - 1B7FFFFH		
	53	32K-WORD	1A8000H - 1AFFFFH		
	52	32K-WORD	1A0000H - 1A7FFFFH		
	51	32K-WORD	198000H - 19FFFFH		
	50	32K-WORD	190000H - 197FFFFH		
	49	32K-WORD	188000H - 18FFFFH		
	48	32K-WORD	180000H - 187FFFFH		
	47	32K-WORD	178000H - 17FFFFH		
	46	32K-WORD	170000H - 177FFFFH		
	45	32K-WORD	168000H - 16FFFFH		
	44	32K-WORD	160000H - 167FFFFH		
	43	32K-WORD	158000H - 15FFFFH		
	42	32K-WORD	150000H - 157FFFFH		
	41	32K-WORD	148000H - 14FFFFH		
	40	32K-WORD	140000H - 147FFFFH		
	39	32K-WORD	138000H - 13FFFFH		
	38	32K-WORD	130000H - 137FFFFH		
	37	32K-WORD	128000H - 12FFFFH		
	36	32K-WORD	120000H - 127FFFFH		
	35	32K-WORD	118000H - 11FFFFH		
	34	32K-WORD	110000H - 117FFFFH		
	33	32K-WORD	108000H - 10FFFFH		
	32	32K-WORD	100000H - 107FFFFH		
	PLANE2 (UNIFORM PLANE)	95	32K-WORD		
94		32K-WORD	2F0000H - 2F7FFFFH		
93		32K-WORD	2E8000H - 2EFFFFH		
92		32K-WORD	2E0000H - 2E7FFFFH		
91		32K-WORD	2D8000H - 2DFFFFH		
90		32K-WORD	2D0000H - 2D7FFFFH		
89		32K-WORD	2C8000H - 2CFFFFH		
88		32K-WORD	2C0000H - 2C7FFFFH		
87		32K-WORD	2B8000H - 2BFFFFH		
86		32K-WORD	2B0000H - 2B7FFFFH		
85		32K-WORD	2A8000H - 2AFFFFH		
84		32K-WORD	2A0000H - 2A7FFFFH		
83		32K-WORD	298000H - 29FFFFH		
82		32K-WORD	290000H - 297FFFFH		
81		32K-WORD	288000H - 28FFFFH		
80		32K-WORD	280000H - 287FFFFH		
79		32K-WORD	278000H - 27FFFFH		
78		32K-WORD	270000H - 277FFFFH		
77		32K-WORD	268000H - 26FFFFH		
76		32K-WORD	260000H - 267FFFFH		
75		32K-WORD	258000H - 25FFFFH		
74		32K-WORD	250000H - 257FFFFH		
73		32K-WORD	248000H - 24FFFFH		
72		32K-WORD	240000H - 247FFFFH		
71		32K-WORD	238000H - 23FFFFH		
70		32K-WORD	230000H - 237FFFFH		
69		32K-WORD	228000H - 22FFFFH		
68		32K-WORD	220000H - 227FFFFH		
67		32K-WORD	218000H - 21FFFFH		
66		32K-WORD	210000H - 217FFFFH		
65		32K-WORD	208000H - 20FFFFH		
64		32K-WORD	200000H - 207FFFFH		
PLANE0 (UNIFORM PLANE)		31	32K-WORD	0F8000H - 0FFFFFFH	Selected by BS="1" (Bank1)
	30	32K-WORD	0F0000H - 0F7FFFFH		
	29	32K-WORD	0E8000H - 0EFFFFH		
	28	32K-WORD	0E0000H - 0E7FFFFH		
	27	32K-WORD	0D8000H - 0DFFFFH		
	26	32K-WORD	0D0000H - 0D7FFFFH		
	25	32K-WORD	0C8000H - 0CFFFFH		
	24	32K-WORD	0C0000H - 0C7FFFFH		
	23	32K-WORD	0B8000H - 0BFFFFH		
	22	32K-WORD	0B0000H - 0B7FFFFH		
	21	32K-WORD	0A8000H - 0AFFFFH		
	20	32K-WORD	0A0000H - 0A7FFFFH		
	19	32K-WORD	098000H - 09FFFFH		
	18	32K-WORD	090000H - 097FFFFH		
	17	32K-WORD	088000H - 08FFFFH		
	16	32K-WORD	080000H - 087FFFFH		
	15	32K-WORD	078000H - 07FFFFH		
	14	32K-WORD	070000H - 077FFFFH		
	13	32K-WORD	068000H - 06FFFFH		
	12	32K-WORD	060000H - 067FFFFH		
	11	32K-WORD	058000H - 05FFFFH		
	10	32K-WORD	050000H - 057FFFFH		
	9	32K-WORD	048000H - 04FFFFH		
	8	32K-WORD	040000H - 047FFFFH		
	7	32K-WORD	038000H - 03FFFFH		
	6	32K-WORD	030000H - 037FFFFH		
	5	32K-WORD	028000H - 02FFFFH		
	4	32K-WORD	020000H - 027FFFFH		
	3	32K-WORD	018000H - 01FFFFH		
	2	32K-WORD	010000H - 017FFFFH		
	1	32K-WORD	008000H - 00FFFFH		
	0	32K-WORD	000000H - 007FFFFH		

6.4.2 Memory Map - F₂ Selected

Memory Area selected by BS="0"

Selected by BS="0" (Bank0)

BLOCK NUMBER	ADDRESS RANGE
134 32K-WORD	3F8000H - 3FFFFFFH
133 32K-WORD	3F0000H - 3F7FFFH
132 32K-WORD	3E8000H - 3E7FFFH
131 32K-WORD	3E0000H - 3E7FFFH
130 32K-WORD	3D8000H - 3DFFFFH
129 32K-WORD	3D0000H - 3D7FFFH
128 32K-WORD	3C8000H - 3CFFFFH
127 32K-WORD	3C0000H - 3C7FFFH
126 32K-WORD	3B8000H - 3BFFFFH
125 32K-WORD	3B0000H - 3B7FFFH
124 32K-WORD	3A8000H - 3AFFFFH
123 32K-WORD	3A0000H - 3A7FFFH
122 32K-WORD	398000H - 39FFFFH
121 32K-WORD	390000H - 397FFFH
120 32K-WORD	388000H - 38FFFFH
119 32K-WORD	380000H - 387FFFH
118 32K-WORD	378000H - 37FFFFH
117 32K-WORD	370000H - 377FFFH
116 32K-WORD	368000H - 36FFFFH
115 32K-WORD	360000H - 367FFFH
114 32K-WORD	358000H - 35FFFFH
113 32K-WORD	350000H - 357FFFH
112 32K-WORD	348000H - 34FFFFH
111 32K-WORD	340000H - 347FFFH
110 32K-WORD	338000H - 33FFFFH
109 32K-WORD	330000H - 337FFFH
108 32K-WORD	328000H - 32FFFFH
107 32K-WORD	320000H - 327FFFH
106 32K-WORD	318000H - 31FFFFH
105 32K-WORD	310000H - 317FFFH
104 32K-WORD	308000H - 30FFFFH
103 32K-WORD	300000H - 307FFFH

BLOCK NUMBER	ADDRESS RANGE
102 32K-WORD	2F8000H - 2FFFFFFH
101 32K-WORD	2F0000H - 2F7FFFH
100 32K-WORD	2E8000H - 2EFFFFH
99 32K-WORD	2E0000H - 2E7FFFH
98 32K-WORD	2D8000H - 2DFFFFH
97 32K-WORD	2D0000H - 2D7FFFH
96 32K-WORD	2C8000H - 2CFFFFH
95 32K-WORD	2C0000H - 2C7FFFH
94 32K-WORD	2B8000H - 2BFFFFH
93 32K-WORD	2B0000H - 2B7FFFH
92 32K-WORD	2A8000H - 2AFFFFH
91 32K-WORD	2A0000H - 2A7FFFH
90 32K-WORD	298000H - 29FFFFH
89 32K-WORD	290000H - 297FFFH
88 32K-WORD	288000H - 28FFFFH
87 32K-WORD	280000H - 287FFFH
86 32K-WORD	278000H - 27FFFFH
85 32K-WORD	270000H - 277FFFH
84 32K-WORD	268000H - 26FFFFH
83 32K-WORD	260000H - 267FFFH
82 32K-WORD	258000H - 25FFFFH
81 32K-WORD	250000H - 257FFFH
80 32K-WORD	248000H - 24FFFFH
79 32K-WORD	240000H - 247FFFH
78 32K-WORD	238000H - 23FFFFH
77 32K-WORD	230000H - 237FFFH
76 32K-WORD	228000H - 22FFFFH
75 32K-WORD	220000H - 227FFFH
74 32K-WORD	218000H - 21FFFFH
73 32K-WORD	210000H - 217FFFH
72 32K-WORD	208000H - 20FFFFH
71 32K-WORD	200000H - 207FFFH

BLOCK NUMBER	ADDRESS RANGE
70 32K-WORD	1F8000H - 1FFFFFFH
69 32K-WORD	1F0000H - 1F7FFFH
68 32K-WORD	1E8000H - 1EFFFFH
67 32K-WORD	1E0000H - 1E7FFFH
66 32K-WORD	1D8000H - 1DFFFFH
65 32K-WORD	1D0000H - 1D7FFFH
64 32K-WORD	1C8000H - 1CFFFFH
63 32K-WORD	1C0000H - 1C7FFFH
62 32K-WORD	1B8000H - 1BFFFFH
61 32K-WORD	1B0000H - 1B7FFFH
60 32K-WORD	1A8000H - 1AFFFFH
59 32K-WORD	1A0000H - 1A7FFFH
58 32K-WORD	198000H - 19FFFFH
57 32K-WORD	190000H - 197FFFH
56 32K-WORD	188000H - 18FFFFH
55 32K-WORD	180000H - 187FFFH
54 32K-WORD	178000H - 17FFFFH
53 32K-WORD	170000H - 177FFFH
52 32K-WORD	168000H - 16FFFFH
51 32K-WORD	160000H - 167FFFH
50 32K-WORD	158000H - 15FFFFH
49 32K-WORD	150000H - 157FFFH
48 32K-WORD	148000H - 14FFFFH
47 32K-WORD	140000H - 147FFFH
46 32K-WORD	138000H - 13FFFFH
45 32K-WORD	130000H - 137FFFH
44 32K-WORD	128000H - 12FFFFH
43 32K-WORD	120000H - 127FFFH
42 32K-WORD	118000H - 11FFFFH
41 32K-WORD	110000H - 117FFFH
40 32K-WORD	108000H - 10FFFFH
39 32K-WORD	100000H - 107FFFH

BLOCK NUMBER	ADDRESS RANGE
38 32K-WORD	0F8000H - 0FFFFFFH
37 32K-WORD	0F0000H - 0F7FFFH
36 32K-WORD	0E8000H - 0EFFFFH
35 32K-WORD	0E0000H - 0E7FFFH
34 32K-WORD	0D8000H - 0DFFFFH
33 32K-WORD	0D0000H - 0D7FFFH
32 32K-WORD	0C8000H - 0CFFFFH
31 32K-WORD	0C0000H - 0C7FFFH
30 32K-WORD	0B8000H - 0BFFFFH
29 32K-WORD	0B0000H - 0B7FFFH
28 32K-WORD	0A8000H - 0AFFFFH
27 32K-WORD	0A0000H - 0A7FFFH
26 32K-WORD	098000H - 09FFFFH
25 32K-WORD	090000H - 097FFFH
24 32K-WORD	088000H - 08FFFFH
23 32K-WORD	080000H - 087FFFH
22 32K-WORD	078000H - 07FFFFH
21 32K-WORD	070000H - 077FFFH
20 32K-WORD	068000H - 06FFFFH
19 32K-WORD	060000H - 067FFFH
18 32K-WORD	058000H - 05FFFFH
17 32K-WORD	050000H - 057FFFH
16 32K-WORD	048000H - 04FFFFH
15 32K-WORD	040000H - 047FFFH
14 32K-WORD	038000H - 03FFFFH
13 32K-WORD	030000H - 037FFFH
12 32K-WORD	028000H - 02FFFFH
11 32K-WORD	020000H - 027FFFH
10 32K-WORD	018000H - 01FFFFH
9 32K-WORD	010000H - 017FFFH
8 32K-WORD	008000H - 00FFFFH
7 4K-WORD	007000H - 007FFFH
6 4K-WORD	006000H - 006FFFH
5 4K-WORD	005000H - 005FFFH
4 4K-WORD	004000H - 004FFFH
3 4K-WORD	003000H - 003FFFH
2 4K-WORD	002000H - 002FFFH
1 4K-WORD	001000H - 001FFFH
0 4K-WORD	000000H - 000FFFH

Memory Area selected by BS="1"

		BLOCK NUMBER	ADDRESS RANGE		
PLANE3 (PARAMETER PLANE)	134	4K-WORD	3FF000H - 3FFFFFFH	Selected by BS="1" (Bank1)	
	133	4K-WORD	3FE000H - 3FEFFFFH		
	132	4K-WORD	3FD000H - 3FDFFFFH		
	131	4K-WORD	3FC000H - 3FCFFFFH		
	130	4K-WORD	3FB000H - 3FBFFFFH		
	129	4K-WORD	3FA000H - 3FAFFFFH		
	128	4K-WORD	3F9000H - 3F9FFFFH		
	127	4K-WORD	3F8000H - 3F8FFFFH		
	126	32K-WORD	3F0000H - 3F7FFFFH		
	125	32K-WORD	3E8000H - 3EFFFFH		
	124	32K-WORD	3E0000H - 3E7FFFFH		
	123	32K-WORD	3D8000H - 3DFFFFH		
	122	32K-WORD	3D0000H - 3D7FFFFH		
	121	32K-WORD	3C8000H - 3CFFFFH		
	120	32K-WORD	3C0000H - 3C7FFFFH		
	119	32K-WORD	3B8000H - 3BFFFFH		
	118	32K-WORD	3B0000H - 3B7FFFFH		
	117	32K-WORD	3A8000H - 3AFFFFH		
	116	32K-WORD	3A0000H - 3A7FFFFH		
	115	32K-WORD	398000H - 39FFFFH		
	114	32K-WORD	390000H - 397FFFFH		
	113	32K-WORD	388000H - 38FFFFH		
	112	32K-WORD	380000H - 387FFFFH		
	111	32K-WORD	378000H - 37FFFFH		
	110	32K-WORD	370000H - 377FFFFH		
	109	32K-WORD	368000H - 36FFFFH		
	108	32K-WORD	360000H - 367FFFFH		
	107	32K-WORD	358000H - 35FFFFH		
	106	32K-WORD	350000H - 357FFFFH		
	105	32K-WORD	348000H - 34FFFFH		
	104	32K-WORD	340000H - 347FFFFH		
	103	32K-WORD	338000H - 33FFFFH		
102	32K-WORD	330000H - 337FFFFH			
101	32K-WORD	328000H - 32FFFFH			
100	32K-WORD	320000H - 327FFFFH			
99	32K-WORD	318000H - 31FFFFH			
98	32K-WORD	310000H - 317FFFFH			
97	32K-WORD	308000H - 30FFFFH			
96	32K-WORD	300000H - 307FFFFH			
PLANE2 (UNIFORM PLANE)	95	32K-WORD	2F8000H - 2FFFFFFH	Selected by BS="1" (Bank1)	
	94	32K-WORD	2F0000H - 2F7FFFFH		
	93	32K-WORD	2E8000H - 2EFFFFH		
	92	32K-WORD	2E0000H - 2E7FFFFH		
	91	32K-WORD	2D8000H - 2DFFFFH		
	90	32K-WORD	2D0000H - 2D7FFFFH		
	89	32K-WORD	2C8000H - 2CFFFFH		
	88	32K-WORD	2C0000H - 2C7FFFFH		
	87	32K-WORD	2B8000H - 2BFFFFH		
	86	32K-WORD	2B0000H - 2B7FFFFH		
	85	32K-WORD	2A8000H - 2AFFFFH		
	84	32K-WORD	2A0000H - 2A7FFFFH		
	83	32K-WORD	298000H - 29FFFFH		
	82	32K-WORD	290000H - 297FFFFH		
	81	32K-WORD	288000H - 28FFFFH		
	80	32K-WORD	280000H - 287FFFFH		
	79	32K-WORD	278000H - 27FFFFH		
	78	32K-WORD	270000H - 277FFFFH		
	77	32K-WORD	268000H - 26FFFFH		
	76	32K-WORD	260000H - 267FFFFH		
	75	32K-WORD	258000H - 25FFFFH		
	74	32K-WORD	250000H - 257FFFFH		
	73	32K-WORD	248000H - 24FFFFH		
	72	32K-WORD	240000H - 247FFFFH		
	71	32K-WORD	238000H - 23FFFFH		
	70	32K-WORD	230000H - 237FFFFH		
	69	32K-WORD	228000H - 22FFFFH		
	68	32K-WORD	220000H - 227FFFFH		
	67	32K-WORD	218000H - 21FFFFH		
	66	32K-WORD	210000H - 217FFFFH		
	65	32K-WORD	208000H - 20FFFFH		
	64	32K-WORD	200000H - 207FFFFH		
PLANE1 (UNIFORM PLANE)	63	32K-WORD	1F8000H - 1FFFFFFH	Selected by BS="1" (Bank1)	
	62	32K-WORD	1F0000H - 1F7FFFFH		
	61	32K-WORD	1E8000H - 1EFFFFH		
	60	32K-WORD	1E0000H - 1E7FFFFH		
	59	32K-WORD	1D8000H - 1DFFFFH		
	58	32K-WORD	1D0000H - 1D7FFFFH		
	57	32K-WORD	1C8000H - 1CFFFFH		
	56	32K-WORD	1C0000H - 1C7FFFFH		
	55	32K-WORD	1B8000H - 1BFFFFH		
	54	32K-WORD	1B0000H - 1B7FFFFH		
	53	32K-WORD	1A8000H - 1AFFFFH		
	52	32K-WORD	1A0000H - 1A7FFFFH		
	51	32K-WORD	198000H - 19FFFFH		
	50	32K-WORD	190000H - 197FFFFH		
	49	32K-WORD	188000H - 18FFFFH		
	48	32K-WORD	180000H - 187FFFFH		
	47	32K-WORD	178000H - 17FFFFH		
	46	32K-WORD	170000H - 177FFFFH		
	45	32K-WORD	168000H - 16FFFFH		
	44	32K-WORD	160000H - 167FFFFH		
	43	32K-WORD	158000H - 15FFFFH		
	42	32K-WORD	150000H - 157FFFFH		
	41	32K-WORD	148000H - 14FFFFH		
	40	32K-WORD	140000H - 147FFFFH		
	39	32K-WORD	138000H - 13FFFFH		
	38	32K-WORD	130000H - 137FFFFH		
	37	32K-WORD	128000H - 12FFFFH		
	36	32K-WORD	120000H - 127FFFFH		
	35	32K-WORD	118000H - 11FFFFH		
	34	32K-WORD	110000H - 117FFFFH		
	33	32K-WORD	108000H - 10FFFFH		
	32	32K-WORD	100000H - 107FFFFH		
PLANE0 (UNIFORM PLANE)	31	32K-WORD	0F8000H - 0FFFFFFH	Selected by BS="1" (Bank1)	
	30	32K-WORD	0F0000H - 0F7FFFFH		
	29	32K-WORD	0E8000H - 0EFFFFH		
	28	32K-WORD	0E0000H - 0E7FFFFH		
	27	32K-WORD	0D8000H - 0DFFFFH		
	26	32K-WORD	0D0000H - 0D7FFFFH		
	25	32K-WORD	0C8000H - 0CFFFFH		
	24	32K-WORD	0C0000H - 0C7FFFFH		
	23	32K-WORD	0B8000H - 0BFFFFH		
	22	32K-WORD	0B0000H - 0B7FFFFH		
	21	32K-WORD	0A8000H - 0AFFFFH		
	20	32K-WORD	0A0000H - 0A7FFFFH		
	19	32K-WORD	098000H - 09FFFFH		
	18	32K-WORD	090000H - 097FFFFH		
	17	32K-WORD	088000H - 08FFFFH		
	16	32K-WORD	080000H - 087FFFFH		
	15	32K-WORD	078000H - 07FFFFH		
	14	32K-WORD	070000H - 077FFFFH		
	13	32K-WORD	068000H - 06FFFFH		
	12	32K-WORD	060000H - 067FFFFH		
	11	32K-WORD	058000H - 05FFFFH		
	10	32K-WORD	050000H - 057FFFFH		
	9	32K-WORD	048000H - 04FFFFH		
	8	32K-WORD	040000H - 047FFFFH		
	7	32K-WORD	038000H - 03FFFFH		
	6	32K-WORD	030000H - 037FFFFH		
	5	32K-WORD	028000H - 02FFFFH		
	4	32K-WORD	020000H - 027FFFFH		
	3	32K-WORD	018000H - 01FFFFH		
	2	32K-WORD	010000H - 017FFFFH		
	1	32K-WORD	008000H - 00FFFFH		
	0	32K-WORD	000000H - 007FFFFH		

6.5 DC Electrical Characteristics for Flash Memory

DC Electrical Characteristics

(T_A = -30°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
C _{IN}	Input Capacitance	4			7	pF	V _{IN} = 0V, f = 1MHz, T _A = 25°C
C _{IO}	I/O Capacitance	4			10	pF	V _{I/O} = 0V, f = 1MHz, T _A = 25°C
I _{LI}	Input Leakage Current				±1	μA	V _{IN} = V _{CC} or GND
I _{LO}	Output Leakage Current				±1	μA	V _{OUT} = V _{CC} or GND
I _{CCS}	V _{CC} Standby Current	1, 9		8	40	μA	V _{CC} = V _{CC} Max., F- $\overline{\text{CE}}$ = F- $\overline{\text{RST}}$ = V _{CC} ±0.2V, $\overline{\text{WP}}/\text{ACC}$ = V _{CC} or GND
I _{CCAS}	V _{CC} Automatic Power Savings Current	1, 3, 6		8	40	μA	V _{CC} = V _{CC} Max., F- $\overline{\text{CE}}$ = GND ±0.2V, $\overline{\text{WP}}/\text{ACC}$ = V _{CC} or GND
I _{CCD}	V _{CC} Reset Power-Down Current	1		8	40	μA	F- $\overline{\text{RST}}$ = GND ±0.2V I _{OUT} (F-RY/ $\overline{\text{BY}}$) = 0mA
I _{CCR}	Average V _{CC} Read Current Normal Mode	1, 6, 8		15	30	mA	V _{CC} = V _{CC} Max., F- $\overline{\text{CE}}$ = V _{IL} , $\overline{\text{OE}}$ = V _{IH} , f = 5MHz I _{OUT} = 0mA
	Average V _{CC} Read Current Page Mode	8 Word Read	1, 6, 8	10	15	mA	
I _{CCW}	V _{CC} (Page Buffer) Program Current	1, 4, 7, 8		40	120	mA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH1}
		1, 4, 7, 8		20	40	mA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH2}
I _{CCCE}	V _{CC} Block Erase, Bank Erase Current	1, 4, 7, 8		20	60	mA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH1}
		1, 4, 7, 8		8	20	mA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH2}
I _{CCWS} I _{CCES}	V _{CC} (Page Buffer) Program or Block Erase Suspend Current	1, 2, 8		20	400	μA	F- $\overline{\text{CE}}$ = V _{IH}
I _{ACCS} I _{ACCR}	$\overline{\text{WP}}/\text{ACC}$ Standby or Read Current	1, 5, 8		4	10	μA	$\overline{\text{WP}}/\text{ACC}$ ≤ V _{CC}
I _{ACCW}	$\overline{\text{WP}}/\text{ACC}$ (Page Buffer) Program Current	1,4,5,7,8		4	10	μA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH1}
		1,4,5,7,8		20	60	mA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH2}
I _{ACCE}	$\overline{\text{WP}}/\text{ACC}$ Block Erase, Bank Erase Current	1,4,5,7,8		4	10	μA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH1}
		1,4,5,7,8		10	30	mA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH2}
I _{ACCWS}	$\overline{\text{WP}}/\text{ACC}$ (Page Buffer) Program Suspend Current	1, 5, 8		4	10	μA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH1}
		1, 5, 8		50	400	μA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH2}
I _{ACCES}	$\overline{\text{WP}}/\text{ACC}$ Block Erase Suspend Current	1, 5, 8		4	10	μA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH1}
		1, 5, 8		50	400	μA	$\overline{\text{WP}}/\text{ACC}$ = V _{ACCH2}

DC Electrical Characteristics (Continue)

(T_A = -30°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
V _{IL}	Input Low Voltage	4	-0.4		0.4	V	
V _{IH}	Input High Voltage	4	2.4		V _{CC} +0.4	V	
V _{OL}	Output Low Voltage	4, 9			0.2	V	V _{CC} = V _{CC} Min, I _{OL} = 100μA
V _{OH}	Output High Voltage	4	V _{CC} -0.2			V	I _{OH} = 100μA
V _{ACCH1}	\overline{WP}/A_{CC} during Block Erase, Bank Erase, (Page Buffer) Program Operations	5	-0.4	3	3.1	V	
V _{ACCH2}	\overline{WP}/A_{CC} during Block Erase, Bank Erase, (Page Buffer) Program Operations	5	11.7	12	12.3	V	
V _{LKO}	V _{CC} Lockout Voltage		1.5			V	

Notes:

- All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{CC} = 3.0V and T_A = +25°C unless V_{CC} is specified.
- I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW}. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR}.
- The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when addresses are changed.
- Sampled, not 100% tested.
- Applying 12V±0.3V to \overline{WP}/A_{CC} provides fast erasing or fast programming mode. In this mode, \overline{WP}/A_{CC} is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the V_{CC} power bus.
Applying 12V±0.3V to \overline{WP}/A_{CC} during erase/program can only be done for a maximum of 1,000 cycles on each block. \overline{WP}/A_{CC} may be connected to 12V±0.3V for a total of 80 hours maximum.
- Never hold F₁- \overline{CE} low and F₂- \overline{CE} low at the same timing.
- F₁ and F₂ should not be operated at the same timing to Block erase, bank erase, (page buffer) program.
- The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.
- Includes F-RY/ \overline{BY}

6.6 AC Electrical Characteristics for Flash Memory

6.6.1 AC Test Conditions ⁽¹⁾

Input Pulse Level	0 V to 2.7 V
Input Rise and Fall Time	5 ns
Input and Output Timing Ref. level	1/2 V _{CC}
Output Load	1TTL + C _L (50pF)

Notes:

1. The capacitance in a chip is not included.

6.6.2 Read Cycle

(T_A = -30°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{AVAV}	Read Cycle Time		70		ns
t _{AVQV}	Address to Output Delay			70	ns
t _{BLQV}	BS to Output Delay			70	ns
t _{ELQV}	F- \overline{CE} to Output Delay	2		70	ns
t _{APA}	Page Address Access Time			35	ns
t _{GLQV}	\overline{OE} to Output Delay	2		20	ns
t _{PHQV}	F- \overline{RST} High to Output Delay			150	ns
t _{EHQZ} , t _{GHQZ}	F- \overline{CE} or \overline{OE} to Output in High-Z, Whichever Occurs First	1		20	ns
t _{ELQX}	F- \overline{CE} to Output in Low-Z	1	0		ns
t _{GLQX}	\overline{OE} to Output in Low-Z	1	0		ns
t _{OH}	Output Hold from First Occurring Address, F- \overline{CE} or \overline{OE} Change	1	0		ns
t _{AVEL} , t _{AVGL}	Address Setup to F- \overline{CE} and \overline{OE} Going Low for Reading Status Register	3,5	10		ns
t _{ELAX} , t _{GLAX}	Address Hold from F- \overline{CE} and \overline{OE} Going Low for Reading Status Register	4,5	30		ns
t _{EHGL} , t _{GHGL}	F- \overline{CE} and \overline{OE} Pulse Width High for Reading Status Register	5	20		ns
t _{AVBV}	Address Setup to BS (Bank Select) for Reading Status Register	6	10		ns
t _{BVAX}	Address Hold from BS (Bank Select) for Reading Status Register	6	30		ns
t _{BVBV}	BS Pulse Width High for Reading Status Register	6	20		ns

Notes:

1. Sampled, not 100% tested.
2. \overline{OE} may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of F- \overline{CE} without impact to t_{ELQV}.
3. Address setup time (t_{AVEL}, t_{AVGL}) is defined from the falling edge of F- \overline{CE} or \overline{OE} (whichever goes low last).
4. Address hold time (t_{ELAX}, t_{GLAX}) is defined from the falling edge of F- \overline{CE} or \overline{OE} (whichever goes low last).
5. Specifications t_{AVEL}, t_{AVGL}, t_{ELAX}, t_{GLAX} and t_{EHGL}, t_{GHGL} for read operations apply to only status register read operations.
6. Specifications t_{AVBV}, t_{BVAX} and t_{BVBV} for read operations apply to only status register read operations.

6.6.3 Write Cycle (\overline{WE} / $F\text{-}\overline{CE}$ Controlled)^(1, 2) $(T_A = -30^\circ\text{C to } +85^\circ\text{C}, V_{CC} = 2.7\text{V to } 3.1\text{V})$

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		70		ns
t_{PHWL} (t_{PHEL})	$F\text{-}\overline{RST}$ High Recovery to \overline{WE} ($F\text{-}\overline{CE}$) Going Low	3	150		ns
t_{BLWL} , t_{WLBL}	BS Setup to \overline{WE} Going Low		0		ns
t_{ELWL} (t_{WLEL})	$F\text{-}\overline{CE}$ (\overline{WE}) Setup to \overline{WE} ($F\text{-}\overline{CE}$) Going Low	4	0		ns
t_{WLWH} (t_{ELEH})	\overline{WE} ($F\text{-}\overline{CE}$) Pulse Width	4	50		ns
t_{DVWH} (t_{DVEH})	Data Setup to \overline{WE} ($F\text{-}\overline{CE}$) Going High	8	40		ns
t_{AVWH} (t_{AVEH})	Address Setup to \overline{WE} ($F\text{-}\overline{CE}$) Going High	8	50		ns
t_{BVWH} (t_{BVEH})	BS Setup to \overline{WE} ($F\text{-}\overline{CE}$) Going High		50		ns
t_{WHBH} , t_{WHBL}	BS Hold from \overline{WE} High		0		ns
t_{WHEH} (t_{EHWH})	$F\text{-}\overline{CE}$ (\overline{WE}) Hold from \overline{WE} ($F\text{-}\overline{CE}$) High		0		ns
t_{WHDX} (t_{EHDX})	Data Hold from \overline{WE} ($F\text{-}\overline{CE}$) High		0		ns
t_{WHAX} (t_{EHAX})	Address Hold from \overline{WE} ($F\text{-}\overline{CE}$) High		0		ns
t_{WHBX} (t_{EHBX})	BS Hold from \overline{WE} ($F\text{-}\overline{CE}$) Going High		0		ns
t_{WHWL} (t_{EHEL})	\overline{WE} ($F\text{-}\overline{CE}$) Pulse Width High	5	20		ns
t_{VVWH} (t_{VVEH})	\overline{WP}/A_{CC} Setup to \overline{WE} ($F\text{-}\overline{CE}$) Going High	3	200		ns
t_{WHGL} (t_{EHGL})	Write Recovery before Read		30		ns
t_{QVVL}	\overline{WP}/A_{CC} Hold from Valid SRD, $F\text{-}RY/\overline{BY}$ High-Z	3, 6	0		ns
t_{WHR0} (t_{EHR0})	\overline{WE} ($F\text{-}\overline{CE}$) High to SR.7 Going "0"	3, 7		$t_{AVQV}+50$	ns
t_{WHRL} (t_{EHL})	\overline{WE} ($F\text{-}\overline{CE}$) High to $F\text{-}RY/\overline{BY}$ Going Low	3		100	ns

Notes:

1. The timing characteristics for reading the status register during block erase, bank erase, (page buffer) program operations are the same as during read-only operations. See the AC Characteristics for read cycle.
2. A write operation can be initiated and terminated with either $F\text{-}\overline{CE}$ or \overline{WE} .
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from the falling or rising edge of BS or the falling edge of $F\text{-}\overline{CE}$ or \overline{WE} (whichever occurs last) to the rising or falling edge of BS or the rising edge of $F\text{-}\overline{CE}$ or \overline{WE} (whichever occurs first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}=t_{BLBH}=t_{WLBH}=t_{BLWH}$.
5. Write pulse width high (t_{WPH}) is defined from the rising edge of $F\text{-}\overline{CE}$ or \overline{WE} (whichever goes high first) to the falling edge of $F\text{-}\overline{CE}$ or \overline{WE} (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$.
6. \overline{WP}/A_{CC} should be held at $\overline{WP}/A_{CC}=V_{ACCH1/2}$ until determination of block erase, bank erase, (page buffer) program success (SR.1/3/4/5=0).
7. t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes command= $t_{AVQV}+100\text{ns}$.
8. See 6.2.1 Command Definitions for valid address and data for block erase, bank erase, (page buffer) program or lock bit configuration.

6.6.4 Block Erase, Bank Erase, (Page Buffer) Program Performance ⁽³⁾(T_A = -30°C to +85°C, V_{CC} = 2.7V to 3.1V)

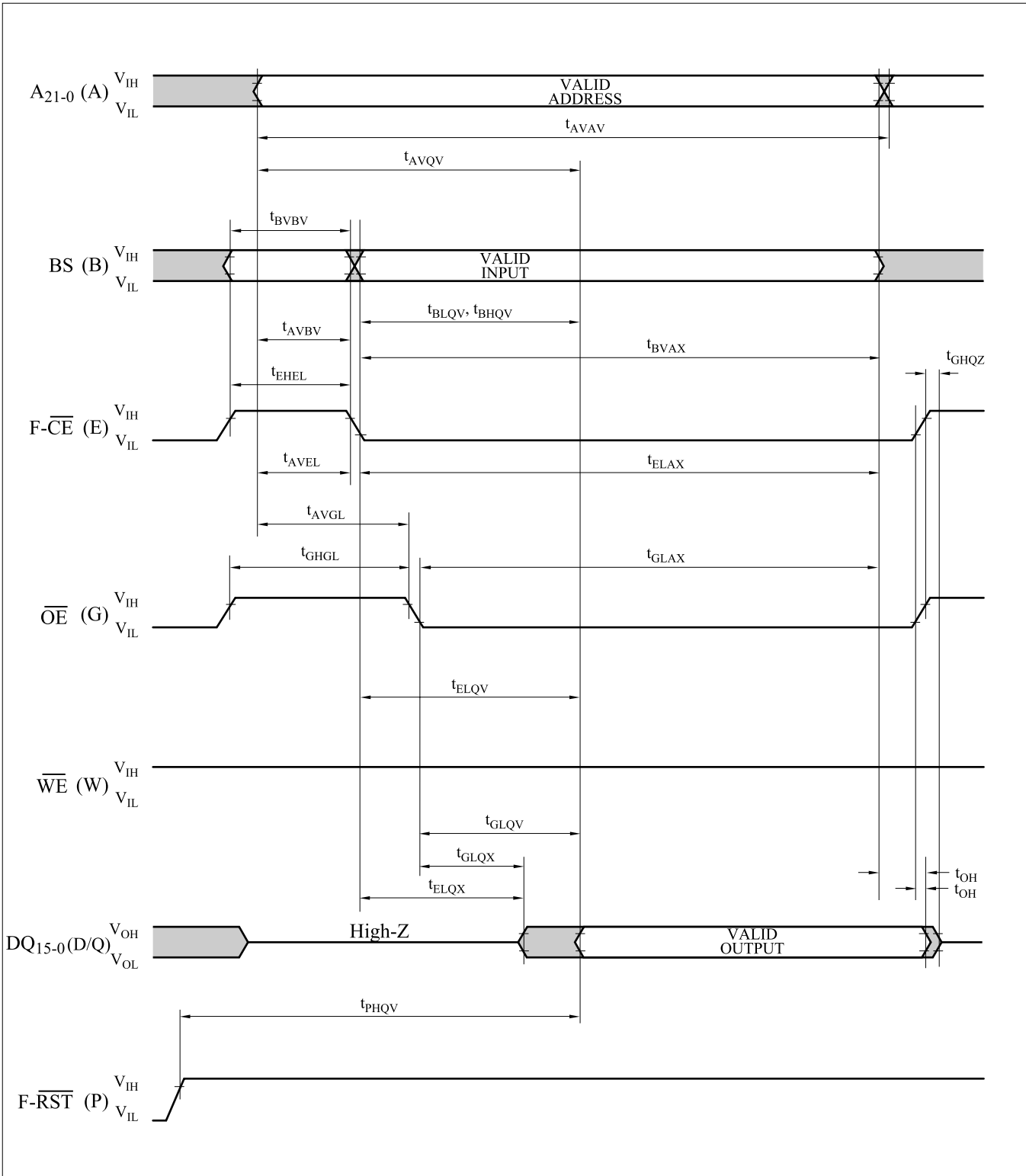
Symbol	Parameter	Notes	Page Buffer Command is Used or not Used	$\overline{WP}/A_{CC}=V_{ACCH1}$			$\overline{WP}/A_{CC}=V_{ACCH2}$			Unit
				Min.	Typ. ⁽¹⁾	Max. ⁽²⁾	Min.	Typ. ⁽¹⁾	Max. ⁽²⁾	
t _{WPB}	4K-Word Parameter Block Program Time	2	Not Used		0.05	0.3		0.04	0.12	s
		2	Used		0.03	0.12		0.02	0.06	s
t _{WMB}	32K-Word Main Block Program Time	2	Not Used		0.38	2.4		0.31	1	s
		2	Used		0.24	1		0.17	0.5	s
t _{WHQV1} / t _{EHQV1}	Word Program Time	2	Not Used		11	200		9	185	μs
		2	Used		7	100		5	90	μs
t _{WHQV2} / t _{EHQV2}	4K-Word Parameter Block Erase Time	2	-		0.3	4		0.2	4	s
t _{WHQV3} / t _{EHQV3}	32K-Word Main Block Erase Time	2	-		0.6	5		0.5	5	s
	Bank Erase Time	2			80	700		65	700	s
t _{WHRH1} / t _{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10		5	10	μs
t _{WHRH2} / t _{EHRH2}	Block Erase Suspend Latency Time to Read	4	-		5	20		5	20	μs
t _{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			500			μs

Notes:

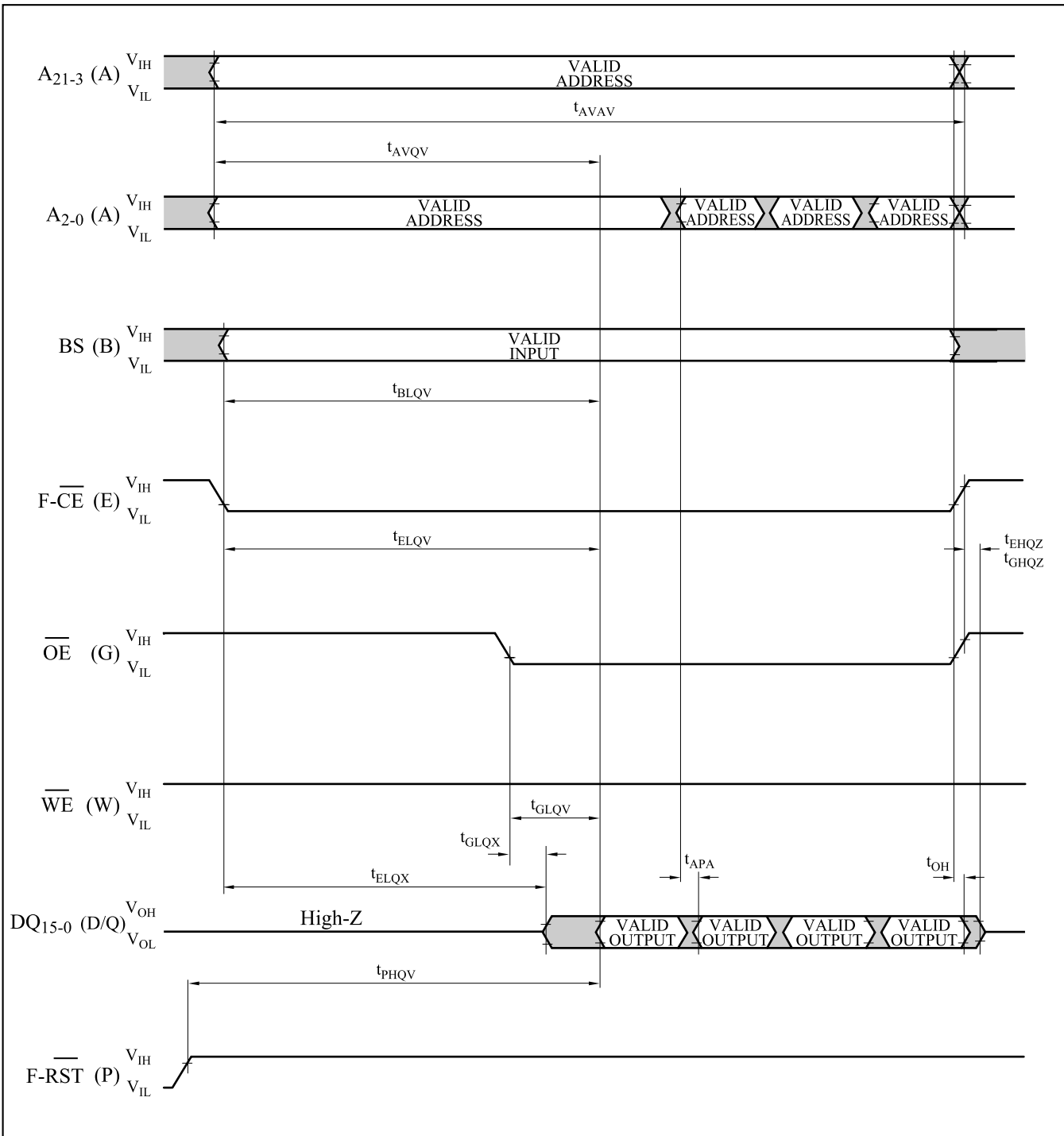
1. Typical values measured at V_{CC} = 3.0V, \overline{WP}/A_{CC} = 3.0V or 12V, and T_A = +25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (\overline{WE} or F- \overline{CE} going high) until SR.7 going "1" or F-RY/ \overline{BY} going High-Z.
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.

6.6.5 Flash Memory AC Characteristics Timing Chart

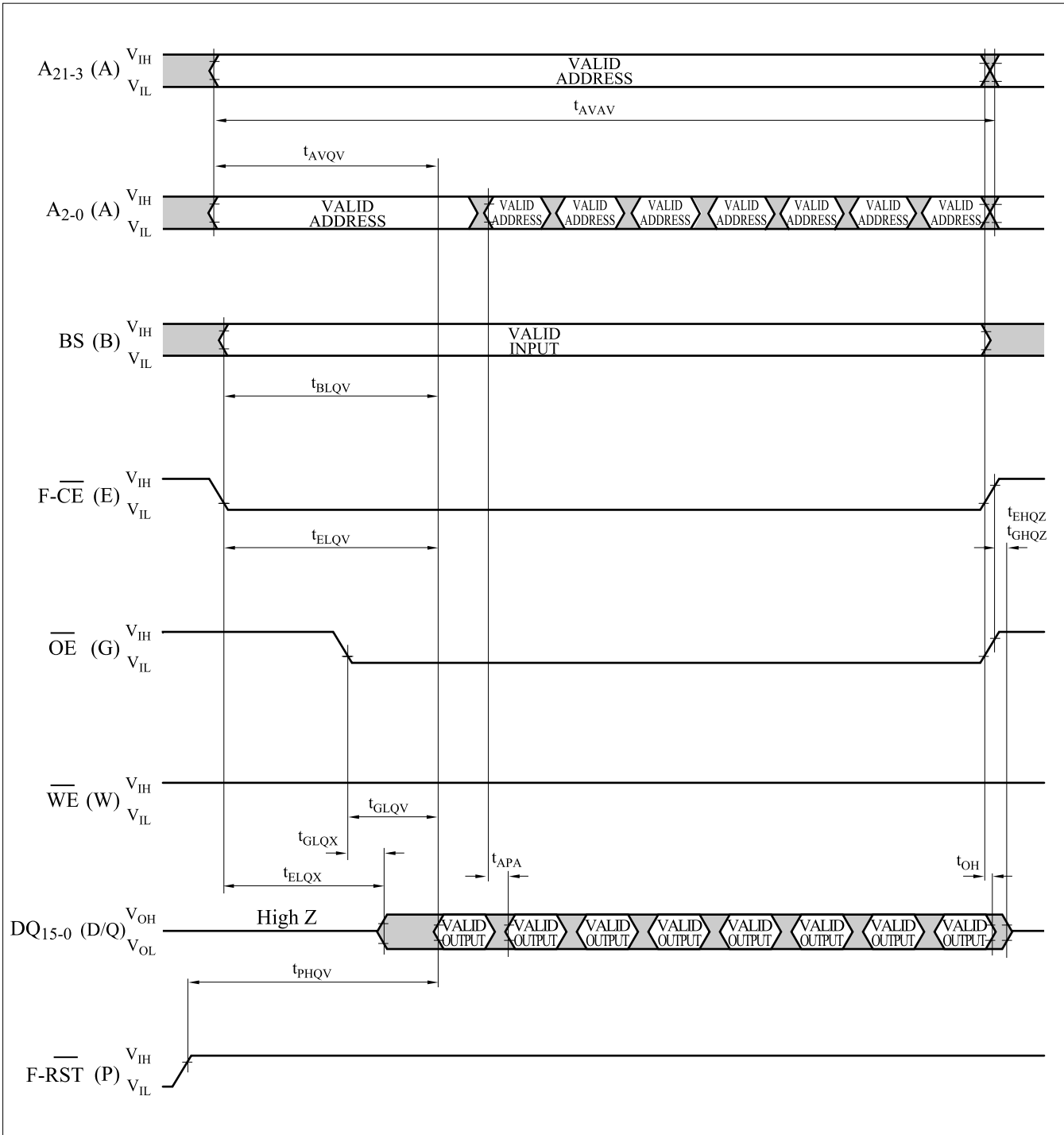
AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier Codes or Query Code



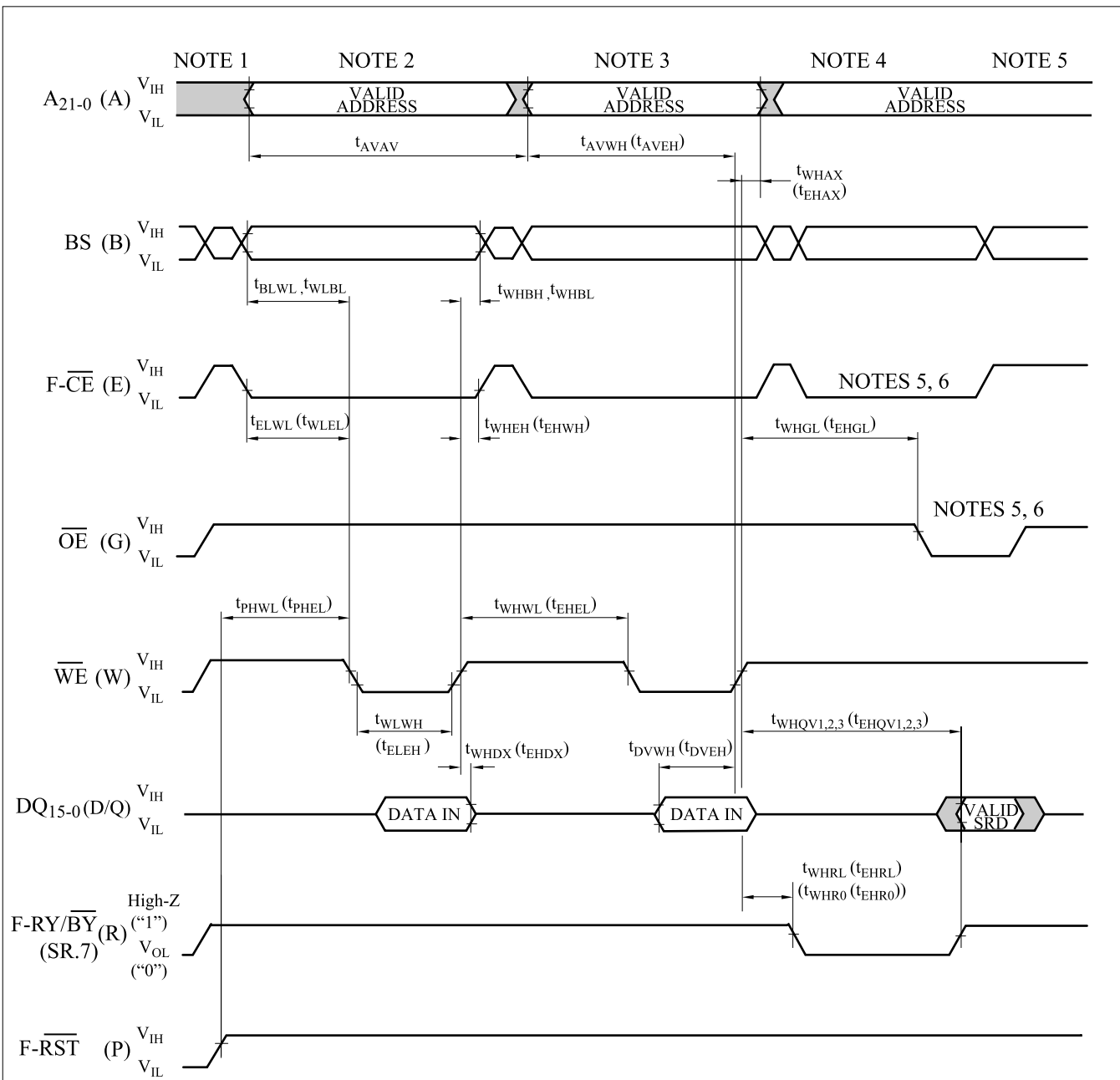
AC Waveform for Asynchronous 4-Word Page Mode Read Operations from Main Blocks or Parameter Blocks



AC Waveform for Asynchronous 8-Word Page Mode Read Operations from Main Blocks or Parameter Blocks



AC Waveform for Write Operations (\overline{WE} / F- \overline{CE}) 1 (\overline{WP}/ACC : VACCH1 Selected)



Notes:

1. VCC power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, \overline{OE} and F- \overline{CE} must be driven active, and \overline{WE} de-asserted.

6.6.6 Reset Operations

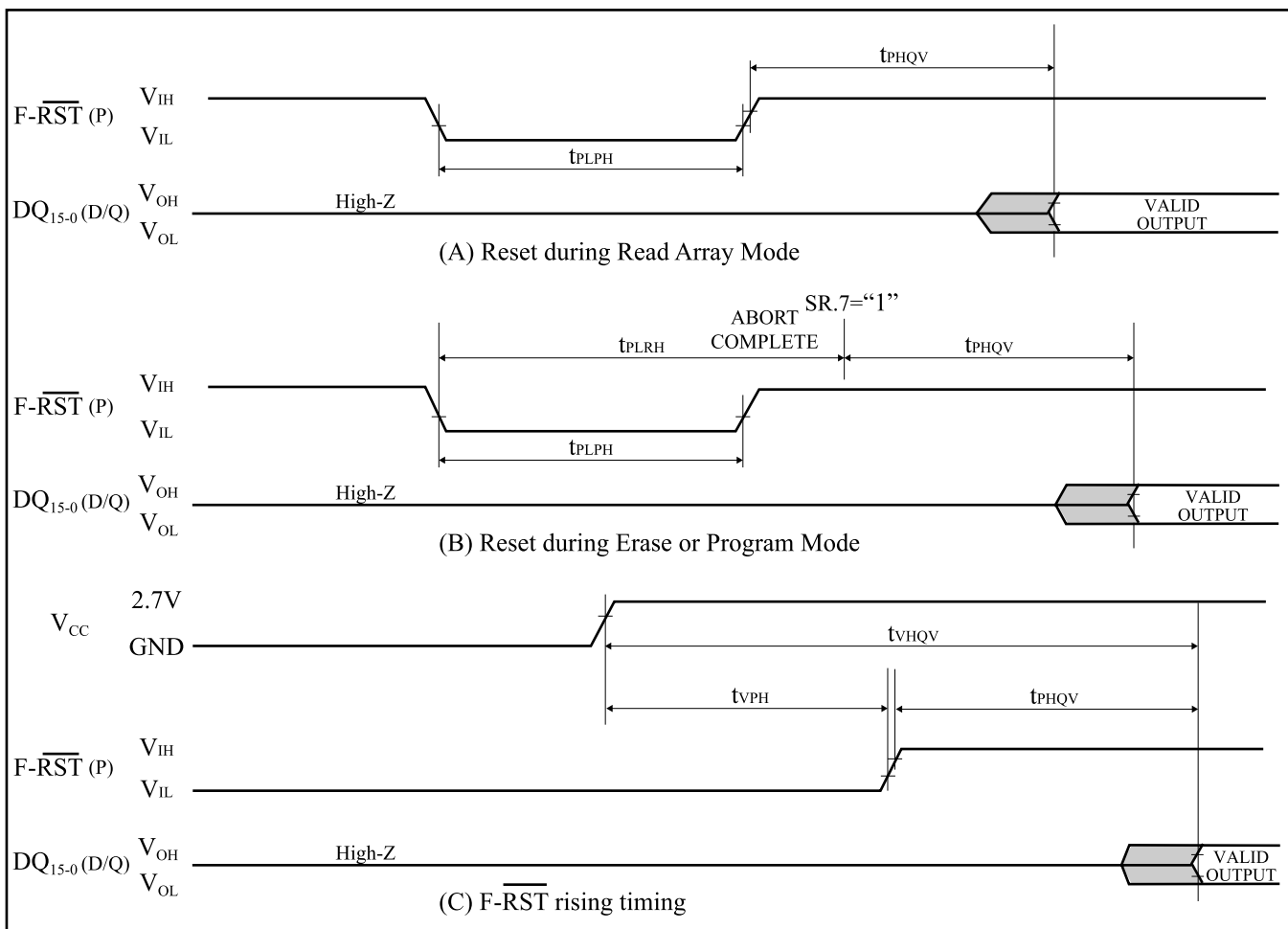
 $(T_A = -30^\circ\text{C to } +85^\circ\text{C}, V_{CC} = 2.7\text{V to } 3.1\text{V})$

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	F- $\overline{\text{RST}}$ Low to Reset during Read (F- $\overline{\text{RST}}$ should be low during power-up.)	1, 2, 3	100		ns
t_{PLRH}	F- $\overline{\text{RST}}$ Low to Reset during Erase or Program	1, 3, 4		22	μs
t_{VPH}	$V_{CC} = 2.7\text{V}$ to F- $\overline{\text{RST}}$ High	1, 3, 5	100		ns
t_{VHQV}	$V_{CC} = 2.7\text{V}$ to Output Delay	3		1	ms

Notes:

1. A reset time, t_{PHQV} , is required from the later of SR.7 (F-RY/ $\overline{\text{BY}}$) going "1" (High-Z) or F- $\overline{\text{RST}}$ going high until outputs are valid. See the AC Characteristics - read cycle for t_{PHQV} .
2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If F- $\overline{\text{RST}}$ asserted while a block erase, bank erase or (page buffer) program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding F- $\overline{\text{RST}}$ low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation



7. Smartcombo RAM

7.1 Truth Table

7.1.1 Bus Operation ⁽¹⁾

Smartcombo RAM	Notes	SC- \overline{CE}_1	SC-CE ₂	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	DQ ₀ to Q ₁₅
Read		L	H	L	H	(3)		(3)
Output Disable				H	H	X	X	High - Z
Write		H		H	L	(3)		(3)
Standby		X	L	X	X	X	X	High - Z
		H				H	H	
Sleep	2	X		X	X	X	X	

Notes:

1. L = V_{IL}, H = V_{IH}, X = H or L, High-Z = High impedance. Refer to the DC Characteristics.
2. SC-CE₂ pin must be fixed to high level except sleep mode.
3. \overline{LB} , \overline{UB} Control Mode

\overline{LB}	\overline{UB}	DQ ₀ to DQ ₇	DQ ₈ to DQ ₁₅
L	L	D _{OUT} /D _{IN}	D _{OUT} /D _{IN}
L	H	D _{OUT} /D _{IN}	High - Z
H	L	High - Z	D _{OUT} /D _{IN}

7.2 DC Electrical Characteristics for Smartcombo RAM

DC Electrical Characteristics

 $(T_A = -30^{\circ}\text{C to } +85^{\circ}\text{C}, V_{CC} = 2.7\text{V to } 3.1\text{V})$

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance	1			8	pF	$V_{IN} = 0\text{V}$
C_{IO}	I/O Capacitance	1			10	pF	$V_{IO} = 0\text{V}$
I_{LI}	Input Leakage Current				± 1	μA	$V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current				± 1	μA	$V_{OUT} = V_{CC}$ or GND
I_{SB}	V_{CC} Standby Current	2			180	μA	$SC-\overline{CE}_1 \geq V_{CC} - 0.2\text{V}, SC-CE_2 \geq 0.2\text{V}$
I_{SLP}	V_{CC} Sleep Mode Current	3			100	μA	$SC-\overline{CE}_1 \geq V_{CC} - 0.2\text{V}, SC-CE_2 \leq 0.2\text{V}$
I_{CC1}	V_{CC} Operation Current				50	mA	$t_{CYCLE} = \text{Min.}, I_{IO} = 0\text{mA},$ $SC-\overline{CE}_1 = V_{IL}$
V_{IL}	Input Low Voltage	1	-0.4		0.4	V	
V_{IH}	Input High Voltage	1	2.4		$V_{CC} + 0.4$	V	
V_{OL}	Output Low Voltage	1			$0.2V_{CC}$	V	$I_{OL} = 0.5\text{mA}$
V_{OH}	Output High Voltage	1	$0.8V_{CC}$			V	$I_{OH} = -0.5\text{mA}$

Notes:

1. Sampled, not 100% tested.
2. Memory cell data is held. ($SC-CE_2 = "V_{IH}"$)
3. Memory cell data is not held. ($SC-CE_2 = "V_{IL}"$)

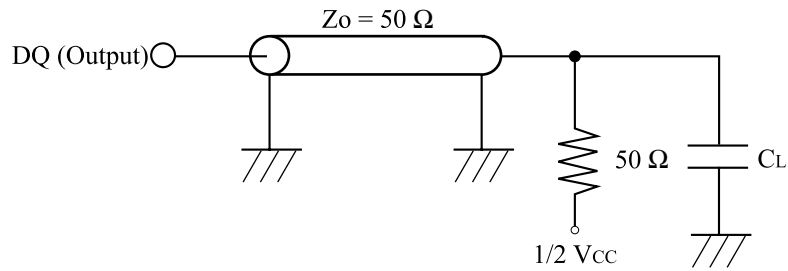
7.3 AC Electrical Characteristic for Smartcombo RAM

7.3.1 AC Test Conditions

Input Pulse Level	$0.2V_{CC}$ to $0.8V_{CC}$
Input Rise and Fall Time	5 ns
Input and Output Timing Ref. Level	$1/2 V_{CC}$
Output Load	1TTL + C_L (50pF) ^(1, 2)

Notes:

1. Including scope and socket capacitance.
2. AC characteristics directed with the note should be measured with the output load shown in below.



7.3.2 Read Cycle

(T_A = -30°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{RC}	Read Cycle Time		70		ns
t _{AA}	Address Access Time			70	ns
t _{ACE}	Chip Enable Access Time			70	ns
t _{OE}	Output Enable to Output Valid			45	ns
t _{BE}	Byte Enable Access Time			70	ns
t _{PAA}	Page Access Time			18	ns
t _{OH}	Output Hold from Address Change		5		ns
t _{PRC}	Page Read Cycle Time		18		ns
t _{CLZ}	SC- \overline{CE}_1 Low to Output Active		10		ns
t _{OLZ}	\overline{OE} Low to Output Active		5		ns
t _{BLZ}	\overline{UB} or \overline{LB} Low to Output Active		5		ns
t _{CHZ}	SC- \overline{CE}_1 High to Output in High-Z			25	ns
t _{OHZ}	\overline{OE} High to Output in High-Z			25	ns
t _{BHZ}	\overline{UB} or \overline{LB} High to Output in High-Z			25	ns
t _{ASO}	Address Setup to \overline{OE} Low		0		ns
t _{OHAH}	\overline{OE} High Level to Address Hold		-5		ns
t _{CHAH}	SC- \overline{CE}_1 High Level to Address Hold		0		ns
t _{BHAH}	\overline{LB} , \overline{UB} High Level to Address Hold	2	0		ns
t _{CLOL}	SC- \overline{CE}_1 Low Level to \overline{OE} Low Level	1	0	10,000	ns
t _{OLCH}	\overline{OE} Low Level to SC- \overline{CE}_1 High Level		45		ns
t _{CP}	SC- \overline{CE}_1 High Level Pulse Width		10		ns
t _{BP}	\overline{LB} , \overline{UB} High Level Pulse Width		10		ns
t _{OP}	\overline{OE} High Level Pulse Width	1	2	10,000	ns

Notes:

1. t_{CLOL} and t_{OP} (Max.) are applied while SC- \overline{CE}_1 is being hold at low level.
2. t_{BHAH} is specified after both \overline{LB} and \overline{UB} are High.

7.3.3 Write Cycle

 $(T_A = -30^{\circ}\text{C to } +85^{\circ}\text{C}, V_{CC} = 2.7\text{V to } 3.1\text{V})$

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{WC}	Write Cycle Time		70		ns
t_{CW}	Chip Enable to End of Write		55		ns
t_{AW}	Address Valid to End of Write		55		ns
t_{BW}	Byte Select Time		55		ns
t_{WP}	Write Pulse Width		50		ns
t_{WR}	Write Recovery Time		0		ns
t_{CP}	$\overline{SC}-\overline{CE}_1$ High Level Pulse Width		10		ns
t_{BP}	$\overline{LB}, \overline{UB}$ High Level Pulse Width		10		ns
t_{WHP}	\overline{WE} High Pulse Width		10		ns
t_{WHZ}	\overline{WE} Low to Output in High-Z			25	ns
t_{OW}	\overline{WE} High to Output Active		15		ns
t_{AS}	Address Setup Time		0		ns
t_{DW}	Input Data Setup Time		30		ns
t_{DH}	Input Data Hold Time		0		ns
t_{OHAH}	\overline{OE} High Level to Address Hold		-5		ns
t_{CHAH}	$\overline{SC}-\overline{CE}_1$ High Level to Address Hold		0		ns
t_{BHAH}	$\overline{LB}, \overline{UB}$ High Level to Address Hold	2	0		ns
t_{OES}	\overline{OE} High Level to \overline{WE} Set	1	0	10,000	ns
t_{OEH}	\overline{WE} High Level to \overline{OE} Set	1	10	10,000	ns

Notes:

- t_{OES} and t_{OEH} (Max.) are applied while $\overline{SC}-\overline{CE}_1$ is being hold at low level.
- t_{BHAH} is specified after both \overline{LB} and \overline{UB} are High.

7.3.4 Initialization

 $(T_A = -30^{\circ}\text{C to } +85^{\circ}\text{C}, V_{CC} = 2.7\text{V to } 3.1\text{V})$

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VHMH}	Power Application to SC-CE ₂ Low Level Hold		50		μs
t_{CHMH}	SC- $\overline{\text{CE}}_1$ High Level to SC-CE ₂ High Level		10		ns
t_{MHCL}	Following Power Application SC-CE ₂ High Level Hold to SC- $\overline{\text{CE}}_1$ Low Level		300		μs

7.3.5 Sleep Mode Entry / Exit

 $(T_A = -30^{\circ}\text{C to } +85^{\circ}\text{C}, V_{CC} = 2.7\text{V to } 3.1\text{V})$

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{CHML}	Sleep Mode Entry SC- $\overline{\text{CE}}_1$ High Level to SC-CE ₂ Low Level		0		ns
t_{MHCL}	Sleep Mode Exit to Normal Operation SC-CE ₂ High Level to SC- $\overline{\text{CE}}_1$ Low Level		300		μs

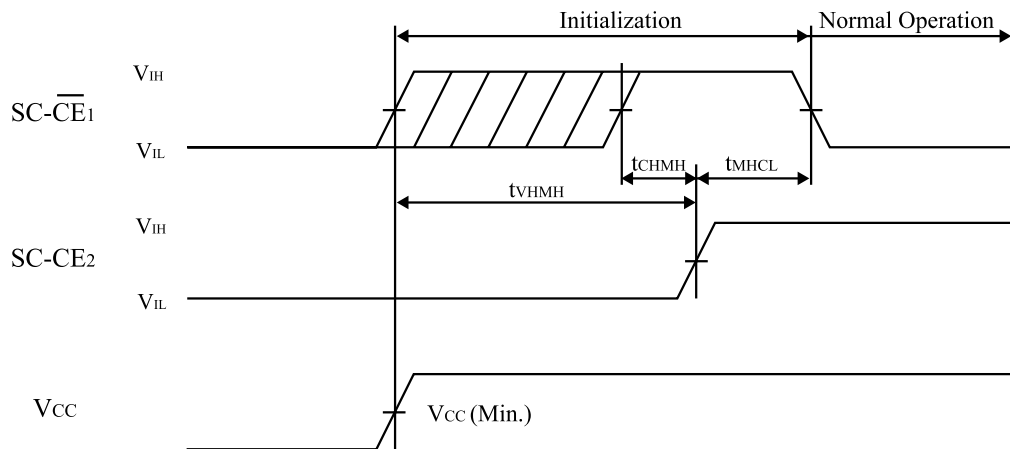
7.4 Initialization

Initialize the power application using the following sequence to stabilize internal circuits.

(1) Following power application, make SC-CE₂ high level after fixing SC-CE₂ to low level for the period of t_{VHMH} . Make SC- \overline{CE}_1 high level before making SC-CE₂ high level.

(2) SC- \overline{CE}_1 and SC-CE₂ are fixed to high level for the period of t_{MHCL} .

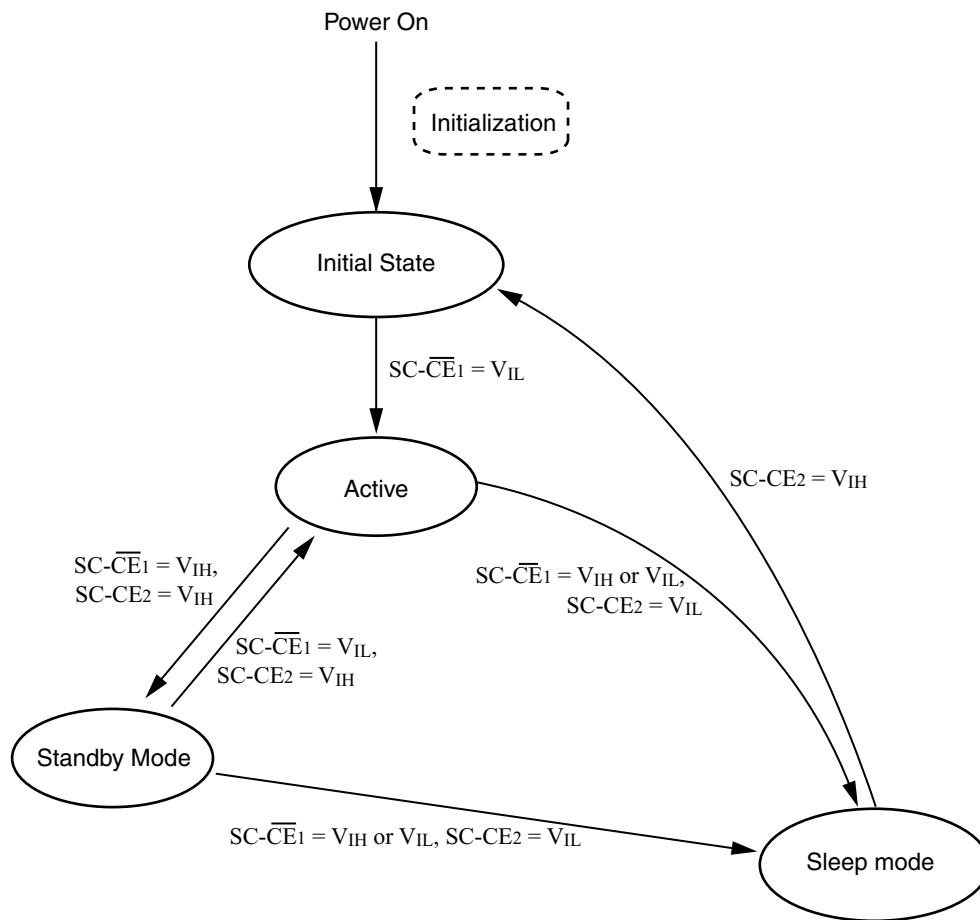
Normal operation is possible after the completion of initialization.



Notes:

1. Make SC-CE₂ low level when starting the power supply.
2. t_{VHMH} is specified from when the power supply voltage reaches the prescribed minimum value ($V_{CC} \text{ Min.}$).

Standby Mode State Machine



7.5 Page Read Operation

7.5.1 Features of Page Read Operation ⁽²⁾

Features	Notes	8 Words Mode
Page Length		8 words
Page Read-corresponding Addresses		A_2, A_1, A_0
Page Read Start Address		Don't care
Page Direction		Don't care
Interrupt during page read operation	1	Enabled

Notes:

1. An interrupt is output when $SC-\overline{CE}_1 = \text{High}$ or in case A_3 or a higher address changes.

2. Page Length:

8 words is supported as the page lengths.

Page-Corresponding Addresses:

The page read-enabled addresses are $A_2, A_1,$ and A_0 . Fix addresses other than $A_2, A_1,$ and A_0 during page read operation.

Page Start Address:

Since random page read is supported, any address (A_2, A_1, A_0) can be used as the page read start address.

Page Direction:

Since random page read is possible, there is not restriction on the page direction.

Interrupt during Page Read Operation:

When generating an interrupt during page read, either make $SC-\overline{CE}_1$ high level or change A_3 and higher addresses.

When page read is not used:

Since random page read is supported, even when not using page read, random access is possible as usual.

7.6 Mode Register Settings

The sleep mode can be set using the mode register. Since the initial value of the mode register at power application is undefined, be sure to set the mode register after initialization at power application. However, since sleep mode is not entered unless SC-CE₂ = Low when sleep mode is not used, it is not necessary to set the mode register. Moreover, when using page read without using sleep mode, it is not necessary to set the mode register.

7.6.1 Mode Register Setting Method

The mode register setting mode can be entered by successively writing two specific data after two continuous reads of the highest address (1FFFFFFH). The mode register setting is a continuous four-cycle operation (two read cycles and two write cycles).

Commands are written to the command register. The command register is used to latch the addresses and data required for executing commands, and it does not have an exclusive memory area.

For the timing chart and flow chart, refer to Mode Register Setting Timing Chart (P.55), Mode Register Setting Flow Chart (P.56).

Following table shows the commands and command sequences.

Command Sequence

Command Sequence	1st Bus Cycle (Read Cycle)		2nd Bus Cycle (Read Cycle)		3rd Bus Cycle (Write Cycle)		4th Bus Cycle (Write Cycle)	
	Address	Data	Address	Data	Address	Data	Address	Data
Sleep Mode	1FFFFFFH	-	1FFFFFFH	-	1FFFFFFH	00H	1FFFFFFH	07H

4th Bus Cycle (Write cycle)

DQ	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode Register Setting	0	0	0	0	0	0	0	0	0	0	0	0	0	PL	1	1

Page Length	1	8 words
-------------	---	---------



7.6.2 Cautions for Setting Mode Register

Since, for the mode register setting, the internal counter status is judged by toggling $SC-\overline{CE}_1$ and $S-\overline{OE}$, toggle $SC-\overline{CE}_1$ at every cycle during entry (read cycle twice, write cycle twice), and toggle $S-\overline{OE}$ like $SC-\overline{CE}_1$ at the first and second read cycles.

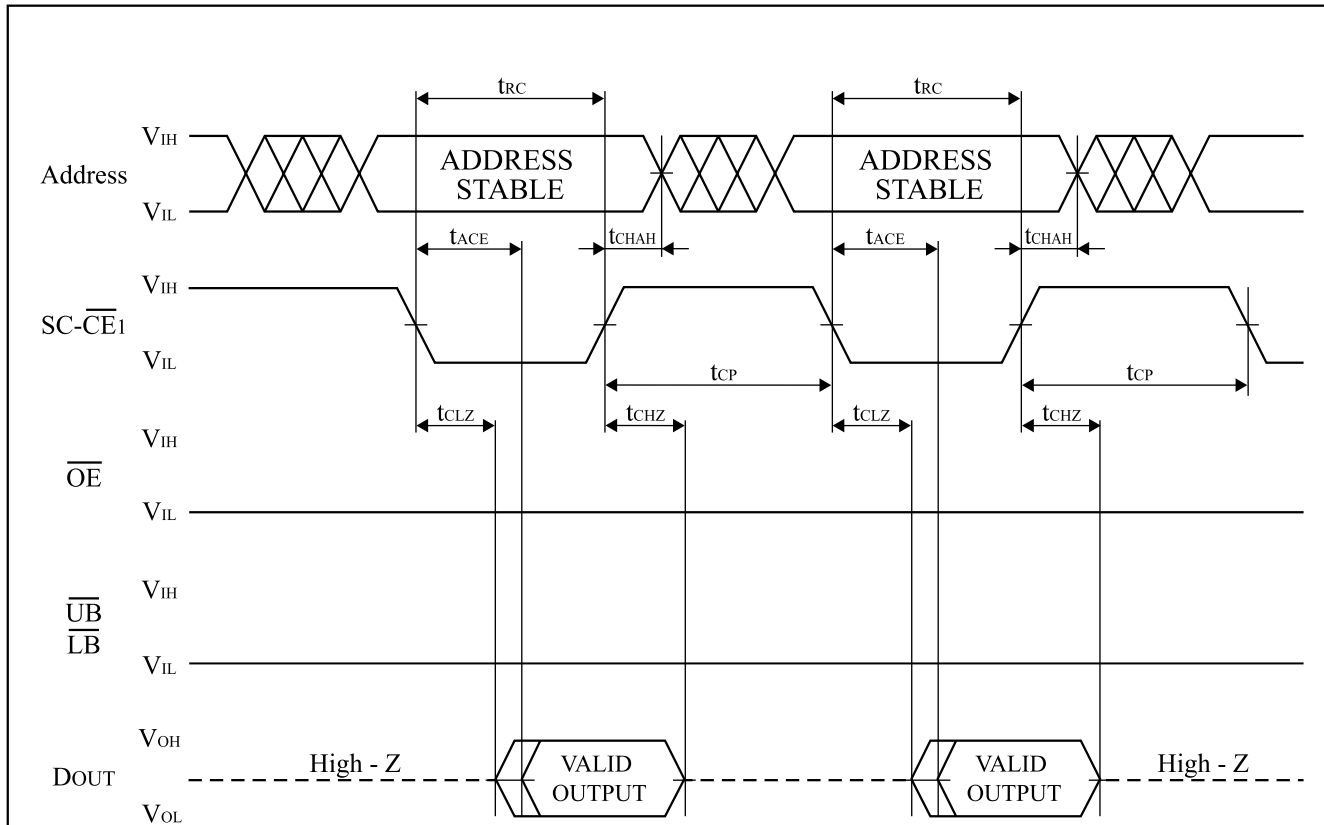
If incorrect addresses or data are written, or if addresses or data are written in the incorrect order, the setting of the mode register are not performed correctly.

When the highest address (1FFFFFFH) is read consecutively three or more times, the mode register setting entries are cancelled.

Once the sleep mode has been set in the mode register, these settings are retained until they are set again, while applying the power supply. However, the mode register setting will become undefined if the power is turned off, so set the mode register again after power application.

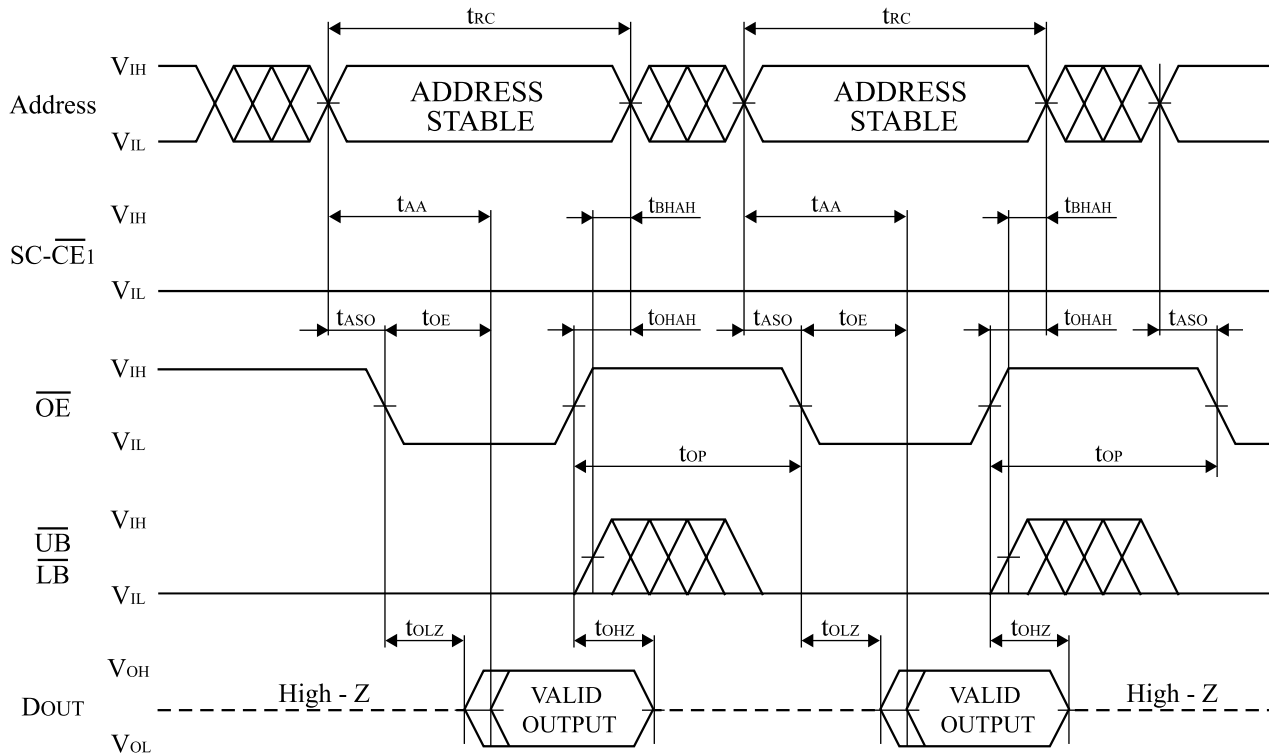
For the timing chart and flow chart, refer to Mode Register Setting Timing Chart (P.55), Mode Register Setting Flow Chart (P.56).

7.7 Smartcombo RAM AC Characteristics Timing Chart

Read Cycle Timing Chart 1 (SC- $\overline{\text{CE}}_1$ Controlled)

Note:

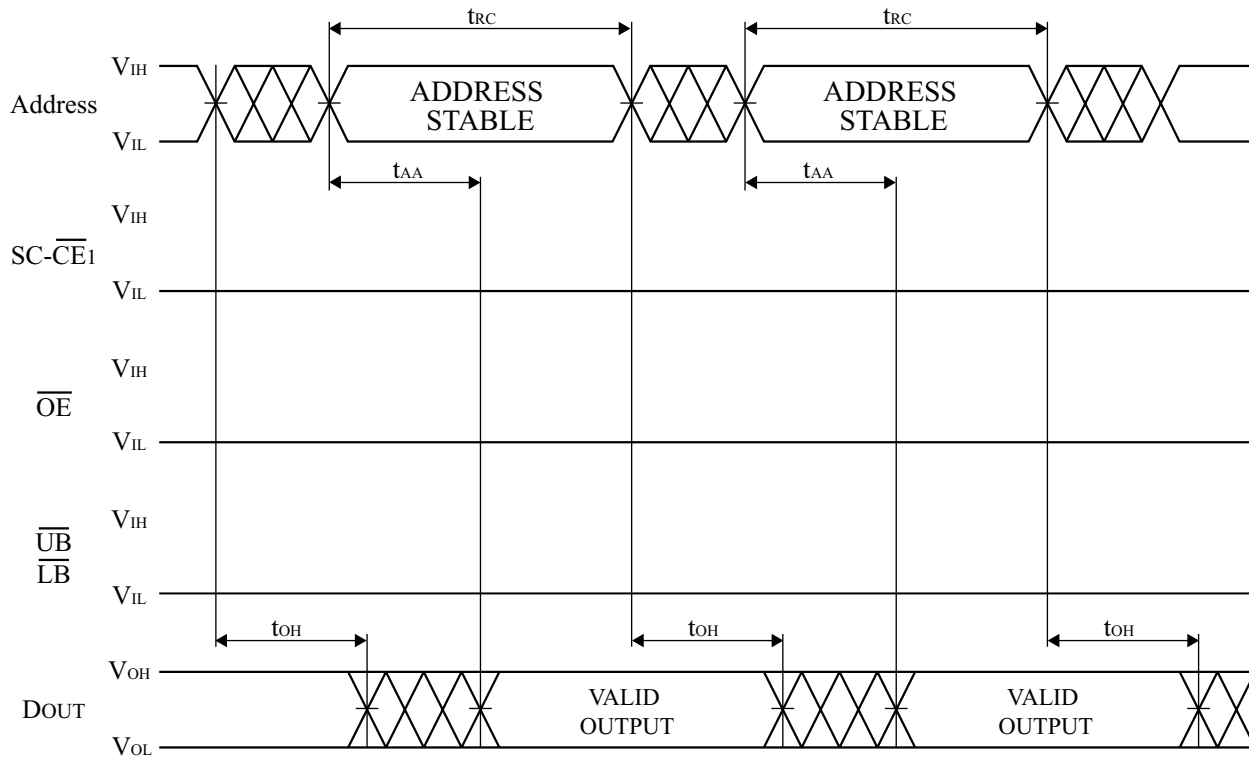
1. In read cycle, SC-CE2 and $\overline{\text{WE}}$ should be fixed to high level.

Read Cycle Timing Chart 2 ($\overline{\text{OE}}$ Controlled)

Note:

1. In read cycle, SC-CE2 and $\overline{\text{WE}}$ should be fixed to high level.

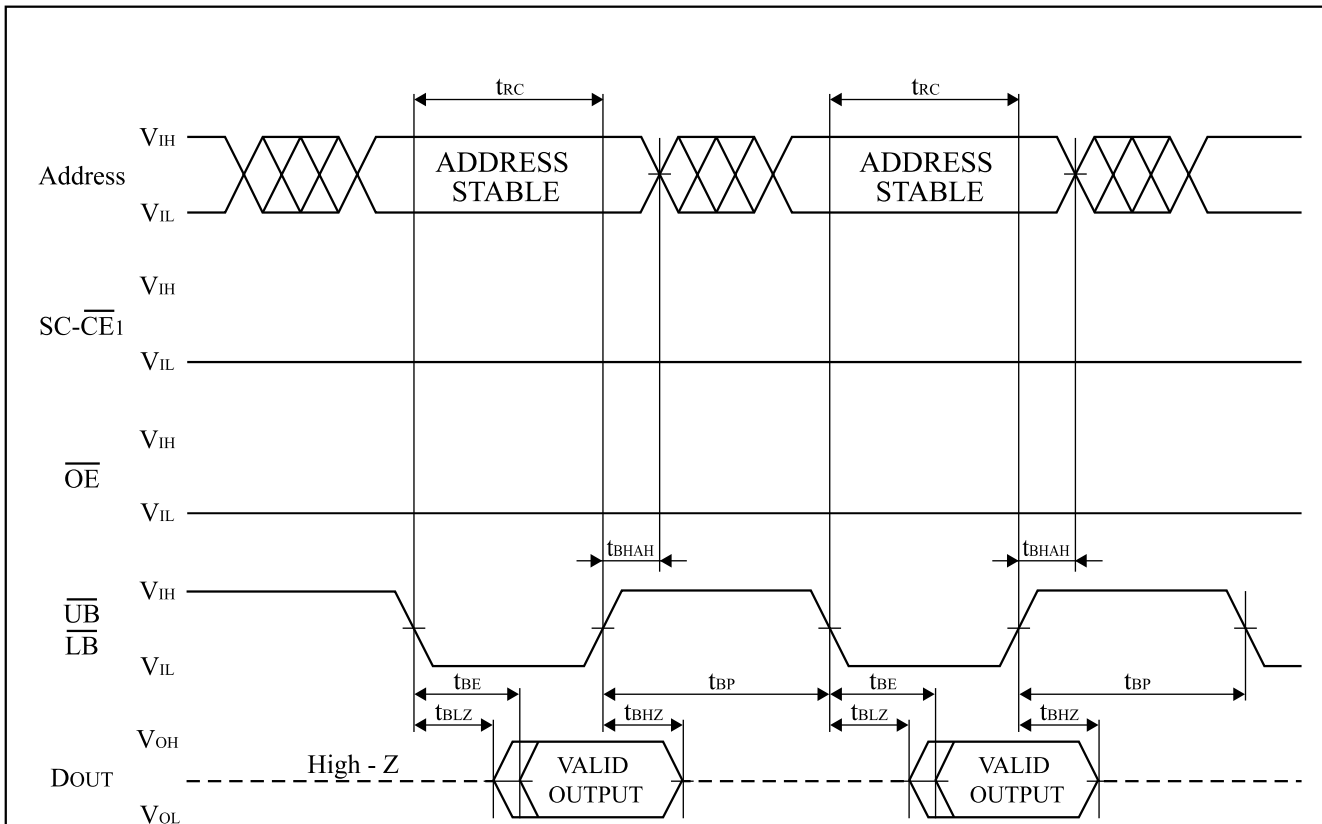
Read Cycle Timing Chart 4 (Address Controlled)



Notes:

1. In read cycle, SC-CE2 and \overline{WE} should be fixed to high level.
2. When read cycle time is less than t_{RC} (Min.), the address access time (t_{AA}) is not guaranteed.

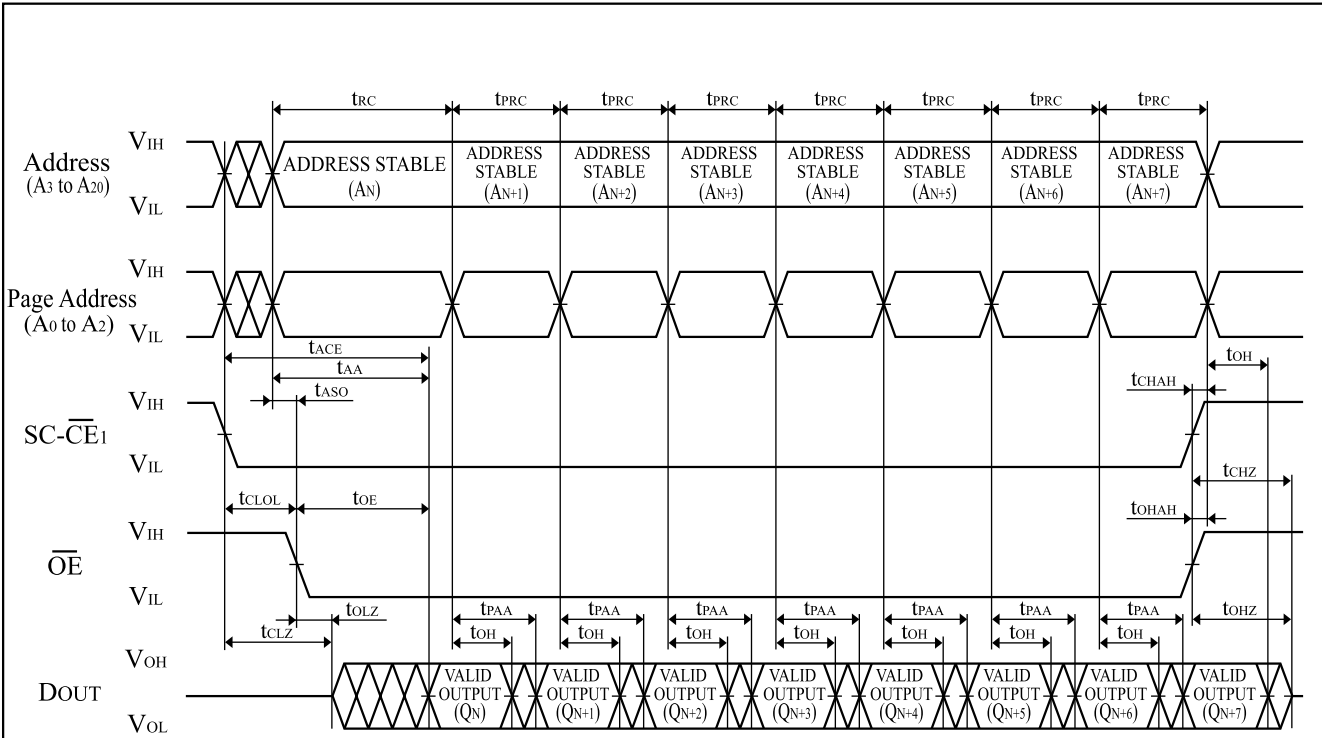
Read Cycle Timing Chart 5 ($\overline{\text{LB}} / \overline{\text{UB}}$ Controlled)



Note:

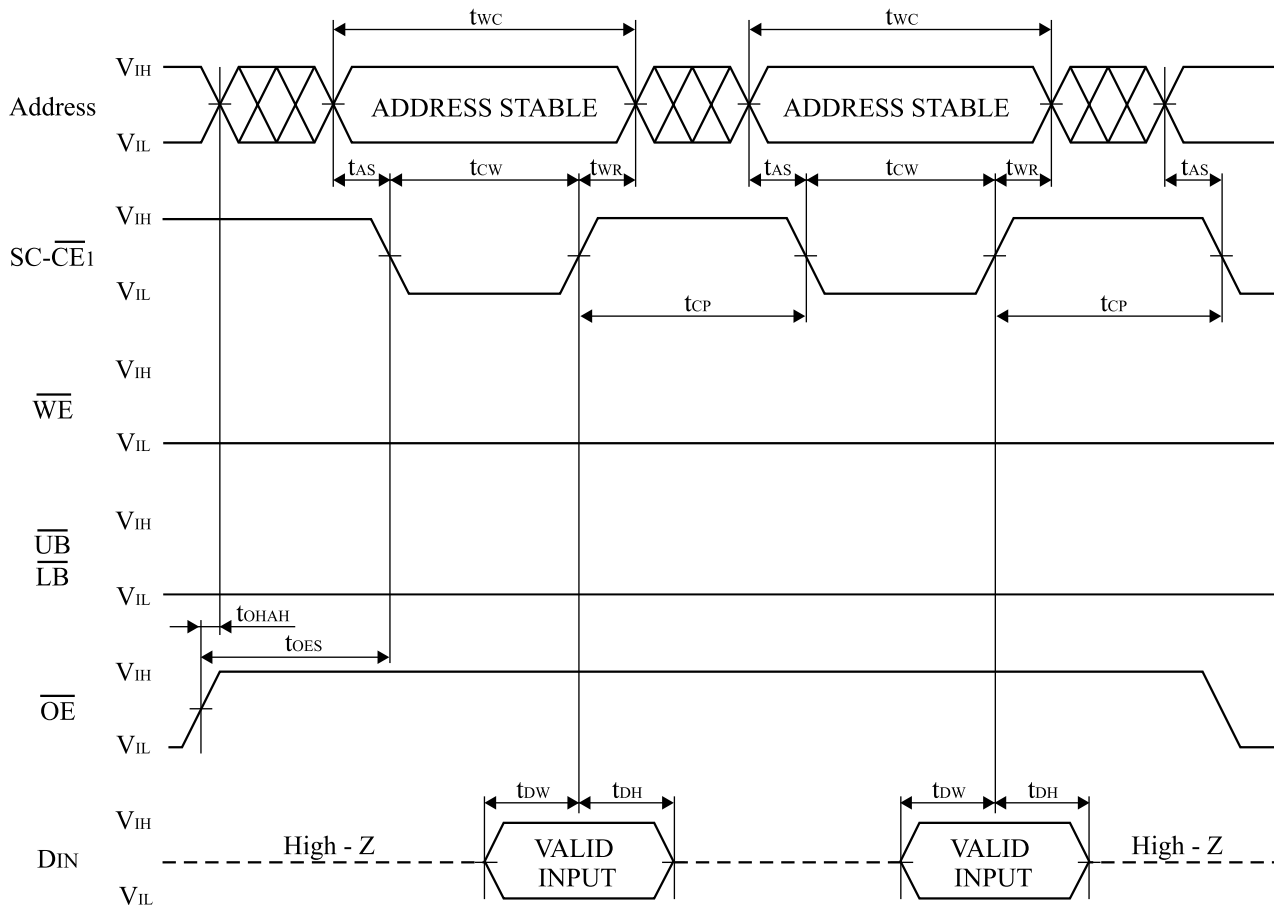
1. In read cycle, SC-CE2 and $\overline{\text{WE}}$ should be fixed to high level.

8 Word Page Read Cycle Timing Chart



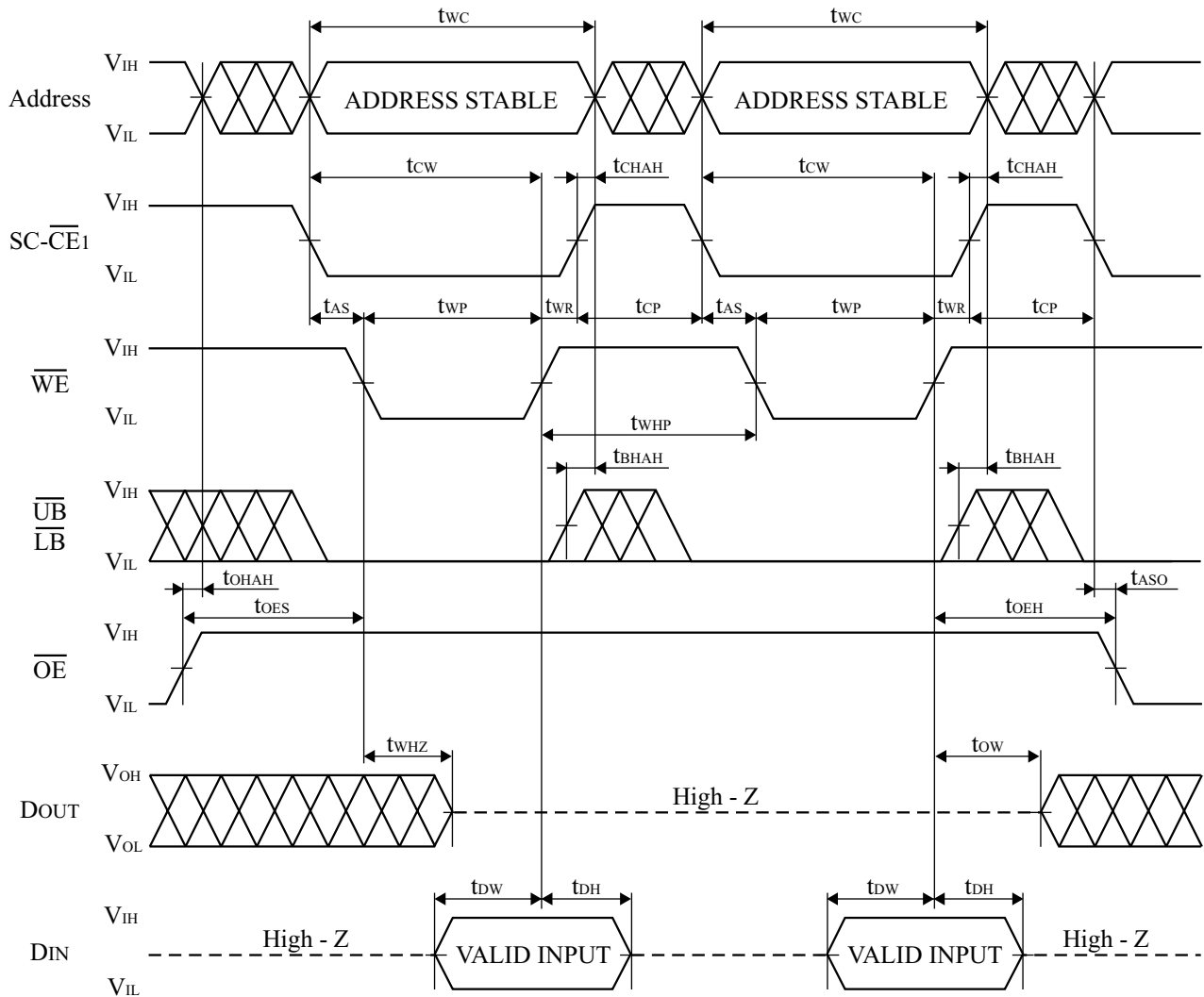
Notes:

1. In read cycle, SC-CE₂ and \overline{WE} should be fixed to high level.
2. \overline{LB} and \overline{UB} are Low level.

Write Cycle Timing Chart 1 (SC- $\overline{\text{CE}}_1$ Controlled)

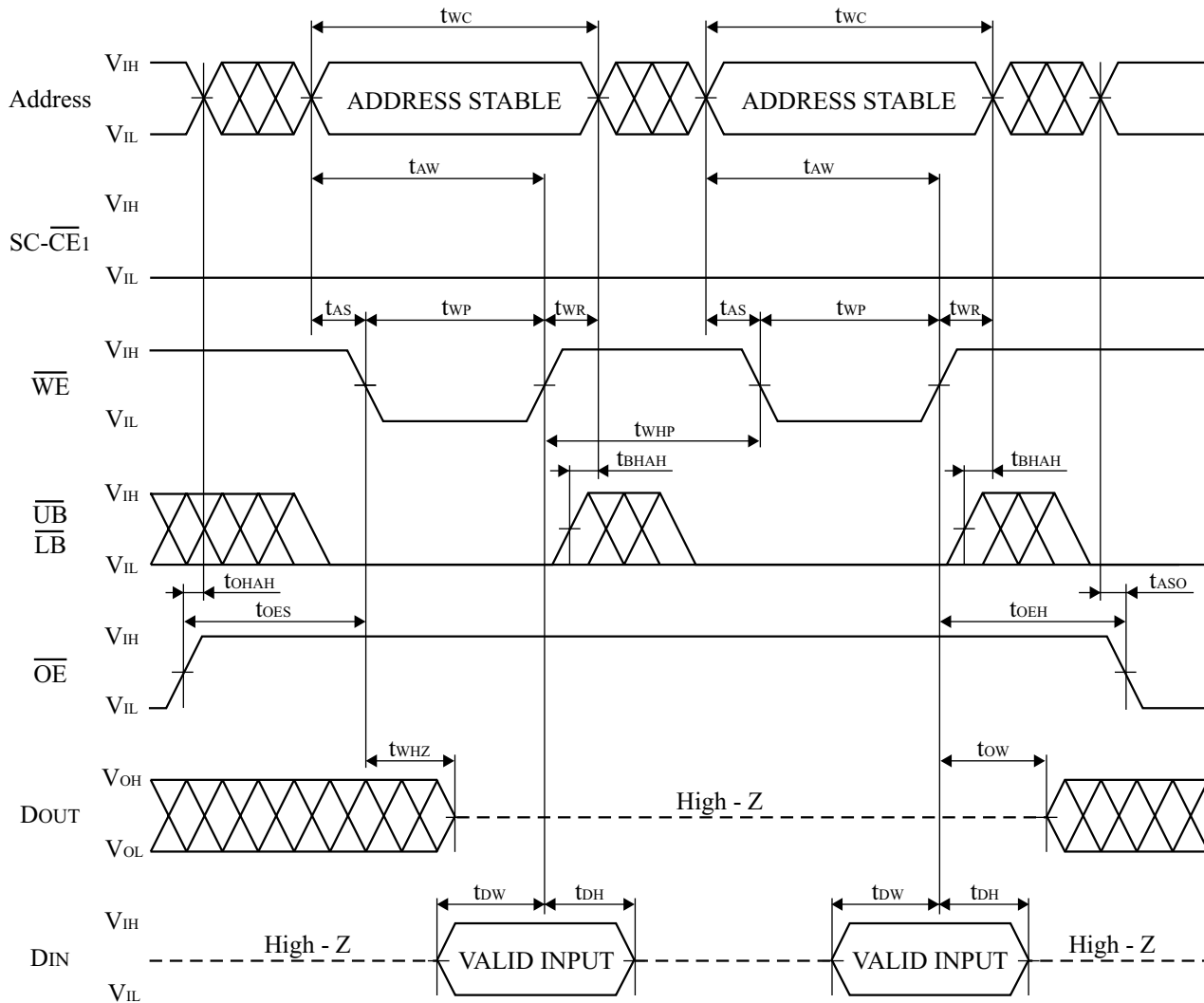
Notes:

1. During address transition, at least one of SC- $\overline{\text{CE}}_1$, $\overline{\text{WE}}$ or $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, SC-CE2 and $\overline{\text{OE}}$ should be fixed to high level.
4. Write operation is done during the overlap time of a low level SC- $\overline{\text{CE}}_1$, $\overline{\text{WE}}$, $\overline{\text{LB}}$ and/or $\overline{\text{UB}}$.

Write Cycle Timing Chart 2 ($\overline{\text{WE}}$ Controlled)

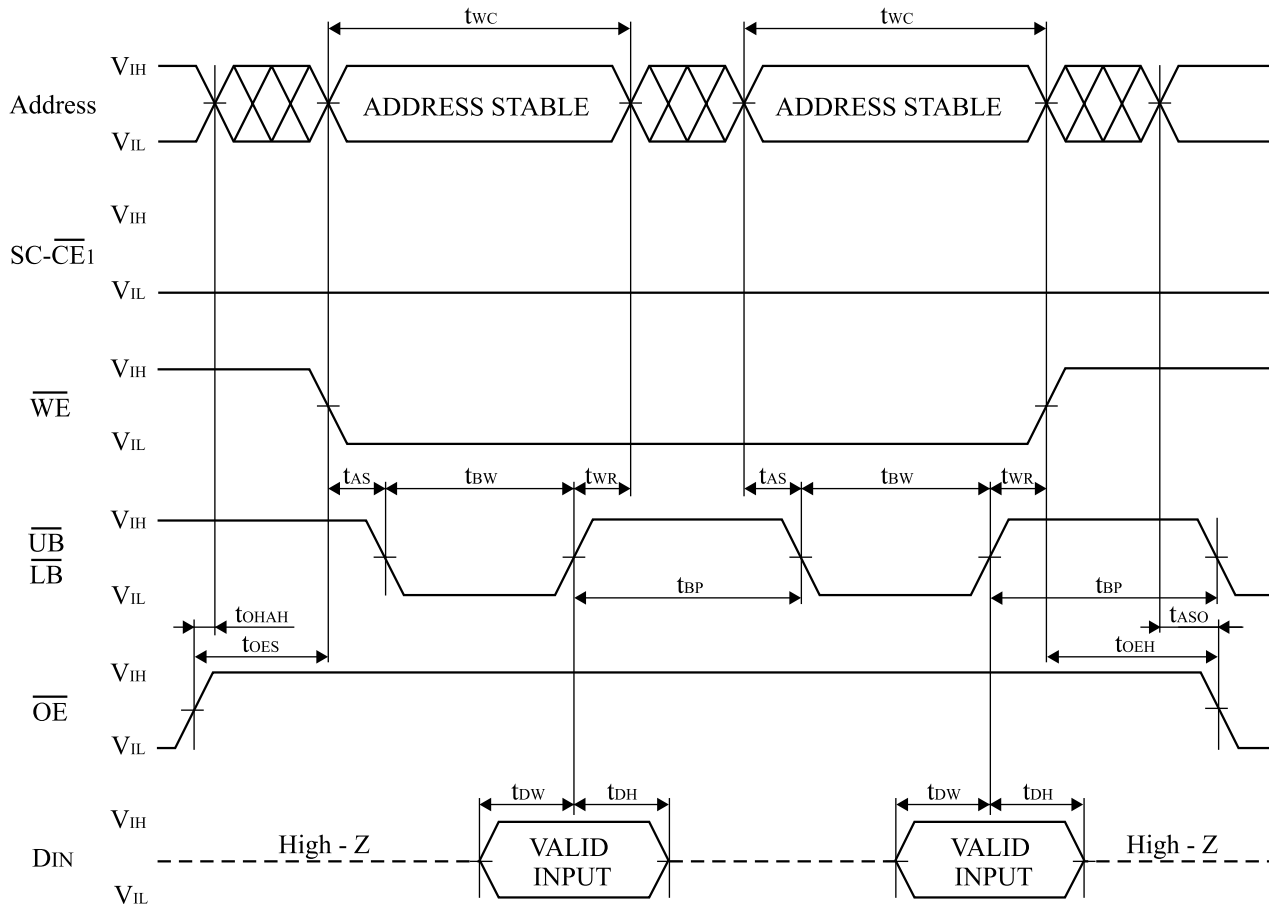
Notes:

1. During address transition, at least one of SC- $\overline{\text{CE}}_1$, $\overline{\text{WE}}$ or $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, SC-CE2 and $\overline{\text{OE}}$ should be fixed to high level.
4. Write operation is done during the overlap time of a low level SC- $\overline{\text{CE}}_1$, $\overline{\text{WE}}$, $\overline{\text{LB}}$ and/or $\overline{\text{UB}}$.

Write Cycle Timing Chart 3 ($\overline{\text{WE}}$ Controlled)

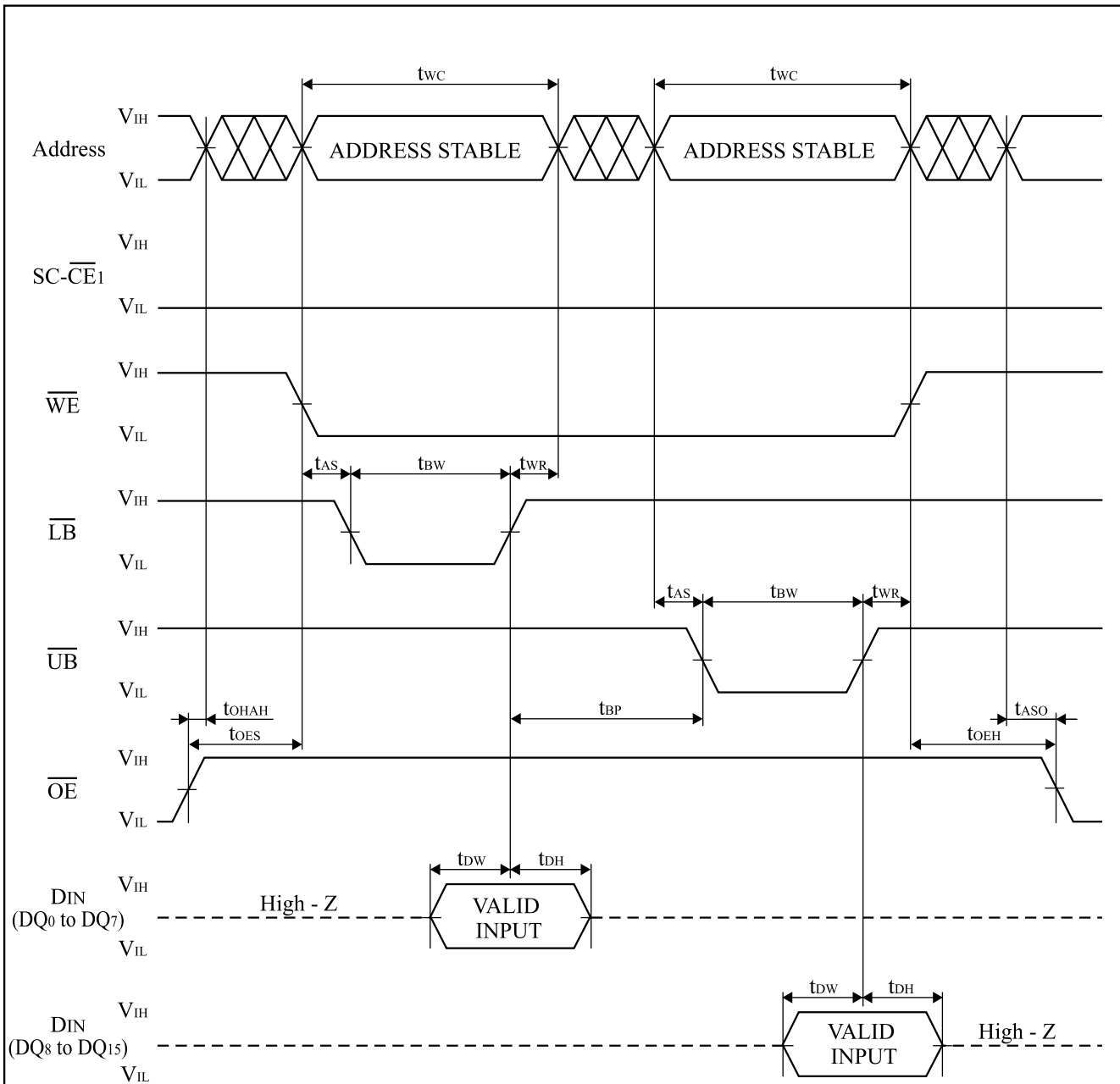
Notes:

1. During address transition, at least one of $\text{SC-}\overline{\text{CE}}_1$, $\overline{\text{WE}}$ or $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, SC-CE_2 and $\overline{\text{OE}}$ should be fixed to high level.
4. Write operation is done during the overlap time of a low level $\text{SC-}\overline{\text{CE}}_1$, $\overline{\text{WE}}$, $\overline{\text{LB}}$ and/or $\overline{\text{UB}}$.

Write Cycle Timing Chart 4 ($\overline{\text{LB}}/\overline{\text{UB}}$ Controlled)

Notes:

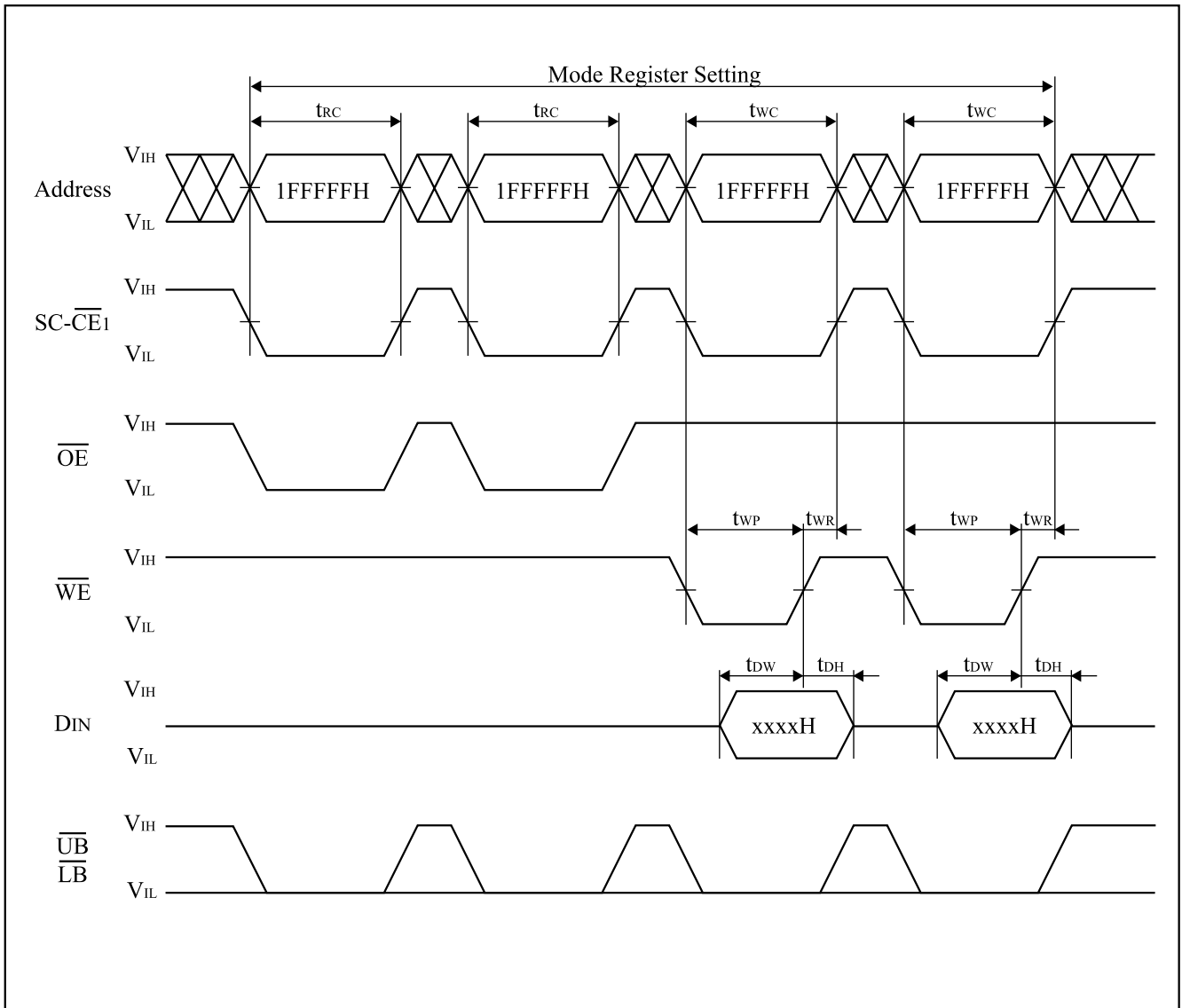
1. During address transition, at least one of $\text{SC-}\overline{\text{CE}}_1$, $\overline{\text{WE}}$ or $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, SC-CE_2 and $\overline{\text{OE}}$ should be fixed to high level.
4. Write operation is done during the overlap time of a low level $\text{SC-}\overline{\text{CE}}_1$, $\overline{\text{WE}}$, $\overline{\text{LB}}$ and/or $\overline{\text{UB}}$.

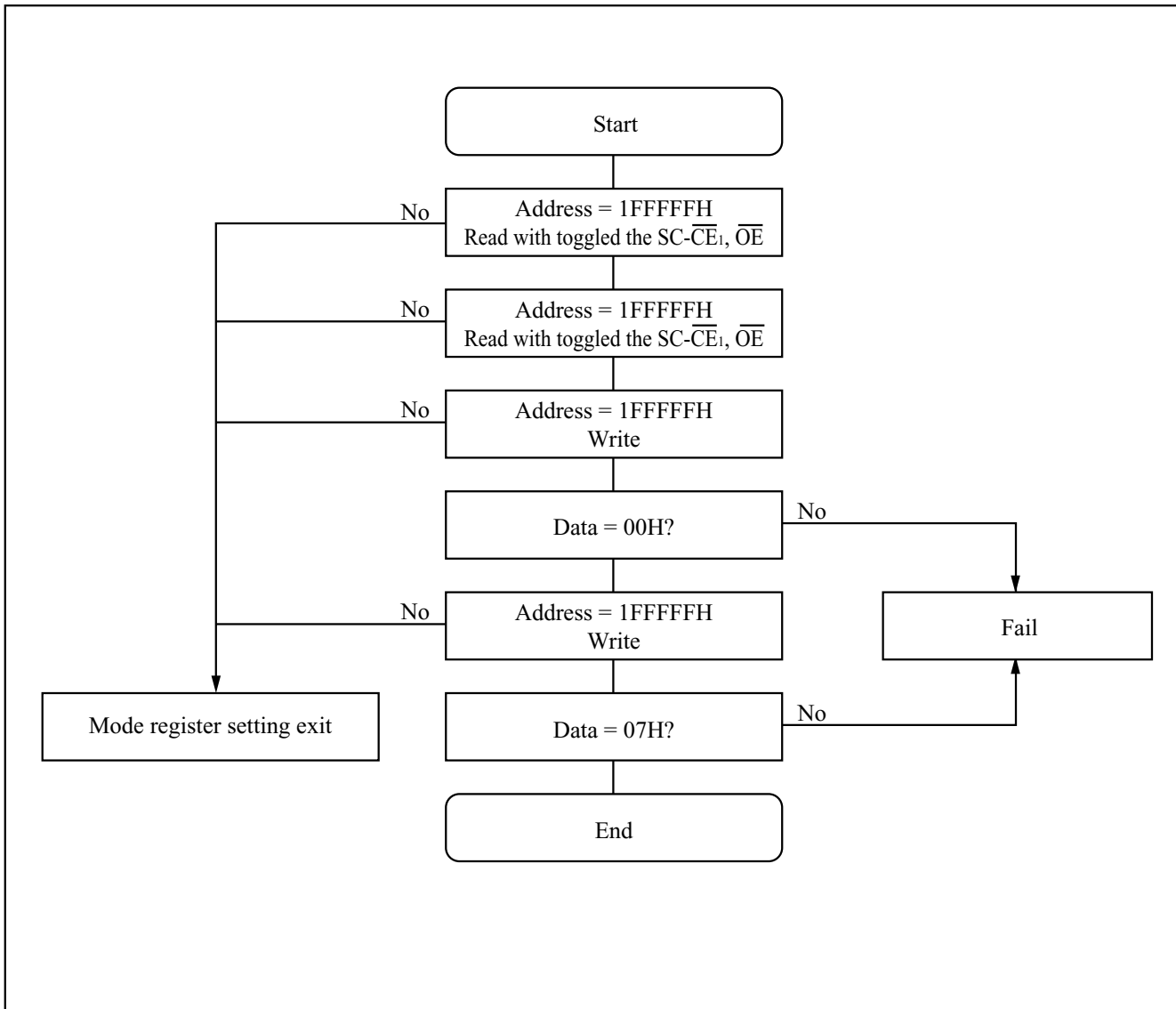
Write Cycle Timing Chart 5 ($\overline{\text{LB}}/\overline{\text{UB}}$ Independent Controlled)

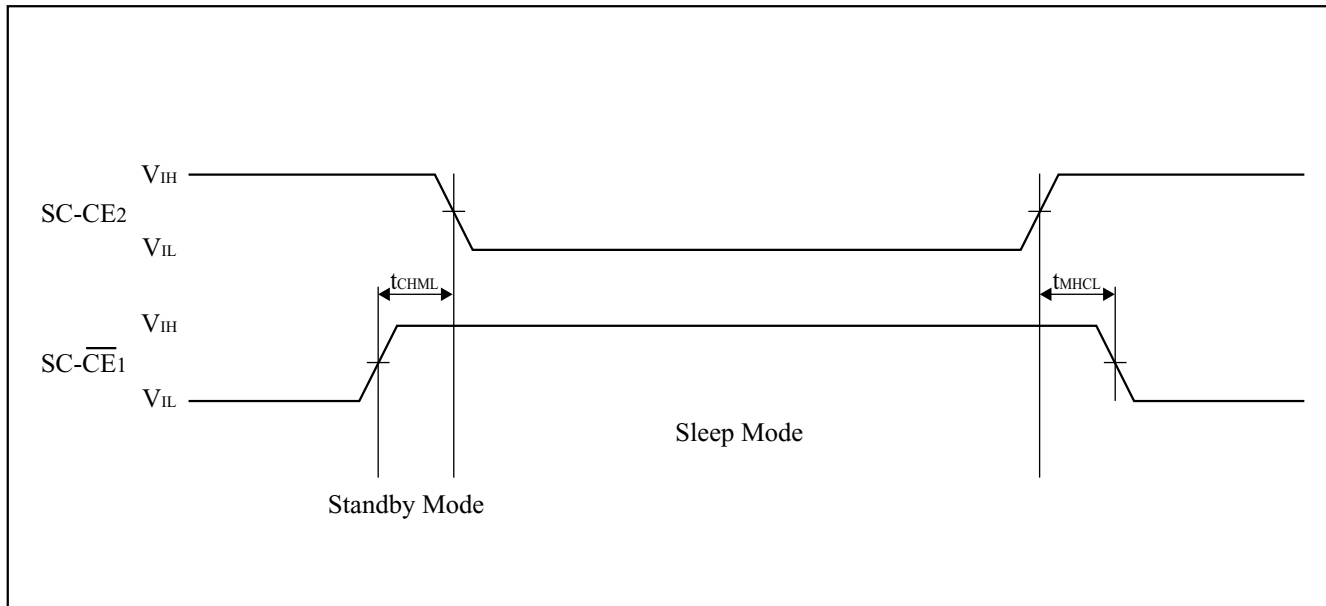
Notes:

1. During address transition, at least one of $\text{SC-}\overline{\text{CE}}_1$, $\overline{\text{WE}}$ or $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, $\text{SC-}\overline{\text{CE}}_2$ and $\overline{\text{OE}}$ should be fixed to high level.
4. Write operation is done during the overlap time of a low level $\text{SC-}\overline{\text{CE}}_1$, $\overline{\text{WE}}$, $\overline{\text{LB}}$ and/or $\overline{\text{UB}}$.

Mode Register Setting Timing Chart



Mode Register Setting Flow Chart

Sleep Mode Entry / Exit Timing Chart

7. Notes

This product is a stacked CSP package that a 128M (x16) bit Flash Memory, a 128M (x16) bit Flash Memory and 32M (x16) bit Smartcombo RAM are assembled into.

-Supply Power

Maximum difference (between F_1-V_{CC} , F_2-V_{CC} and $SC-V_{CC}$) of the voltage is less than 0.3V.

-Power Supply and Chip Enable of Flash Memory, Smartcombo RAM

Two or more chips among Flash memory (F_1 , F_2), Smartcombo RAM should not be active simultaneously.

If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.

Both F_1-V_{CC} , F_2-V_{CC} and $SC-V_{CC}$ are needed to be applied by the recommended supply voltage at the same time except Smartcombo RAM sleep mode.

-Power Up Sequence

When turning on Flash memory power supply, keep $F-\overline{RST}$ low. After F_1, F_2-V_{CC} reaches over 2.7V, keep $F-\overline{RST}$ low for more than 100 nsec.

-Device Decoupling

This is a 3 chips stacked CSP package. When one of the chips is active, others are in standby mode. Therefore, these power supplies should be designed very carefully.

Exclusive power supply pins for each Memory and GND pin need careful decoupling of devices. Especially, note Flash Memory and Smartcombo RAM peak current caused by transition of control signals.

When one of the Flash Memory is in busy mode, (page buffer) program, block erase and Bank erase command should not be inputted to the other (F_1-CE , F_2-CE , $SC-CE_1$, $SC-CE_2$).

8. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto \overline{WE} signal or power supply, may be interpreted as false commands and causes undesired memory updating. To protect the data stored in the flash memory against unwanted writing, systems operating with the flash memory should have the following write protect designs, as appropriate:

■ The below describes data protection method.

1. Protection of data in each block

- Any locked block by setting its block lock bit is protected against the data alternation. When \overline{WP}/A_{CC} is low, any locked- down block by setting its block lock-down bit is protected from lock status changes.
By using this function, areas can be defined, for example, program area (locked blocks), and data area (unlocked blocks).
- For detailed block locking scheme, see Section 6.2 Command Definitions for Flash Memory.

2. Protection of data with $F\text{-}\overline{RST}$

- Especially during power transitions such as power-up and power-down, the flash memory enters reset mode by bringing $F\text{-}\overline{RST}$ to low, which inhibits write operation to all blocks.
- For detailed description on $F\text{-}\overline{RST}$ control, see Section 6.6.6 AC Electrical Characteristics for Flash Memory, Reset Operations.

■ Protection against noises on \overline{WE} signal

To prevent the recognition of false commands as write commands, system designer should consider the method for reducing noises on \overline{WE} signal.

9. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory, Smartcombo RAM power switching characteristics, each device should have a 0.1 μ F ceramic capacitor connected between V_{CC} and GND, between \overline{WP}/A_{CC} and GND.

Low inductance capacitors should be placed as close as possible to package leads.

2. \overline{WP}/A_{CC} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the \overline{WP}/A_{CC} Power Supply trace. Use similar trace widths and layout considerations given to the V_{CC} power bus.

3. The Inhibition of Overwrite Operation

Please do not execute reprogramming "0" for the bit which has already been programmed "0". Overwrite operation may generate unerasable bit.

In case of reprogramming "0" to the data which has been programmed "1".

- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which has already been programmed "0".

For example, changing data from "1011110110111101" to "1010110110111100" requires "111011111111110" programming.

4. Power Supply

Block erase, bank erase, (page buffer) program with an invalid \overline{WP}/A_{CC} (See Chapter 6.5 DC Electrical Characteristics for Flash Memory) produce spurious results and should not be attempted.

Device operations at invalid V_{CC} voltage (See Chapter 6.5 DC Electrical Characteristics for Flash Memory, 7.2 DC Electrical Characteristics for Smartcombo RAM) produce spurious results and should not be attempted.

10. Related Document Information⁽¹⁾

Document No.	Document Name
FUM00701	LH28F320BF, LH28F640BF, LH28F128BF Series Appendix

Note:

1. International customers should contact their local SHARP or distribution sales offices.

12 Package and packing specification

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5~40°C
- Normal humidity : 80% R.H. max.

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

(1) Storage conditions for one-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

- Temperature : 5~25°C
- Humidity : 60% R.H. max.
- Period : 96 hours max. after opening.

(2) Storage conditions for two-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5~25°C
- Humidity : 60% R.H. max.
- Period : 96 hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5~25°C
- Humidity : 60% R.H. max.
- Period : 96 hours max. after completion of the 1st reflow.

*1:Air or nitrogen environment.

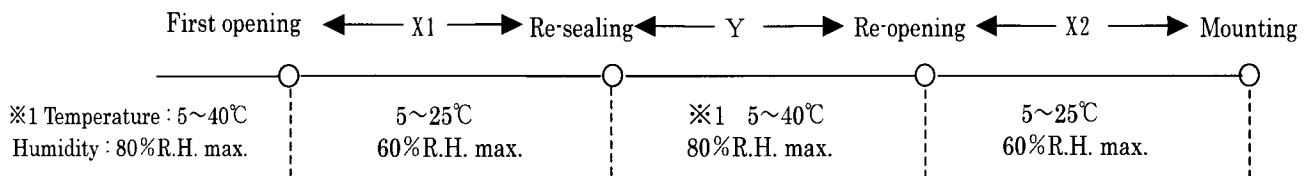
1-3.Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



(2) Storage period.

- X1 + X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
- Y : Two weeks max.

2. Baking Condition.

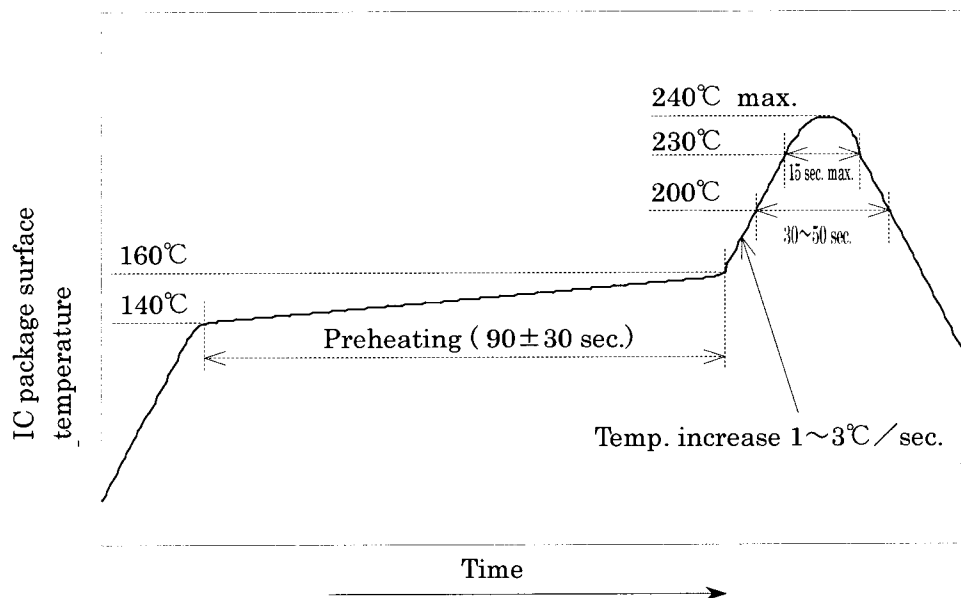
- (1) Situations requiring baking before mounting.
 - Storage conditions exceed the limits specified in Section 1-2 or 1-3.
 - Humidity indicator in the desiccant was already red (pink) when opened.
(Also for re-opening.)
- (2) Recommended baking conditions.
 - Baking temperature and period :
120+10/-0°C for 1~3 hours.
 - The above baking conditions apply since the trays are heat-resistant.
- (3) Storage after baking.
 - After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

3. Surface mount conditions.

The following soldering condition are recommended to ensure device quality.

3-1. Soldering.

- (1) Convection reflow or IR/Convection. (one-time soldering or two-time soldering in air or nitrogen environment)
 - Temperature and period :
 - Peak temperature of 240°C max., above 230°C for 15 sec. max.
 - Above 200°C for 30~50 sec.
 - Preheat temperature of 140~160°C for 90±30 sec.
 - Temperature increase rate of 1~3°C/sec.
 - Measuring point : IC package surface.
 - Temperature profile :



4. Condition for removal of residual flux.

- (1) Ultrasonic washing power : 25 watts / liter max.
- (2) Washing time : Total 1 minute max.
- (3) Solvent temperature : 15~40°C

5. Package outline specification.

Refer to the attached drawing.

6. Markings.

6-1. Marking details. (The information on the package should be given as follows.)

(1) Product name : LRS1830

(2) Company name : S

(3) Date code

(Example) YY WW XXX

→ Denotes the production ref. code (1~3 digits).

→ Denotes the production week. (01 · 02 · ~ · 52 · 53)

→ Denotes the production year. (Last two digits of the year.)

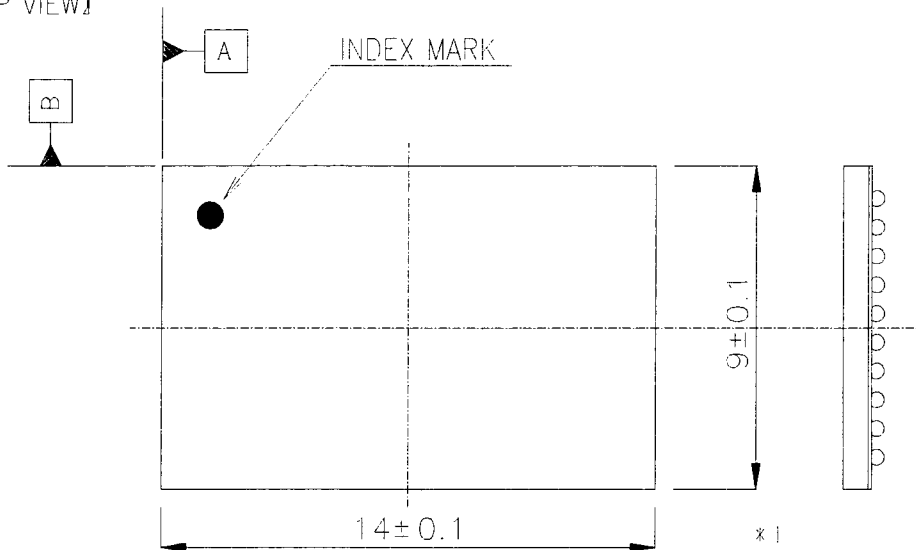
6-2. Marking layout.

The layout is shown in the attached drawing.

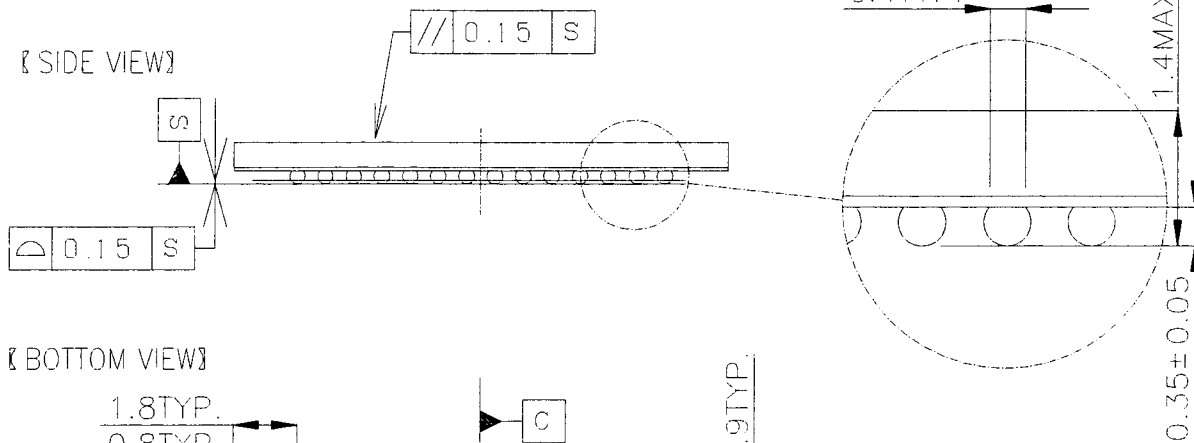
(However, this layout does not specify the size of the marking character and marking position.)

矩形タイプ
Rectangle type

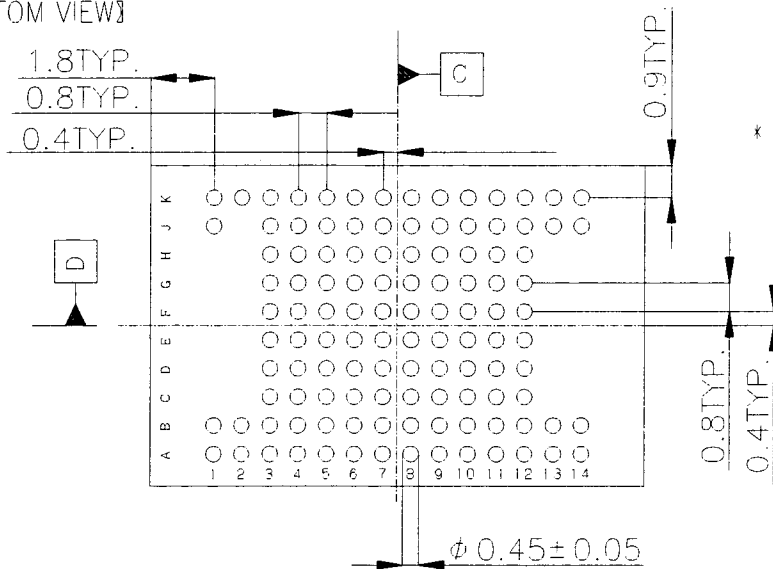
【TOP VIEW】



【SIDE VIEW】



【BOTTOM VIEW】



*1 LAND HOLE DIAMETER FOR BALL MOUNTING

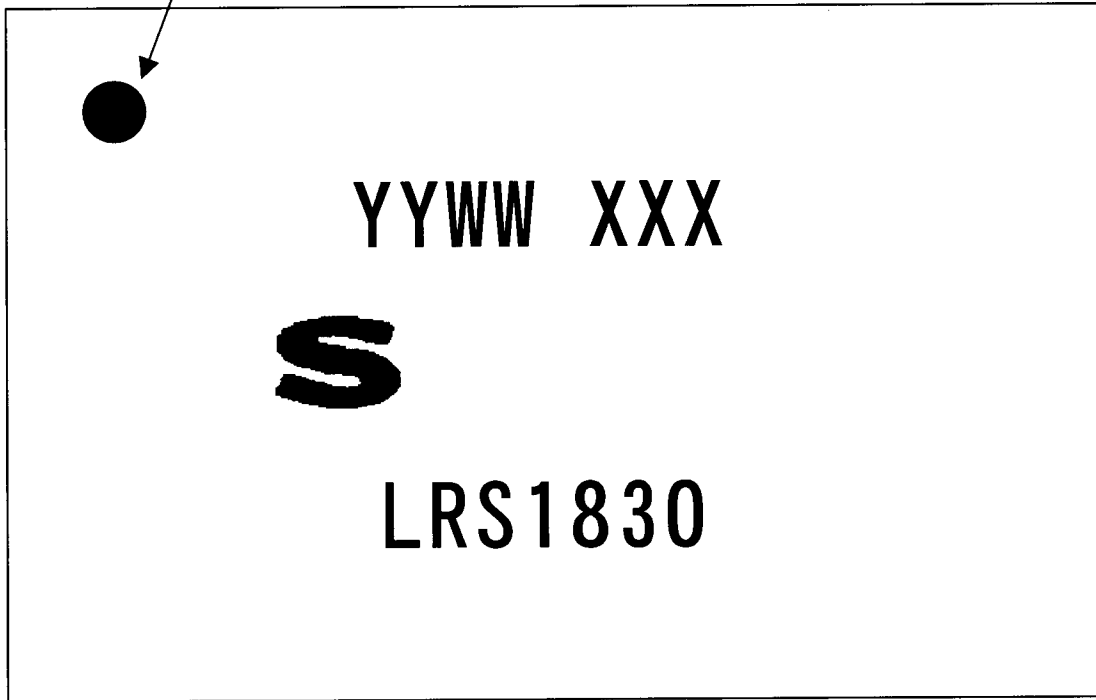
⊕	φ0.30	(M)	S	AB
⊕	φ0.15	(M)	S	CD

名称 NAME	LFBGA115-P-0914 (LCSP115-P-0914)			備考
DRAWING NO.	AA2232	単位 UNIT	mm	NOTE

矩形タイプ
Rectangle type

マークイメーヅ☒
Marking image

INDEX MARK



7.Packing Specifications (Dry packing for surface mount packages.)

7-1.Packing materials.

Material name	Material specifications	Purpose
Inner carton	Cardboard (1440 devices / inner carton max.)	Packing the devices. (10 trays / inner carton)
Tray	Conductive plastic (144 devices / tray)	Securing the devices.
Upper cover tray	Conductive plastic (1 tray / inner carton)	Securing the devices.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity, and packed date.
PP band	Polypropylene (3 pcs. / inner carton)	Securing the devices.
Outer carton	Cardboard (5760 devices / outer carton max.)	Outer packing.

(Devices must be placed on the tray in the same direction.)

7-2.Outline dimension of tray.

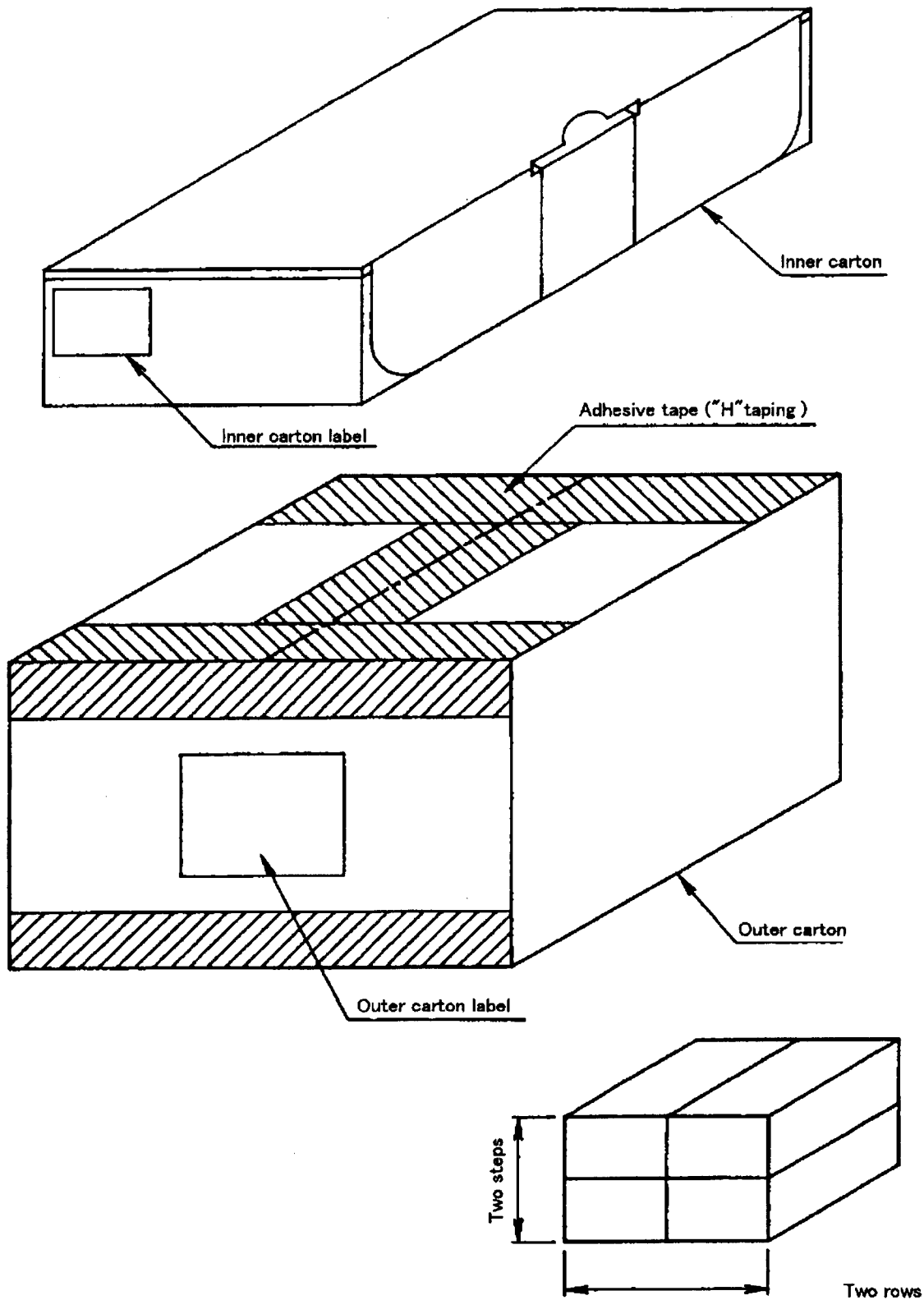
Refer to the attached drawing.

7-3.Outline dimension of carton.

Refer to the attached drawing.

8. Precautions for use.

- (1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.
- (2) The trays have undergone either conductive or anti-ESD treatment.
If another tray is used, make sure it has also undergone conductive or anti-ESD treatment.
- (3) The devices should be mounted the devices within one year of the date of delivery.



L × W × H

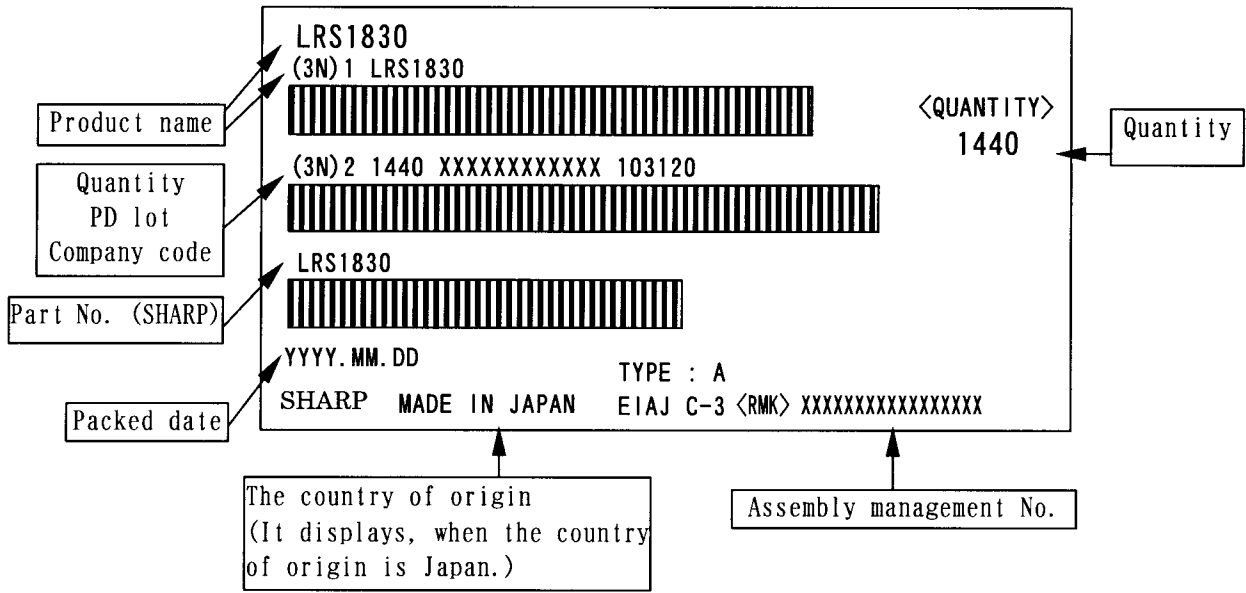
Inner carton - Outer dimensions : 348×152×90

Outer carton - Outer dimensions : 350×335×215

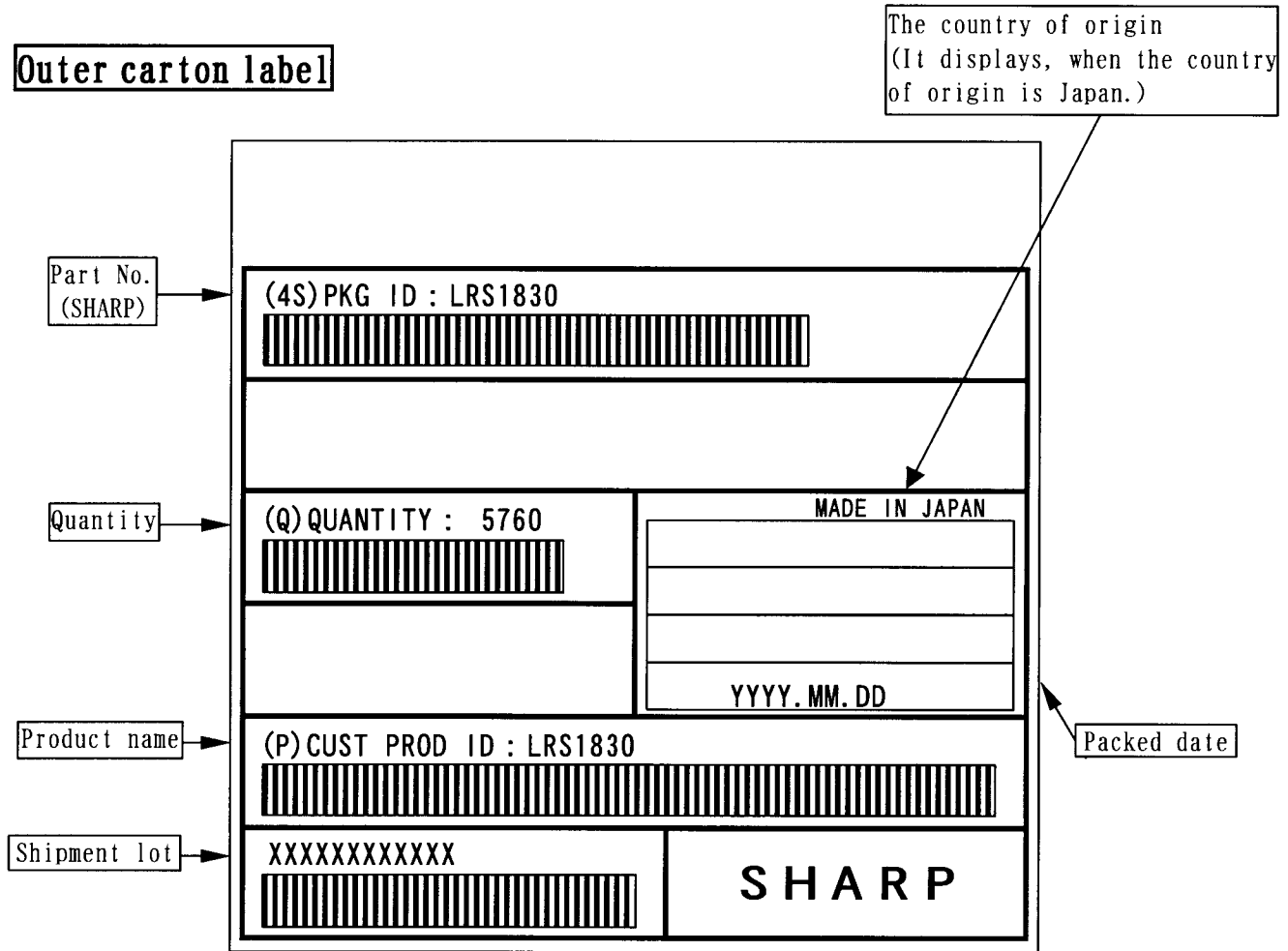
名称 NAME	トレイ品 包装仕様 Packing specifications		
DRAWING NO.	BJ433J	単位 UNIT	mm

備考 出荷数量が端数の場合、本仕様と異なることがあります。
NOTE There is a possibility different from this specification when the number of shipments is fractions.

Inner carton label



Outer carton label

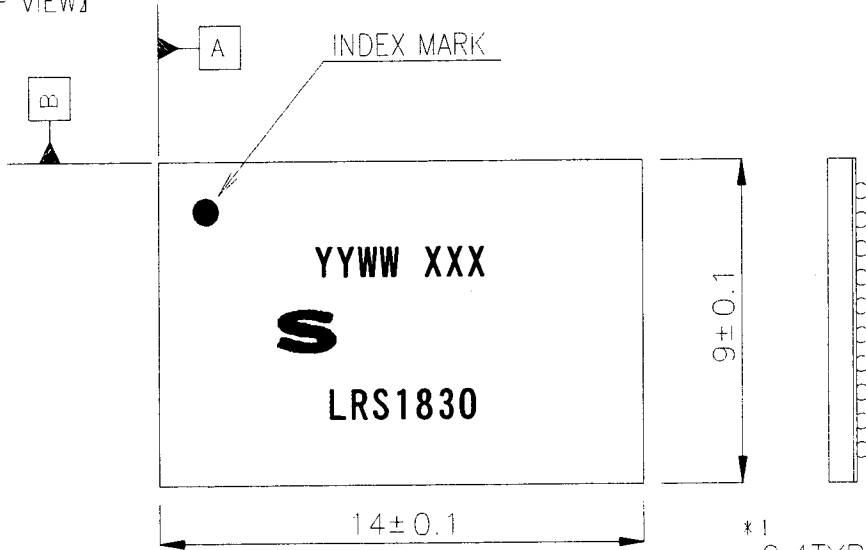


(Former) EIAJ B Standard conforming

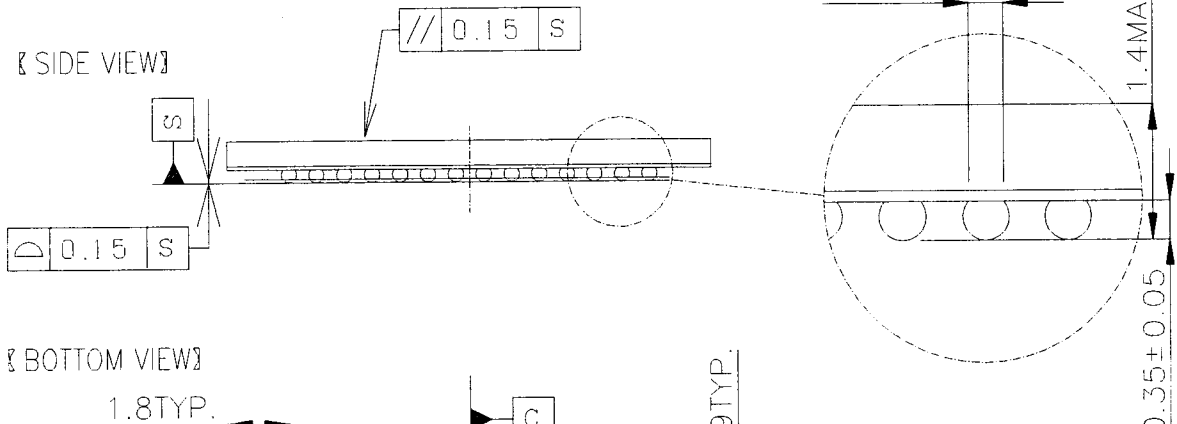
イメージ図 (Image)

矩形タイプ
Rectangle type

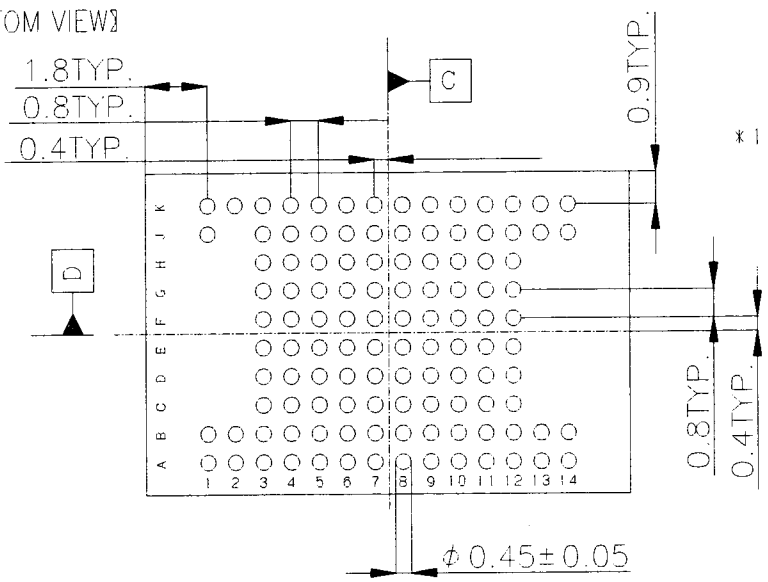
【 TOP VIEW 】



【 SIDE VIEW 】



【 BOTTOM VIEW 】



*1 LAND HOLE DIAMETER FOR BALL MOUNTING

⊕	φ0.30	(M)	S	AB
⊕	φ0.15	(M)	S	CD

名称 NAME	LFBGA115-P-0914 (LCSP115-P-0914)			備考
DRAWING NO.	AA2232	単位 UNIT	mm	NOTE

LRS1830 Flash MEMORY ERRATA

1. AC Characteristics**PROBLEM**

The table below summarizes the AC characteristics.

AC Characteristics - Write Operations

$$V_{CC}=2.7V-3.1V$$

Page	Symbol	Parameter	Min.	Max.	Unit
25	t_{AVAV}	Write Cycle Time	75		ns
25	t_{WHWL} (t_{EHEL})	F- \overline{WE} (F- \overline{CE}) Pulse Width High	25		ns

WORKAROUND

System designers should consider these specifications.

STATUS

This is intended to be fixed in future devices.

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

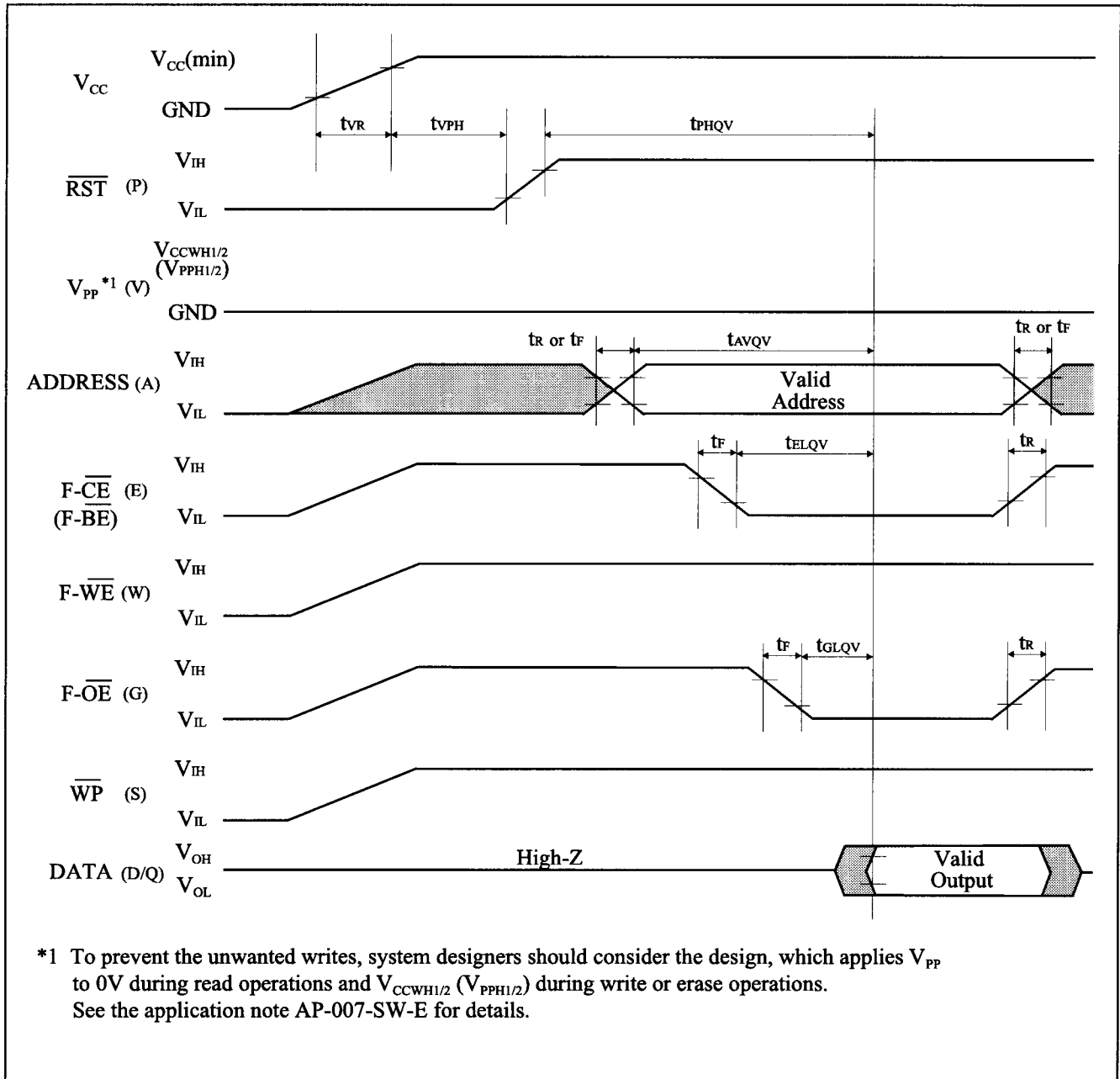


Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR} , t_R , t_F in the figure, refer to the next page. See the “AC Electrical Characteristics for Flash Memory” described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	V_{CC} Rise Time	1	0.5	30000	$\mu\text{s/V}$
t_R	Input Signal Rise Time	1, 2		1	$\mu\text{s/V}$
t_F	Input Signal Fall Time	1, 2		1	$\mu\text{s/V}$

NOTES:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

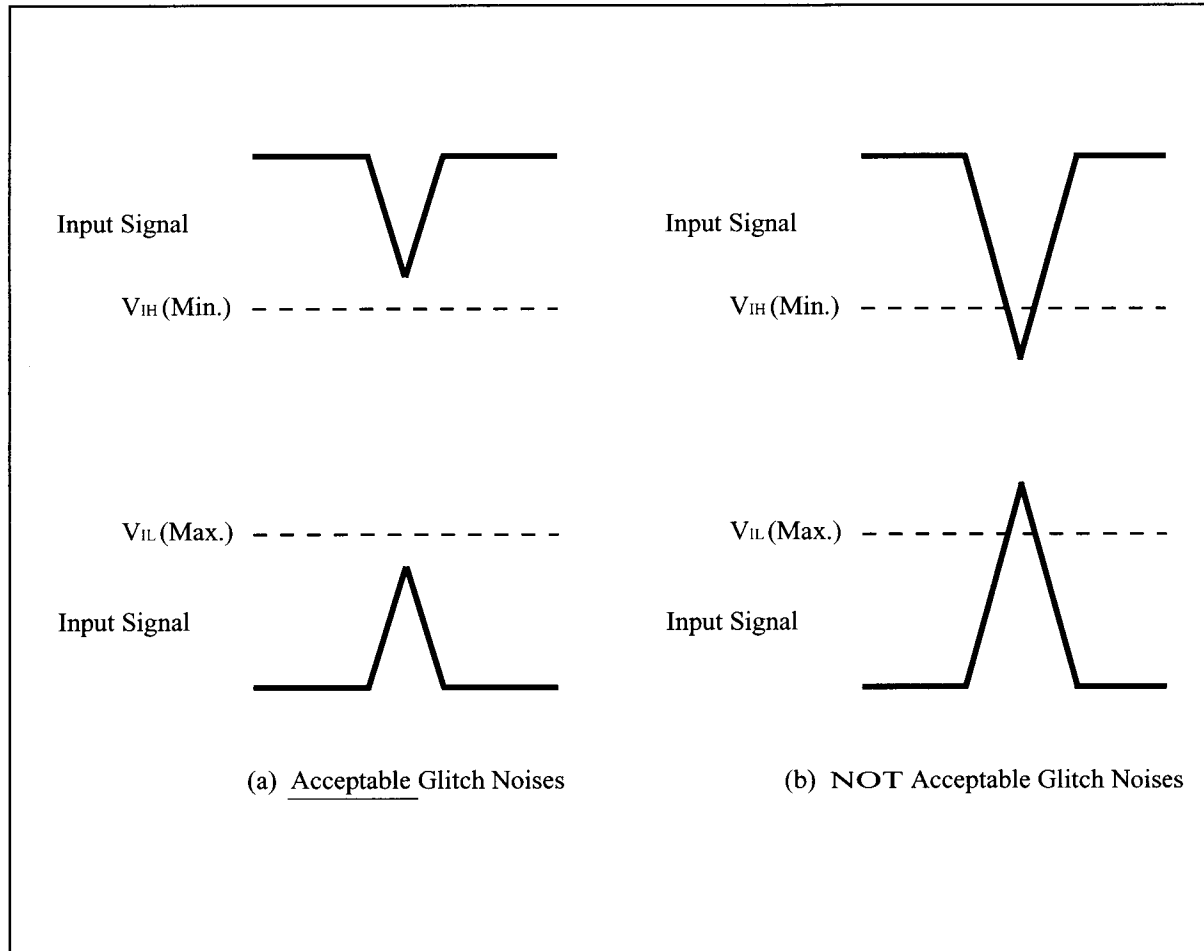


Figure A-2. Waveform for Glitch Noises

See the “DC Electrical Characteristics” described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION⁽¹⁾

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{pp} Electric Potential Switching Circuit

NOTE:

1. International customers should contact their local SHARP or distribution sales office.

A-3 STATUS REGISTER READ OPERATIONS

If AC timing for reading the status register described in specifications is not satisfied, a system processor can check the status register bit SR.15 instead of SR.7 to determine when the erase or program operation has been completed.

Table A-3-1. Status Register Definition (SR.15 and SR.7)

		NOTES:
SR.15 = WRITE STATE MACHINE STATUS: (DQ ₁₅)	1 = Ready in All Partitions 0 = Busy in Any Partition	SR.15 indicates the status of WSM (Write State Machine). If SR.15="0", erase or program operation is in progress in any partition.
SR.7 = WRITE STATE MACHINE STATUS FOR EACH PARTITION: (DQ ₇)	1 = Ready in the Addressed Partition 0 = Busy in the Addressed Partition	

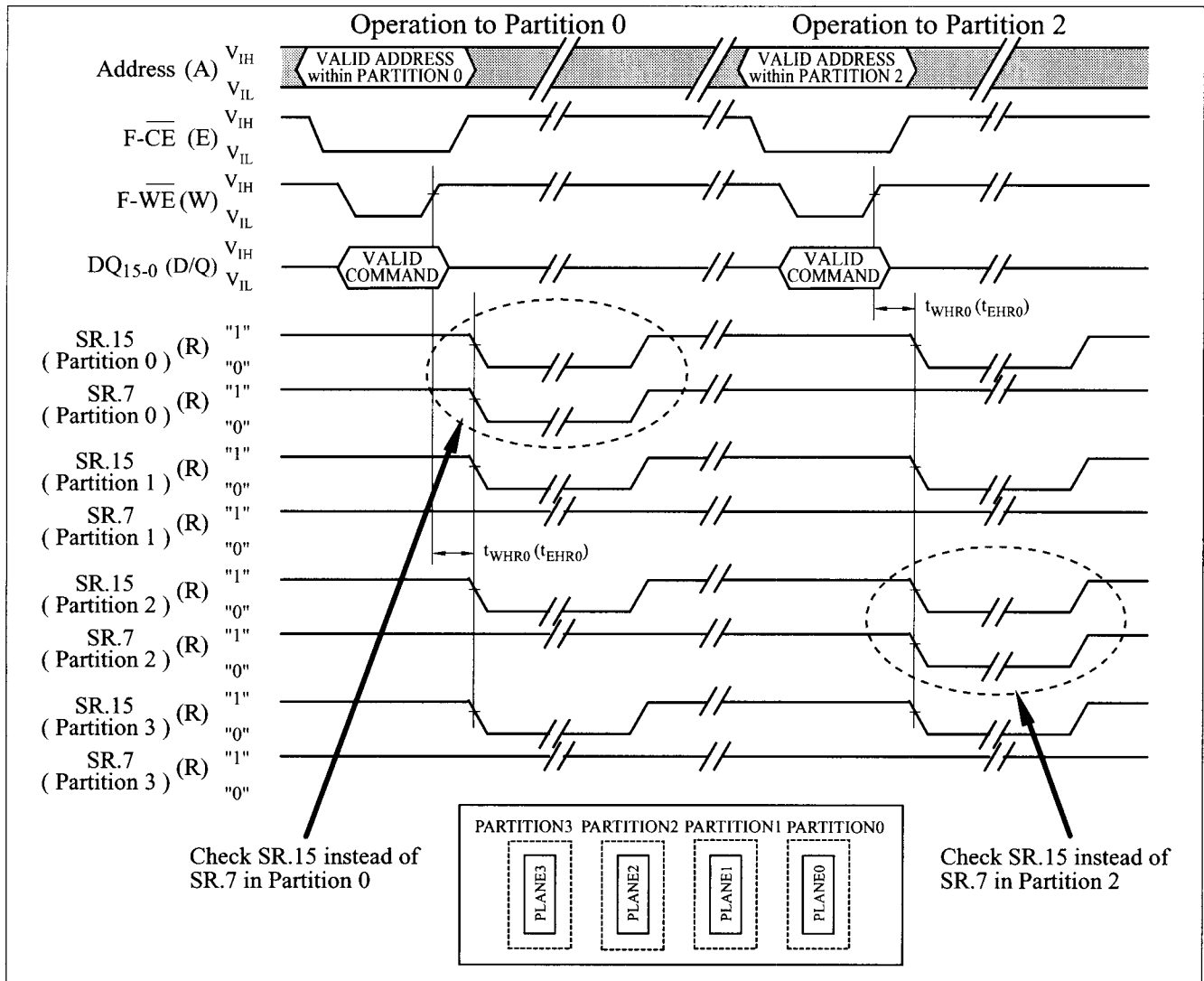


Figure A-3-1. Example of Checking the Status Register
(In this example, the device contains four partitions.)

B-1 POWER UP SEQUENCE OF Smartcombo RAM

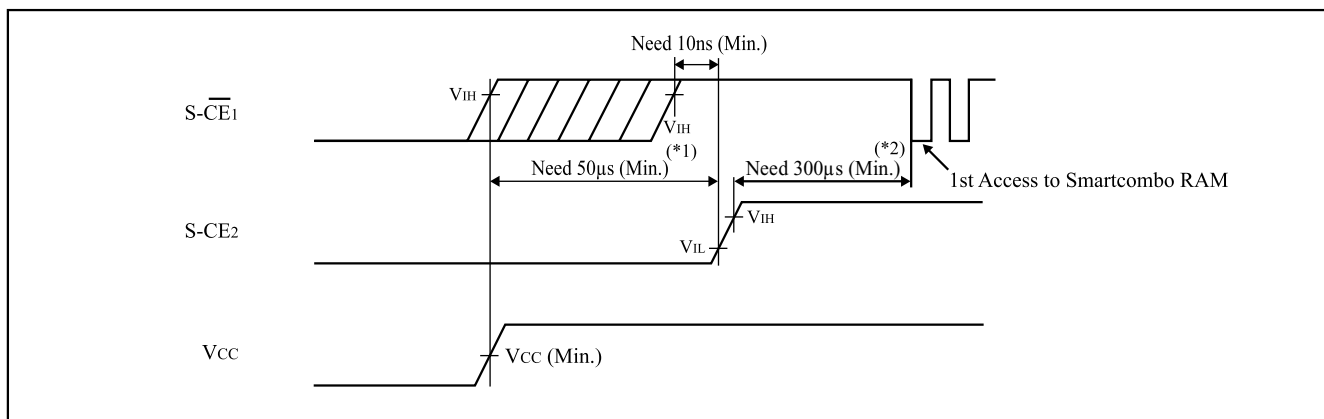
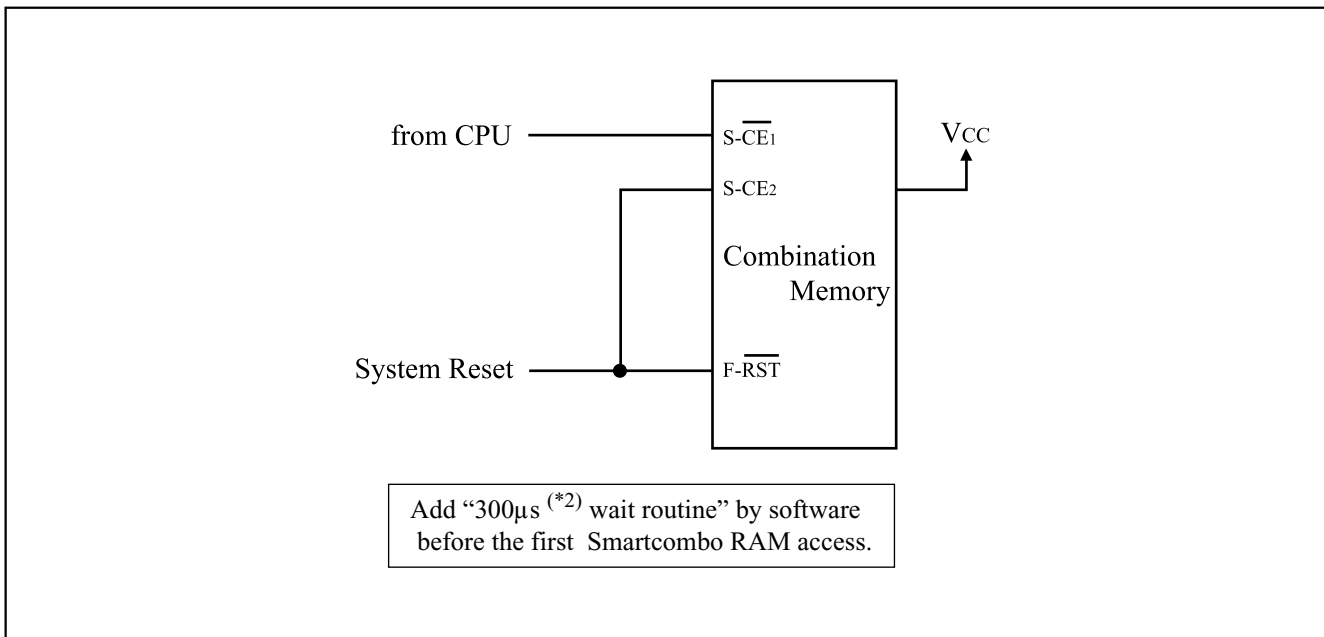
When turning on Smartcombo RAM power supply, the following sequence is needed.

B-1.1 Sequence of Smartcombo RAM Power Supply

- (1) Supply power.
- (2) Keep S-CE₂ low longer than or equal to 50μs. (See NOTES *1)
- (3) Keep S- $\overline{\text{CE}}_1$ and S-CE₂ high longer than or equal to 300μs. (See NOTES *2)
- (4) End of Initialization.

By executing above (1) to (4), the initialization of chip inside and the power occurred inside become stable.

<Example of the actual connection>



NOTES:

- *1) Connect System Reset signal to S-CE₂ and hold S-CE₂ low longer than or equal to 50μs.
- *2) By adding "300μs Wait Routine" (S- $\overline{\text{CE}}_1$ and S-CE₂ high) in the software, delay the first access to Smartcombo RAM longer than or equal to 300μs.

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