

LRS1337

Stacked Chip

32M Flash Memory and 4M SRAM

(Model No.: LRS1337)

Spec No.: MFM2-J11504A
Issue Date: June 21, 1999

- Handle this document carefully for it contains material protected by international copyright law. Any reproduction, full or in part, of this material is prohibited without the express written permission of the company.

- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.
 - (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
 - Office electronics
 - Instrumentation and measuring equipment
 - Machine tools
 - Audiovisual equipment
 - Home appliances
 - Communication equipment other than for trunk lines

 - (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
 - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
 - Mainframe computers
 - Traffic control systems
 - Gas leak detectors and automatic cutoff devices
 - Rescue and security equipment
 - Other safety devices and safety equipment, etc.

 - (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
 - Aerospace equipment
 - Communications equipment for trunk lines
 - Control equipment for the nuclear power industry
 - Medical equipment related to life support, etc.

 - (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

- Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

1. Description	2
2. Pin Configuration	3
3. Truth Table	4
4. Block Diagram	4
5. Command Definitions for Flash Memory	5
6. Status Register Definition	7
7. Memory Map for Flash Memory	8
8. Absolute Maximum Ratings	9
9. Recommended DC Operating Conditions	9
10. Pin Capacitance	9
11. DC Electrical Characteristics	10
12. AC Electrical Characteristics (Flash Memory)	12
13. AC Electrical Characteristics (SRAM)	19
14. Data Retention Characteristics for SRAM	23
15. Notes	24
16. Flash Memory Data Protection	25
17. Design Consideration	26

Part 1 Overview

1. Description

The LRS1337 is a combination memory organized as 2,097,152×16 bit flash memory and 262,144×16 bit static RAM in one package.

Features

- Power supply 2.7 V to 3.6 V
- Operating temperature -25 °C to +85 °C
- Not designed or rated as radiation hardened
- 72 pin CSP (LCSP072-P-0811) plastic package
- Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon.

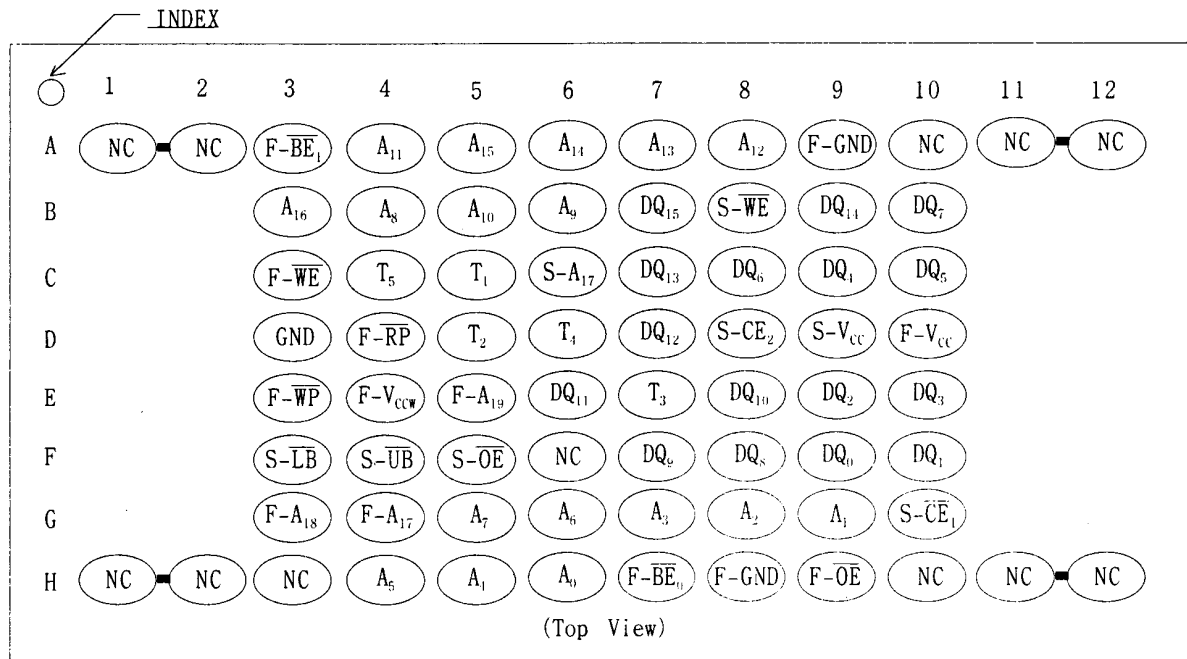
Flash Memory

- Access Time 90 ns (Max.)
- Operating current (The current for F-V_{CC} pin and F-V_{CCW} pin)
 - Read 25 mA (Max. t_{CYCLE}=200ns)
 - Word write 57 mA (Max.)
 - Block erase 42 mA (Max.)
- Standby current (The current for F-V_{CC} pin) 20 μA (Max. F-V_{CCW} ≤ 0.2V
F-BE, F-RP ≥ F-V_{CC} - 0.2V)
- Optimized Array Blocking Architecture for each Bank.
 - Two 4k-word Boot Blocks
 - Six 4k-word Parameter Blocks
 - Thirty-one 32k-word Main Blocks
 - Bottom Boot Location
- Extended Cycling Capability
 - 100,000 Block Erase Cycles
- Enhanced Automated Suspend Options
 - Word Write Suspend to Read
 - Block Erase Suspend to Word Write
 - Block Erase Suspend to Read

SRAM

- Access Time 85 ns (Max.)
- Operating current 45 mA (Max.)
 - 8 mA (Max. t_{RC}, t_{WC}=1 μs)
- Standby current 15 μA (Max.)
- Data retention current 15 μA (Max. V_{CCDR}=3.0V)

2. Pin Configuration



Note: Two pins of corner are connected.
From T₁ to T₅ are needed to be open.

Pin	Description	Type
A ₀ to A ₁₆	Address Inputs (Common)	Input
F-A ₁₇ to F-A ₁₉	Address Inputs (Flash)	Input
S-A ₁₇	Address Input (SRAM)	Input
F-BE ₀ , F-BE ₁	Bank Enable Inputs(Flash)	Input
S-CE ₁ , S-CE ₂	Chip Enable Inputs(SRAM)	Input
F-WE	Write Enable Input (Flash)	Input
S-WE	Write Enable Input (SRAM)	Input
F-OE	Output Enable Input(Flash)	Input
S-OE	Output Enable Input (SRAM)	Input
S-LB	SRAM Byte Enable Input(DQ ₀ to DQ ₇)	Input
S-UB	SRAM Byte Enable Input(DQ ₈ to DQ ₁₅)	Input
F-RP	Reset Power Down Input (Flash) Block erase and Write : V _{IH} Read : V _{IH} Reset Power Down : V _{IL}	Input
F-WP	Write Protect Input (Flash) Two Boot Blocks Locked : V _{IL}	Input
DQ ₀ to DQ ₁₅	Data Inputs and Outputs (Common)	Input/Output
F-V _{cc}	Write, Erase Power Supply(Flash)	Power
S-V _{cc}	Power Supply(SRAM)	Power
F-V _{ccw}	Write, Erase Power Supply(Flash) Block Erase and Write : F-V _{ccw} = V _{ccwLK} All Blocks Locked : F-V _{cc} < V _{ccwLK}	Power
F-GND	GND (Flash)	Power
GND	GND (Common)	Power
NC	Non Connection	-
T ₁ to T ₅	Test pins(Should be open)	-

3. Truth Table (*1)

Flash	SRAM	Note	F-BE _{0,1}	F-RP	F-OE	F-WE	S-CE ₁	S-CE ₂	S-OE	S-WE	S-LB	S-UB	DQ ₀ to DQ ₁₅
Read	Standby	*3, 5, 6	L	H	L	H	*7		X	X	*7		Dout
Output Disable		*5, 6			H	H							High-Z
Write		*2, 3, 4, 5, 6			L	L							Din
Standby	Read		H	H	X	X	L	H	L	H	*8		High-Z
	Output Disable								H	H	X	X	
	Write								X	X	H	H	
Reset Power Down	Read		X	L	X	X	L	H	L	H	*8		High-Z
	Output Disable								H	H	X	X	
	Write								X	X	H	H	
Standby	Standby	*5	H	H	X	X	*7		X	X	*7		High-Z
Reset Power Down		*5	X	L									

Notes) *1. L=V_{IL}, H=V_{IH}, X=H or L. Refer to DC Characteristics.

*2. Command writes involving block erase, bank erase, word write or lock-bit configuration are reliably executed when F-V_{CCW}=V_{CCWH} and F-V_{CC}=2.7V to 3.6V.

*3. Never hold F-OE low and F-WE low at the same timing.

*4. Refer Section 5. Flash Memory Comand Definition for valid DIN during a write operation.

*5. F-WP set to V_{IL} or V_{IH}.

*6. Both F-BE₀ and F-BE₁ must not be low at the same time.

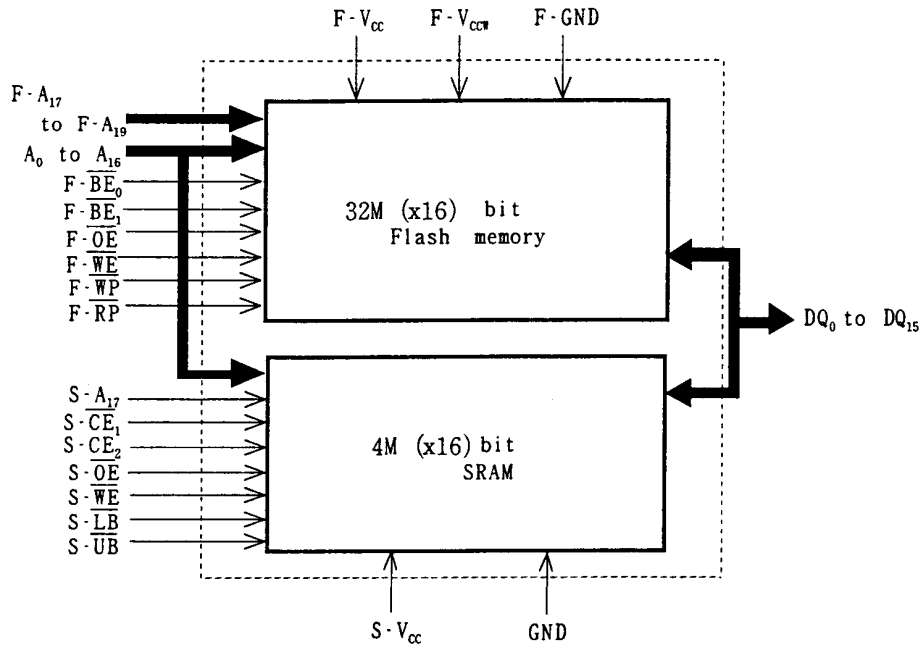
*7) SRAM Standby Mode

Mode	Pin			
	S-CE ₁	S-CE ₂	S-LB	S-UB
Standby (SRAM)	H	X	X	X
	X	L	X	X
	X	X	H	H

*8) S-LB, S-UB Control Mode

Mode (SRAM)	S-LB	S-UB	DQ ₀ to DQ ₇	DQ ₈ to DQ ₁₅
Read/Write	L	L	Dout/Din	Dout/Din
	L	H	Dout/Din	High-Z
	H	L	High-Z	Dout/Din

4. Block Diagram



5 Command Definitions for Flash Memory (*1)

Command	Bus Cycles Req'd.	Note	First Bus Cycle			Second Bus Cycle		
			Oper(*2)	Address (*3)	Data (*3)	Oper(*2)	Address (*3)	Data (*3)
Read Array/Reset	1		Write	XA	FFH			
Read Identifier Codes	≥ 2	*4	Write	XA	90H	Read	IA	ID
Read Status Register	2		Write	XA	70H	Read	XA	SRD
Clear Status Register	1		Write	XA	50H			
Block Erase	2	*5	Write	BA	20H	Write	BA	DOH
Bank Erase	2		Write	XA	30H	Write	XA	DOH
Word Write	2	*5	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word Write Suspend	1	*5	Write	XA	B0H			
Block Erase and Word Write Resume	1	*5	Write	XA	D0H			
Set Block Lock-Bits	2	*7	Write	BA	60H	Write	BA	01H
Clear Block Lock-Bits	2	*6,7	Write	XA	60H	Write	XA	DOH
Set Permanent Lock-Bits	2	*8	Write	XA	60H	Write	XA	F1H

Note)

- *1. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.
- *2. BUS operations are defined in 3. Truth Table.
- *3. XA=Any valid address within the device.
IA=Identifier Code Address.
BA=Address within the block being erased.
WA=Address of memory location to be written.
SRD=Data read from status register. See the next section "Status Register Definition"
WD=Data to be written at location WA. Data is latched on the rising edge of $\overline{F-WE}$ or $\overline{F-BE}$ [$\overline{F-BE_0}$, $\overline{F-BE_1}$] (whichever goes high first).
ID=Data read from identifier codes.
- *4. See Identifier Codes at the next page.
- *5. See Write Protection Alternatives at the next page.
- *6. The clear block lock-bits operation simultaneously clears all block lock-bits.
- *7. If the permanent lock-bit is set, Set Block Lock-Bit and Clear Block Lock-Bits commands can not be done.
- *8. Once the permanent lock-bit is set, it cannot be cleared.

Identifier Codes

Codes		Address [A ₁₉ -A ₀]	Data [DQ ₁₅ -DQ ₀]
Manufacture Code		00000H	00B0H
Device Code		00001H	00E1H
Block Lock Configuration	Unlocked	BA ^(*) +2	DQ ₀ =0 (*2)
	locked	BA ^(*) +2	DQ ₀ =1 (*2)
Permanent Lock Configuration	Unlocked	00003H	DQ ₀ =0 (*2)
	locked	00003H	DQ ₀ =1 (*2)

NOTE: 1. BA selects the specific block lock configuration code to be read.
 2. DQ₁₅-DQ₁ are reserved for future use.

Write Protection Alternatives

Operation	F-V _{CCW}	F- \overline{RP}	Permanent Lock-Bit	Block Lock-Bit	F- \overline{WP}	Effect
Block Erase or Word Write	$\leq V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$> V_{CCWLK}$	V _{IL}	X	X	X	All Blocks Locked.
		V _{IH}	X	0	V _{IL}	2 Boot Blocks Locked.
					V _{IH}	Block Erase and Word Write Enabled.
		1	V _{IL}	Block Erase and Word Write Disabled.		
V _{IH}	Block Erase and Word Write Disabled.					
Bank Erase	$\leq V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$> V_{CCWLK}$	V _{IL}	X	X	X	All Blocks Locked.
		V _{IH}	X	X	V _{IL}	All Unlocked Blocks are Erased. 2 Boot Blocks and Locked Blocks are NOT Erased.
					V _{IH}	All Unlocked Blocks are Erased. Locked Blocks are NOT Erased.
Set Block Lock-Bit	$\leq V_{CCWLK}$	X	X	X	X	Set Block Lock-Bit Disabled.
	$> V_{CCWLK}$	V _{IL}	X	X	X	Set Block Lock-Bit Disabled.
		V _{IH}	0	X	X	Set Block Lock-Bit Enabled.
			1	X	X	Set Block Lock-Bit Disabled.
Clear Block Lock-Bits	$\leq V_{CCWLK}$	X	X	X	X	Clear Block Lock-Bits Disabled.
	$> V_{CCWLK}$	V _{IL}	X	X	X	Clear Block Lock-Bits Disabled.
		V _{IH}	0	X	X	Clear Block Lock-Bits Enabled.
			1	X	X	Clear Block Lock-Bits Disabled.
Set Permanent Lock-Bit	$\leq V_{CCWLK}$	X	X	X	X	Set Permanent Lock-Bit Disabled.
	$> V_{CCWLK}$	V _{IL}	X	X	X	Set Permanent Lock-Bit Disabled.
		V _{IH}	X	X	X	Set Permanent Lock-Bit Enabled.

6. Status Register Definition

WSMS	BESS	ECBLBS	WWSLBS	VCCWS	WSS	DPS	R
7	6	5	4	3	2	1	0

<p>S R . 7 = WRITE STATE MACHINE STATUS(W S M S) 1 = Ready 0 = Busy</p> <p>S R . 6 = BLOCK ERASE SUSPEND STATUS(B E S S) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed</p> <p>S R . 5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS(E C B L B S) 1 = Error in Block Erase, Bank Erase or Clear Block Lock-Bits 0 = Successful Block Erase, Bank Erase or Clear Block Lock-Bits</p> <p>S R . 4 = WORD WRITE AND SET LOCK-BIT STATUS (W W S L B S) 1 = Error in Word Write or Set Block /Permanent Lock-Bit 0 = Successful Word Write or Set Block /Permanent Lock-Bits</p> <p>S R . 3 = V_{CCW} STATUS (V C C W S) 1 = V_{CCW} Low Detect, Operation Abort 0 = V_{CCW} OK</p> <p>S R . 2 = WORD WRITE SUSPENDED STATUS (W W S S) 1 = Word Write Suspended 0 = Word Write in Progress/Completed</p> <p>S R . 1 = DEVICE PROTECT STATUS (D P S) 1 = Block Lock-Bits, Permanent Lock-Bit and/or F-\overline{WP} Lock Detected, Operation Abort 0 = Unlock</p> <p>S R . 0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p>	<p>NOTES:</p> <p>Check SR.7 to determine block erase, bank erase, word write or lock-bit configuration completion. SR.6-0 are invalid while SR.7="0".</p> <p>If both SR.5 and SR.4 are "1"s after a block erase, bank erase or lock-bit configuration attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of F-V_{CCW} level. The WSM interrogates and indicates the F-V_{CCW} level only after Block Erase, Bank Erase, Word Write or Lock-Bit Configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when F-V_{CCW} ≠ F-V_{CCW1/2}.</p> <p>SR.1 does not provide a continuous indication of permanent and block lock-bit and F-\overline{WP} values. The WSM interrogates the permanent lock-bit, block lock-bit and F-\overline{WP} only after Block Erase, Bank Erase, Word Write or Lock-Bit Configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, permanent lock-bit is set and/or F-\overline{WP} is F-V_{IL}. Reading the block lock and permanent lock configuration codes after writing the Read Identifier Codes command indicates permanent and block lock-bit status.</p> <p>SR.0 is reserved for future use and should be masked out when polling the status register.</p>
-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

7. Memory Map for Flash Memory

Memory Map

Address

[A₁₉-A₀]

FFFF		
F8000	32K-word Main Block	30
F7FFF	32K-word Main Block	29
F0000	32K-word Main Block	28
EFFFF	32K-word Main Block	27
E8000	32K-word Main Block	26
E7FFF	32K-word Main Block	25
E0000	32K-word Main Block	24
DFFFF	32K-word Main Block	23
D8000	32K-word Main Block	22
D7FFF	32K-word Main Block	21
D0000	32K-word Main Block	20
CFFFF	32K-word Main Block	19
C8000	32K-word Main Block	18
C7FFF	32K-word Main Block	17
C0000	32K-word Main Block	16
BFFFF	32K-word Main Block	15
B8000	32K-word Main Block	14
B7FFF	32K-word Main Block	13
B0000	32K-word Main Block	12
AFFFF	32K-word Main Block	11
A8000	32K-word Main Block	10
A7FFF	32K-word Main Block	9
A0000	32K-word Main Block	8
9FFFF	32K-word Main Block	7
98000	32K-word Main Block	6
97FFF	32K-word Main Block	5
90000	32K-word Main Block	4
8FFFF	32K-word Main Block	3
88000	32K-word Main Block	2
87FFF	32K-word Main Block	1
80000	32K-word Main Block	0
7FFFF		
78000		
77FFF		
70000		
6FFFF		
68000		
67FFF		
60000		
5FFFF		
58000		
57FFF		
50000		
4FFFF		
48000		
47FFF		
40000		
3FFFF		
38000		
37FFF		
30000		
2FFFF		
28000		
27FFF		
20000		
1FFFF		
18000		
17FFF		
10000		
0FFFF		
08000		
07FFF	4K-word Parameter Boot Block	5
07000	4K-word Parameter Boot Block	4
06FFF	4K-word Parameter Boot Block	3
06000	4K-word Parameter Boot Block	2
05FFF	4K-word Parameter Boot Block	1
05000	4K-word Parameter Boot Block	0
04FFF		
04000		
03FFF		
03000		
02FFF		
02000		
01FFF	4K-word Boot Block	1
01000	4K-word Boot Block	0
00FFF		
00000		

Bottom Boot

Bank0

(F- \overline{BE}_0 ="L", F- \overline{BE}_1 ="H")

Address

[A₁₉-A₀]

FFFF		
F8000	32K-word Main Block	30
F7FFF	32K-word Main Block	29
F0000	32K-word Main Block	28
EFFFF	32K-word Main Block	27
E8000	32K-word Main Block	26
E7FFF	32K-word Main Block	25
E0000	32K-word Main Block	24
DFFFF	32K-word Main Block	23
D8000	32K-word Main Block	22
D7FFF	32K-word Main Block	21
D0000	32K-word Main Block	20
CFFFF	32K-word Main Block	19
C8000	32K-word Main Block	18
C7FFF	32K-word Main Block	17
C0000	32K-word Main Block	16
BFFFF	32K-word Main Block	15
B8000	32K-word Main Block	14
B7FFF	32K-word Main Block	13
B0000	32K-word Main Block	12
AFFFF	32K-word Main Block	11
A8000	32K-word Main Block	10
A7FFF	32K-word Main Block	9
A0000	32K-word Main Block	8
9FFFF	32K-word Main Block	7
98000	32K-word Main Block	6
97FFF	32K-word Main Block	5
90000	32K-word Main Block	4
8FFFF	32K-word Main Block	3
88000	32K-word Main Block	2
87FFF	32K-word Main Block	1
80000	32K-word Main Block	0
7FFFF		
78000		
77FFF		
70000		
6FFFF		
68000		
67FFF		
60000		
5FFFF		
58000		
57FFF		
50000		
4FFFF		
48000		
47FFF		
40000		
3FFFF		
38000		
37FFF		
30000		
2FFFF		
28000		
27FFF		
20000		
1FFFF		
18000		
17FFF		
10000		
0FFFF		
08000		
07FFF	4K-word Parameter Boot Block	5
07000	4K-word Parameter Boot Block	4
06FFF	4K-word Parameter Boot Block	3
06000	4K-word Parameter Boot Block	2
05FFF	4K-word Parameter Boot Block	1
05000	4K-word Parameter Boot Block	0
04FFF		
04000		
03FFF		
03000		
02FFF		
02000		
01FFF	4K-word Boot Block	1
01000	4K-word Boot Block	0
00FFF		
00000		

Bottom Boot

Bank1

(F- \overline{BE}_0 ="H", F- \overline{BE}_1 ="L")

8. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (*1)	V_{CC}	-0.2 to +4.6	V
Input voltage (*1, 2)	V_{IN}	-0.2 (*3) to 3.9	V
Operating temperature	T_{opr}	-25 to +85	°C
Storage temperature	T_{stg}	-65 to 125	°C
F- V_{CCW} voltage (*1)	F- V_{CCW}	-0.3 (*3) to +4.6	V

Notes) *1. The maximum applicable voltage on any pins with respect to GND.

*2. Except F- V_{CC} , F- V_{CCW} .

*3. -2.0V undershoot is allowed when the pulse width is less than 20nsec.

9. Recommended DC Operating Conditions

($T_a = -25^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
Input voltage	V_{IH}	2.0		$V_{CC} + 0.2$ (*1)	V
	V_{IL}	-0.2 (*2)		0.4	V

Notes) *1. V_{CC} is the lower one of S- V_{CC} and F- V_{CC} .

*2. -2.0V undershoot is allowed when the pulse width is less than 20nsec.

10. Pin Capacitance

($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0\text{V}$			30	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$			34	pF

*1

*1

Note) *1 Sampled but not 100% tested

11. DC Characteristics

DC Characteristics ($T_a = -25^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V)

Parameter	Symbol	Conditions	Min.	Typ. (*1)	Max.	Unit
Input leakage current (I_{LI})	I_{LI}	$V_{IN} = V_{CC}$ or GND	-2		+2	μA
Output leakage current (I_{LO})	I_{LO}	$V_{OUT} = V_{CC}$ or GND	-2		+2	μA
F- V_{CC} V_{CC} Standby Current	I_{CCS} (*3)	$F-\overline{BE} = F-\overline{RP} = F-V_{CC} \pm 0.2\text{V}$ $F-\overline{WP} = F-V_{CC} \pm 0.2\text{V}$ or $F-\text{GND} \pm 0.2\text{V}$		4	20	μA
		$F-\overline{BE} = F-\overline{RP} = V_{IH}$ $F-\overline{WP} = V_{IH}$ or V_{IL}		0.4	4	mA
Auto Power-Save Current	I_{CCAS} (*2, 3)	$F-\overline{BE} = \text{GND} \pm 0.2\text{V}$		4	20	μA
Reset Power-Down Current	I_{CCD}	$F-\overline{RP} = F-\text{GND} \pm 0.2\text{V}$, $I_{OUT}(F-\text{RY}/\overline{\text{BY}}) = 0\text{mA}$		4	20	μA
V_{CC} Read Current	I_{CCR} (*3)	CMOS Input $F-\overline{BE} = F-\text{GND}$, $f = 5\text{MHz}$, $I_{OUT} = 0\text{mA}$		15	25	mA
		TTL Input $F-\overline{BE} = F-\text{GND}$, $f = 5\text{MHz}$, $I_{OUT} = 0\text{mA}$			30	mA
V_{CC} Word Write or Set Lock-Bit Current	I_{CCW}	$F-V_{CCW} = V_{CCWH}$		5	17	mA
V_{CC} Block Erase, Bank Erase or Clear Block Lock-Bits Current	I_{CCE}	$F-V_{CCW} = V_{CCWH}$		4	17	mA
V_{CC} Word Write Block Erase Suspend Current	I_{CCWS}	$F-\overline{BE} = V_{IH}$		1	6	mA
	I_{CCES}					
F- V_{CCW} V_{CCW} Standby or Read Current	I_{CCWS}	$F-V_{CCW} = F-V_{CC}$		± 4.0	± 20	μA
	I_{CCWR}	$F-V_{CCW} > F-V_{CC}$		10	200	μA
V_{CCW} Auto Power-Save Current	I_{CCWAS} (*2, 3)	$F-\overline{BE} = \text{GND} \pm 0.2\text{V}$		0.2	5	μA
V_{CCW} Reset Power-Down Current	I_{CCWD}	$F-\overline{RP} = F-\text{GND} \pm 0.2\text{V}$		0.2	5	μA
V_{CCW} Word Write or Set Lock-Bit Current	I_{CCWW}	$F-V_{CCW} = V_{CCWH}$		12	40	mA
V_{CCW} Block Erase, Bank Erase or Clear Block Lock-Bits Current	I_{CCWE}	$F-V_{CCW} = V_{CCWH}$		8	25	mA
V_{CCW} Word Write or Block Erase Suspend Current	I_{CCWWS}	$F-V_{CCW} = V_{CCWH}$		10	200	μA
	I_{CCWES}					
S- V_{CC} Standby Current	I_{SB}	$S-\overline{CE}_1, S-\overline{CE}_2 \geq S-V_{CC} - 0.2\text{V}$ or $S-\overline{CE}_2 \leq 0.2\text{V}$		1.0	15	μA
	I_{SB1}	$S-\overline{CE}_1 = V_{IH}$ or $S-\overline{CE}_2 = V_{IL}$			3	mA
Operation Current	I_{CC1}	$S-\overline{CE}_1 = V_{IL}$, $S-\overline{CE}_2 = V_{IH}$ $V_{IN} = V_{IL}$ or V_{IH}	$t_{CYCLE} = \text{Min.}$ $I_{I/O} = 0\text{mA}$		45	mA
	I_{CC2}	$S-\overline{CE}_1 = 0.2\text{V}$, $S-\overline{CE}_2 = S-V_{CC} - 0.2\text{V}$ $V_{IN} = S-V_{CC} - 0.2\text{V}$ or 0.2V	$t_{CYCLE} = 1\mu\text{s}$ $I_{I/O} = 0\text{mA}$		8	mA

DC Characteristics (Continue)

 $(T_a = -25^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V)

Parameter	Symbol	Test Conditions	Min.	Typ. (*1)	Max.	Unit
Input Low Voltage	V_{IL}		-0.2		0.4	V
Input High Voltage	V_{IH}		2.0		$V_{CC} + 0.2$	V
Output Low Voltage	V_{OL}	$I_{OL} = 0.5\text{mA}$			0.4	V
Output High Voltage (CMOS)	V_{OH1}	$I_{OH} = -0.5\text{mA}$	2.0			V
F- V_{CCW} Lockout during Normal Operations	V_{CCWLK} (*4)				1.5	V
F- V_{CCW} during Block Erase, Bank Erase, Word Write or Lock-Bit Configuration Operations	V_{CCWH}		2.7		3.6	V
F- V_{CC} Lockout Voltage	V_{LKO}		2.0			V

Notes)

- Reference values at $V_{CC} = 3.0\text{V}$ and $T_a = +25^\circ\text{C}$.
- The Automatic Power Savings (APS) feature is placed automatically power save mode that addresses not switching more than 300ns while read mode.
- CMOS inputs are either $V_{CC} \pm 0.2\text{V}$ or $\text{GND} \pm 0.2\text{V}$. TTL inputs are either V_{IL} or V_{IH} .
- Block erases, bank erases, word writes and lock-bits configurations are inhibited when $F\text{-}V_{CCW} \leq V_{CCWLK}$ and not guaranteed in the range between V_{CCWLK} (Max) and V_{CCWH} (Min), and above V_{CCWH} (Max).

12. Flash memory AC Characteristics

AC Test Conditions

Input pulse level	0 V to 2.7 V
Input rise and fall time	10 ns
Input and Output timing Ref. level	1.35 V
Output load	1TTL+C _L (50pF)

Read Cycle (T_a= -25°C to +85°C , V_{CC}= 2.7V to 3.6 V)

Parameter	Sym.	Min.	Max.	Unit
Read Cycle Time	t _{AVAV}	90		ns
Address to Output Delay	t _{AVQV}		90	ns
F- \overline{BE} to Output Delay	t _{ELQV}		90	ns
F- \overline{RP} High to Output Delay	t _{PHQV}		600	ns
F- \overline{OE} to Output Delay	t _{GLQV}		55	ns
F- \overline{BE} to Output in Low Z	t _{ELQX}	0		ns
F- \overline{BE} High to Output in High Z	t _{EHQZ}		55	ns
F- \overline{OE} to Output in Low Z	t _{GLQX}	0		ns
F- \overline{OE} High to Output in High Z	t _{CHQZ}		30	ns
Output Hold from Address, F- \overline{BE} or F- \overline{OE} Change, Whichever Occurs First	t _{OH}	0		ns

Notes)

*1. F- \overline{OE} may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of F- \overline{BE}_0 or F- \overline{BE}_1 without impact on t_{ELQV}.

Write Cycle (F- \overline{WE} Controlled) (*2) (T_a= -25°C to +85°C , V_{CC}=2.7 V to 3.6 V)

Parameter	Sym.	Min.	Max.	Unit
Write Cycle Time	t _{AVAV}	90		ns
F- \overline{RP} High Recovery to F- \overline{WE} going to Low	t _{PHWL}	1		μs
F- \overline{BE} Setup to F- \overline{WE} Going Low	t _{ELWL}	15		ns
F- \overline{WE} Pulse Width	t _{WLWH}	60		ns
F- \overline{WP} V _{IH} Setup to F- \overline{WE} Going High	t _{SHWH}	115		ns
F-V _{CCW} Setup to F- \overline{WE} Going High	t _{VPWH}	115		ns
Address Setup to F- \overline{WE} Going High	t _{AVWH}	60		ns
Data Setup to F- \overline{WE} Going High	t _{DVWH}	60		ns
Data Hold from F- \overline{WE} High	t _{WHDX}	5		ns
Address Hold from F- \overline{WE} High	t _{WHAX}	5		ns
F- \overline{BE} Hold from F- \overline{WE} High	t _{WHEH}	10		ns
F- \overline{WE} Pulse Width High	t _{WHWL}	20		ns
Write Recovery before Read	t _{WHGL}	5		ns
F-V _{CCW} Hold from Valid SRD	t _{QVVL}	0		ns
F- \overline{WP} V _{IH} Hold from Valid SRD	t _{QVSL}	0		ns

Write Cycle (F- $\overline{\text{BE}}$ Controlled) (*4) $(T_a = -25\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}, V_{cc} = 2.7\text{ V to } 3.6\text{ V})$

Parameter	Sym.	Min.	Max.	Unit
Write Cycle Time	t_{AVAV}	90		ns
F- $\overline{\text{RP}}$ High Recovery to F- $\overline{\text{BE}}$ going to Low	t_{PHL}	1		μs
F- $\overline{\text{WE}}$ Setup to F- $\overline{\text{BE}}$ Going Low	t_{WLEL}	0		ns
F- $\overline{\text{BE}}$ Pulse Width	t_{ELEH}	70		ns
F- $\overline{\text{WP}}$ V_{IH} Setup to F- $\overline{\text{BE}}$ Going High	t_{SHEH}	115		ns
F- V_{CCW} Setup to F- $\overline{\text{BE}}$ Going High	t_{VPEH}	115		ns
Address Setup to F- $\overline{\text{BE}}$ Going High	t_{AVEH}	60		ns
Data Setup to F- $\overline{\text{BE}}$ Going High	t_{DVEH}	60		ns
Data Hold from F- $\overline{\text{BE}}$ High	t_{EHDX}	5		ns
Address Hold from F- $\overline{\text{BE}}$ High	t_{EHAX}	5		ns
F- $\overline{\text{WE}}$ Hold from F- $\overline{\text{BE}}$ High	t_{EWHH}	0		ns
F- $\overline{\text{BE}}$ Pulse Width High	t_{EHEL}	25		ns
Write Recovery before Read	t_{EHGL}	5		ns
F- V_{CCW} Hold from Valid SRD	t_{QVVL}	0		ns
F- $\overline{\text{WP}}$ V_{IH} Hold from Valid SRD	t_{QVSL}	0		ns

*3

*3

Notes) *2. Read timing characteristics during block erase, bank erase, word write and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.

*3. Refer to Section 5. Flash Memory Command Definition for valid AIN and DIN for block erase, bank erase, word write or lock-bit configuration.

*4. In system where F- $\overline{\text{BE}}$ defines the pulse width (within a longer F- $\overline{\text{WE}}$ timing waveform), all setup, hold, and inactive F- $\overline{\text{WE}}$ times should be measured relative to the F- $\overline{\text{BE}}$ waveform.

Block Erase, Bank Erase, Word Write and Lock-Bits Configuration Performance

($T_a = -25^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V)

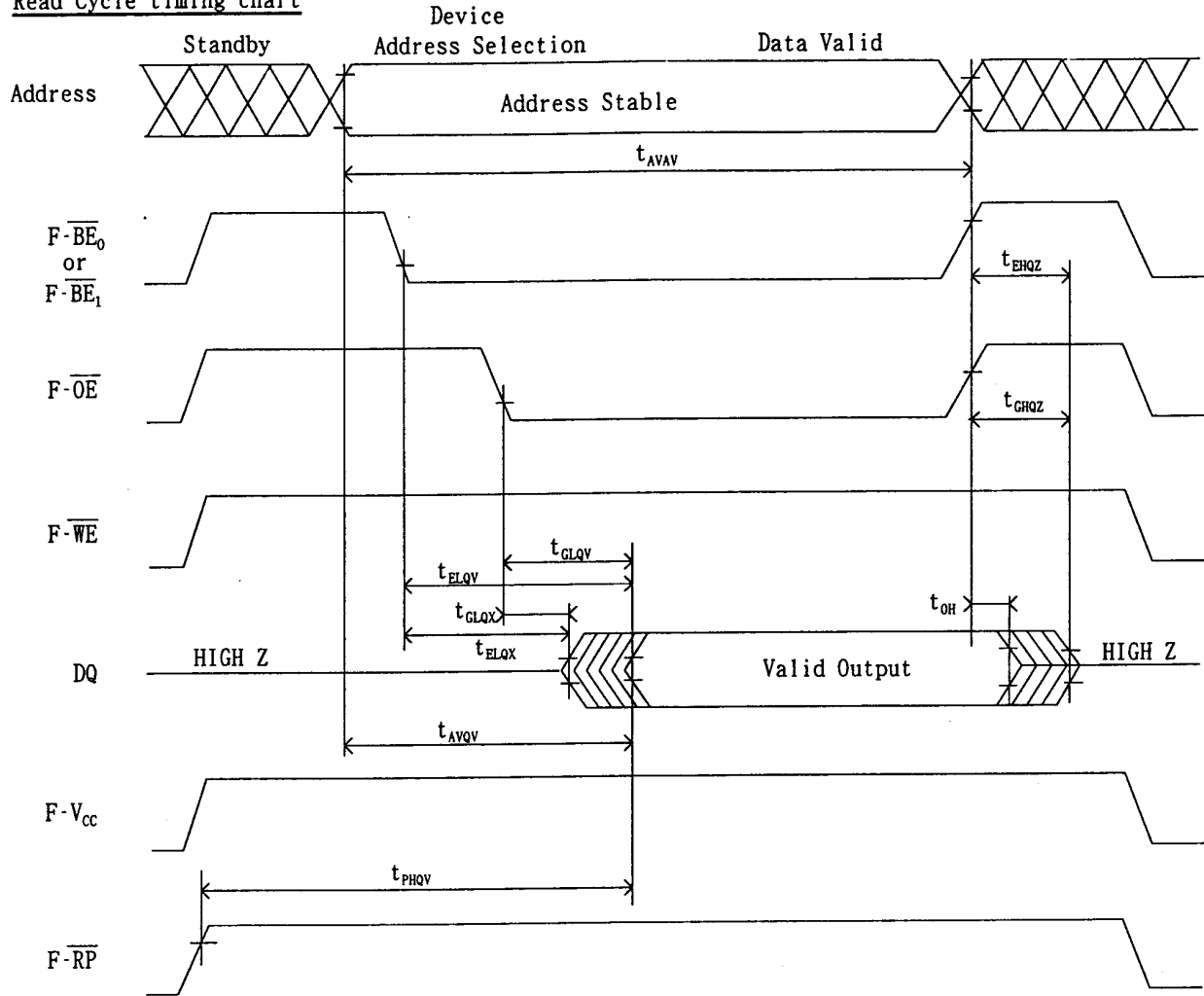
Sym.	Parameter		$V_{CC} = 2.7\text{V}$ to 3.6V		Unit	
			Typ. ^(*4)	Max.		
t_{WHQV1} t_{EHQV1}	Word Write Time	32K-word Block	33	200	μs	*5
		4K-word Block	36	200	μs	*5
	Block Write Time	32K-word Block	1.1	4	s	*5
		4K-word Block	0.15	0.5	s	*5
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K-word Block	1.2	6	s	*5
		4K-word Block	0.6	5	s	*5
	Bank Erase Time		42.0	210	s	*5
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time		56	200	μs	*5
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time		1	5	s	*5
t_{WHRZ1} t_{EHRZ1}	Word Write Suspend Latency Time to Read		6.0	15.0	μs	
t_{WHRZ2} t_{EHRZ2}	Erase Suspend Latency Time to Read		16.0	30.0	μs	

Notes) *4. Reference values at $T_a = +25^\circ\text{C}$ and $V_{CC} = 3.0\text{V}$, $V_{CCW} = 3.0\text{V}$. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.

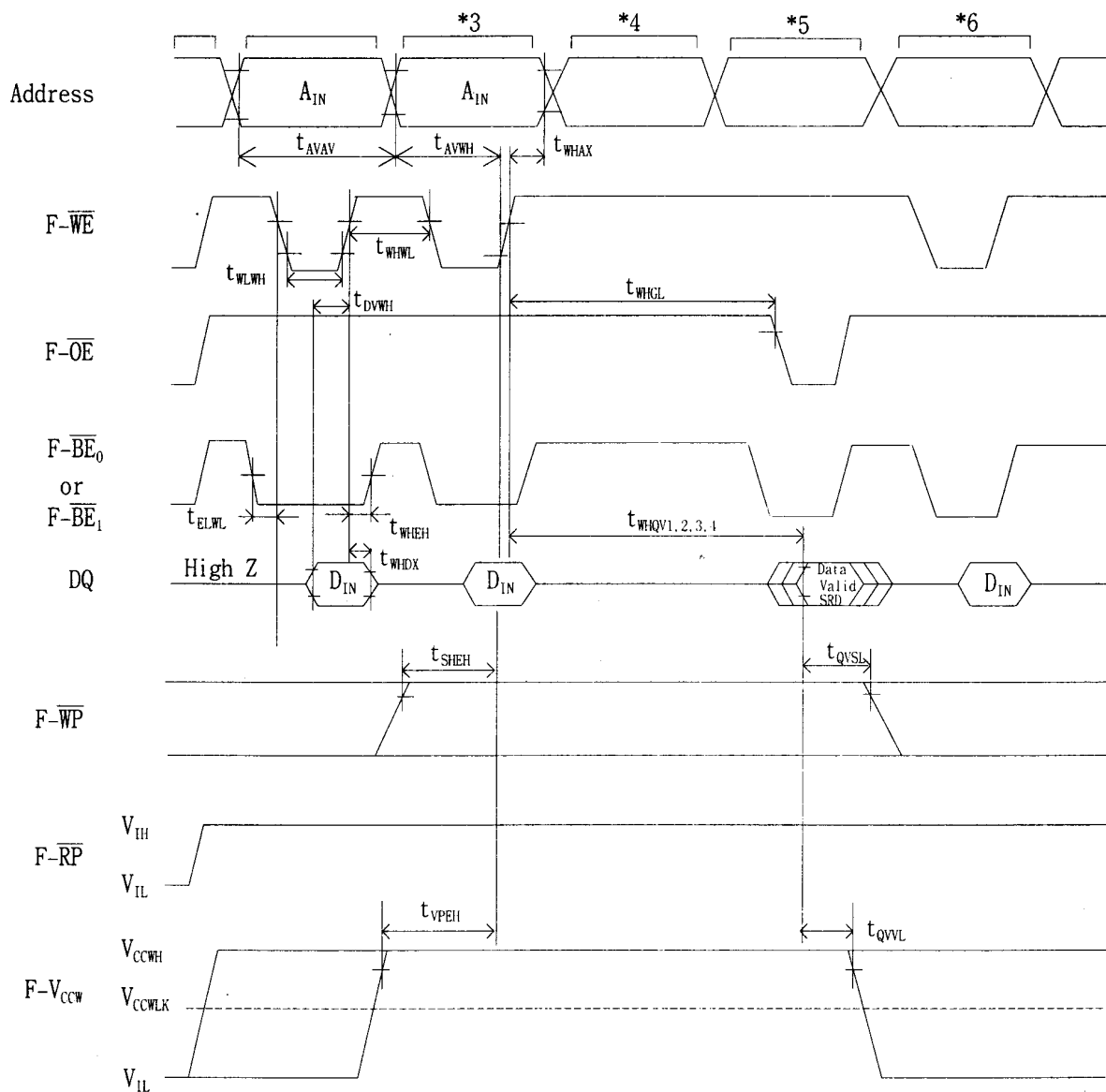
*5. Excludes system-level overhead.

Flash Memory AC Characteristics Timing Chart

Read Cycle timing chart



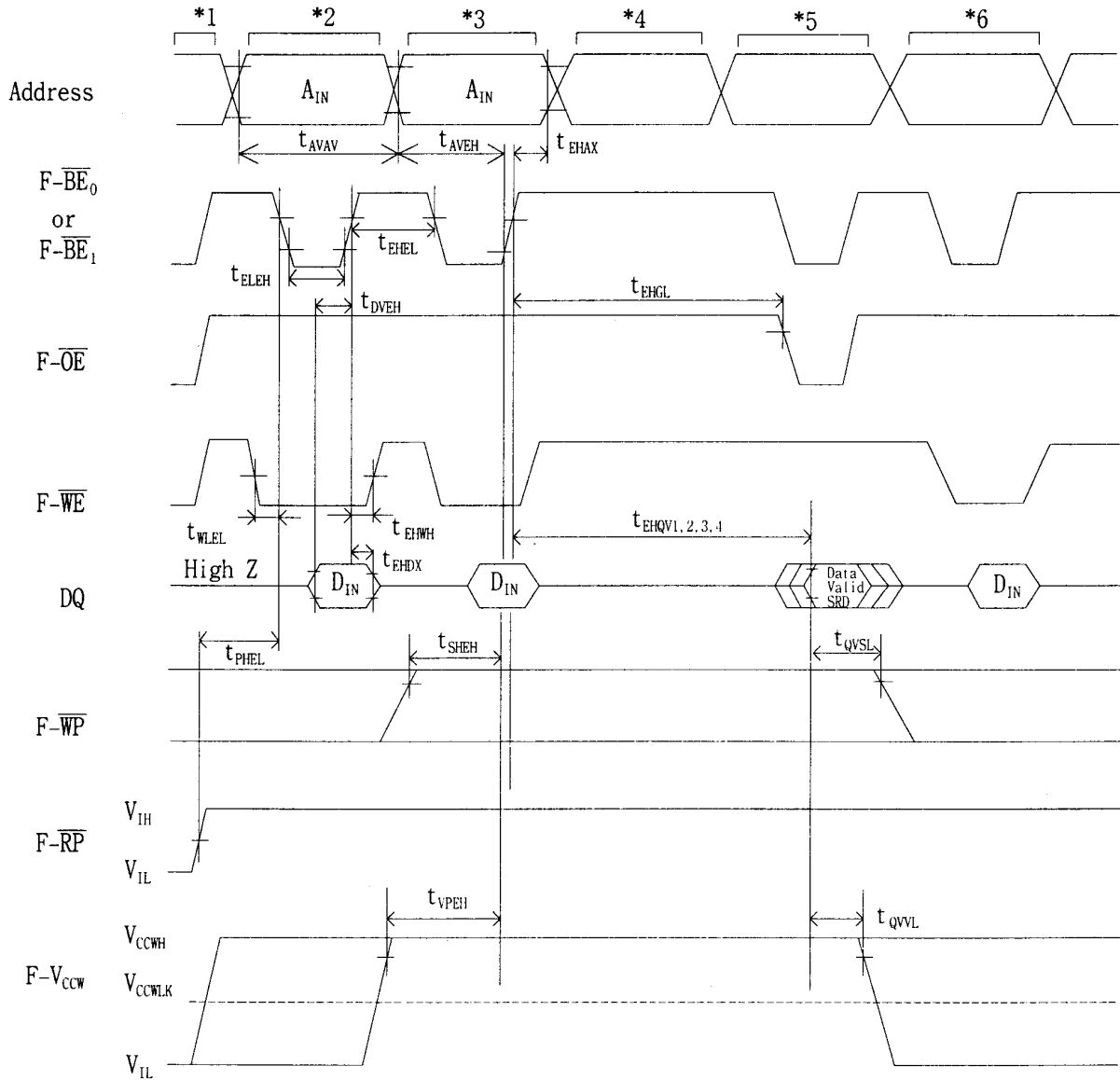
Write cycle timing chart (F-WE Controlled)



NOTES:

- *1. V_{CC} power-up and standby.
- *2. Write each setup command.
- *3. Write each confirm command or valid address and data.
- *4. Automated erase or program delay.
- *5. Read status register data.
- *6. Write Read Array command.

Write cycle timing chart (F- \overline{BE} controlled)



NOTES:

- *1. V_{CC} power-up and standby.
- *2. Write each setup command.
- *3. Write each confirm command or valid address and data.
- *4. Automated erase or program delay.
- *5. Read status register data.
- *6. Write Read Array command.

Reset Operations

($T_a = -25\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{cc} = 2.7\text{V}$ to 3.6V)

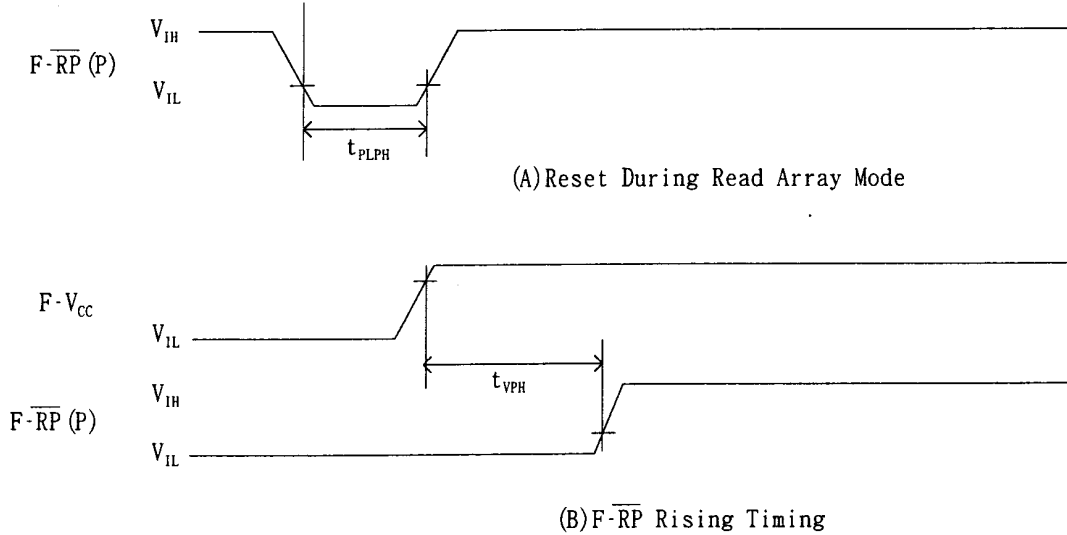
Parameter	Sym.	Min.	Max.	Unit
F- $\overline{\text{RP}}$ Pulse Low Time (If F- $\overline{\text{RP}}$ is tied to V_{cc} , this specification is not applicable.)	t_{PLPH}	100		ns
F- $\overline{\text{RP}}$ Low to Reset during Block Erase, Bank Erase, Word Write or Lock-bit Configuration *1	t_{PLRZ}		30	μs
F- V_{cc} 2.7V to F- $\overline{\text{RP}}$ High	t_{VPH}	100		ns

Notes) *1. If F- $\overline{\text{RP}}$ is asserted while a block erase, bank erase, word write or lock-bit configuration operation is not executing, the reset will complete with 100ns.

*2. A reset time, t_{PHQV} , is required from the later of F- $\overline{\text{RP}}$ going high until outputs are valid.

*3. When the device power-up, holding F- $\overline{\text{RP}}$ low minimum 100ns is required after V_{cc} has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation



13. SRAM AC Electrical Characteristics

SRAM AC Test Conditions

Input pulse level	0.4 V to 2.2 V
Input rise and fall time	5 ns
Input and Output timing Ref. level	1.5 V
Output load	1TTL+C _L (30pF) (*1)

Note) *1. Including scope and jig capacitance.

Read Cycle

(T_a= -25 °C to +85 °C , V_{CC}= 2.7 V to 3.6 V)

Parameter	Sym.	Min.	Max.	Unit	
Read Cycle Time	t _{RC}	85		ns	
Address access time	t _{AA}		85	ns	
Chip enable access time (S- \overline{CE}_1) (S- \overline{CE}_2)	t _{ACE1}		85	ns	
	t _{ACE2}		85	ns	
Byte enable access time	t _{BE}		85	ns	
Output enable to output valid	t _{OE}		45	ns	
Output hold from address change	t _{OH}	15		ns	
S- \overline{CE}_1 , S- \overline{CE}_2 Low (S- \overline{CE}_1) to output active (S- \overline{CE}_2)	t _{LZ1}	10		ns	*2
	t _{LZ2}	10		ns	*2
S- \overline{OE} Low to output active	t _{OLZ}	5		ns	*2
S- \overline{UB} or \overline{LB} Low to output in High impedance	t _{BLZ}	10		ns	*2
S- \overline{CE}_1 , S- \overline{CE}_2 High to (S- \overline{CE}_1) output in High impedance (S- \overline{CE}_2)	t _{HZ1}	0	25	ns	*2
	t _{HZ2}	0	25	ns	*2
S- \overline{OE} High to output in High impedance	t _{OHZ}	0	25	ns	*2
S- \overline{UB} or \overline{LB} High to output active	t _{BHZ}	0	25	ns	*2

Write Cycle

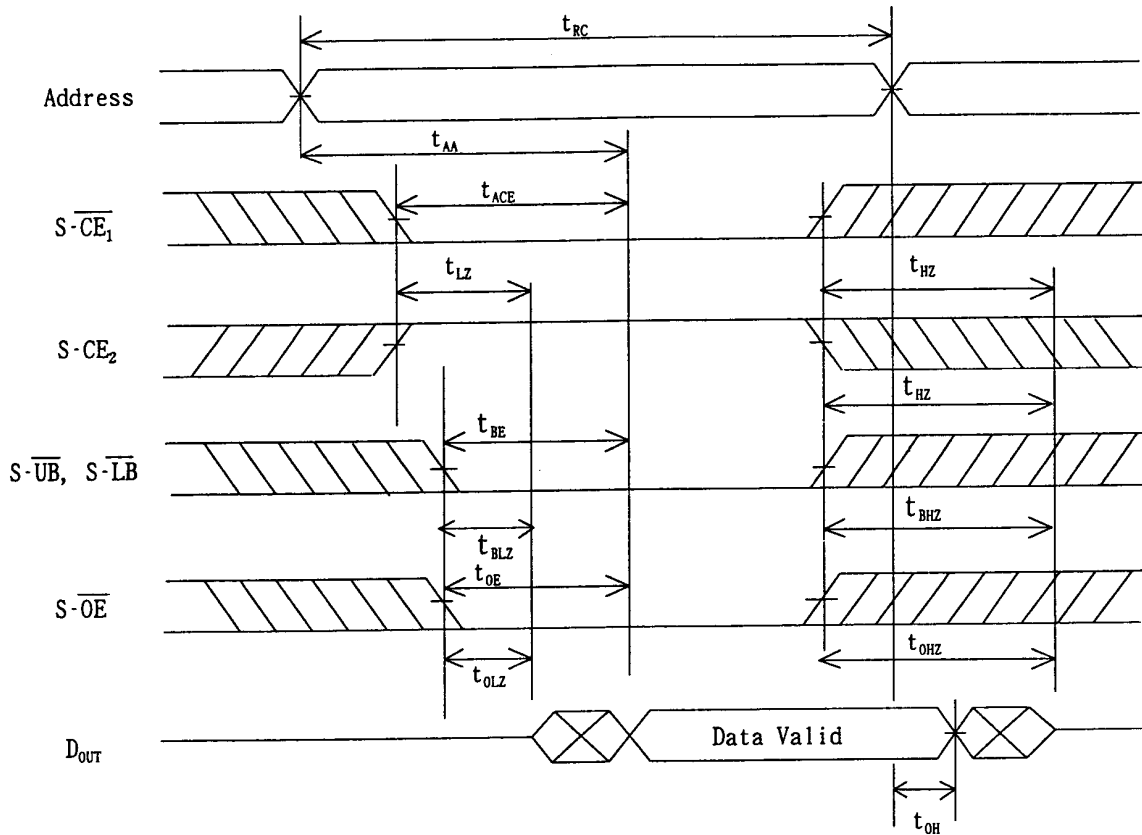
(T_a= -25 °C to +85 °C , V_{CC}=2.7 V to 3.6 V)

Parameter	Sym.	Min.	Max.	Unit	
Write cycle time	t _{WC}	85		ns	
Chip enable to end of write	t _{CW}	70		ns	
Address valid to end of write	t _{AW}	70		ns	
Byte select time	t _{BW}	70		ns	
Address setup time	t _{AS}	0		ns	
Write pulse width	t _{WP}	60		ns	
Write recovery time	t _{WR}	0		ns	
Input data setup time	t _{DW}	35		ns	
Input data hold time	t _{DH}	0		ns	*2
S- \overline{WE} High to output active	t _{OW}	5		ns	*2
S- \overline{WE} Low to output in High impedance	t _{WZ}	0	25	ns	

*2. Active output to High impedance and High impedance to output active tests specified for a ± 200 mV transition from steady state levels into the test load.

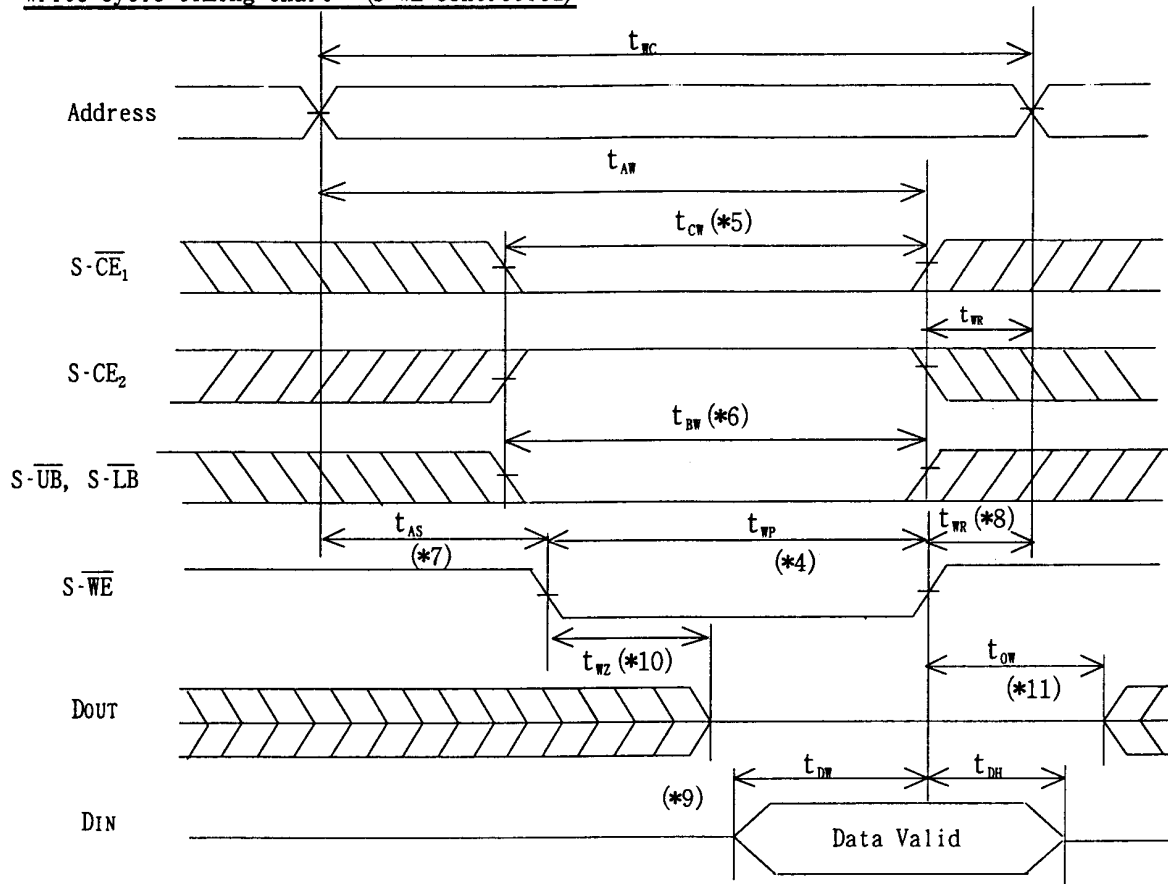
SRAM AC Characteristics Timing Chart

Read cycle timing chart - (*3)

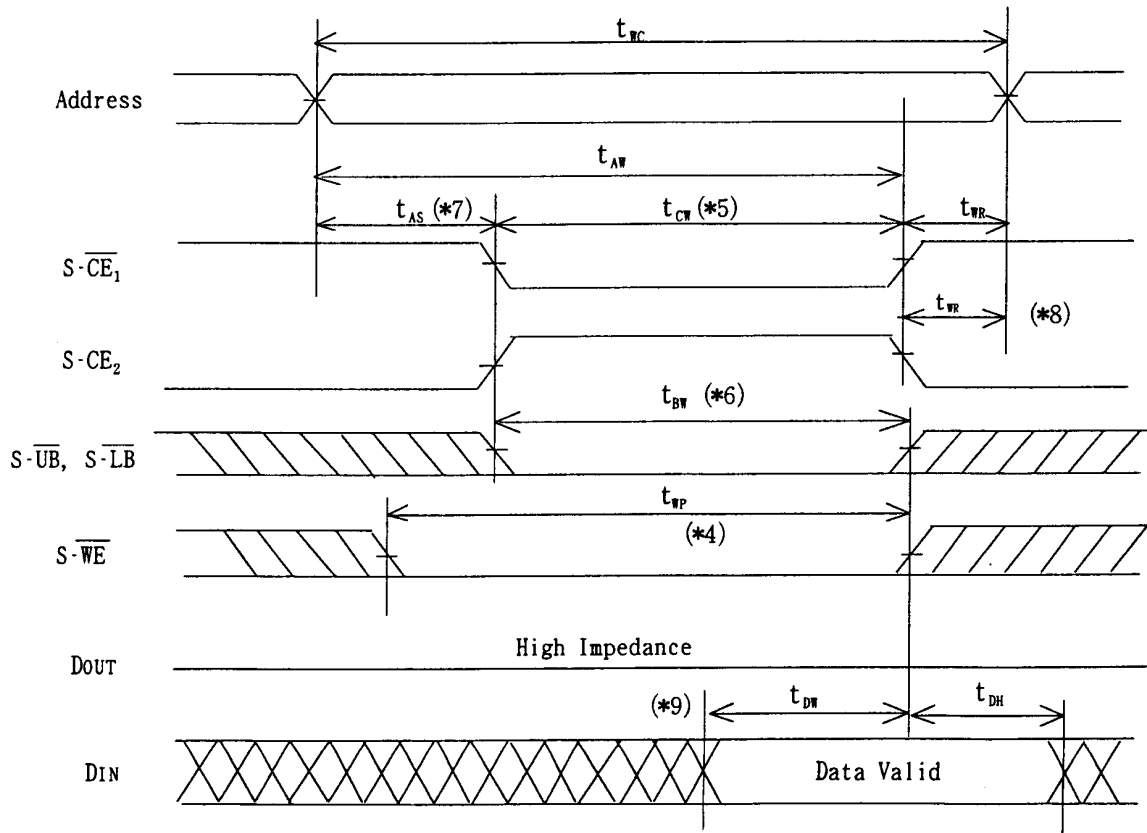


*3 $S-\overline{WE}$ is high for Read cycle.

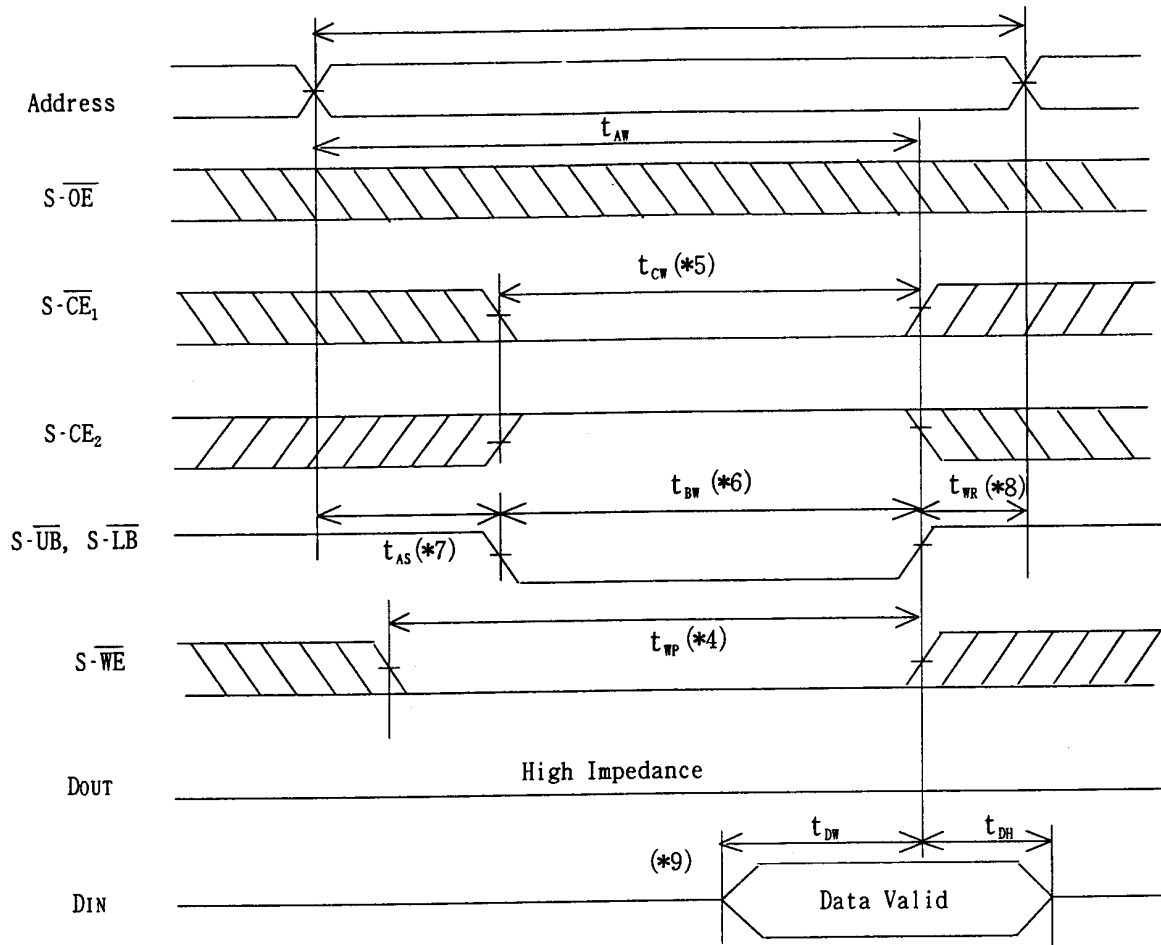
Write cycle timing chart - (S-WE Controlled)



Write cycle timing chart - (S-CE Controlled)



Write cycle timing chart (S-UB, S-LB control)



Notes:

- *4. A write occurs during the overlap of a low S-CE₁, a high S-CE₂ and a low S-WE. A write begins at the latest transition among S-CE₁ going low, S-CE₂ going high and S-WE going low. A write ends at the earliest transition among S-CE₁ going high, S-CE₂ going low and S-WE going high. t_{WP} is measured from the beginning of write to the end of write.
- *5. t_{CW} is measured from the later of S-CE₁ going low or S-CE₂ going high to the end of write.
- *6. t_{BW} is measured from the time of going low S-UB or low S-LB to the end of write.
- *7. t_{AS} is measured from the address valid to the beginning of write.
- *8. t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at S-CE₁ or S-WE going high. t_{WR2} applies in case a write ends at S-CE₂ going low.
- *9. During this period, DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- *10. If S-CE₁ goes low or S-CE₂ goes high simultaneously with S-WE going low or after S-WE going low, the outputs remain in high impedance state.
- *11. If S-CE₁ goes high or S-CE₂ goes low simultaneously with S-WE going high or S-WE going high, the outputs remain in high impedance state.

14. SRAM Data Retention Characteristics

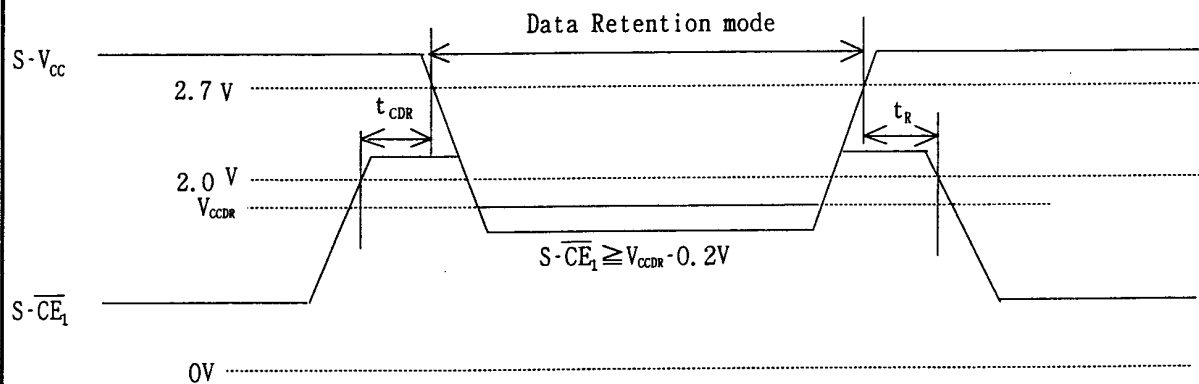
($T_a = -25^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Sym.	Conditions	Min.	Typ. (*1)	Max.	Unit
Data Retention Supply voltage	V_{CCDR}	$S\text{-CE}_2 \leq 0.2\text{V}$ or $S\text{-}\overline{\text{CE}}_1 \geq V_{CCDR} - 0.2\text{V}$ (*2)	1.5		3.6	V
Data Retention Supply current	I_{CCDR}	$V_{CCDR} = 3.0\text{V}$ $S\text{-CE}_2 \leq 0.2\text{V}$ or $S\text{-}\overline{\text{CE}}_1 \geq V_{CCDR} - 0.2\text{V}$ (*2)		1.0	15	μA
Chip enable setup time	t_{CDR}		0			ns
Chip enable hold time	t_R		t_{RC}			ns

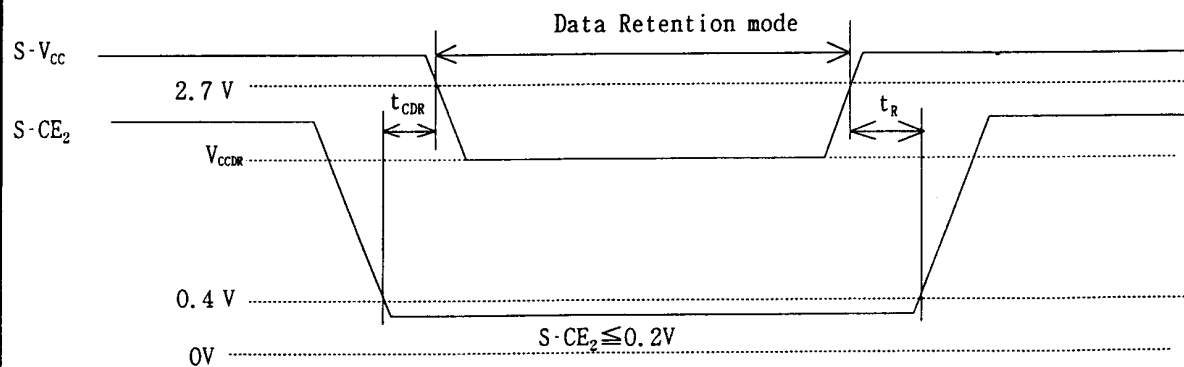
Notes) *1. Reference value at $T_a = 25^\circ\text{C}$, $S\text{-}V_{CC} = 3.0\text{V}$.

*2. $S\text{-}\overline{\text{CE}}_1 \geq V_{CC} - 0.2\text{V}$, $S\text{-CE}_2 \geq V_{CC} - 0.2\text{V}$ ($S\text{-}\overline{\text{CE}}_1$ controlled) or $S\text{-CE}_2 \leq 0.2\text{V}$ ($S\text{-CE}_2$ controlled)

Data Retention timing chart ($S\text{-}\overline{\text{CE}}_1$ Controlled) (*3)



Data Retention timing chart ($S\text{-CE}_2$ Controlled)



Note) *3. To control the data retention mode at $S\text{-}\overline{\text{CE}}_1$, fix the input level of $S\text{-CE}_2$ between V_{CCDR} and $V_{CCDR} - 0.2\text{V}$ or 0V or 0.2V and during the data retention mode.

15. Notes

This product is a stacked CSP package that a 32M (x16) bit Flash Memory and a 4M (x16) bit SRAM are assembled into.

Supply Power

Maximum difference (between F-V_{CC} and S-V_{CC}) of the voltage is less than 0.3V.

Power Supply and Chip Enable of Flash Memory and SRAM

S- \overline{CE}_1 should not be LOW and S-CE₂ should not be HIGH when F- \overline{BE}_0 or F- \overline{BE}_1 is LOW simultaneously.

If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.

Both F-V_{CC} and S-V_{CC} are needed to be applied by the recommended supply voltage at the same time except SRAM data retention mode.

Power UP Sequence

When turning on Flash memory power supply, keep F- \overline{RP} LOW. After F-V_{CC} reaches over 2.7V, keep F- \overline{RP} LOW for more than 100nsec.

Device Decoupling

The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals(F- \overline{BE}_0 , F- \overline{BE}_1 , S- \overline{CE}_1 , S-CE₂).

16. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems.

Such noises, when induced onto $F\text{-}\overline{WP}$ signal or power supply may be interpreted as false commands, causing undesired memory updating.

To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

1) Protecting data in specific block

By setting a $F\text{-}\overline{WP}$ to low, only the boot block can be protected against overwriting.

Parameter and main blocks cannot be locked.

System program, etc., can be locked by storing them in the boot block.

When a high voltage is applied to $F\text{-}\overline{RP}$, overwrite operation is enabled for all blocks.

For further information on setting/resetting of block bit, and controlling of $F\text{-}\overline{WP}$ and $F\text{-}\overline{RP}$, refer to the specification. (See 5. Command Definitions P.5)

2) Data protection through $F\text{-}V_{CCW}$

When the level of $F\text{-}V_{CCW}$ is lower than V_{CCWLK} (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.

For the lockout voltage, refer to the specification. (See Chapter 11. DC Characteristics P.10)

Data protection during voltage transition

1) Data protection thorough $F\text{-}\overline{RP}$

When the $F\text{-}\overline{RP}$ is kept low during power up and power down sequence, write operation on the flash memory is disabled, write protecting all blocks.

For the details of $F\text{-}\overline{RP}$ control, refer to the specification. (See chapter 12. Flash Memory AC Electrical Characteristics)

17. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory power switching characteristics, each device should have a $0.1\mu\text{F}$ ceramic capacitor connected between its F- V_{CC} and GND and between its F- V_{CCW} and GND. Low inductance capacitors should be placed as close as possible to package leads.

2. F- V_{CCW} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{CCW} Power Supply trace. Use similar trace widths and layout considerations given to the V_{CC} power bus.

3. The Inhibition of Overwrite Operation

Please do not execute reprogramming "0" for the bit which has already been programmed "0". Overwrite operation may generate unerasable bit.

In case of reprogramming "0" to the data which has been programmed "1".

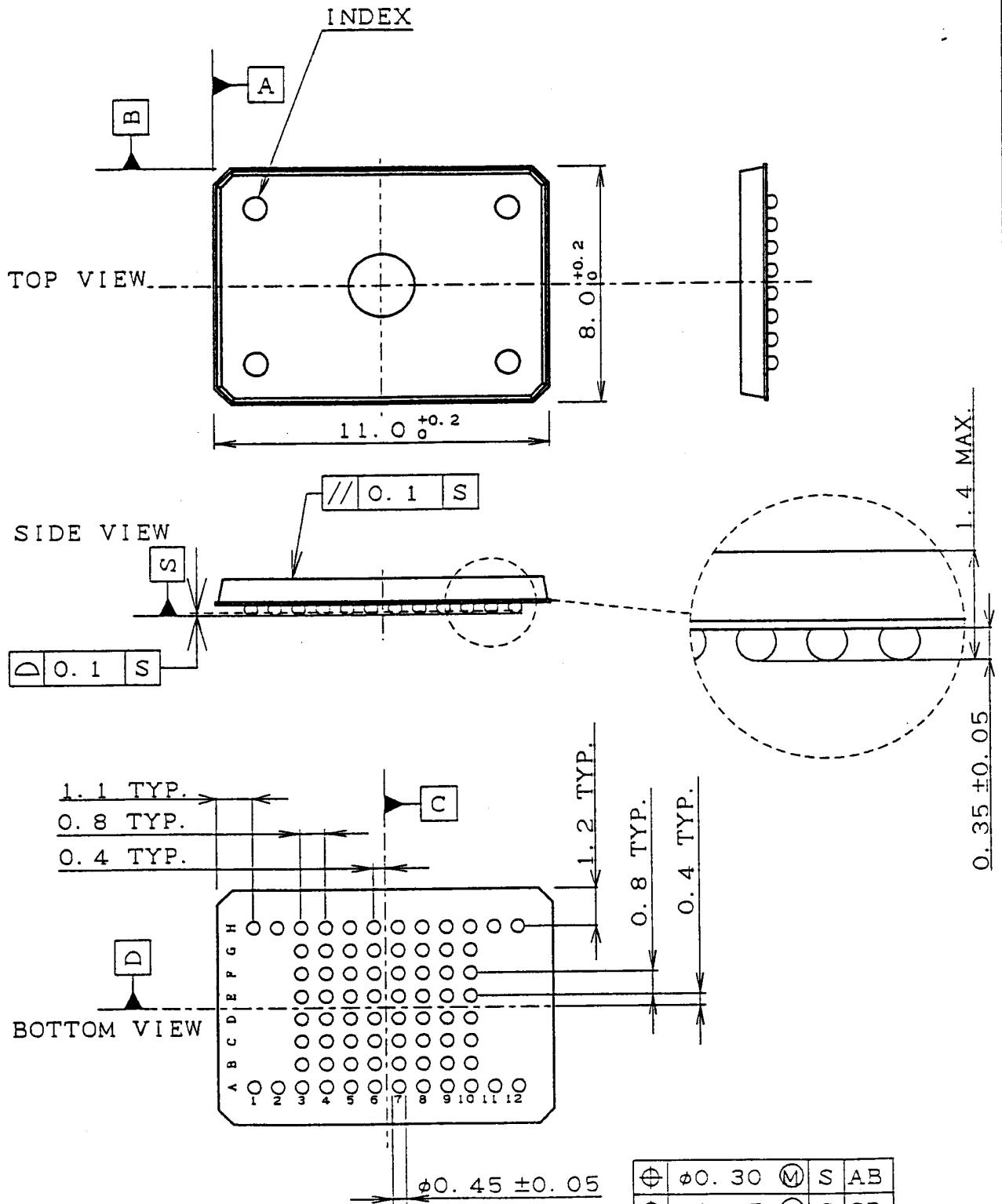
- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which has already been programmed "0".

For example, changing data from "1011110110111101" to "1010110110111100" requires "111011111111110" programming.

4. Power Supply

Block erase, bank erase, word write and lock-bit configuration with an invalid F- V_{CCW} (See 11. DC Characteristics) produce spurious results and should not be attempted. Device operations at invalid F- V_{CC} voltage (see 11. DC Characteristics) produce spurious results and should not be attempted.

SHARP



			尺度 SCALE	単位 UNIT	適用機種	16M FLASH MEMORY(X16BB)
			5/1	1=1/1mm	APPLICABLE	+2M SRAM (X9)
			端子マトリクス MATRIX	12 X 8	MODEL	
改訂日 DATE	改訂記事 REVISE	担当 CHARGE	端子数 COUNTS	72	名称 NAME	LCSP072-P-0811 (LFBGA072-P-0811)
日付 DATE	1998. 2. 10		端子ピッチ PITCH	0.8	コード CODE	LCSP-GR-072-1 -0811
設計 DRAW	製図 TRACE	図号 CHECK	SHARP CORPORATION IC 天理事業本部 TENRI IC GROUP		図番	
SOTA	SOTA		超LSI 開発研究所 VLSI DEVELOPMENT LABORATORIES		DRAWING No.	AA2078
			生産技術開発部 PRODUCTION ENGINEERING DEPT.			

SRAM, Flash Memory, Memory ICs, Stacked Chip Combo Chips Combination Chip Stack Chip