SHARP

Data Sheet

LRS1338A
Stacked Chip
8M Flash Memory and 2M SRAM

FEATURES

- Flash memory and SRAM
- Stacked die chip scale package
- 48-pin TSOP (TSOP48-P-1014) plastic package
- Power supply: 2.7 V to 3.6 V
- Operating temperature: -40°C to +85°C
- Access time (MAX.):
  - Flash memory: 120 ns
  - SRAM: 85 ns
- Operating current (MAX.):
  - Flash memory
    - Read: 25 mA (t_{CYCLE} = 200 ns)
    - Word write: 57 mA (F-V_{CC} ≥ 3.0 V)
    - Block erase: 42 mA (F-V_{CC} ≥ 3.0 V)
  - SRAM: 25 mA (t_{CYCLE} = 200 ns)
- Standby current[2]
  - Flash memory: 20 µA MAX. (F-$\overline{CE}$ ≥ F-V_{CC} - 0.2 V, F-$\overline{RP}$ ≤ 0.2 V, F-V_{PP} ≤ 0.2 V)
  - SRAM:
    - 40 µA MAX. (S-$\overline{CE}$ ≥ S-V_{CC} - 0.2 V)
    - 0.6 µA TYP. (T_A = 25°C, S-V_{CC} = 3 V, S-$\overline{CE}$ ≥ S-V_{CC} - 0.2 V)
- Fully static operation
- Three-state output

NOTES:
1. Block erase and word write operations of flash memory with T_A < -30°C are not supported.
2. Total standby current is the summation of flash's memory standby current and SRAM's one.

DESCRIPTION

The LRS1338A is a combination memory organized as 524,288 × 16-bit flash memory and 262,144 × 8-bit static RAM in one package. It is fabricated using silicon-gate CMOS process technology.

PIN CONFIGURATION

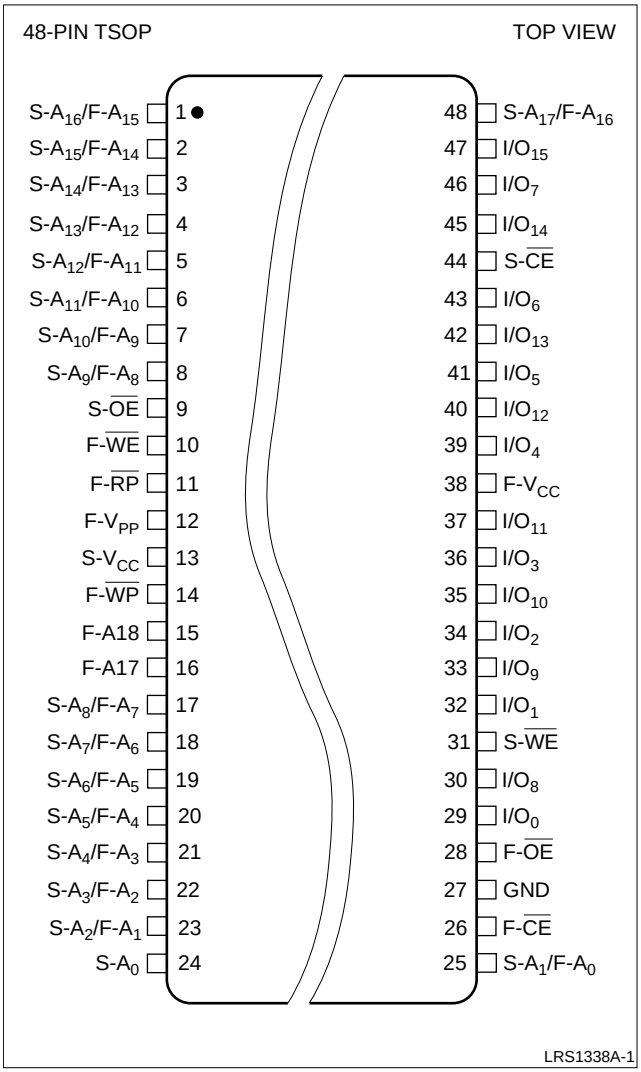


Figure 1. LRS1338A Pin Configuration

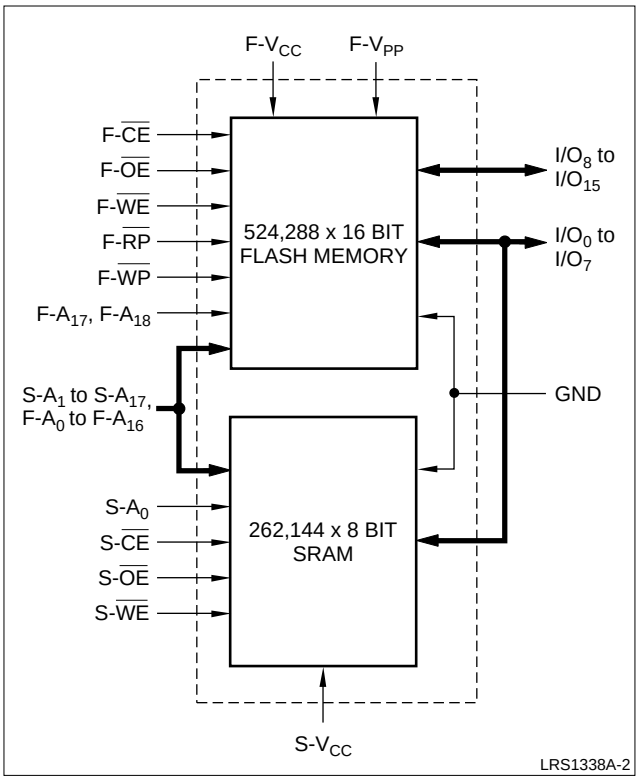


Figure 2. LRS1338A Block Diagram

Table 1. Pin Descriptions

PIN	DESCRIPTION
S-A_1 to S-A_{17} F-A_0 to F-A_{16}	Common Address Input Pins
S-A_0	Address Input Pin for SRAM
F-A_{17} to F-A_{18}	Address Input Pin for Flash Memory
F-$\overline{CE}$	Chip Enable Input Pin for Flash Memory
S-$\overline{CE}$	Chip Enable Input Pin for SRAM
F-$\overline{WE}$	Write Enable Input Pin for Flash Memory
S-$\overline{WE}$	Write Enable Input Pin for SRAM
F-$\overline{OE}$	Output Enable Input Pin for Flash Memory
S-$\overline{OE}$	Output Enable Input Pin for SRAM
I/O_0 to $I/0_7$	Common Data Input/Output Pins
I/O_8 to I/O_{15}	Data Input/Output Pins for Flash Memory
F-$\overline{RP}$	Reset/Deep Power Down Input Pin for Flash Memory
F-$\overline{WP}$	Write Protect Pin for Flash Memory's Boot Block
F-V_{CC}	Power Supply Pin for Flash Memory
F-V_{PP}	Power Supply Pin for Flash Memory Write/Erase
S-V_{CC}	Power Supply Pin for SRAM
GND	Common Ground

GENERAL DESIGN GUIDELINES

Supply Power

Maximum difference (between F-V_{CC} and S-V_{CC}) of the voltage is less than 0.3 V.

Power Supply and Chip Enable of Flash Memory and SRAM

It is forbidden that both F-$\overline{CE}$ and S-$\overline{CE}$ should be LOW simultaneously. If the two memories are active together, they many not operate normally due to interference noises or data collision on I/O bus. Both F-V_{CC} and S-V_{CC} need to be applied by the recommended supply voltage at the same time except SRAM data retention mode.

SRAM Data Retention

SRAM data retention is capable in three ways. SRAM power switching between a system battery and a backup battery needs careful device decoupling from Flash Memory to prevent SRAM supply voltage from falling lower than 2.0 V by a Flash Memory peak current caused by transition of Flash Memory supply voltage or of control signals (F-$\overline{CE}$, F-$\overline{OE}$, and $\overline{RP}$).

CASE 1: FLASH MEMORY IS IN STANDBY MODE (F-V_{CC} = 2.7 V TO 3.6 V)

- SRAM inputs and input/outputs except S-$\overline{CE}$ need to be applied with voltages in the range of -0.3 V to S-V_{CC} + 0.3 V or to be open (HIGH-Z).
- Flash Memory inputs and input/outputs except F-$\overline{CE}$ and $\overline{RP}$ need to be applied with voltages in the range of -0.3 V to S-V_{CC} + 0.3 V or to be open (HIGH-Z).

CASE 2: FLASH MEMORY IS IN DEEP POWER DOWN MODE (F-V_{CC} = 2.7 V TO 3.6 V)

- SRAM inputs and input/outputs except S-$\overline{CE}$ need to be applied with voltages in the range of -0.3 V to S-V_{CC} + 0.3 V or to be open.
- Flash Memory inputs and input/outputs except $\overline{RP}$ need to be applied with voltages in the range of -0.3 V to S-V_{CC} + 0.3 V or to be open (HIGH-Z). $\overline{RP}$ needs to be at the same level as F-V_{CC} or to be open.

CASE 3: FLASH MEMORY POWER SUPPLY IS TURNED OFF (F-V_{CC} = 0 V)

- Fix $\overline{RP}$ LOW level before turning off Flash memory power supply.
- SRAM inputs and input/outputs except S-$\overline{CE}$ need to be applied with voltages in the range of -0.3 V to S-V_{CC} + 0.3 V or to be open (HIGH-Z).
- Flash Memory inputs and input/outputs except $\overline{RP}$ need to be applied with voltages in the range of -0.3 V to S-V_{CC} + 0.3 V or to be open (HIGH-Z).

Power Up Sequence

When turning on Flash memory power supply, keep $\overline{RP}$ LOW. After F-V_{CC} reaches over 2.7 V, keep $\overline{RP}$ LOW for more than 100 ns.

Device Decoupling

The power supply needs to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals (F-$\overline{CE}$, S-$\overline{CE}$).

Table 2. Truth Table[1,2]

F-$\overline{CE}$	F-$\overline{OE}$	F-$\overline{WE}$	F-$\overline{RP}$	S-$\overline{CE}$	S-$\overline{OE}$	S-$\overline{WE}$	ADDRESS	MODE	I/O_0 to I/O_{15}	CURRENT	NOTE
L	L	H	H	H	X	X	X	Flash read	Output	I_{CC}	3, 4
L	H	H	H	H	X	X	X	Flash read	HIGH-Z	I_{CC}	5
L	H	L	H	H	X	X	X	Flash write	Input	I_{CC}	4, 6, 7
H	X	X	X	L	L	H	X	SRAM read	Output	I_{CC}	
H	X	X	X	L	H	H	X	SRAM read	HIGH-Z	I_{CC}	
H	X	X	X	L	X	L	X	SRAM write	Input	I_{CC}	
H	X	X	H	H	X	X	X	Standby	HIGH-Z	I_{SB}	
X	X	X	L	H	X	X	X	Deep power down	HIGH-Z	I_{SB}	5

NOTES:

1. F-$\overline{CE}$ should not be LOW when S-$\overline{CE}$ is LOW simultaneously.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or V_{PPH} for F-V_{PP}. See DC Characteristics for V_{PPLK} and V_{PPH} voltages.
3. Refer to DC Characteristics. When F-$V_{PP} \le V_{PPLK}$, memory contents can be read, but not altered.
4. Do not use in a timing that both F-$\overline{OE}$ and F-$\overline{WE}$ is LOW level.
5. F-$\overline{RP}$ at GND ± 0.2 V ensures the lowest deep power down current.
6. Command writes involving block erase, write, or lock-bit configuration are reliably executed when F-V_{PP} = V_{PPH} and F-V_{CC} = V_{CC1} block erase or word write operations with V_{IH} < F-$\overline{RP}$ < V_{HH} or T_A < -30°C produce spurious results and should not be attempted.
7. Refer to Table 6 for valid D_{IN} during a write operation.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT	NOTES
Supply voltage	V_{CC}	-0.2 to +4.6	V	1, 2
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1, 3, 4
Operating temperature	T_{OPR}	-40 to +85	°C	
Storage temperature	T_{STG}	-65 to +125	°C	
V_{PP} voltage	V_{PP}	-0.2 to +12.6	V	1, 5
Input voltage	$\overline{RP}$	-0.5 to +12.6	V	1, 4, 5

NOTES:
1. The maximum applicable voltage on any pins with respect to GND.
2. Except V_{PP}.
3. Except $\overline{RP}$.
4. -2.0 V undershoot is allowed when the pulse width is less than 20 ns.
5. +14.0 V overshoot is allowed when the pulse width is less than 20 ns.

RECOMMENDED DC OPERATING CONDITIONS

T_A = -40°C to +85°C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
Input voltage	V_{IH}	2.0		V_{CC} + 0.3	V	1
	V_{IL}	-0.3		0.8	V	2
	V_{HH}	11.4		12.6		3

NOTES:
1. V_{CC} is the lower one of S-V_{CC} and F-V_{CC}.
2. -2.0 V undershoot is allowed when the pulse width is less than 20 ns.
3. This voltage is applicable to F-$\overline{RP}$ pin only.

PIN CAPACITANCE

T_A = 25°C, f = 1 MHz

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input capacitance*	C_{IN}	V_{IN} = 0 V			20	pF
I/O capacitance*	$C_{I/O}$	$V_{I/O}$ = 0 V			22	pF

**NOTE: ***Sampled by not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to + 85°C, V_{CC} = 2.7 V to 3.6 V

PARAMETER		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTES
Input leakage current		I_{LI}	V_{IN} = 0V to V_{CC}	-1.5		1.5	µA	
Output leakage current		I_{LO}	F-$\overline{CE}$, S-$\overline{CE}$ = V_{IH} or F-$\overline{OE}$, S-$\overline{OE}$ = V_{IH} or F-$\overline{WE}$, S-$\overline{WE}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}	-1.5		1.5	µA	
Operating supply current	Flash	I_{CC}	Read current, F-V_{PP} ≤ F-V_{CC}, F-$\overline{CE}$ ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V t_{CYCLE} = 200 ns, $I_{I/O}$ = 0 mA			25	mA	1
			Summation of V_{CC} Byte Write or set lock-bit current, and V_{PP} Byte Write or set lock-bit current. F-V_{CC} ≥ 3.0 V			57	mA	2, 3
			Summation of V_{CC} Block Erase or Clear Block lock-bits current, and V_{PP} Block Erase or Clear Block lock-bits current. F-V_{CC} ≥ 3.0 V			42	mA	2, 4
	SRAM	I_{CC}	S-$\overline{CE}$ = 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≥ 0.2 V t_{CYCLE} = 200 ns, $I_{I/O}$ = 0 mA			25	mA	5
Standby current	Flash	I_{SB}	F-$\overline{CE}$ = V_{IH}, $\overline{RP}$ = V_{IH}			2.0	mA	6
			F-$\overline{CE}$ ≥ V_{CC} – 0.2 V, $\overline{RP}$ ≤ 0.2 V			20	µA	7
	SRAM	I_{SB}	S-$\overline{CE}$ = V_{IH}			3.0	mA	8
			S-$\overline{CE}$ ≥ V_{CC} – 0.2 V		0.6	40	µA	9, 10
Output voltage		V_{OL}, V_{OH}	I_{OL} = 2.0 mA			0.4	V	
			I_{OH} = 1.0 mA	2.4			V	

NOTES:
1. This value is read current (I_{CCR} + I_{PPR}) of flash memory.
2. Sampled but not 100% tested.
3. This value is operation current (I_{CCW} + I_{PPW}) of flash memory.
4. This value is operation current (I_{CCE} + I_{PPE}) of flash memory.
5. This value is operation current (I_{CC1}) of SRAM.
6. This value is standby current (I_{CCS} + I_{PPS}) of flash memory.
7. This value is deep power down current (I_{CCD} + I_{PPD}) of flash memory.
8. This value is standby current (I_{SB1}) of SRAM
9. This value is standby current (I_{SB}) of SRAM.
10. Reference values at V_{CC} = 3.0 V and T_A = +25°C

FLASH MEMORY*

New Features

The LRS1388A flash memory maintains backwards compatibility with SHARP's LH28F800BG-L.

- SmartVoltage technology
- Enhanced suspend capabilities
- Boot block architecture

Please note the following important differences:

- V_{PPLK} has been lowered to 1.5 V to support 3.0 V block erase and word write operations. Designs that switch V_{PP} off during read operations should make sure that the V_{PP} voltage transitions to GND.
- Allow V_{PP} connection to 3.0 V.

Product Overview

The LRS1338A is a high-performance 8M SmartVoltage flash memory organized as 512K-word of 16 bits. The 512K-word of data is arranged in two 4K-word boot blocks, six 4K-word parameter blocks and fifteen 32K-word main blocks which are individually erasable in-system. The memory map is shown in Figure 4.

SmartVoltage technology provides a choice of V_{CC} and V_{PP} combinations, as shown in Table 3, to meet system performance and power expectations. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Table 3. V_{CC} and V_{PP} Voltage Combinations

V_{CC} Voltage	V_{PP} Voltage
2.7 V to 3.6 V	2.7 V to 3.6 V

Internal V_{CC} and V_{PP} detection circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase and word write operations.

A block erase operation erases on e of the device's 32K-word blocks typically within 1.14 seconds, 4K-word blocks typically within 0.38 seconds independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word increments of the device's 32K-word blocks typically within 44.6 µs, 4K-word blocks typically within 45.9 µs. Word write suspend mode enables the system to read data or execute code from any other flash memory array location.

The boot blocks can be locked for the $\overline{WP}$ pin. Block erase or word write for boot block must not be carried out by $\overline{WP}$ to LOW and $\overline{RP}$ to V_{IH}.

The status register indicates when the WSM's block erase or word write operation is finished.

The access time is 120 ns (t_{AVQV}) over the commercial temperature range (-40°C to +85°C) and V_{CC} supply voltage range of 2.7 V to 3.6 V.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 1 mA at 3.3 V V_{CC}.

When $\overline{CE}$ and $\overline{RP}$ pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the $\overline{RP}$ pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from $\overline{RP}$ switching HIGH until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from $\overline{RP}$ HIGH until writes to the CUI are recognized. With $\overline{RP}$ at GND, the WSM is reset and the status register is cleared.

**NOTE: ***In the Flash Memory section all reference to pins, commands, voltage, etc. refer only to the Flash portion of this chip.

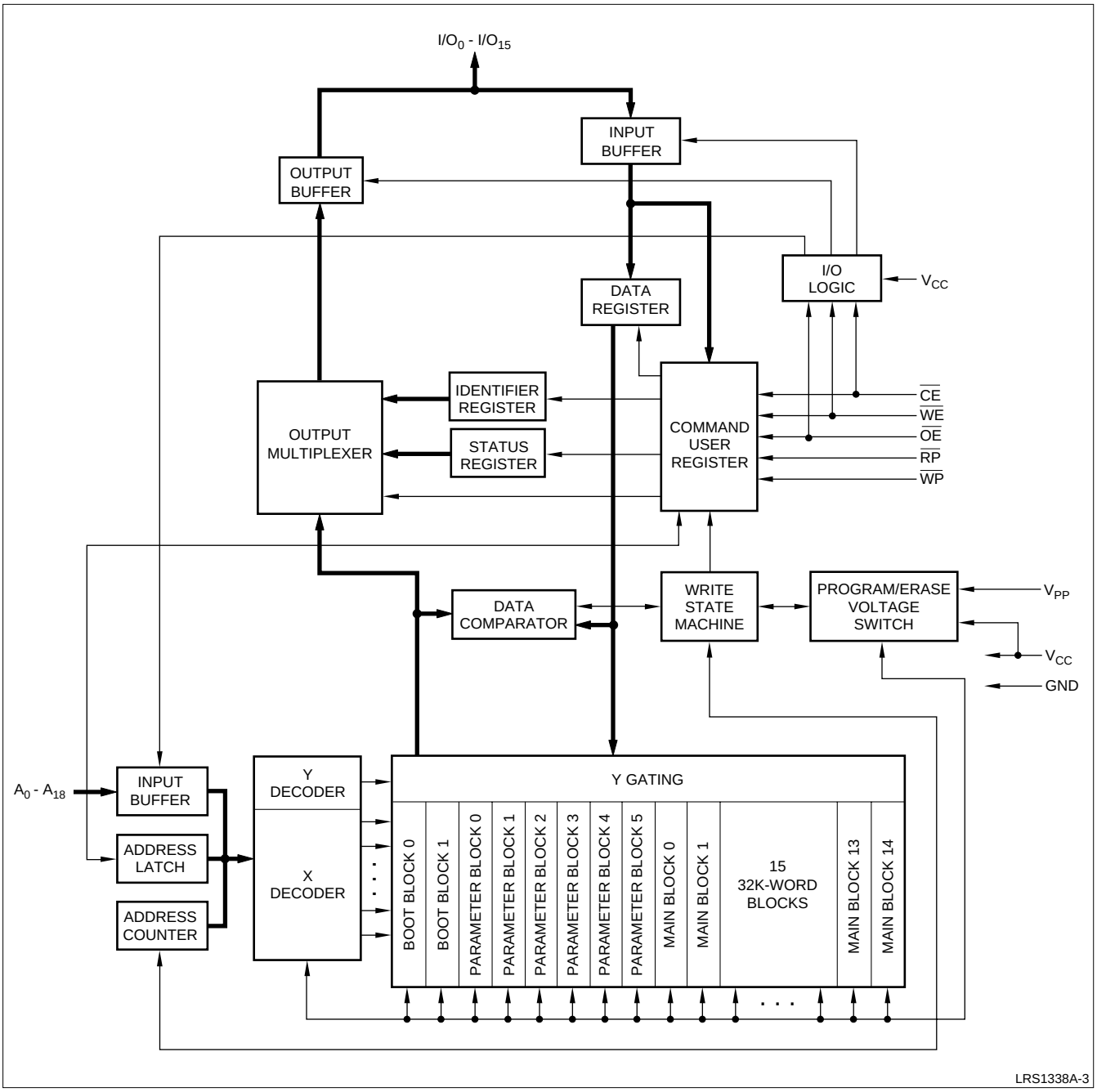


Figure 3. Flash Memory Block Diagram

Table 4. Flash Pin Descriptions

SYMBOL	TYPE	NAME AND FUNCTION
A_0 - A_{18}	Input	ADDRESS INPUTS: Inputs for addresses during read and write operations. Addresses are internally latched during the write cycle.
I/O_0 - I/O_{15}	Input/Output	DATA INPUT/OUTPUTS: Inputs data and commands during CUI write cycles; outputs data during memory array, status register, and identifier code read cycles. Data pins float to HIGH-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	Input	CHIP ENABLE: Activates the device's control logic, input buffers, decoders, and sense amplifiers. $\overline{CE}$-HIGH deselects the device and reduces power consumption to standby levels.
$\overline{RP}$	Input	RESET/DEEP POWER-DOWN: Puts the device in deep power-down mode and resets internal automation. $\overline{RP}$-HIGH enables normal operation. When driven LOW, $\overline{RP}$ inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode. With $\overline{RP} = V_{HH}$, block erase or word write can operate to all blocks without $\overline{WP}$ state. Block erase or word write with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.
$\overline{OE}$	Input	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
$\overline{WE}$	Input	WRITE ENABLE: Controls writes to the CIU and array blocks. Addresses and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	Input	WRITE PROTECT: Master control for boot blocks locking. When V_{IL}, locked boot blocks cannot be erased and programmed.
V_{PP}	Supply	BLOCK ERASE and WORD WRITE POWER SUPPLY: For erasing array blocks or writing words. With $V_{PP} \le V_{PPLK}$, memory contents cannot be altered. Block erase and word write with an invalid V_{PP} (see 'DC Characteristics') produce spurious results and should not be attempted.
V_{CC}	Supply	DEVICE POWER SUPPLY: Do not float any power pins. With $V_{CC} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see 'DC Characteristics') produce spurious results and should not be attempted.
GND	Supply	GROUND: Do not float any ground pins.

Principles of Operation

The LRS1388A SmartVoltage flash memory includes an on-chip WSM to manage block erase and word write functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure, word write, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see 'Bus Operation'), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the F-V_{PP} voltage. High voltage on F-V_{PP} enables successful block erasure and word writing. All functions associated with altering memory contents — block erase, word write, status, and identifier codes — are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase and word write. The internal algorithms are regulated by the WSM including pulse repetition, internal verification, and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of block erase and word write can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspended. Word write suspend allows system software to suspend a word write to read data from any other flash memory array location.

DATA PROTECTION

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory block erases or word writes are required) or hardwired to V_{PPH}. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with two-step block erase or word write command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when $\overline{V_{CC}}$ is below the write lockout voltage V_{LKO} or when $\overline{RP}$ is at V_{IL}. The device's boot blocks locking capability for $\overline{WP}$ provides additional protection from inadvertent code or data alteration by block erase and word write operations.

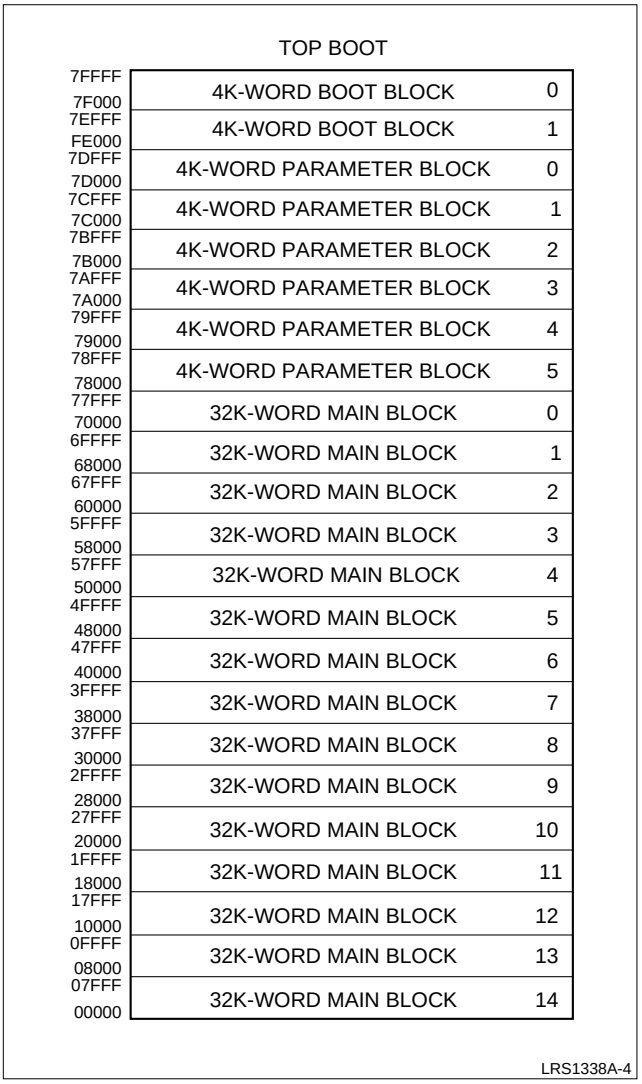


Figure 4. Memory Map

Bus Operation

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

READ

Information can be read from any block, identifier codes or status register independent of the V_{PP} voltage. $\overline{RP}$ can be either V_{IH} or V_{HH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Five control pins dictate the data flow in and out of the component: $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, $\overline{RP}$ and $\overline{WP}$. $\overline{CE}$ and $\overline{OE}$ must be driven active to obtain data at the outputs. $\overline{CE}$ is the device selection control, and when active enables the selected memory device. $\overline{OE}$ is the data output (I/O_0 - I/O_{15}) control and when active drives the selected memory data onto the I/O bus. $\overline{WE}$ must be at V_{IH} and $\overline{RP}$ must be at V_{IH} or V_{HH}. Figure 12 illustrates a read cycle.

OUTPUT DISABLE

With $\overline{OE}$ at a logic-HIGH level (V_{IH}), the device outputs are disabled. Output pins (I/O_0 - I/O_{15}) are placed in a HIGH impedance state.

STANDBY

$\overline{CE}$ at a logic HIGH level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. I/O_0 - I/O_{15} outputs are placed in a HIGH-impedance state independent of $\overline{OE}$. If deselected during block erase or word write, the device continues functioning, and consuming active power until the operation completes.

DEEP POWER-DOWN

$\overline{RP}$ at V_{IL} initiates the deep power down mode.

In read modes, $\overline{RP}$-LOW deselects the memory, places output drivers in a HIGH-impedance state and turns off all internal circuits. $\overline{RP}$ must be held LOW for a minimum of 100 ns. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase or word write modes, $\overline{RP}$-LOW will abort the operation. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after $\overline{RP}$ goes to logic HIGH (V_{IH}) before another command can be written.

As with any automated device, it is important to assert $\overline{RP}$ during system reset. When the system comes out of reset, it expects to read from flash memory. Automated flash memories provide status information when accessed during block erase or word write modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of $\overline{RP}$ input. In this application, $\overline{RP}$ is controlled by the same $\overline{RESET}$ signal that resets the system CPU.

READ IDENTIFIER CODES OPERATION

The read identifier codes operation outputs the manufacturer code and device codes, the system CPU can automatically match the device with its proper algorithms.

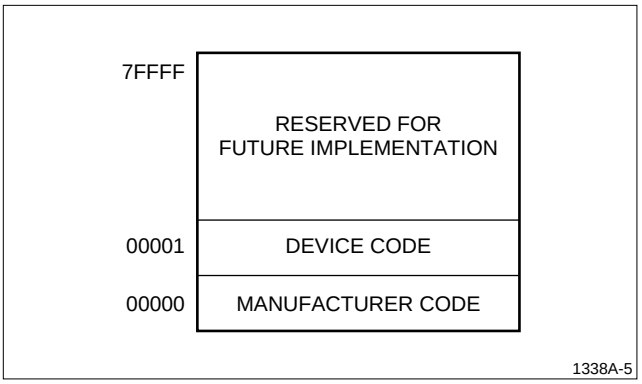


Figure 5. Device Identifier Code Memory Map

WRITE

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register.

When $V_{CC} = V_{CC1}$ and $V_{PP} = V_{PPH}$, the CUI additionally controls block erasure and word write. The Block Erase command requires appropriate command data and an address within the block to be erased. The Word Write command requires the command and address of the location to be written.

The CUI does not occupy an addressable memory location. It is written when $\overline{WE}$ and $\overline{CE}$ are active. The address and data needed to execute a command are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever goes HIGH first). Standard microprocessor write timings are used. Figure 13 and 14 illustrate $\overline{WE}$ and $\overline{CE}$ controlled write operations.

COMMAND DEFINITIONS

When $V_{PP} \leq V_{PPLK}$, Read operations from the status register, identifier codes or blocks are enabled. Placing V_{PPH} on V_{PP} enables successful block erase and word write operations.

Device operations are selected by writing specific commands into the CUI. Table 6 defines these commands.

Table 5. Bus Operations

MODE	$\overline{RP}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ADDRESS	V_{PP}	I/O_0 - I/O_{15}	NOTES
Read	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	1, 2, 3
Output Disable	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	HIGH Z	
Standby	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	HIGH Z	
Deep Power-Down	V_{IL}	X	X	X	X	X	HIGH Z	4
Read Identifier Codes	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 3	X		5
Write	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	3, 6, 7

NOTES:
1. Refer to 'DC Characteristics'. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or V_{PPH} for V_{PP}.
   See 'DC Characteristics' for V_{PPLK} and V_{PPH} voltages.
3. Never hold $\overline{OE}$ LOW and $\overline{WE}$ LOW at the same time.
4. $\overline{RP}$ at GND ± 0.2 V ensures the lowest deep power-down current.
5. See 'Read Identifier Codes Command' for read identifier code data.
6. Command writes involving block erase or word write are reliably executed when $V_{PP} = V_{PPH}$ and $V_{CC} = V_{CC1}$.
   Block erase or word write with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.
7. Refer to Table 6 for valid D_{IN} during a write operations.

Table 6. Command Definitions[1]

COMMAND	BUS CYCLES REQUIRED	FIRST BUS CYCLE			SECOND BUS CYCLE			NOTES
		OPER.[2]	ADDR.[3]	DATA[4]	OPER.[2]	ADDR.[3]	DATA[4]	
Read Array/Reset	1	Write	X	FFH				
Read Identifier Codes	≥ 2	Write	X	90H	Read	IA	ID	5
Read Status Register	2	Write	X	70H	Read	X	SRD	
Clear Status Register	1	Write	X	50H				
Block Erase	2	Write	BA	20H	Write	BA	D0H	6
Word Write	2	Write	WA	40H or 10H	Write	WA	WD	6, 7
Block Erase and Word Write Suspend	1	Write	X	B0H				6
Block Erase and Word Write Resume	1	Write	X	D0H				6

NOTES:
1. Commands other than those shown in table are reserved by SHARP for future device implementations and should not be used.
2. BUS operations are defined in Table 5.
3. X = Any valid address within the device; IA = Identifier Code Address, see Figure 5.
   BA = Address within the block being erased; WA = Address of memory location to be written.
4. SRD = Data read from status register. See Table 9 for a description of the status register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever goes HIGH first).
   ID = Data read from identifier codes.
5. Following the Read Identifier Codes command, read operations access manufacturer and device codes.
   See 'Read Identifier Codes Command' for read identifier code data.
6. When $\overline{WP} = V_{IL}$, $\overline{RP}$ must beat V_{HH} to enable block erase or word write operations.
   Attempts to issue a block erase or word write to a locked boot block while $\overline{RP} = V_{IH}$.
7. Either 40H or 10H are recognized by the WSM as the word write setup.

READ ARRAY COMMAND

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase or word write, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word Write Suspend command. The Read Array command functions independently of V_{PP} voltage and $\overline{RP}$ can be V_{IH} or V_{HH}.

READ IDENTIFIER CODES COMMAND

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 5 retrieve the manufacturer and device codes (see Table 7 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and $\overline{RP}$ can be V_{IH} or V_{HH}. Following the Read Identifier Codes command, the following information can be read.

Table 7. Identifier Codes

CODE	ADDRESS	DATA
Manufacture Code	00000H	00B0H
Device Code (Top Boot)	00001H	0060H

READ STATUS REGISTER COMMAND

The status register may be read to determine when a block erase or word write is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs. $\overline{OE}$ or $\overline{CE}$ must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. $\overline{RP}$ can be V_{IH} or V_{HH}.

CLEAR STATUS REGISTER COMMAND

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to '1's by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table x). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several words in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

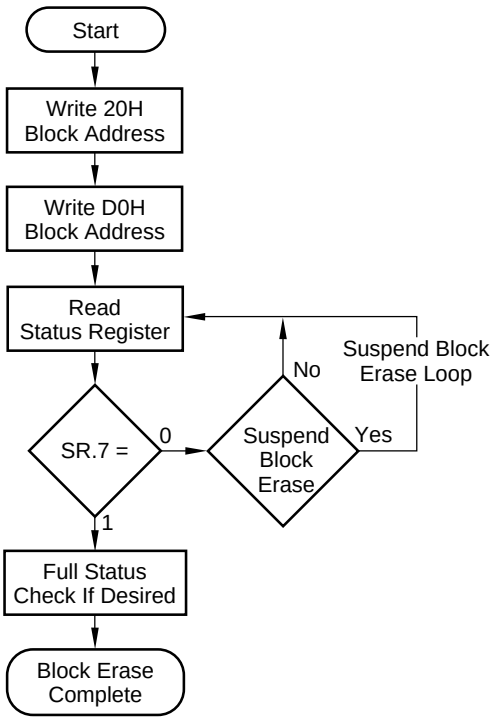
To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} voltage. $\overline{RP}$ can be V_{IH} or V_{HH}. This command is not functional during block erase or word write suspend modes.

BLOCK ERASE COMMAND

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by a block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFFFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect block erase completion by analyzing the output data of the status register bit SR.7.

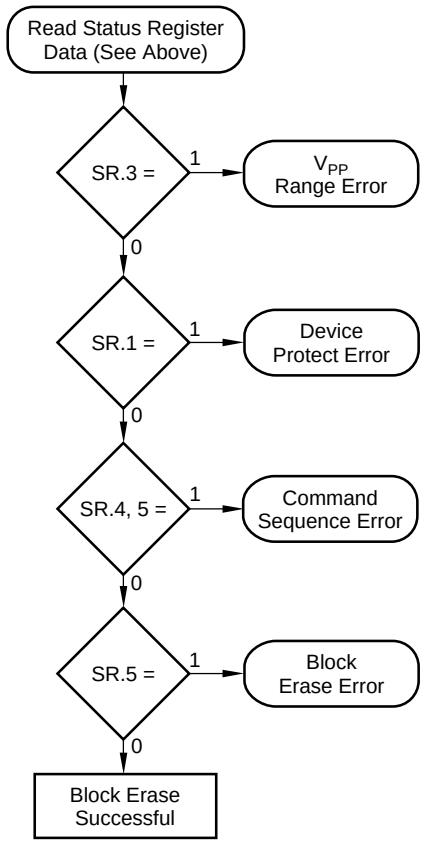
When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective action. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to '1'. Also, reliable block erasure can only occur when $V_{CC} = V_{CC1}$ and $V_{PP} = V_{PPH}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to '1'. Successful block erase for boot blocks requires that if set $\overline{WP} = V_{IH}$ or $\overline{RP} = V_{HH}$. If block erase is attempted to boot block when the corresponding $\overline{WP} = V_{IL}$ or $\overline{RP} = V_{IH}$, SR.1 and SR.5 will be set to '1'. Block erase operations with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.



BUS OPERATION	COMMAND	COMMENTS
Write	Erase Setup	Data = 20H Addr = Within Block to be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent block erasures. Full status check can be done after each block erase or after a sequence of block erasures. Write FFH after the last operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
SR.5, SR.4, SR.3, and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

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Figure 6. Automated Block Erase Flowchart

WORD WRITE COMMAND

Word write is executed by a two-cycle command sequence. Word write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of $\overline{WE}$). The WSM then takes over, controlling the word write and write verify algorithms internally. After the word write sequence is written, the device automatically outputs status register data when read (see Figure 7). The CPU can detect the completion of the word write event by analyzing the status register bit SR.7.

When word write is complete, status register bit SR.4 should be checked. If word write error is detected, the status register should be cleared. The internal WSM verify only detects errors for '1's that do not successfully write to '0's. The CUI remains in read status register mode until it receives another command.

Reliable word writes can only occur when $V_{CC} = V_{CC1}$ and V_{PP} and V_{PPH}. In the absence of this high voltage, memory contents are protected against word writes. If word write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to '1'.

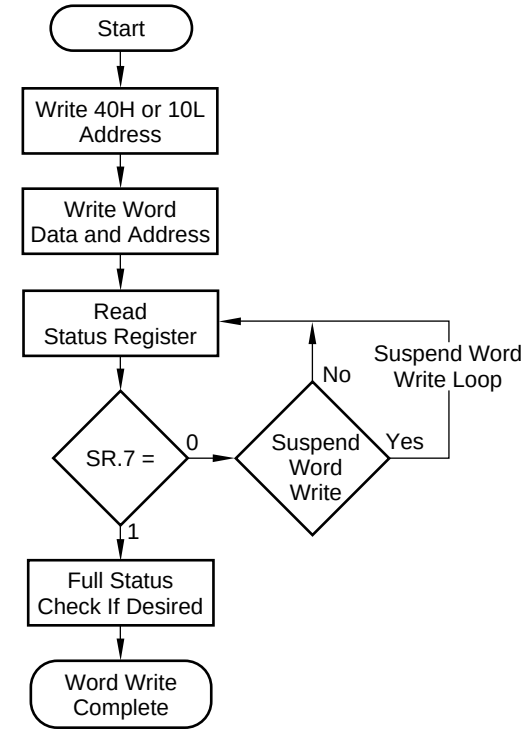
Successful word write for boot blocks requires that if set, that $\overline{WP} = V_{IH}$ or $\overline{RP} = V_{HH}$. If word write is attempted to boot block when the corresponding $\overline{WP} = V_{IL}$ or $\overline{RP} = V_{IH}$, SR.1 and SR.4 will be set to '1'. Word write operations with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.

BLOCK ERASE SUSPEND COMMAND

The Block Erase Suspend command allows block-erase interruption to read or word-write data in another block of memory. Once the block-erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to '1'). Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Word Write command sequence can also be issued during erase suspend to program data in other blocks. using the Word Write Suspend command (see 'Word Write Suspend Command' section), a word write operation can also be suspended. During a word write operation with block erase suspended, status register bit SR.7 will return to '0'. However, SR.6 will remain '1' to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 8). V_{PP} must remain at V_{PPH} (the same V_{PP} level used for block erase) while block erase is suspended. $\overline{RP}$ must also remain at V_{IH} or V_{HH} (the same $\overline{RP}$ level used for block erase). $\overline{WP}$ must also remain at V_{IL} or V_{IH} (the same $\overline{WP}$ level used for block erase). Block erase cannot resume until word write operations initiated during block erase suspend have completed.



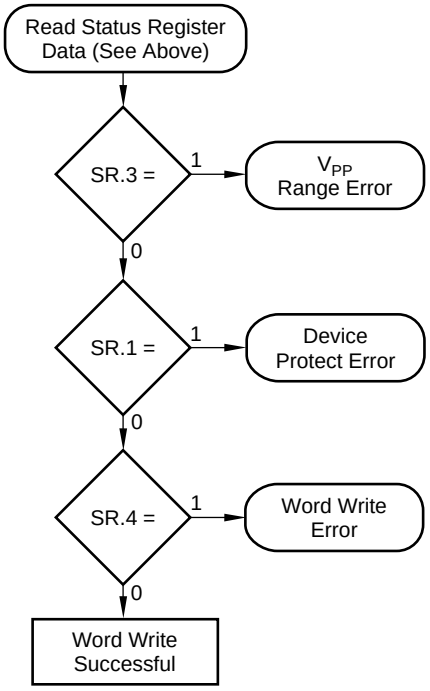
BUS OPERATION	COMMAND	COMMENTS
Write	Setup Word Write	Data = 40H or 10H Addr = Location to be Written
Write	Word Write	Data = Data to be Written Addr = Location to be Written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent byte writes.

SR full status check can be done after each byte write or after a sequence of byte writes.

Write FFH after the last byte write operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect
Standby		Check SR.4 1 = Data Write Error

SR.4, SR.3, and SR.1 are only cleared by the Clear Status Register Command in cases where multiple locations are written before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

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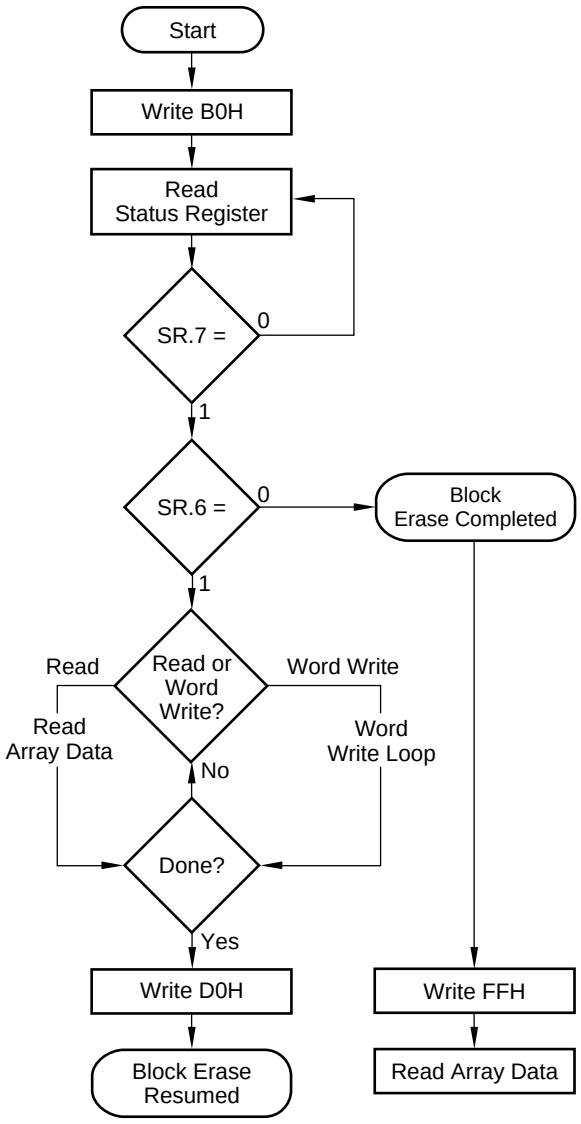
Figure 7. Automated Word Write Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	Data = D0H Addr = X

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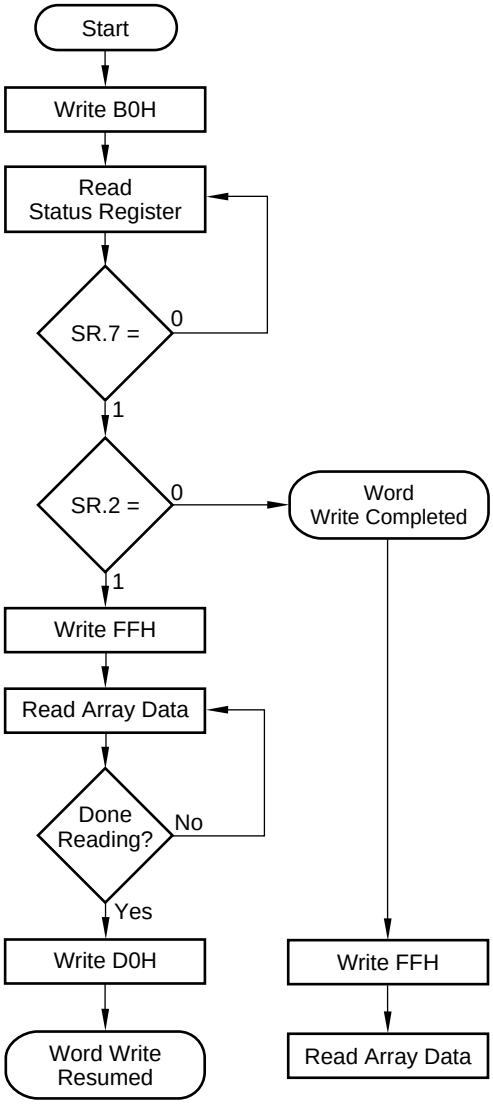
Figure 8. Block Erase Suspend/Resume Flowchart

WORD WRITE SUSPEND COMMAND

The Word Write Suspend command allows word write interruption to read data in other flash memory locations. Once the word write process starts, writing the Word Write Suspend command requests that the WSM suspend the word write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word write operation has been suspended (both will be set to '1'). Specification t_{WHRH1} defines the word write suspend latency.

At this point a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word write is suspended are Read Status Register and Word Write Resume. After Word Write Resume command is written to the flash memory, the WSM will continue the word write process. Status register bits SR.2 and SR.7 will automatically clear. After the Word Write Resume command is written, the device automatically outputs status register data when read (see Figure 9). V_{PP} must remain at V_{PPH} (the same V_{PP} level used for word write) while in word write suspend mode. $\overline{RP}$ must also remain at V_{IH} or V_{HH} (the same $\overline{RP}$ level used for word write). $\overline{WP}$ must also remain V_{IL} or V_{IH} (the same $\overline{WP}$ level used for word write).



BUS OPERATION	COMMAND	COMMENTS
Write	Word Write Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Word Write Suspended 0 = Word Write Completed
Write	Read Array	Data = FFH Addr = X
Read		Read Array locations other than that being written
Write	Word Write Resume	Data = D0H Addr = X

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Figure 9. Word Write Suspend/Resume Flowchart

Table 8. Write Protection Alternatives

OPERATION	V_{PP}	$\overline{RP}$	$\overline{WP}$	EFFECT
Word Write or Block Erase	V_{IL}	X	X	All blocks locked
	> V_{PPLK}	V_{IL}	X	All blocks locked
		V_{HH}	X	All blocks unlocked
		V_{IH}	V_{IL}	Two boot blocks locked
			V_{IH}	All blocks unlocked

Table 9. Status Register Definition

WSMS	ESS	ES	WWS	VPPS	WWSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = Write State Machine Status (WSMS)
1 = Ready
0 = Busy

SR.6 = Erase Suspend Status (ESS)
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = Erase(s)
1 = Error in Block Erasure
0 = Successful Block Erase

SR.4 = Word Write (WWS)
1 = Error in Word Write
0 = Successful Word Write

SR.3 = V_{PP} Status (VPPS)
1 = V_{PP} LOW Detect, Operation Abort
0 = V_{PP} Okay

SR.2 = Word Write Suspend Status (WWSS)
1 = Word Write Suspended
0 = Word Write in Progress/Completed

SR.1 = Device Protect Status (DPS)
1 = $\overline{WP}$ and/or $\overline{RP}$ Lock Detected, Operation Abort
0 = Unlock

SR.0 = Reserved for future enhancements (R)

NOTES:
1. Check SR.7 to determine block erase or word write completion. SR.6 - SR.0 are invalid while SR.7 = 0.
2. If both SR.5 and SR.4 are '1's after a block erase attempt, an improper command sequence was entered.
3. SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase or Word Write command sequences. SR.3 is not guaranteed to report accurate feedback only when $V_{PP} \neq V_{PPH}$.
4. The WSM interrogates the $\overline{WP}$ and $\overline{RP}$ only after Block Erase or Word Write command sequences. It informs the system, depending on the attempted operation, if the $\overline{WP}$ is not V_{IH} or $\overline{RP}$ is not V_{HH}.
5. SR.0 is reserved for future use and should be masked out when polling the status register.

Design Considerations

THREE-LINE OUTPUT CONTROL

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

- Lowest possible memory power dissipation.
- Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable $\overline{CE}$ while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. $\overline{RP}$ should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

POWER SUPPLY DECOUPLING

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby current levels, active current levels and transient peaks produced by falling and rising edges of $\overline{CE}$ and $\overline{OE}$. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

V_{PP} TRACE ON PRINTED CIRCUIT BOARDS

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for word writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

V_{CC}, V_{PP} $\overline{RP}$ TRANSITIONS

Block erase and word write are not guaranteed if V_{PP} falls outside of a valid V_{PPH} range, V_{CC} falls outside of a valid V_{CC1} range, or $\overline{RP} \neq V_{IH}$ or V_{HH}. If V_{PP} error is detected, status register bit SR.3 is set to '1' along with SR.4 or SR.5, depending on the attempted operation. If $\overline{RP}$ transitions to V_{IL} during block erase or word write, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or $\overline{RP}$ transitions to V_{IL} clear the status register.

The CIU latches commands issued by system software and is not altered by V_{PP} or $\overline{CE}$ transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}.

After block erase or word write, even after V_{PP} tarnation down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

POWER-UP/DOWN PROTECTION

The device is designed to offer protection against accidental block erasure or word writing during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be LOW for a command write, driving either to V_{HH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

$\overline{WP}$ provide additional protection from inadvertent code or data alteration.

The device is disabled while $\overline{RP} = V_{IL}$ regardless of its control inputs state.

POWER DISSIPATION

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's non-volatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering $\overline{RP}$ to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after $\overline{RP}$ is first raised to V_{IH}. See 'AC Characteristics — Read Only and Write Operations' and Figure 12, 13 and 14 for more information.

Electrical Specifications

ABSOLUTE MAXIMUM RATINGS*

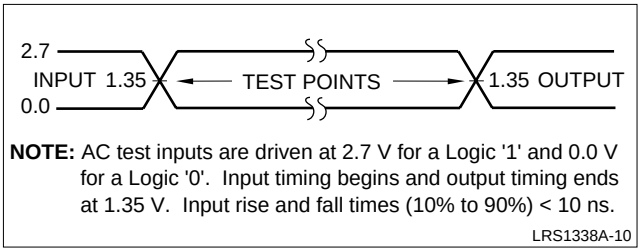
- Commercial Operating Temperature
  - During Read, Block Erase and Word Write: -40°C to +85°C (Note 1)
  - Temperature under Bias: -40°C to +85°C (Note 1)
- Storage Temperature: -65°C to +125°C
- Voltage on any pin except V_{CC}, V_{PP} and $\overline{RP}$: -2.0 V to +7.0 V (Note 2)
- V_{CC} Supply Voltage: -2.0 V to +7.0 V (Note 2)
- V_{PP} Update Voltage during Block Erase and Word Write: -2.0 V to +14.0 V (Note 2 and 3)
- $\overline{RP}$ Voltage: -2.0 V to +14.0 V (Note 2 and 3)
- Output Short Circuit Current: 100 mA (Note 4)

WARNING: *Stressing the device beyond the 'Absolute Maximum Ratings' may cause permanent damage. These are stress ratings only. Operation beyond the 'Operating Conditions' is not recommended and extended exposure beyond the 'Operating Conditions' may affect device reliability.

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5 V on input/output pins and -0.2 V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC} + 0.5 V which, during transitions, may overshoot to V_{CC} + 2.0 V for periods < 20 ns.
3. Maximum DC voltage on V_{PP} and $\overline{RP}$ may overshoot to +14.0 V for periods <20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

AC Test Conditions



NOTE: AC test inputs are driven at 2.7 V for a Logic '1' and 0.0 V for a Logic '0'. Input timing begins and output timing ends at 1.35 V. Input rise and fall times (10% to 90%) < 10 ns.

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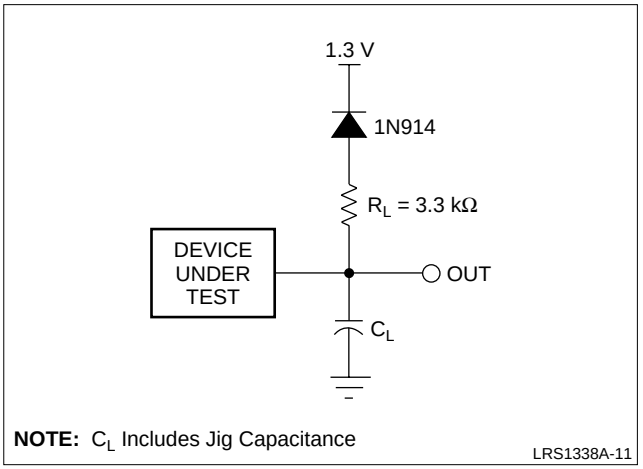
Figure 10. Transient Input/Output Reference Waveform for V_{CC} = 2.7 V to 3.6 V



NOTE: C_L Includes Jig Capacitance

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Figure 11. Transient Equivalent Testing Load Circuit

Table 10. Test Configuration Capacitance Loading Value

TEST CONFIGURATION	C_L (pF)
V_{CC} = 2.7 V to 3.6 V	50

FLASH DC CHARACTERISTICS

SYMBOL	PARAMETER	V_{CC} = 2.7 V to 3.6 V		UNIT	TEST CONDITIONS	NOTES
		MIN.	MAX.			
I_{LI}	Input Load Current		±0.5	µA	$V_{CC} = V_{CC}$ MAX., $V_{IN} = V_{CC}$ or GND	1
I_{LO}	Output Leakage Current		±0.5	µA	$V_{CC} = V_{CC}$ MAX., $V_{OUT} = V_{CC}$ or GND	1
I_{CCS}	V_{CC} Standby Current	25	50	µA	CMOS Inputs, $V_{CC} = V_{CC}$ MAX., $\overline{CE} = \overline{RP} = V_{CC} \pm 0.2$ V	1, 2
		0.2	2	mA	TTL Inputs, $V_{CC} = V_{CC}$ MAX., $\overline{CE} = \overline{RP} = V_{IH}$	1, 2
I_{CCD}	V_{CC} Deep Power-Down Current	4	20	µA	$\overline{RP}$ = GND ± 0.2 V	1
I_{CCR}	V_{CC} Read Current	15	25	mA	CMOS Inputs, $V_{CC} = V_{CC}$ MAX., $\overline{CE}$ = GND, f = 5 MHz, I_{OUT} = 0 mA	1, 2, 3
			30	mA	TTL Inputs, $V_{CC} = V_{CC}$ MAX., $\overline{CE}$ = GND, f = 5 MHz, I_{OUT} = 0 mA	1, 2, 3
I_{CCW}	V_{CC} Word Write Current	5	17	mA	$V_{PP} = V_{PPH}$	1, 4
I_{CCE}	V_{CC} Block Erase Current	4	17	mA	$V_{PP} = V_{PPH}$	1, 4
I_{CCWS} I_{CCES}	V_{CC} Word Write or Block Erase Suspend Current	1	6	mA	$\overline{CE} = V_{IH}$	1, 5
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current	±2	±15	µA	$V_{PP} \le V_{CC}$	1
		10	20.0	µA	$V_{PP} > V_{CC}$	1
I_{PPD}	V_{PP} Deep Power-Down Current	0.1	5	µA	$\overline{RP}$ = GND ± 0.2 V	1
I_{PPW}	V_{PP} Word Write Current	12	40	mA	$V_{PP} = V_{PPH}$	1, 4
I_{PPE}	V_{PP} Block Erase Current	8	25	mA	$V_{PP} = V_{PPH}$	1, 4
I_{PPWS} I_{PPES}	V_{PP} Word Write or Block Erase Suspend Current	10	200	µA	$V_{PP} = V_{PPH}$	1
V_{IL}	Input LOW Voltage	-0.5	0.8	V		4
V_{IH}	Input HIGH Voltage	2.0	V_{CC} + 0.5	V		4
V_{OL}	Output LOW Voltage		0.4	V	$V_{CC} = V_{CC}$ MIN., I_{OL} = 2.0 mA	4
V_{OH1}	Output HIGH Voltage (TTL)	2.4		V	$V_{CC} = V_{CC}$ MIN., I_{OH} = 1.0 mA	4
V_{OH2}	Output HIGH Voltage (CMOS)	0.85 V_{CC}		V	$V_{CC} = V_{CC}$ MIN., I_{OH} = 2.5 mA	4
		V_{CC} -0.4		V	$V_{CC} = V_{CC}$ MIN., I_{OH} = -100 µA	4
V_{PPLK}	V_{PP} Lockout during Normal Operations		1.5	V		4, 6
V_{PPH}	V_{PP} during Word Write or Block Erase Operations	2.7	3.6	V		
V_{LKO}	V_{CC} Lockout Voltage	2.0		V		
V_{HH}	$\overline{RP}$ Unlock Voltage	11.4	12.6	V	Unable $\overline{WP}$	7, 8

NOTES:

1. All currents are in RMS unless otherwise noted.
2. CMOS inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL inputs are either V_{IL} or V_{IH}.
3. Automatic Power Savings (APS) reduces typical I_{CCR} to 3 mA at 3.3 V V_{CC} in static operation.
4. Sampled, not 100% tested.
5. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or word written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
6. Block erases and word writes are inhibited when $V_{PP} \le V_{PPLK}$, and not guaranteed in the range between V_{PPLK} (MAX.) and V_{PPH} (MIN.).
7. Block erases and word writes are inhibited when the corresponding $\overline{RP} = V_{IH}$ or $\overline{WP} = V_{IL}$. Block erase and word write operations are not guaranteed with $V_{CC} < 3.0$ V or $V_{IH} < \overline{RP} < V_{HH}$ and should not be attempted.
8. $\overline{RP}$ connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.

FLASH AC CHARACTERISTICS — READ ONLY OPERATIONS[1]

V_{CC} = 2.7 V to 3.6 V, T_A = 40°C to +85°C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{AVAV}	Read Cycle Time	120		ns	
t_{AVQV}	Address to Output Delay		120	ns	
t_{ELQV}	$\overline{CE}$ to Output Delay		120	ns	2
t_{PHQV}	$\overline{RP}$ HIGH to Output Delay		600	ns	
t_{GLQV}	$\overline{OE}$ to Output Delay		50	ns	2
t_{ELQX}	$\overline{CE}$ to Output in LOW Z	0		ns	3
t_{EHQZ}	$\overline{CE}$ HIGH to Output in HIGH Z		55	ns	3
t_{GLQX}	$\overline{OE}$ to Output in LOW Z	0		ns	3
t_{GHQZ}	$\overline{OE}$ HIGH to Output in HIGH Z		20	ns	3
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Change, Whichever Occurs First	0		ns	3

NOTES:
1. See 'AC Input/Output Reference Waveform' section for maximum allowable input slew rate.
2. $\overline{OE}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{CE}$ without impact on t_{ELQV}.
3. Sampled, not 100% tested.

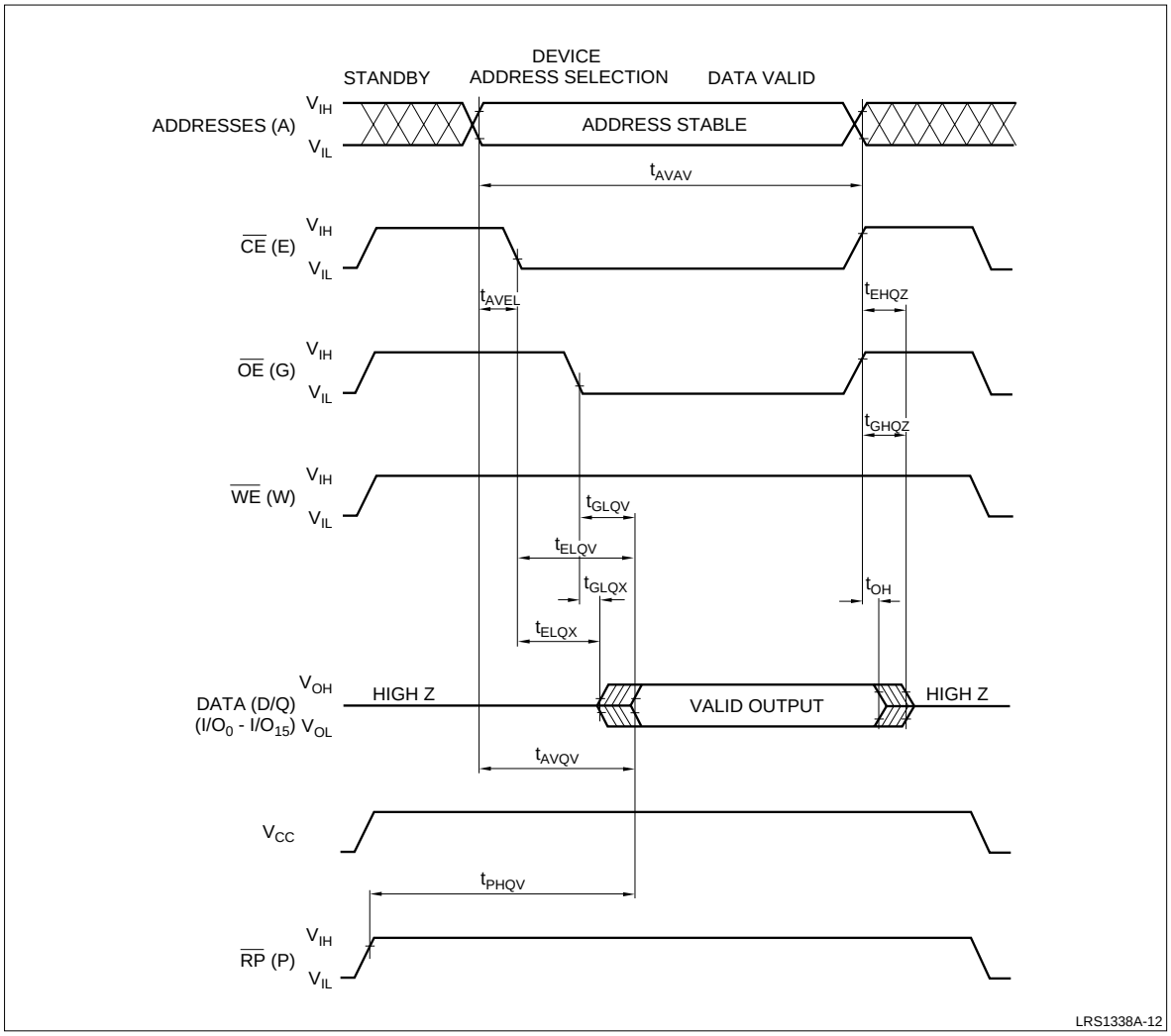


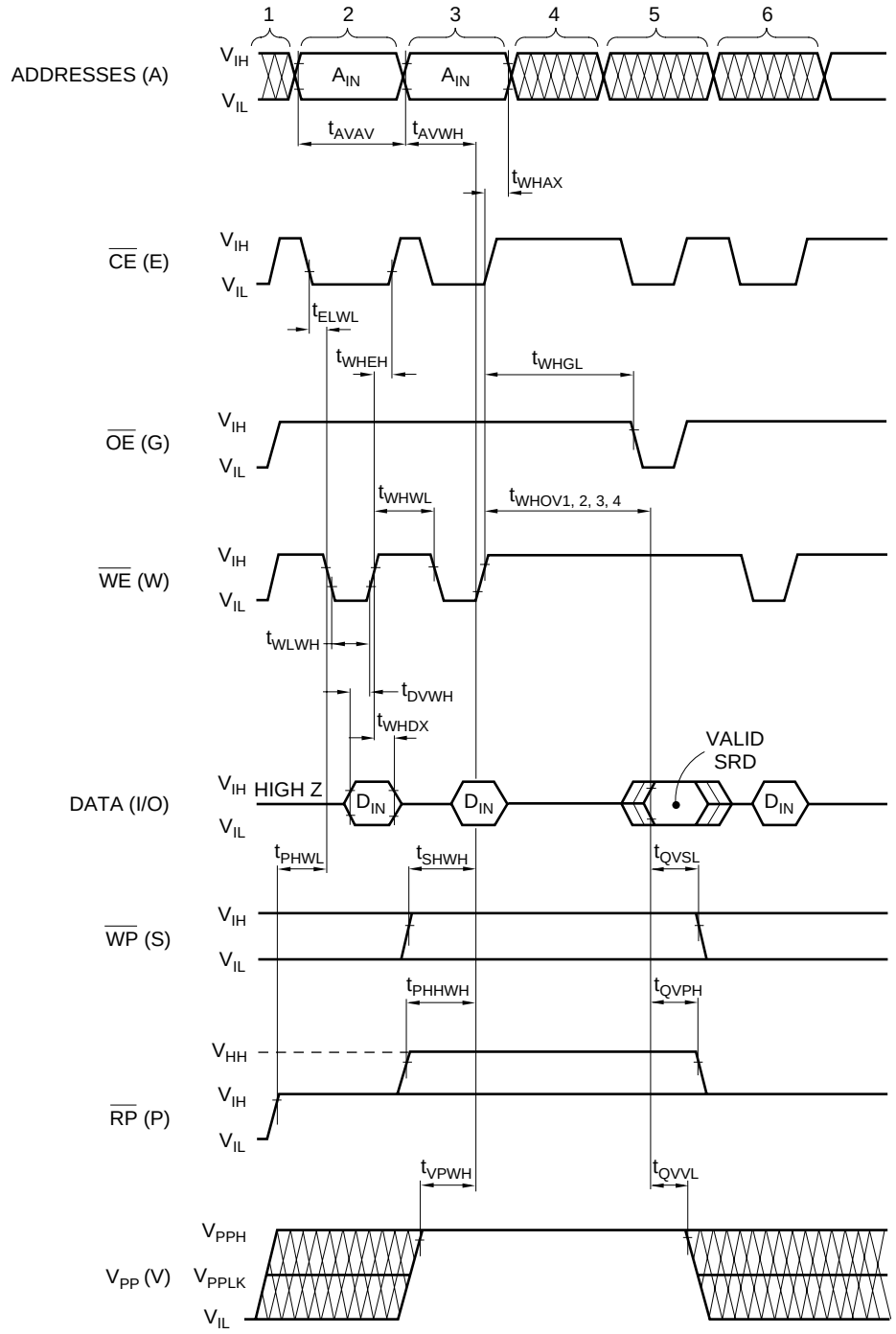
Figure 12. AC Waveforms for Read Operations

FLASH AC CHARACTERISTICS — WRITE OPERATIONS[1]

V_{CC} = 2.7 V to 3.6 V, T_A = -40°C to +85°C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{AVAV}	Write Cycle Time	120		ns	
t_{PHWL}	$\overline{RP}$ HIGH Recovery to $\overline{WE}$ Going LOW	1		µs	2
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going LOW	10		ns	
t_{WLWH}	$\overline{WE}$ Pulse Width	50		ns	
t_{PHHWH}	$\overline{RP}$ V_{HH} to $\overline{WE}$ Going HIGH	100		ns	2
t_{SHWH}	$\overline{WP}$ V_{IH} Setup to $\overline{WE}$ Going HIGH	100		ns	2
t_{VPWH}	V_{PP} Setup to $\overline{WE}$ Going HIGH	100		ns	2
t_{AVWH}	Address Setup to $\overline{WE}$ Going HIGH	50		ns	3
t_{DVWH}	Data Setup to $\overline{WE}$ Going HIGH	50		ns	3
t_{WHDX}	Data Hold from $\overline{WE}$ HIGH	5		ns	
t_{WHAX}	Address Hold from $\overline{WE}$ HIGH	5		ns	
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ HIGH	10		ns	
t_{WHWL}	$\overline{WE}$ Pulse Width HIGH	30		ns	
t_{WHGL}	Write Recovery before Read	0		ns	
t_{QVVL}	V_{PP} Hold from Valid SRD HIGH	0		ns	2, 4
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD HIGH	0		ns	2, 4
t_{QVSL}	$\overline{WP}$ V_{IH} Hold from Valid SRD HIGH	0		ns	2, 4

NOTES:
1. Read timing characteristics during block erase and word write operations are the same as during read-only operations. Refer to 'AC Characteristics' section for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 6 for valid A_{IN} and D_{IN} for block erase or word write.
4. V_{PP} should be held at V_{PPH} (and if necessary $\overline{RP}$ should be held at V_{HH}) until determination of block erase or word write success (SR.1, SR.3, SR.4, SR.5 = 0).



NOTES:
1. V_{CC} power-up and standby.
2. Write block erase or word write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

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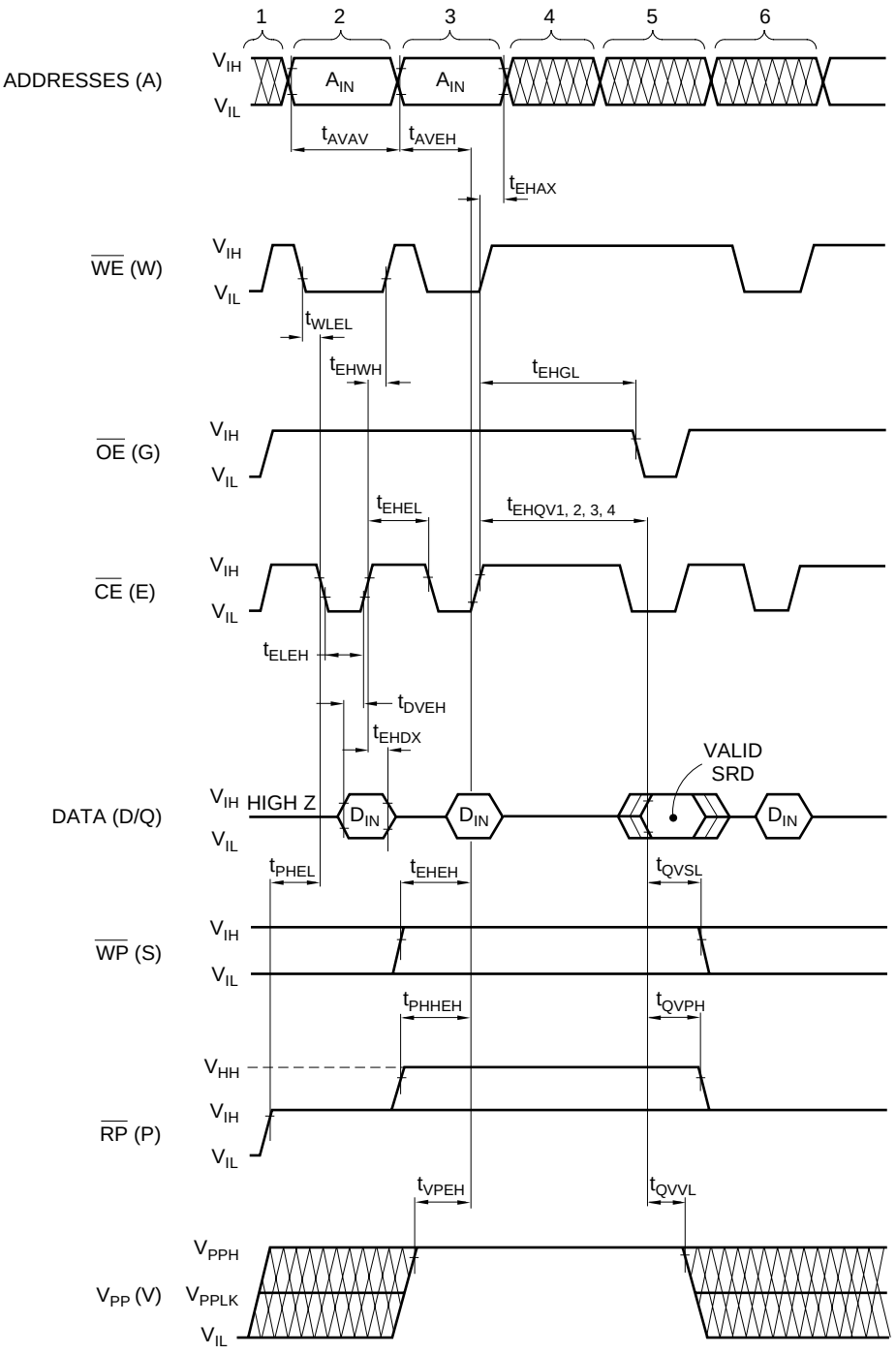
Figure 13. AC Waveform for $\overline{WE}$ Controlled Write Operations

ALTERNATIVE $\overline{CE}$ CONTROLLED WRITES[1]

V_{CC} = 2.7 V to 3.6 V, T_A = 40°C to +85°C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{AVAV}	Write Cycle Time	120		ns	
t_{PHEL}	$\overline{RP}$ HIGH Recovery to $\overline{CE}$ Going LOW	1		µs	2
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going LOW	0		ns	
t_{ELEH}	$\overline{CE}$ Pulse Width	70		ns	
t_{PHHEH}	$\overline{RP}$ V_{HH} Setup to $\overline{CE}$ Going HIGH	100		ns	2
t_{SHEH}	$\overline{WP}$ V_{IH} Setup to $\overline{CE}$ Going HIGH	100		ns	2
t_{VPEH}	V_{PP} Setup to $\overline{CE}$ Going HIGH	100		ns	2
t_{AVEH}	Address Setup to $\overline{CE}$ Going HIGH	50		ns	3
t_{DVEH}	Data Setup to $\overline{CE}$ Going HIGH	50		ns	3
t_{EHDX}	Data Hold from $\overline{CE}$ HIGH	5		ns	
t_{EHAX}	Address Hold from $\overline{CE}$ HIGH	5		ns	
t_{EHWH}	$\overline{WE}$ Hold from $\overline{CE}$ HIGH	0		ns	
t_{EHEL}	$\overline{CE}$ Pulse Width HIGH	25		ns	
t_{EHGL}	Write Recovery before Read	0		ns	
t_{QVVL}	V_{PP} Hold from Valid SRD HIGH	0		ns	2, 4
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD HIGH	0		ns	2, 4
t_{QVSL}	$\overline{WP}$ V_{IH} Hold from Valid SRD HIGH	0		ns	2, 4

NOTES:
1. In systems where $\overline{CE}$ defines the write pulse width (within a longer $\overline{WE}$ timing waveform), all setup, hold, and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.
2. Sampled, not 100% tested.
3. Refer to Table 6 for valid A_{IN} and D_{IN} for block erase or word write.
4. V_{PP} should be held at V_{PPH} (and if necessary $\overline{RP}$ should be held at V_{HH}) until determination of block erase or word write success (SR.1, SR.3, SR.4, SR.5 = 0).



NOTES:
1. V_{CC} power-up and standby.
2. Write block erase or word write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

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Figure 14. Alternate AC Waveform for $\overline{CE}$ Controlled Write Operations

RESET OPERATIONS

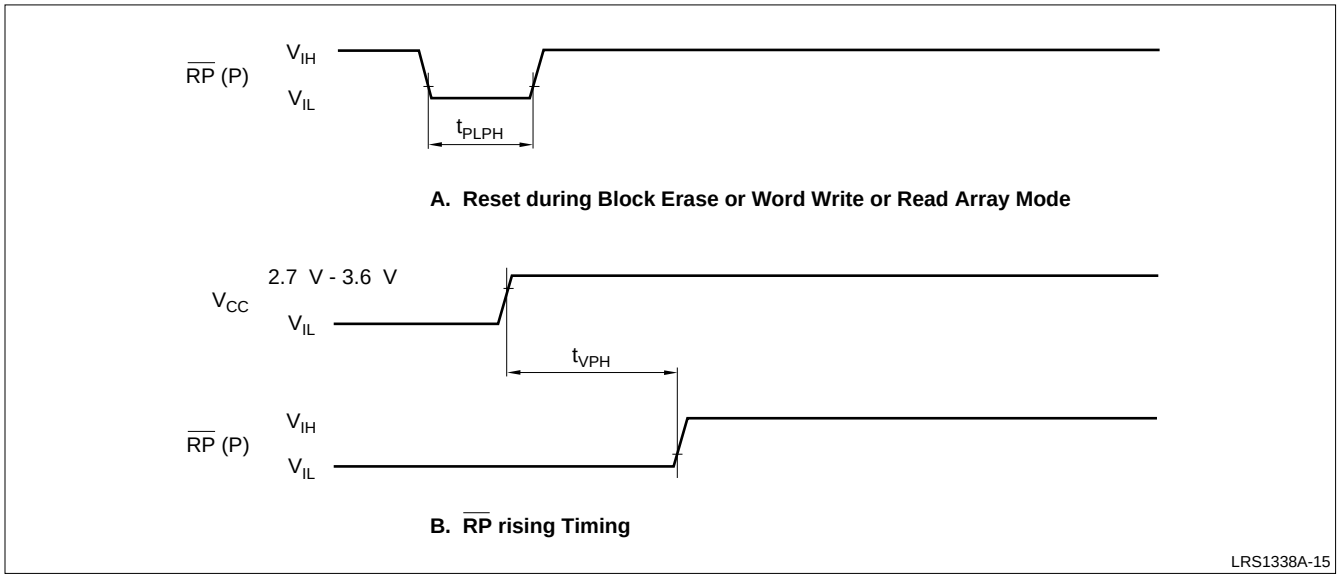


Figure 15. AC Waveform for Reset Operation

Table 11. Reset AC Specifications

SYMBOL	PARAMETER	V_{CC} = 2.7 V to 3.6 V		UNIT	NOTES
		MIN.	MAX.		
t_{PLPH}	$\overline{RP}$ Pulse LOW Time (if $\overline{RP}$ is tied to V_{CC}, this specification is not applicable)	100		ns	1
t_{VPH}	V_{CC} 2.7 V to $\overline{RP}$ HIGH	100		ns	2

NOTES:
1. If $\overline{RP}$ is asserted while a block erase or word write operation is not executing, the reset will complete within 100 ns.
2. When the device power-up holding $\overline{RP}$ LOW minimum 100 ns is required after V_{CC} has been in predefined range and also has been stable there.

BLOCK ERASE AND WORD WRITE PERFORMANCE[1]

V_{CC} = 2.7 V to 3.6 V, T_A = 40°C to +85°C

SYMBOL	PARAMETER	V_{PP} = 2.7 V to 3.6 V			UNIT	NOTES
		MIN.	MAX.	TYP.[2]		
t_{WHQV1} t_{EHQV1}	Word Write Time 32K-word Block			44.6	µs	3
	Word Write Time 4K-word Block			45.9	µs	3
	Block Write Time 32K-word Block			1.46	sec	3
	Block Write Time 4K-word Block			0.19	sec	3
t_{WHQV2} t_{EHQV2}	Block Erase Time 32K-word Block			1.14	sec	3
	Block Erase Time 4K-word Block			0.38	sec	3
t_{WHRH1}, t_{EHRH1}	Word Write Suspend Latency Time to Read		7	8	µs	
t_{WHRH2}, t_{EHRH2}	Erase Suspend Latency Time to Read		18	22	µs	

NOTES:
1. Sampled, but not 100% tested.
2. Typical values measured at T_A = +25°C and nominal voltages. Subject to change based on device characterization.
3. Excludes system-level overhead.

SRAM*

Description

The LRS1388A is a 2M bit static RAM organized as 262,144 × 8 bit which provides low-power standby mode.

Features

- Access Time: 85 ns (MAX.)
- Operating Current:
  - 40 mA (MAX.)
  - 25 mA (MAX.)
- Standby Current: 40 µA (MAX.)
- Data Retention Current: 0.6 µA (TYP. V_{CCDR} = 3 V, T_A = 25°C)
- Single Power Supply: 2.7 V to 3.6 V
- Operating Temperature: -40°C to +85°C
- Fully Static Operation
- Three-state Output
- Not Designed or Rated as Radiation Hardened
- P-Type Bulk Silicon

**NOTE: ***In the SRAM section all reference to pins, commands, voltage, etc. refer only to the SRAM portion of this chip.

Table 12. Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_0 - I/O_7	SUPPLY CURRENT
H	X	X	Standby	HIGH Impedance	Standby (I_{SB})
L	L	X	Write	Data Input	Active (I_{CC})
L	H	L	Read	Data Output	Active (I_{CC})
L	H	H	Output Disable	HIGH Impedance	Active (I_{CC})

NOTE: X = Don't care, L= LOW, H = HIGH.

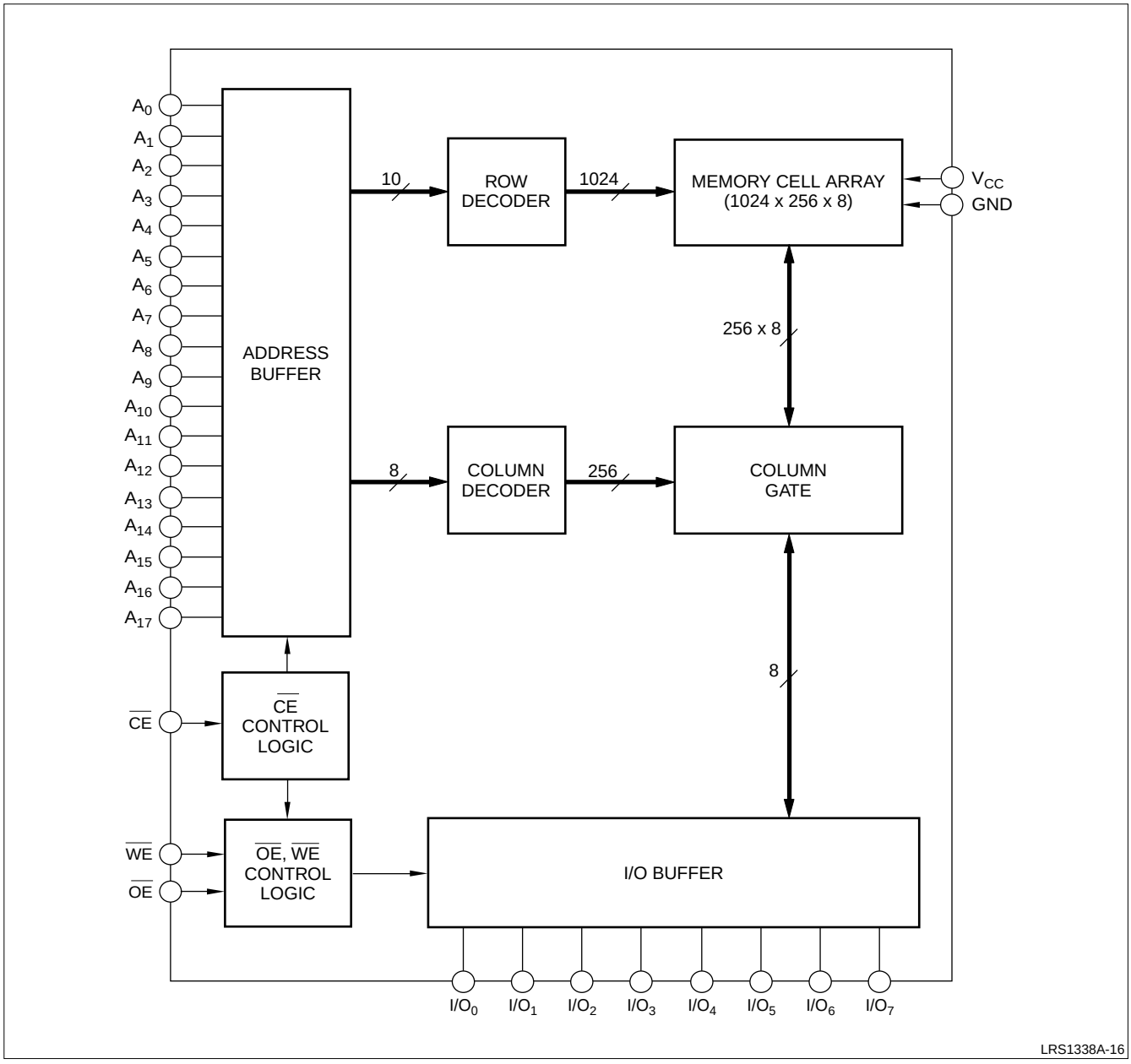


Figure 16. SRAM Block Diagram

SRAM Absolute Maximum Ratings

PARAMETER	SYMBOL	RATINGS	UNIT	NOTES
Supply voltage	V_{CC}	-0.2 to +4.6	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1, 2
Operating temperature	T_{OPR}	-40 to +85	°C	
Storage temperature	T_{STG}	-65 to +125	°C	

NOTES:
1. The maximum applicable voltage on any pins with respect to GND.
2. -2.0 V undershoot is allowed when the pulse width is less than 20 ns.

SRAM Recommended DC Operating Conditions

T_A = -40°C to +85°C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
Input voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
	V_{IL}	-0.3		0.8	V	1

NOTES:
1. -2.0 V undershoot is allowed when the pulse width is less than 20 ns.

SRAM DC Electrical Characteristics

T_A = -40°C to + 85°C, V_{CC} = 2.7 V to 3.6 V

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.*	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = 0V to V_{CC}	-1.0		1.0	µA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = 0 V to V_{CC}	-1.0		1.0	µA
Operating supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH} t_{CYCLE} = MIN., $I_{I/O}$ = 0 mA			40	mA
	I_{CC2}	$\overline{CE}$ ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or ≤ 0.2 V t_{CYCLE} = 200 ns, $I_{I/O}$ = 0 mA			25	mA
Standby current	I_{SB}	$\overline{CE}$ ≥ V_{CC} – 0.2 V		0.6	40	µA
	I_{SB1}	$\overline{CE}$ = V_{IH}			3.0	mA
Output voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4			V

NOTES: *Reference value at T_A = 25°C, V_{CC} = 3.0 V.

SRAM AC Electrical Characteristics

AC TEST CONDITIONS

PARAMETER	RATINGS
Input pulse level	0.6 V to 2.2 V
Input rise and fall time	5 ns
Input and output timing reference level	1.5 V
Output load*	1 TTL + C_L (30 pF)

NOTE: *Including scope and jig capacitance.

READ CYCLE

T_A = -40°C to + 85°C, V_{CC} = 2.7 V to 3.6 V

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read cycle time	t_{RC}	85		ns
Address access time	t_{AA}		85	ns
$\overline{CE}$ access time	t_{ACE}		85	ns
Output enable to output valid	t_{OE}		45	ns
Output hold from address change	t_{OH}	10		ns
$\overline{CE}$ LOW to output active*	t_{LZ}	10		ns
$\overline{OE}$ LOW to output active*	t_{OLZ}	5		ns
$\overline{CE}$ HIGH to output in HIGH impedance*	t_{HZ}	0	30	ns
$\overline{OE}$ HIGH to output in HIGH impedance*	t_{OHZ}	0	30	ns

NOTE: *Active output to HIGH impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

WRITE CYCLE

T_A = -40°C to + 85°C, V_{CC} = 2.7 V to 3.6 V

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write cycle time	t_{WC}	85		ns
Chip enable to end of write	t_{CW}	75		ns
Address valid to end of write	t_{AW}	75		ns
Address setup time	t_{AS}	0		ns
Write pulse width	t_{WP}	65		ns
Write recovery time	t_{WR}	0		ns
Input data setup time	t_{DW}	35		ns
Input data hold time	t_{DH}	0		ns
$\overline{WE}$ HIGH to output active*	t_{OW}	5		ns
$\overline{WE}$ LOW to output in HIGH impedance*	t_{WZ}	0	30	ns
$\overline{OE}$ HIGH to output in HIGH impedance*	t_{OHZ}	0	30	ns

NOTE: *Active output to HIGH impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

DATA RETENTION CHARACTERISTICS

T_A = -40°C to + 85°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V	2		3.6	V
Data retention supply voltage	I_{CCDR}	V_{CCDR} = 3 V, $\overline{CE} \geq V_{CCDR}$ – 0.2 V, T_A = 25°C		0.6	1.0	µA
		V_{CCDR} = 3 V, $\overline{CE} \geq V_{CCDR}$ – 0.2 V			35	µA
Chip enable setup time	t_{CDR}		0			ns
Chip enable hold time	t_R		5			ms

Timing Diagrams

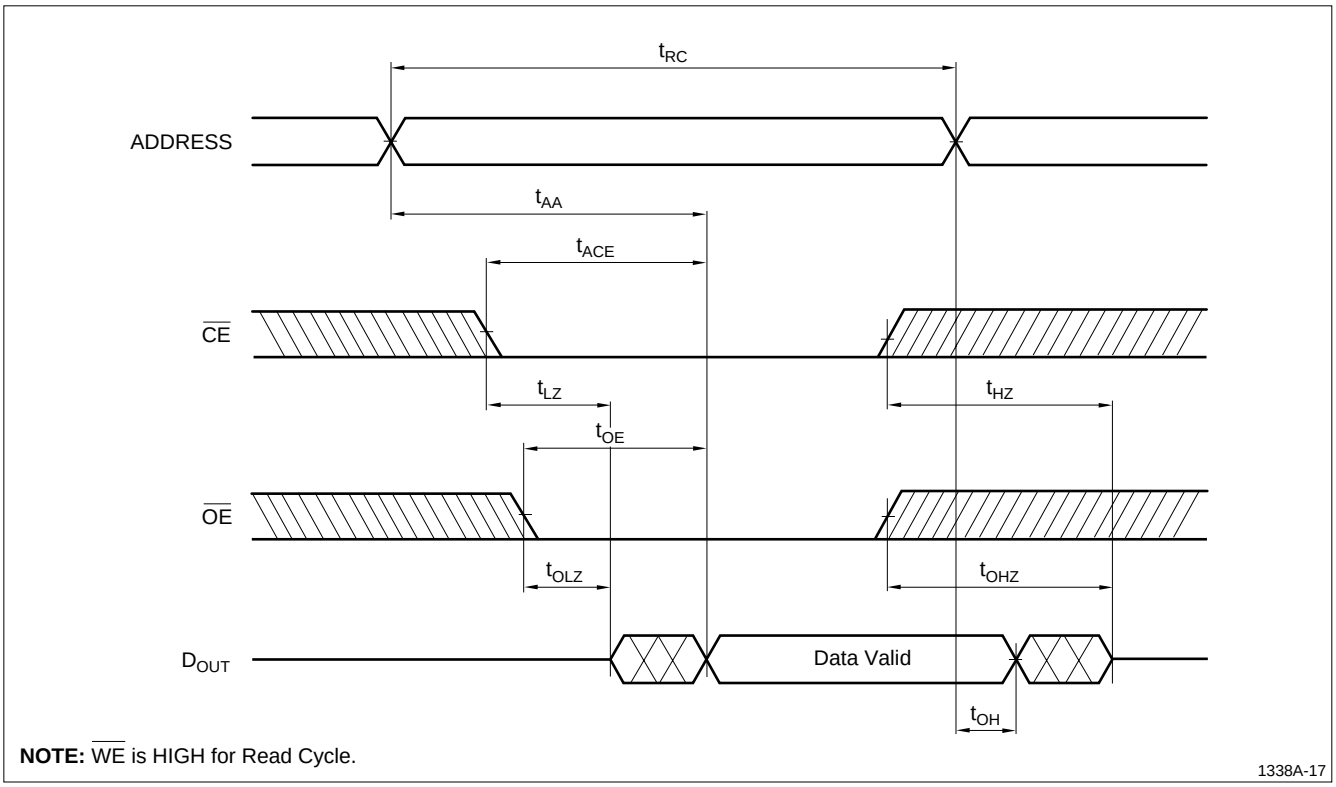
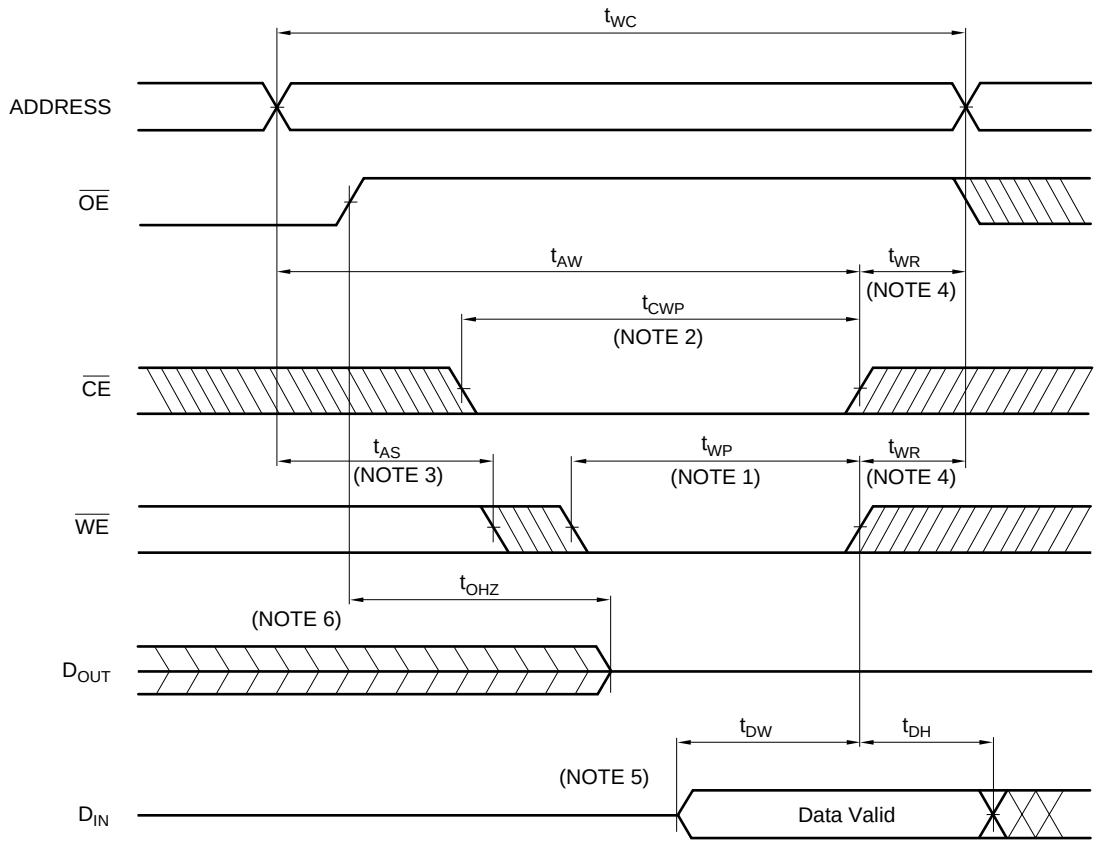


Figure 17. Read Cycle Timing Diagram



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CE}$ and a LOW $\overline{WE}$.
   A write begins at the latest transition among $\overline{CE}$ going LOW and $\overline{WE}$ going LOW.
   A write ends at the earliest transition among $\overline{CE}$ going HIGH and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CE}$ going LOW to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at $\overline{CE}$ or $\overline{WE}$ going HIGH.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CE}$ goes LOW simultaneously with $\overline{WE}$ going LOW or after $\overline{WE}$ going LOW, the outputs remain in HIGH impedance state.
7. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH or before $\overline{WE}$ going HIGH, the outputs remain in HIGH impedance state.

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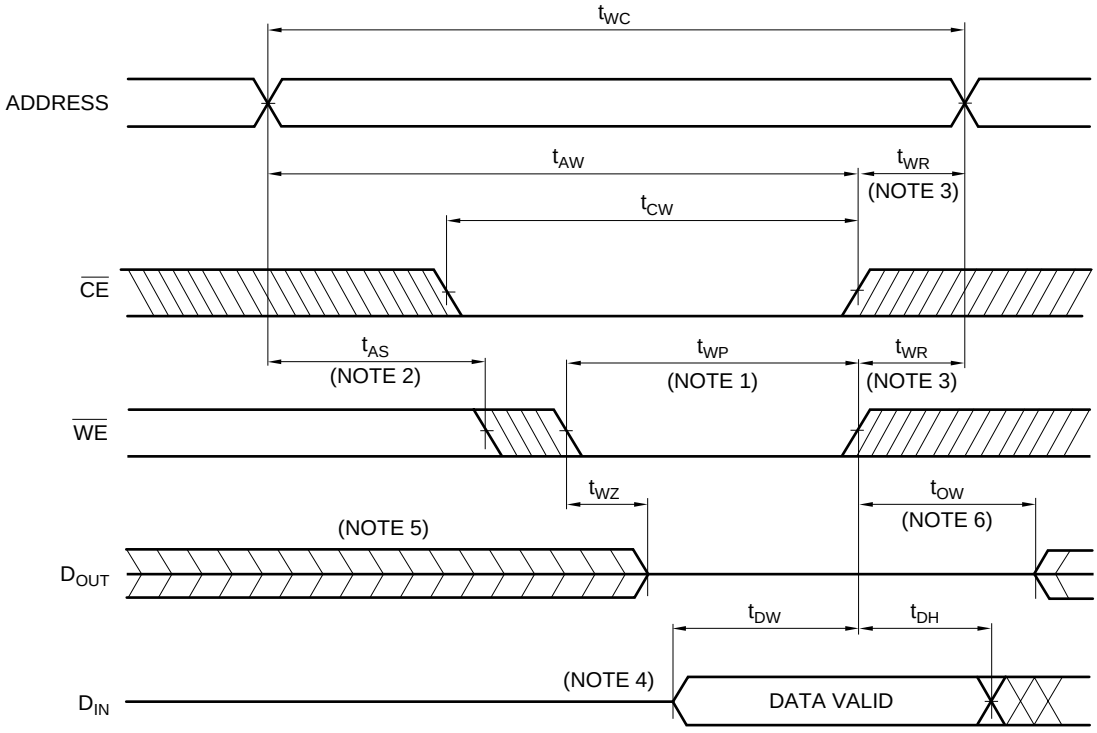
Figure 18. Write Cycle Timing Diagram ($\overline{OE}$ Controlled)



NOTES:

1. t_{CW} is measured from the later of $\overline{CE}$ going LOW to the end of write.
2. t_{AS} is measured from the address valid to the beginning of write.
3. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at $\overline{CE}$ or $\overline{WE}$ going HIGH.
4. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
5. If $\overline{CE}$ goes LOW simultaneously with $\overline{WE}$ going LOW or after $\overline{WE}$ going LOW, the outputs remain in HIGH impedance state.
6. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH or before $\overline{WE}$ going HIGH, the outputs remain in HIGH impedance state.

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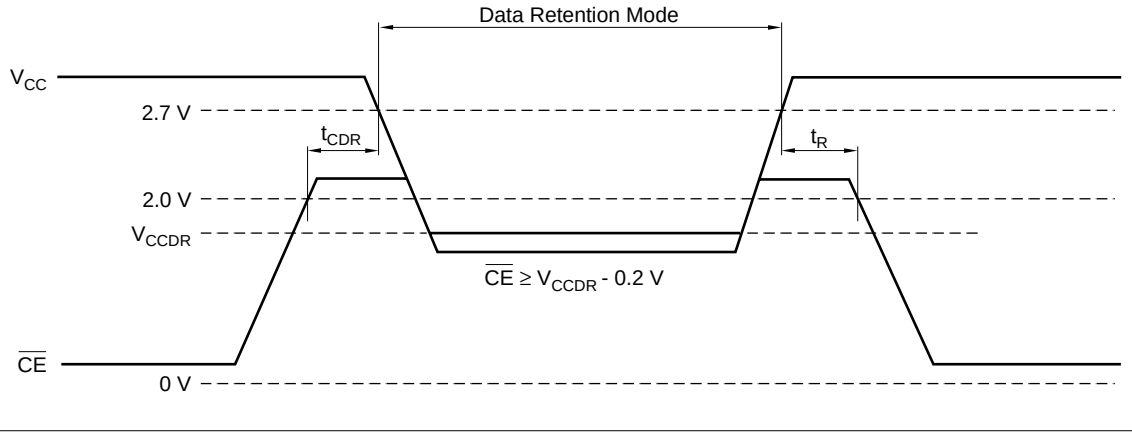
Figure 19. Write Cycle Timing Diagram ($\overline{OE}$ LOW Fixed)

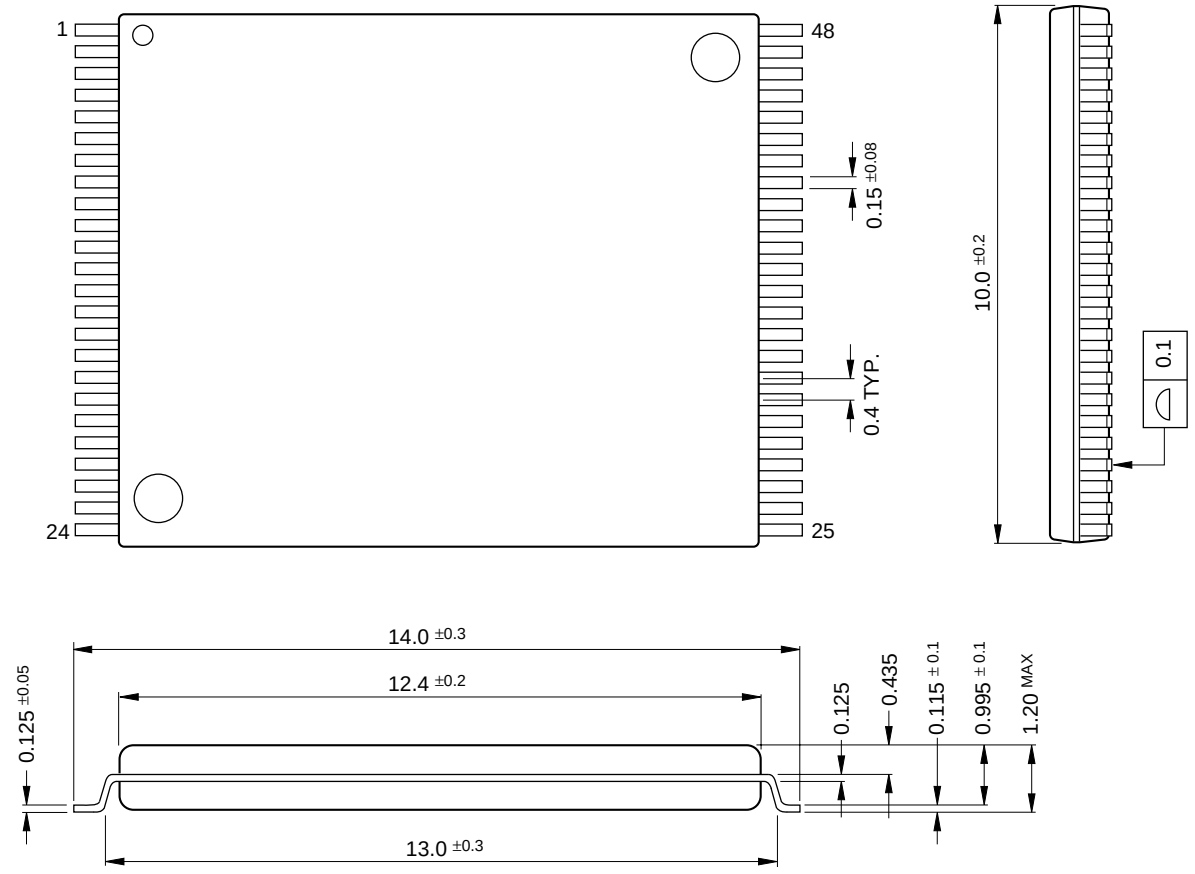


1338A-20

Figure 20. Data Retention Timing Diagram

OUTLINE DIMENSIONS

48TSOP (TSOP48-P-1014)



NOTE: Dimensions are in mm.

48TSOP2

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