

S71VS/XS-R Memory Subsystem Solutions

MirrorBit® 1.8 Volt-only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory and Burst Mode pSRAM

**256/128/64 Mb (16/8/4 Mb x 16-bit) Flash,
128/64/32 Mb (8/4/2 Mb x 16-bit) pSRAM**

Data Sheet



Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See [Notice On Data Sheet Designations](#) for definitions.

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Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

“This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur.”

Questions regarding these document designations may be directed to your local sales office.

S71VS/XS-R Memory Subsystem Solutions

MirrorBit® 1.8 Volt-only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory and Burst Mode pSRAM

256/128/64 Mb (16/8/4 Mb x 16-bit) Flash, 128/64/32 Mb (8/4/2 Mb x 16-bit) pSRAM



Data Sheet

Features

- Power supply voltage of 1.7 V to 1.95 V
- Flash Burst Speed: 104 MHz, 83 MHz
- pSRAM Burst Speed: 104 MHz
- MCP BGA Packages
 - 52 ball, 7.5 x 5.0 mm, 0.5 mm ball pitch
 - 56 ball, 7.7 x 6.2 mm, 0.5 mm ball pitch
 - 56 ball, 9.2 x 8.0 mm, 0.5 mm ball pitch
- Operating Temperature
 - Wireless, -25°C to +85°C

General Description

The S71VS-R Series is a product line of stacked Multi-Chip Package (MCP) memory solutions and consists of the following items:

- One or more S29VS-R or S29XS-R Flash memory die
- One or more pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to their individual datasheet for further details.

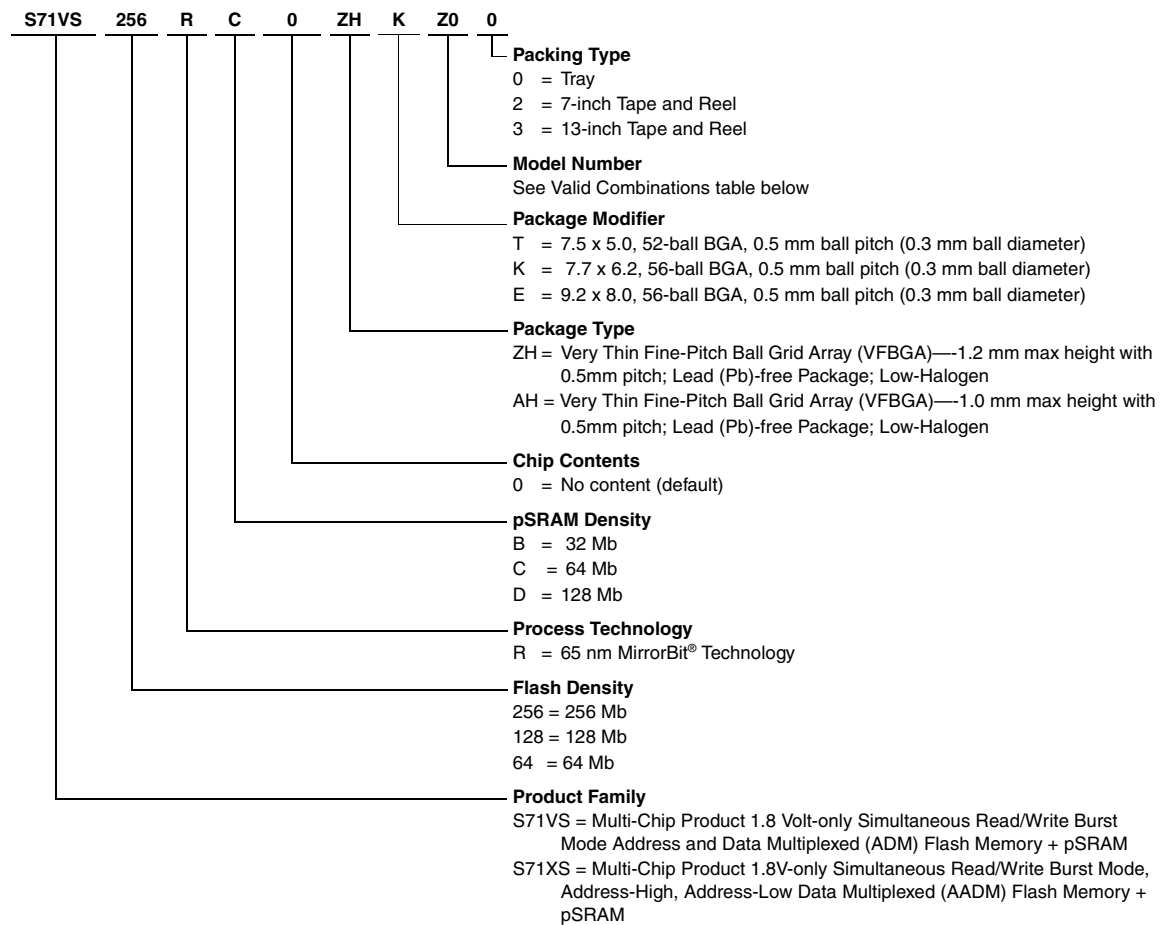
Flash Density	pSRAM Density	Product
64 Mb	32 Mb	S71VS064RB0
128 Mb	64 Mb	S71VS128RC0
256 Mb	64 Mb	S71VS256RC0
256 Mb	128 Mb	S71VS256RD0
256 Mb	128 Mb	S71XS256RD0

For detailed specifications, please refer to the individual data sheets:

Document	Publication Identification Number
S29VS-R	S29VS_XS-R_00
S29XS-R	S29VS_XS-R_00
128 Mb MUX pSRAM Type 5	pSRAM_39
64 Mb MUX pSRAM Type 3	muxpsram_15
32 Mb MUX pSRAM	CustComspec_01

1. Ordering Information

The order number is formed by a valid combinations of the following:



1.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Base Ordering Part Number	Package	Model Number	Packing Type	pSRAM Type	pSRAM Speed	Flash Boot	Flash Speed
S71VS064RB0	AHT	00	0, 2, 3	Mux pSRAM	104 MHz	Top Boot	104 MHz
		04				Top Boot	83 MHz
		80				Bottom Boot	104 MHz
		84				Bottom Boot	83 MHz
S71VS128RC0	AHK	20		Mux pSRAM Type 3		Top Boot	104 MHz
S71VS128RC0	ZHK	20		Mux pSRAM Type 3		Top Boot	104 MHz
		A0				Bottom Boot	
		24				Top Boot	83 MHz
		A4				Bottom Boot	
S71VS256RC0		20				Top Boot	104 MHz
		A0				Bottom Boot	
		24				Top Boot	83 MHz
		A4				Bottom Boot	
S71VS256RD0	ZHE	40		Mux pSRAM Type 5		Top Boot	104 MHz
		C0				Bottom Boot	
		44				Top Boot	83 MHz
		C4	Bottom Boot				
S71XS256RD0		40	Top Boot		104 MHz		
		C0	Bottom Boot				
		44	Top Boot		83 MHz		
		C4	Bottom Boot				

2. Input/Output Descriptions

Table 2.1 identifies the input and output package connections provided on the device.

Table 2.1 Input/Output Descriptions

Symbol	Description	Flash	RAM
AMAX – A16	Address inputs	X	X
A/DQ15-A/DQ0	Multiplexed Address/Data	X	X
OE#	Output Enable input. Asynchronous relative to CLK for the Burst mode.	X	X
WE#	Write Enable input.	X	X
V _{SS}	Ground	X	X
V _{SSQ}	Input/Output Ground	X	X
NC	No Connect; not connected internally	X	X
F-RDY/R-WAIT	Ready output; indicates the status of the Burst read. Flash Memory RDY (using default "Active HIGH" configuration) V _{OL} = data invalid V _{OH} = data valid Note: The default polarity for the pSRAM WAIT signal is opposite the default polarity of the Flash RDY signal. pSRAM WAIT (using default "Active HIGH" configuration) V _{OL} = data valid V _{OH} = data invalid To match polarities, change bit 10 of the pSRAM Bus Configuration Register to 0 (Active LOW WAIT). Alternately, change bit 10 of the Flash Configuration Register to 0 (Active LOW RDY)	X	X
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V _{IL} or V _{IH} while in asynchronous mode	X	X
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs. Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched. High = device ignores address inputs	X	X
F-RST#	Hardware reset input. Low = device resets and returns to reading array data	X	
F-V _{PP}	Accelerated input. At V _{IHH} , accelerates programming; automatically places device in unlock bypass mode. At V _{IL} , disables all program and erase functions. Should be at V _{IH} for all other conditions.	X	
R-CE#	Chip-enable input for pSRAM.		X
F-CE#	Chip-enable input for Flash. Asynchronous relative to CLK for Burst Mode.	X	
R-CRE	Control Register Enable (pSRAM).		X
V _{CC}	Flash and pSRAM 1.8 Volt-only single power supply.	X	X
V _{CCQ}	Flash and pSRAM Input/Output Power Supply	X	X
R-UB#	Upper Byte Control (pSRAM).		X
R-LB#	Lower Byte Control (pSRAM)		X
RFU	Reserved For Future Use		

3. MCP Block Diagram

Figure 3.1 S71VS-R MCP Block Diagram

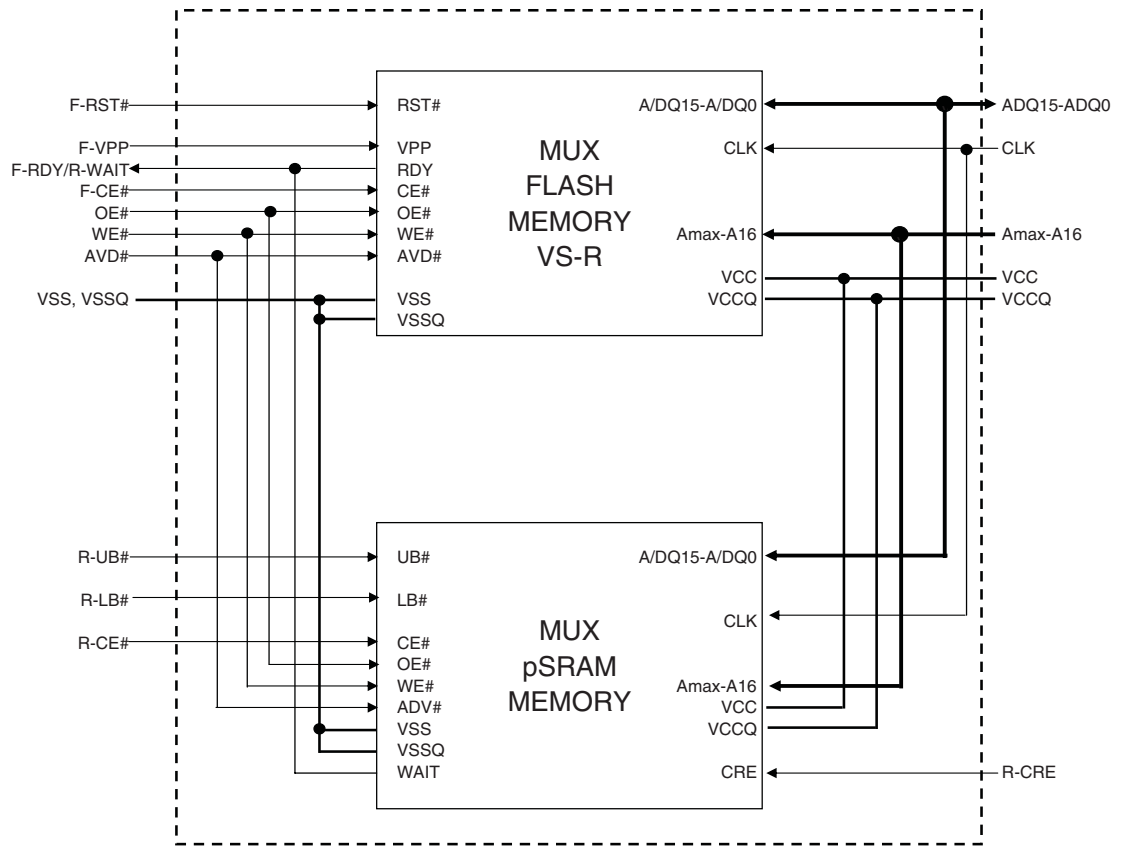
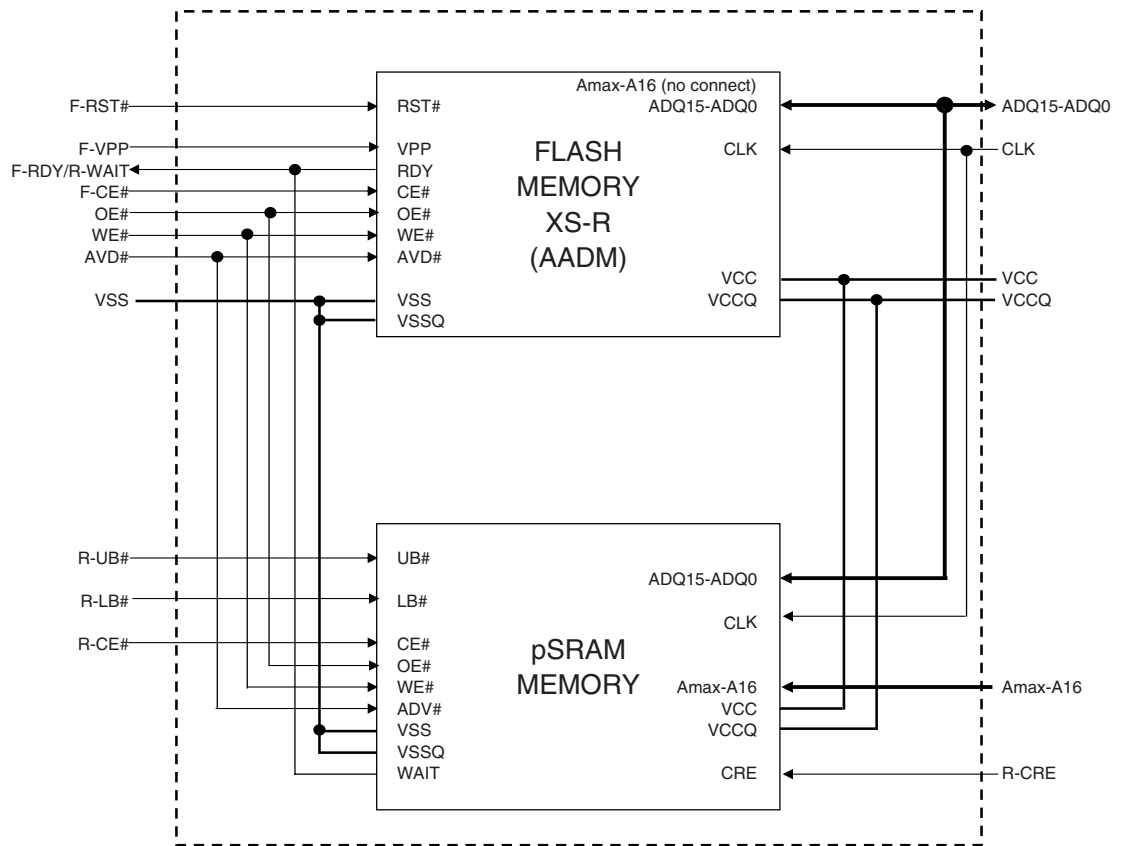


Figure 3.2 S71XS-R MCP Block Diagram



4. Connection Diagrams/Physical Dimensions

This section contains the I/O designations and package specifications for the S71VS-R.

4.1 Special Handling Instructions for FBGA Packages

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4.2 Connection Diagrams

Figure 4.1 S71VS-R 56-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)

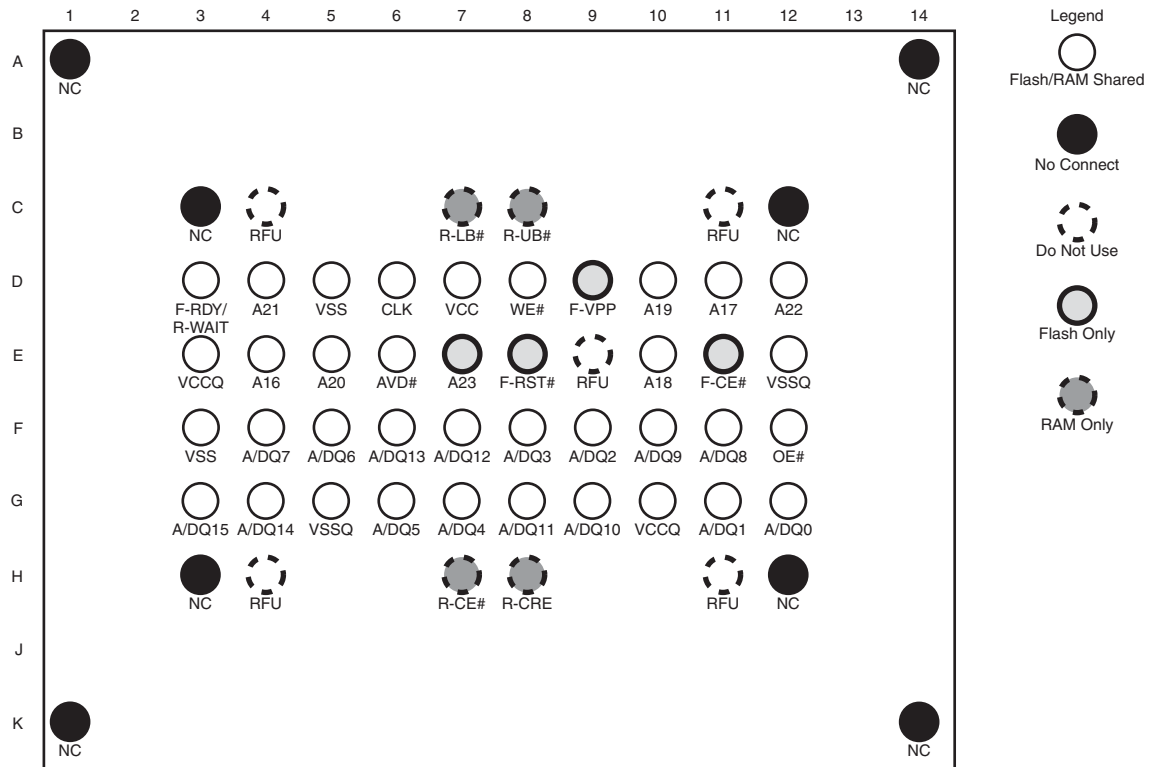
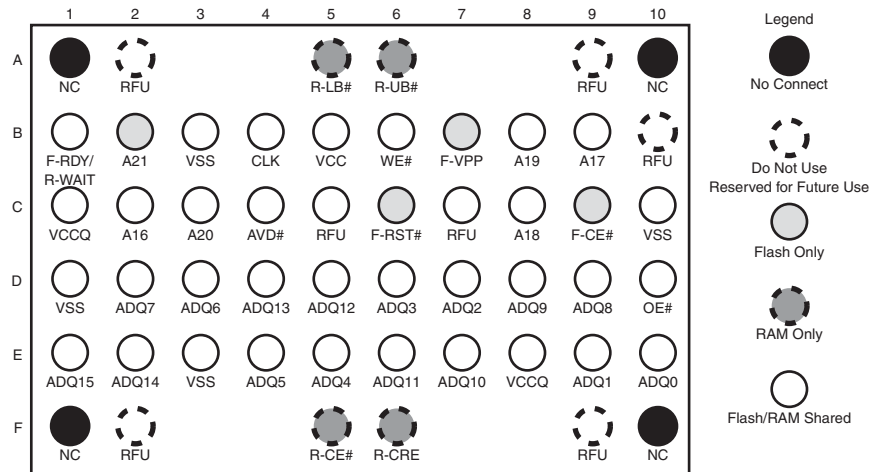


Figure 4.2 S71VS-R 52-ball Fine-Pitch Ball Grid Array

(Top View, Balls Facing Down)

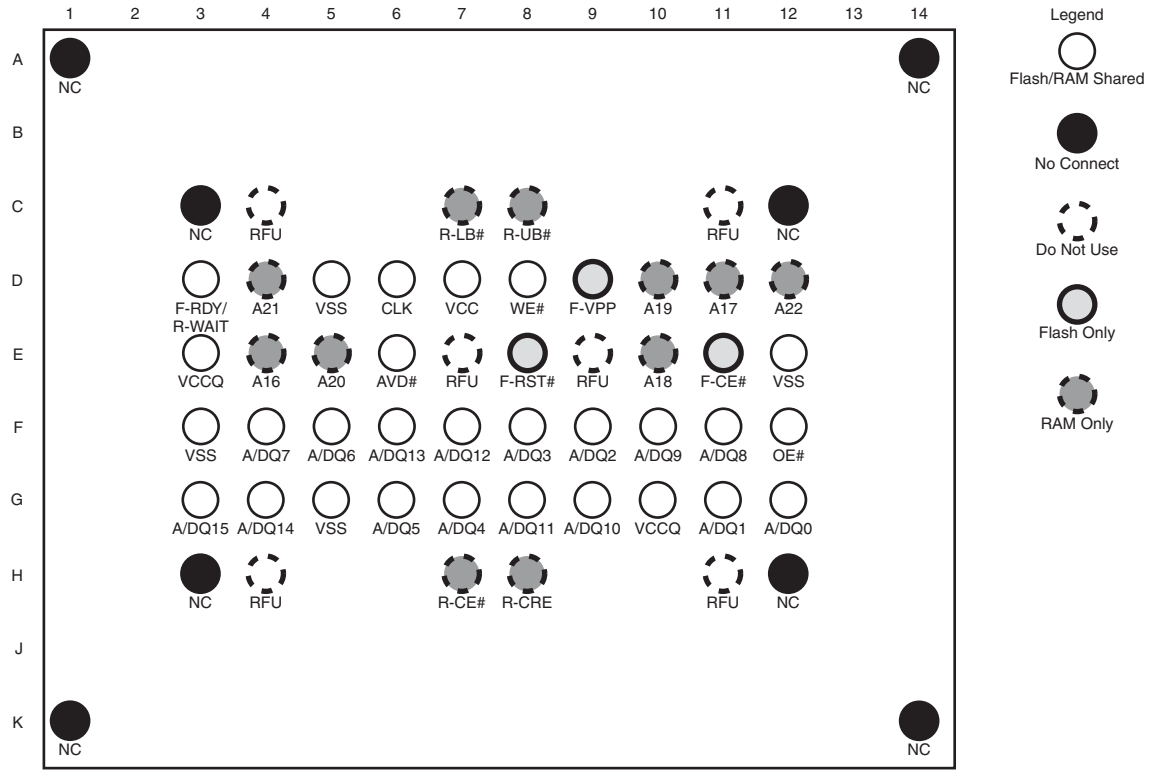


Notes

1. Addresses are shared between Flash and RAM depending on the density of the pSRAM.
2. V_{SS} and V_{SSQ} must be connected together.

MCP	Flash-Only Addresses	Shared Addresses	Shared ADQ Pins
S71VS064RB0	A21	A20-A16	A/DQ15-A/DQ0
S71VS128RC0	A22	A21-A16	
S71VS256RC0	A23-A22	A21-A16	
S71VS256RD0	A23	A22-A16	

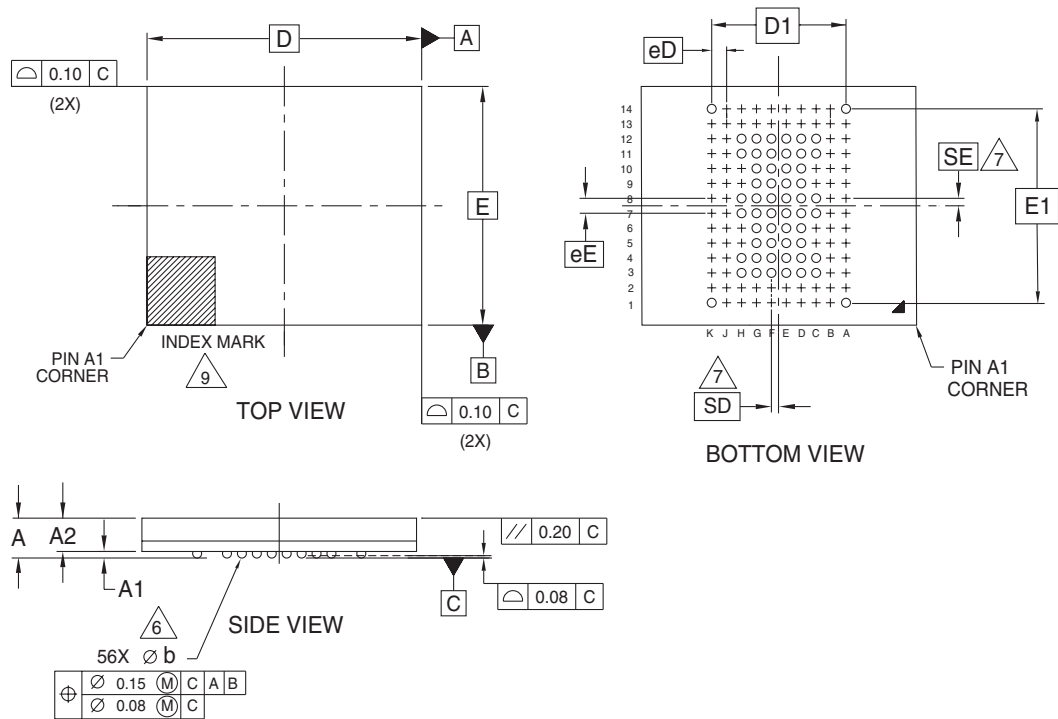
Figure 4.3 S71XS-R 56-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



MCP	pSRAM-Only Addresses	Shared Addresses	Shared ADQ Pins
S71XS256RD0	A22-A16	N/A	A/DQ15-A/DQ0

4.3 Physical Dimensions

Figure 4.4 NLB056—56-ball VFBGA 9.2 x 8.0 mm



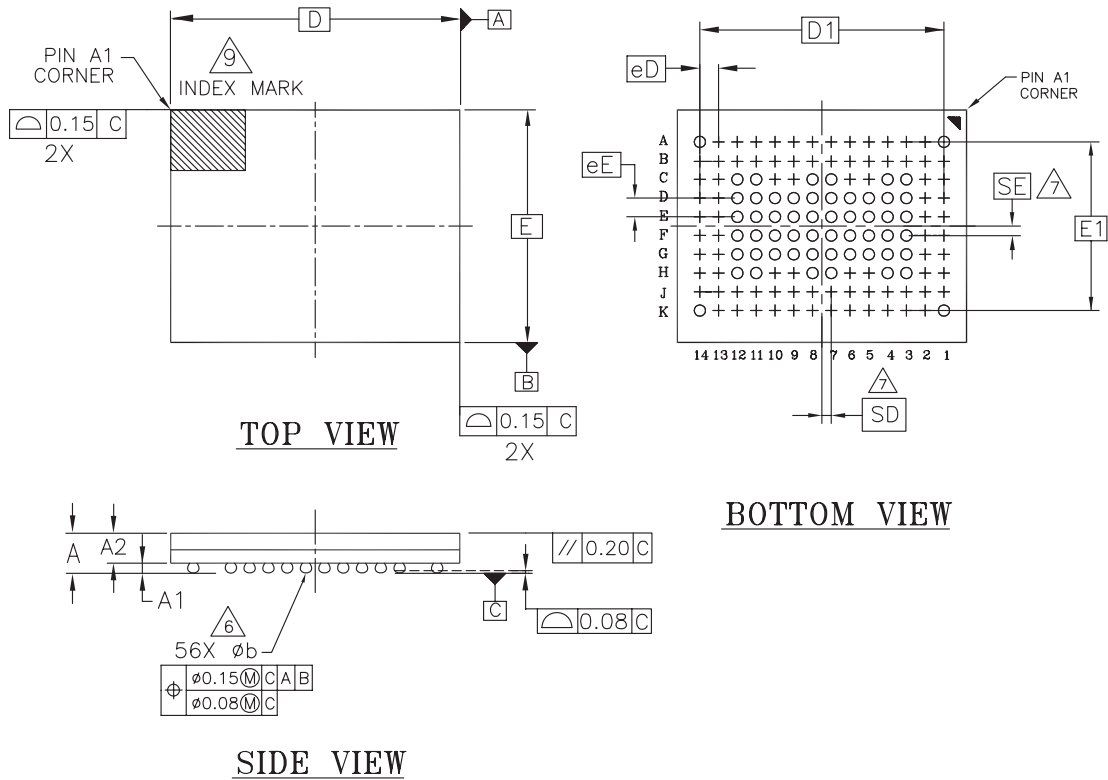
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $e/2$
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

PACKAGE	NLB 056			
JEDEC	N/A			
D x E	9.20 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.85	---	0.97	BODY THICKNESS
D	9.20 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	4.50 BSC.			MATRIX FOOTPRINT
E1	6.50 BSC.			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC.			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
	A2 - A13, B1 - B14 C1, C2, C5, C6, C9, C10, C13, C14 D1, D2, D13, D14, E1, E2, E13, E14, F1, F2, F13, F14 G1, G2, G13, G14, H1, H2, H5, H6, H9, H10, H13, H14 J1 - J14, K2 - K13			DEPOPULATED SOLDER BALLS

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Figure 4.5 NSD056—56-ball VFBGA 7.7 x 6.2 mm



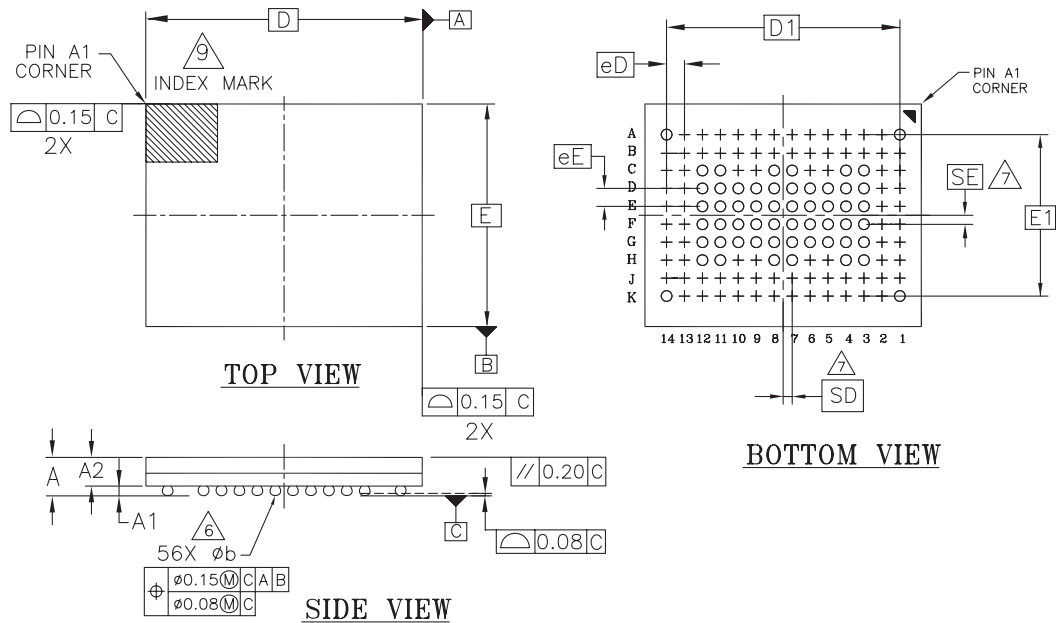
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

PACKAGE	NSD 056			
JEDEC	N/A			
D x E	7.70 mm x 6.20 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.85	---	0.97	BODY THICKNESS
D	7.70 BSC.			BODY SIZE
E	6.20 BSC.			BODY SIZE
D1	6.50 BSC.			MATRIX FOOTPRINT
E1	4.50 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC.			BALL PITCH
SD SE	0.25 BSC.			SOLDER BALL PLACEMENT
	A2~A9, B1~B10, C1,C2,C9,10,D1,D2,D9,D10 E1,E2,E3,E8,E9,E10,F1,F2,F3,F8,F9,F10,G1,G2,G9,G10 H1,H2,H9,H10,I1,I2,I3,I8,I9,I10,K1,K2,K9,K10 L1,L2,L9,L10,M1,M2,M9,M10, N1~N10, P2~P9			DEPOPULATED SOLDER BALLS

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Figure 4.6 RSD056—56-ball VFBGA 7.7 x 6.2 mm



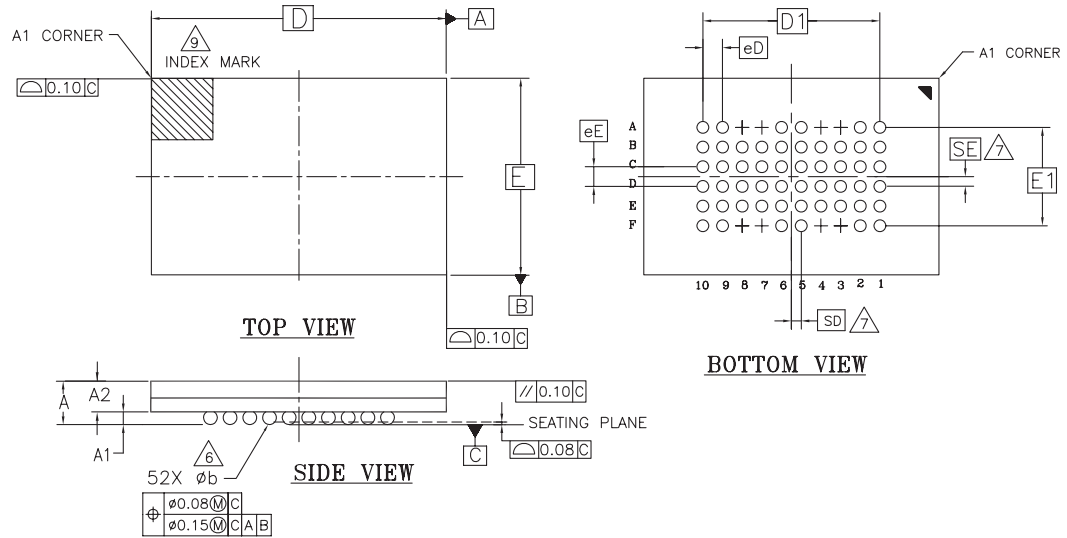
PACKAGE	RSD 056			NOTE
JEDEC	N/A			
D x E	7.70 mm x 6.20 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	0.80	0.90	1.00	PROFILE
A1	0.18	---	---	BALL HEIGHT
A2	0.62	---	0.74	BODY THICKNESS
D	7.70 BSC			BODY SIZE
E	6.20 BSC			BODY SIZE
D1	6.50 BSC			MATRIX FOOTPRINT
E1	4.50 BSC			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
ϕb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC			BALL PITCH
eD	0.50 BSC			BALL PITCH
SE SD	0.25 BSC			SOLDER BALL PLACEMENT
	<small>A2~A9, B1~B10, C1,C2,C9,10,D1,D2,D9,D10 E1,E2,E3,E8,E9,E10,F1,F2,F3,F9,F10,G1,G2,G9,G10 H1,H2,H9,H10,I1,I2,I3,I8,I9,I10,K1,K2,K3,K8,K9,K10 L1,L2,L9,L10,M1,M2,M9,M10, N1~N10, P2~P9</small>			DEPOPULATED SOLDER BALLS

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
- WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
- OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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Figure 4.7 RSB052—52-ball VFBGA 5.0 x 7.5 mm



PACKAGE	RSB 052			
JEDEC	N/A			
D x E	7.50 mm x 5.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	---	1.00	PROFILE
A1	0.18	---	---	BALL HEIGHT
A2	0.62	---	0.77	BODY THICKNESS
D	7.50 BSC			BODY SIZE
E	5.00 BSC			BODY SIZE
D1	4.50 BSC			MATRIX FOOTPRINT
E1	2.50 BSC			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME	6			MATRIX SIZE E DIRECTION
n	52			BALL COUNT
ϕb	0.25	0.30	0.35	BALL DIAMETER
e	0.50 BSC			BALL PITCH
SE/SD	0.25 BSC			BALL PITCH
	3A,3F,4A,4F,7A,7F,8A,8F			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

⚠ DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

⚠ SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

⚠ A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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5. Revision History

Section	Description
Revision 01 (August 25, 2008)	
	Initial release
Revision 02 (November 4, 2008)	
Global	Added OPNs S71VS064RB0AHT00/04/80/84
Connection Diagrams	Added S71VS-R 52-ball connection diagram
Physical Dimensions	Added RSB052
General Description	Changed 128 Mb Mux pSRAM PID from TBD to pSRAM_39
Revision 03 (November 10, 2008)	
General Description	Changed 64 Mb MUX pSRAM Type 3 PID from muxpsram_14 to muxpsram_15
Revision 04 (January 13, 2009)	
Physical Dimensions	Replaced NLD056 with NSD056
Revision 05 (January 23, 2009)	
Valid Combinations	Added OPN S71VS128RC0AHK20
Physical Dimensions	Added RSD056

Colophon

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