S72NS-S Based MCPs

MirrorBit® Eclipse™ Flash Memory and DRAM

2 Gb (128M x 16 bit), 1.8 Volt-only, Multiplexed Simultaneous Read/ Write, Burst Mode Flash Memory
512 Mb (32M x 16 bit) DDR DRAM on Split Bus

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S72NS-S_00 **Revision** 02 **Issue Date** January 9, 2009

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Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **Burst Speeds**
  - Flash = 104 MHz
  - DDR DRAM = 166 MHz
- **Packages**
  - 11.0 x 13.0 mm, 186-ball MCP
- **Operating Temperature of –25°C to +85°C**

General Description

This document contains information on the S72NS-S MCP stacked products. Refer to the S29NS-S data sheet (S29NS_WS_XS-S_00) for full electrical specifications of the Flash memory component.

The S72NS Series is a product line of stacked products (MCPs), and consists of:

- S29NS family multiplexed Flash memory die
- DDR DRAM

The products covered by this document are listed in the tables below.

	DRAM Density
Flash Density	**512 Mb**
2 Gb	S72NS02GSF0

DDR Specification Reference

		Spansion Documentation
Density	**Manufacturer**	**Publication Number**
512	DRAM Type 5	DRAM_11

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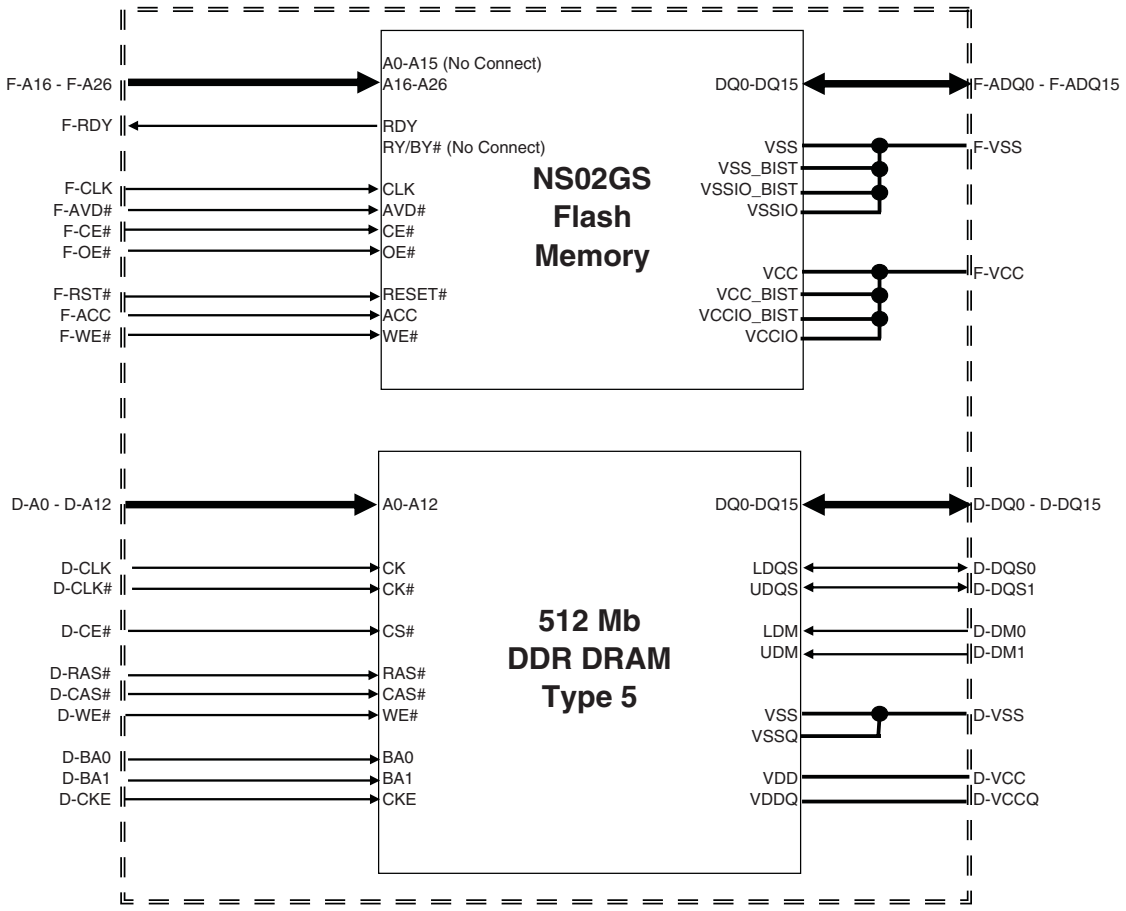
1. Product Selector Guide

Device OPN	Flash Boot	Flash Density	DDR DRAM Density	Flash Speed (MHz)	DDR DRAM Speed (MHz)	DRAM Supplier	Package
S72NS02GSF0YHMG9	Uniform	2 Gb	512 Mb	104	166	Type 5	11.0 x 13.0 mm 186-ball MCP (ALN186)

2. Product Block Diagram

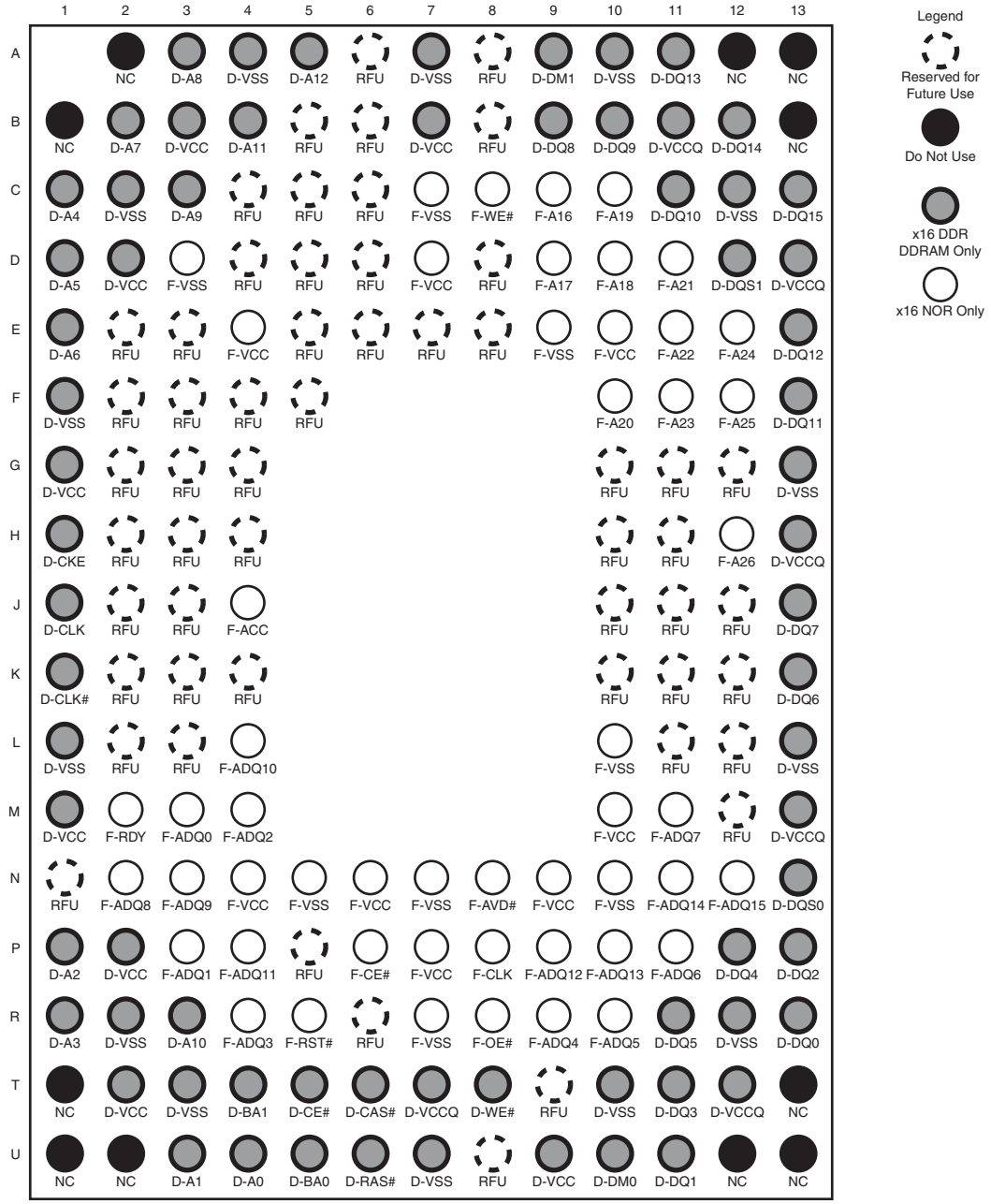


Notes:

1. *Amax indicates highest address bit for memory component:*
   a. *Amax = A26 for NS02GS*
   b. *Amax = A12 for 512 Mb DDR DRAM*
2. *For Flash, A15 - A0 is tied to DQ15 - DQ0.*

3. Connection Diagrams

Figure 3.1 186-ball Fine-Pitch Ball Grid Array MCP



Note:
Additional NC locations are in reference to the superset connection diagram shown here

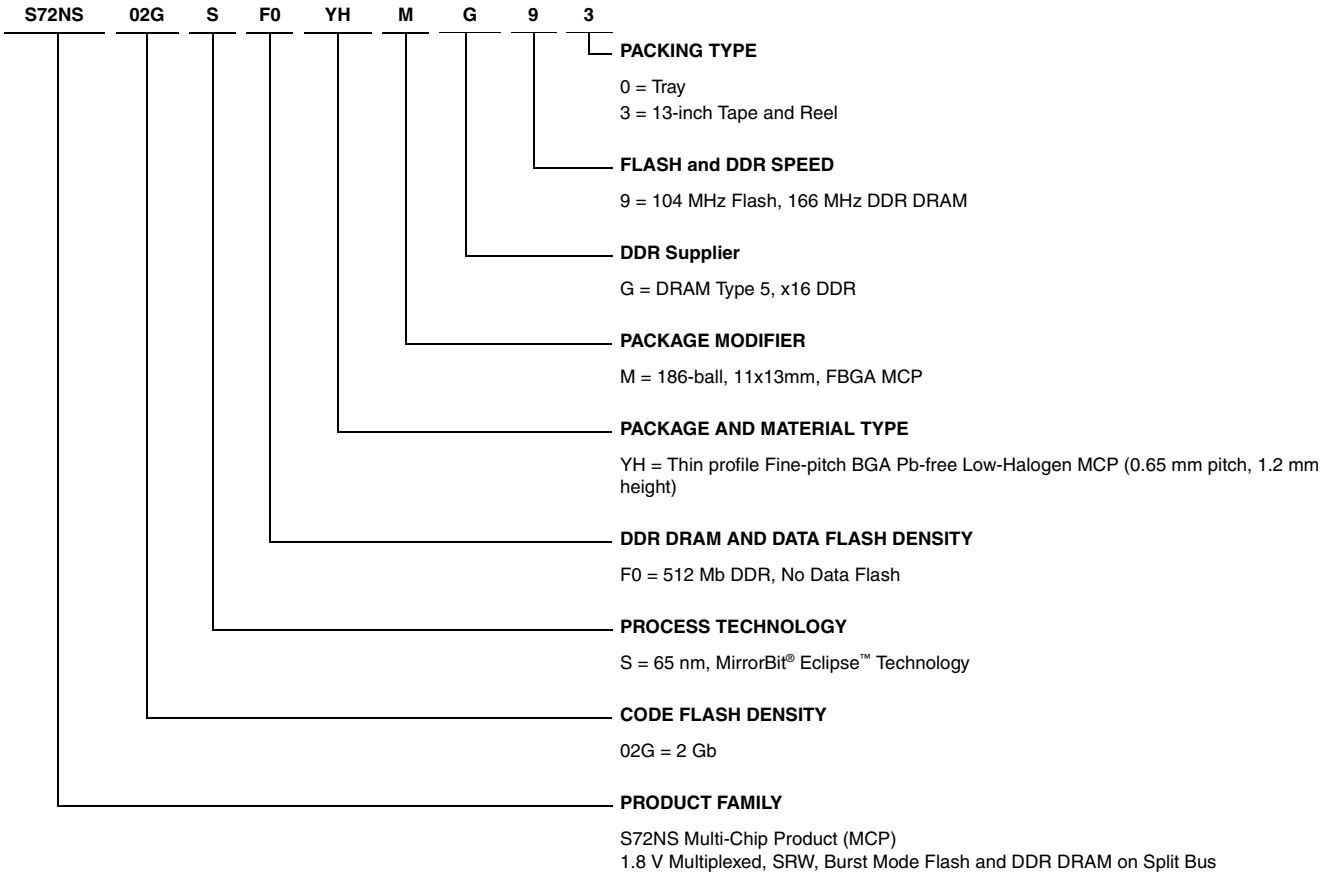
Device OPN	Flash Address Amax	DDR DRAM Address Amax	Additional NC Locations
S72NS02GSF0	A26	A12	N/A

4. Input/Output Descriptions

Amax – A16	=	Flash Address inputs
ADQ15 – ADQ0	=	Flash multiplexed Address and Data
F-CE#	=	Flash Chip-enable input.
F-OE#	=	Flash Output Enable input. Asynchronous relative to CLK for Burst mode.
F-WE#	=	Flash Write Enable input
F-VCC	=	Flash device power supply (1.7 V to 1.95 V)
F-VSS	=	Flash Ground
F-RDY	=	Flash ready output. Indicates the status of the Burst read. V_{OL} = data invalid. V_{OH} = data valid.
F-CLK	=	Flash Clock. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
F-AVD#	=	Flash Address Valid input. Indicates to device that the valid address is present on the address inputs. V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs
F-RST#	=	Flash hardware reset input. V_{IL}= device resets and returns to reading array data
F-ACC	=	Flash accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.
D-A12 – D-A0	=	DRAM Address inputs.
D-DQ15 – D-DQ0	=	DRAM Data input/output
D-CLK	=	DRAM System Clock
D-CE#	=	DRAM Chip Select
D-CKE	=	DRAM Clock Enable
D-BA1 – BA0	=	DRAM Bank Select
D-RAS#	=	DRAM Row Address Strobe
D-CAS#	=	DRAM Column Address Strobe
D-UDQM – D-LDQM	=	DRAM Data Input Mask
D-WE#	=	DRAM Write Enable input
D-VSS	=	DRAM Ground
D-VSSQ	=	DRAM Input/Output Buffer ground
D-VCCQ	=	DRAM Input/Output Buffer power supply
D-VCC	=	DRAM device power supply
D-UDQS	=	DRAM Upper Data Strobe, output with read data and input with write data
D-LDQS	=	DRAM Lower Data Strobe, output with read data and input with write data
D-CLK#	=	DDR Clock for negative edge of CLK
RFU	=	Reserved for Future Use
NC	=	No Connect. Can be connected to ground or left floating.
D-TEST	=	Internal Test mode pin for DDR DRAM only. Do not apply any signal on this pin. Can be connected to ground or left floating.
DNU	=	Do Not Use

5. Ordering Information

The order number (Valid Combination) is formed by the following:



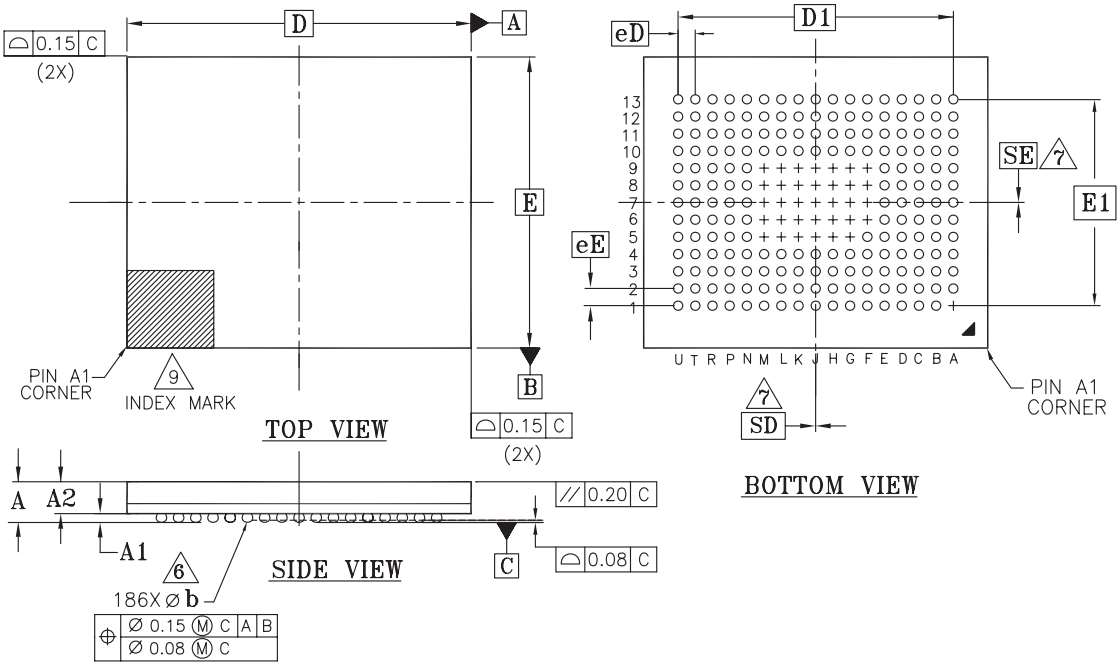
Valid Combinations							
Product Family	**Code Flash Density (Mb)**	**Process Technology**	**DDR Density (Mb)**	**Package Type/ Material**	**DDR Vendor**	**Flash & DDR Speed**	**Packing Type**
S72NS	02G	S	F0	YHM	G	9	0, 3 (Note 1)

Notes

1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*
3. *Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.*

6. Physical Dimensions

6.1 ALN186—186-ball Fine-Pitch Ball Grid Array (FBGA) 11.0 x 13.0 mm



PACKAGE	ALN 186			
JEDEC	N/A			
D x E	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.79	---	0.95	BODY THICKNESS
D		13.00 BSC		BODY SIZE
E		11.00 BSC		BODY SIZE
D1		10.40 BSC		MATRIX FOOTPRINT
E1		7.80 BSC		MATRIX FOOTPRINT
MD		17		MATRIX SIZE D DIRECTION
ME		13		MATRIX SIZE E DIRECTION
n		186		BALL COUNT
Ø b	0.325	0.375	0.425	BALL DIAMETER
eE		0.65 BSC		BALL PITCH
eD		0.65 BSC		BALL PITCH
SD SE		0.00 BSC		SOLDER BALL PLACEMENT
	A1,F6,F7,F8,F9,G5,G6,G7,G8,G9 H5,H6,H7,H8,H9,J5,J6,J7,J8,J9, K5,K6,K7,K8,K9,L5,L6,L7,L8,L9, M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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7. Revision History

Section	Description
Revision 01 (October 7, 2008)	
	Initial release
Revision 02 (January 9, 2009)	
Connection Diagrams	Changed ball E13 to D-DQ12.

Colophon

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