S72NS-R Based MCPs

MirrorBit® Flash Memory and DRAM

128/256/512 Mb (8/16/32 M x 16 bit), 1.8 Volt-only, Multiplexed Simultaneous Read/Write, Burst Mode Flash Memory
128/256 Mb (8/16 M x 16 bit) DDR DRAM on Split Bus

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S72NS-R_00 **Revision** 05 **Issue Date** May 9, 2008

Notice On Data Sheet Designations

Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion Inc. is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion Inc. therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion Inc. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion Inc. reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local sales office.

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Data Sheet *(Advance Information)*

Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **Burst Speeds**
  - Flash = 83MHz, 104 MHz
  - DDR DRAM = 133 MHz, 166 MHz
- **Packages**
  - 8.0 x 8.0 mm, 133-ball MCP
  - 11.0 x 10.0 mm, 133-ball MCP
- **Operating Temperature of –25°C to +85°C**

General Description

This document contains information on the S72NS-R MCP stacked products. Refer to the S29NS-R data sheet (S29NS-R_00) for full electrical specifications of the Flash memory component.

The S72NS Series is a product line of stacked products (MCPs), and consists of:

- S29NS family multiplexed Flash memory die
- DDR DRAM

The products covered by this document are listed in the tables below.

Flash Density	DRAM Density	
	128 Mb	256 Mb
128 Mb	S72NS128RD0	
256 Mb	S72NS256RD0	
512 Mb	S72NS512RD0	S72NS512RE0
1 Gb		

DDR Specification Reference

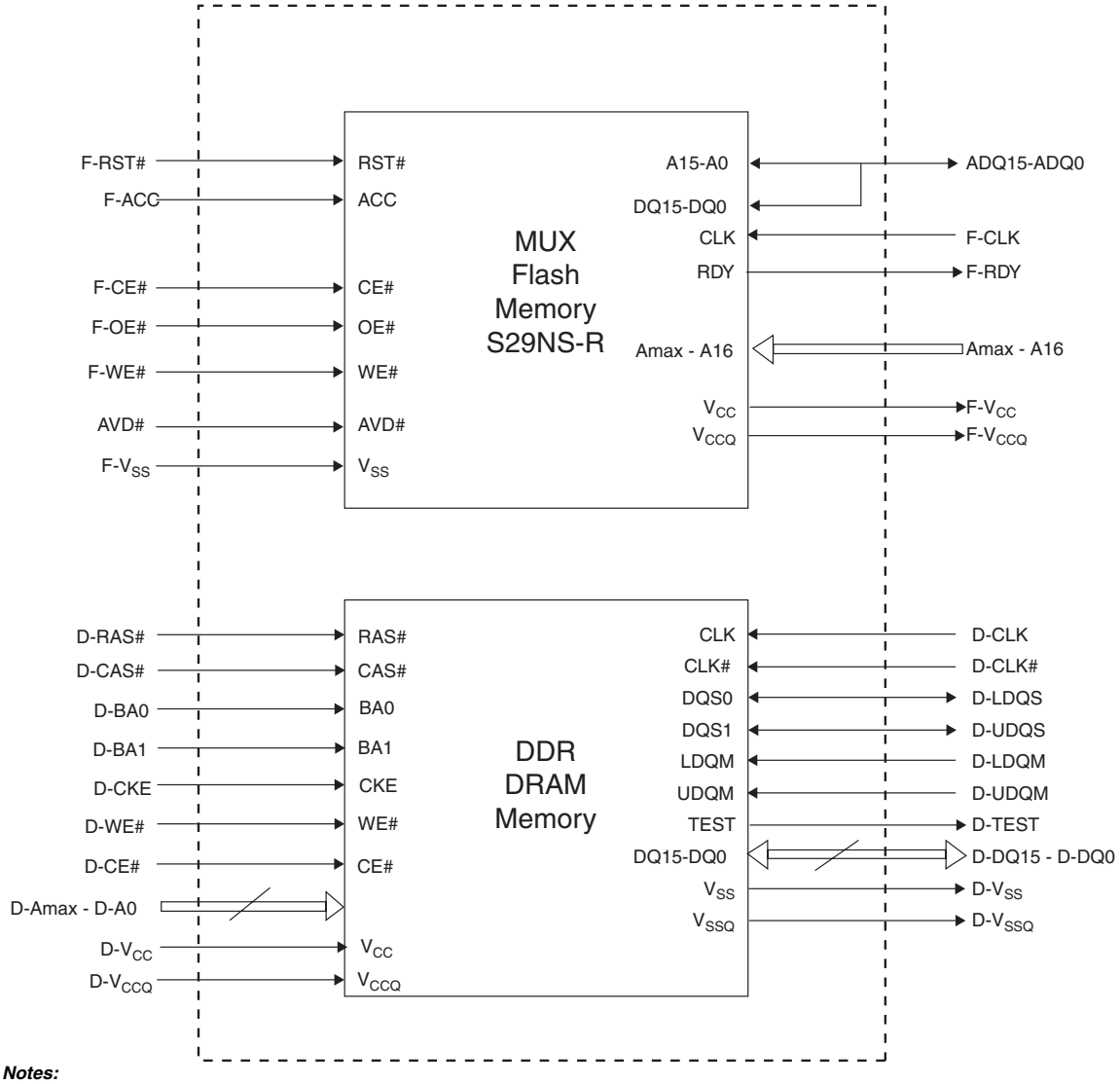
Density	Manufacturer	Spansion Documentation
		Publication Number
128	DRAM Type 5	DRAM_15
	DRAM Type 1	DRAM_07
	DRAM Type 6	DRAM_09
256	DRAM Type 5	DRAM_14
	DRAM Type 1	DRAM_08

Publication Number S72NS-R_00 **Revision** 05 **Issue Date** May 9, 2008

1. Product Selector Guide

Device OPN	Flash Density	DDR DRAM Density	Flash Speed (MHz)	DDR DRAM Speed (MHz)	DRAM Supplier	Package
S72NS128RD0AHBL0	128 Mb	128 Mb	83	166	Type 5	8.0 x 8.0 mm 133-ball MCP (RLB133)
S72NS128RD0AHBG0					Type 1	
S72NS128RD0AHBM0					Type 6	
S72NS256RD0AHBL0	256 Mb	128 Mb	83	166	Type 5	8.0 x 8.0 mm 133-ball MCP (RLB133)
S72NS256RD0AHBG0					Type 1	
S72NS256RD0AHBM0					Type 6	
S72NS512RD0AHGL0	512 Mb	128 Mb	83	166	Type 5	11.0 x 10.0mm 133-ball MCP (RLD133)
S72NS512RD0AHGG0					Type 1	
S72NS512RD0AHGM0					Type 6	
S72NS512RD0KHFL0					Type 5	12.0 x 12.0 mm 128-ball PoP (ALF128)
S72NS512RD0KHFM0					Type 6	
S72NS512RE0AHGL0	512 Mb	256 Mb	83	166	Type 5	11.0 x 10.0 mm 133-ball MCP (RLD133)
S72NS512RE0AHGG0					Type 1	
S72NS512RE0KHFL0					Type 5	12.0 x 12.0 mm 128-ball PoP (ALF128)
S72NS512RE0KHFG0					Type 1	

2. Product Block Diagram

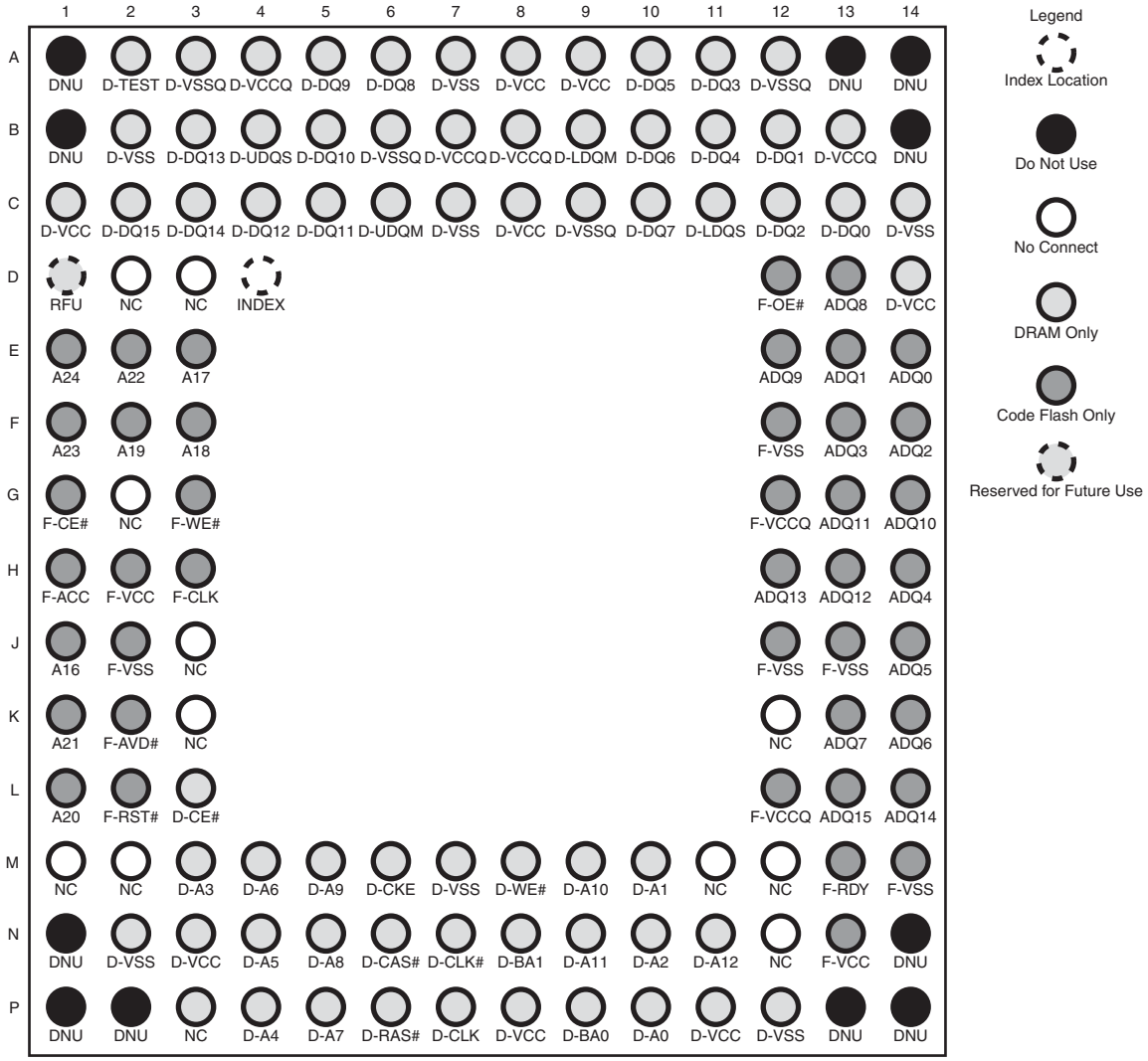


Notes:

1. *Amax indicates highest address bit for memory component:*
   a. *Amax = A25 for NS01GR , A24 for NS512R, A23 for NS256R, A22 for NS128R*
   b. *Amax = A11 for 128 Mb DDR DRAM*
   c. *Amax = A12 for 256 Mb DDR DRAM*
2. *For Flash, A15 - A0 is tied to DQ15 - DQ0.*

3. Connection Diagrams

Figure 3.1 133-ball Fine-Pitch Ball Grid Array MCP



Note:
Additional NC locations are in reference to the superset connection diagram shown here

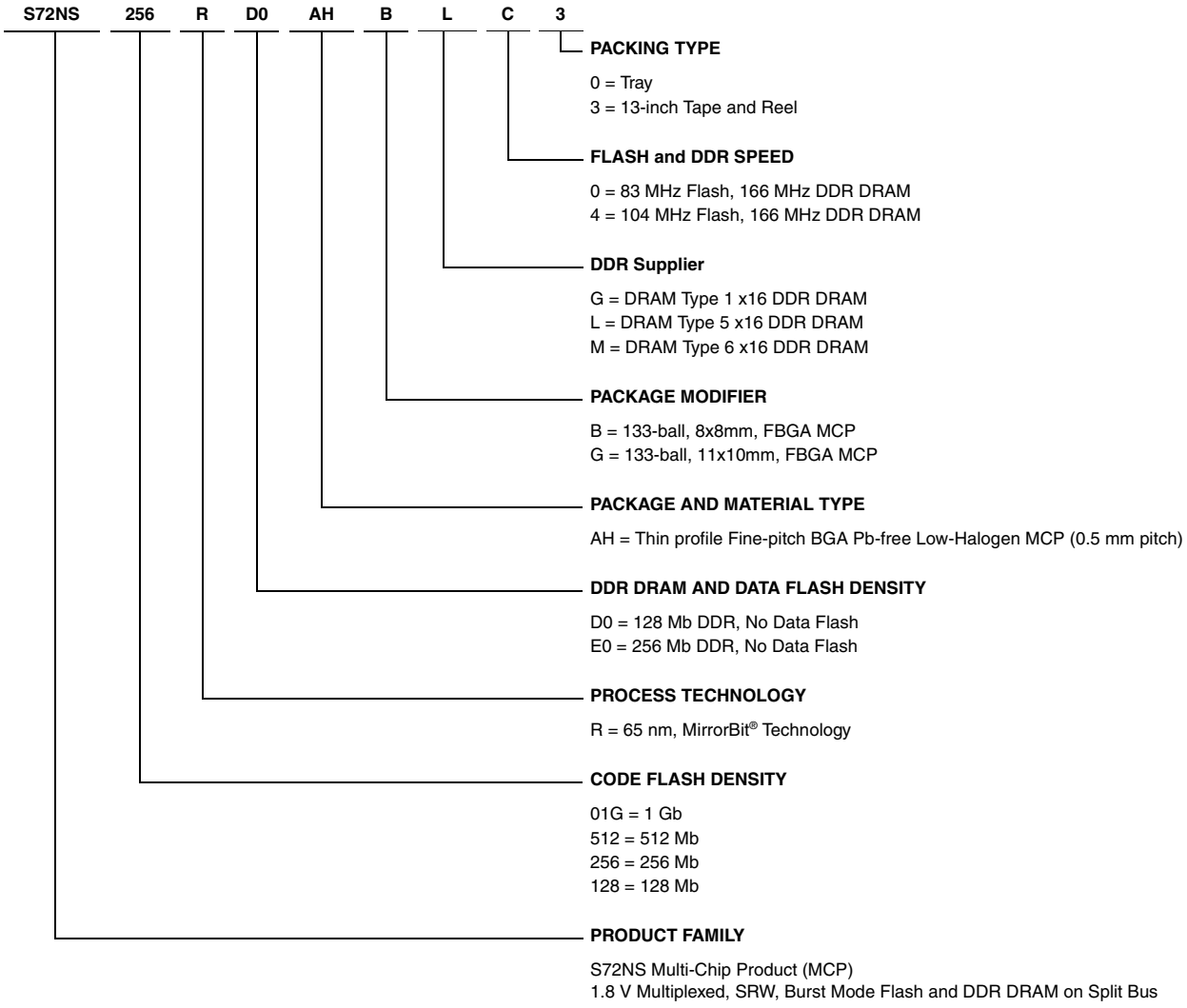
Device OPN	Flash Address Amax	DDR DRAM Address Amax	Additional NC Locations
S72NS128RD0	A22	A11	Ball F1, Ball E1, Ball N11
S72NS256RD0	A23	A11	Ball E1, Ball N11
S72NS512RD0	A24	A11	Ball N11
S72NS512RE0	A24	A12	N/A

4. Input/Output Descriptions

Amax – A16	=	Flash Address inputs
ADQ15 – ADQ0	=	Flash multiplexed Address and Data
F-CE#	=	Flash Chip-enable input.
F-OE#	=	Flash Output Enable input. Asynchronous relative to CLK for Burst mode.
F-WE#	=	Flash Write Enable input
F-VCC	=	Flash device power supply (1.7 V to 1.95 V)
F-VCCQ	=	Flash Input/Output Buffer power supply
F-VSS	=	Flash Ground
F-RDY	=	Flash ready output. Indicates the status of the Burst read. V_{OL} = data invalid. V_{OH} = data valid.
F-CLK	=	Flash Clock. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
F-AVD#	=	Flash Address Valid input. Indicates to device that the valid address is present on the address inputs. V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs
F-RST#	=	Flash hardware reset input. V_{IL}= device resets and returns to reading array data
F-ACC	=	Flash accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.
D-A12 – D-A0	=	DRAM Address inputs.
D-DQ15 – D-DQ0	=	DRAM Data input/output
D-CLK	=	DRAM System Clock
D-CE#	=	DRAM Chip Select
D-CKE	=	DRAM Clock Enable
D-BA1 – BA0	=	DRAM Bank Select
D-RAS#	=	DRAM Row Address Strobe
D-CAS#	=	DRAM Column Address Strobe
D-UDQM – D-LDQM	=	DRAM Data Input Mask
D-WE#	=	DRAM Write Enable input
D-VSS	=	DRAM Ground
D-VSSQ	=	DRAM Input/Output Buffer ground
D-VCCQ	=	DRAM Input/Output Buffer power supply
D-VCC	=	DRAM device power supply
D-UDQS	=	DRAM Upper Data Strobe, output with read data and input with write data
D-LDQS	=	DRAM Lower Data Strobe, output with read data and input with write data
D-CLK#	=	DDR Clock for negative edge of CLK
RFU	=	Reserved for Future Use
NC	=	No Connect. Can be connected to ground or left floating.
D-TEST	=	Internal Test mode pin for DDR DRAM only. Do not apply any signal on this pin. Can be connected to ground or left floating.
DNU	=	Do Not Use

5. Ordering Information

The order number (Valid Combination) is formed by the following:



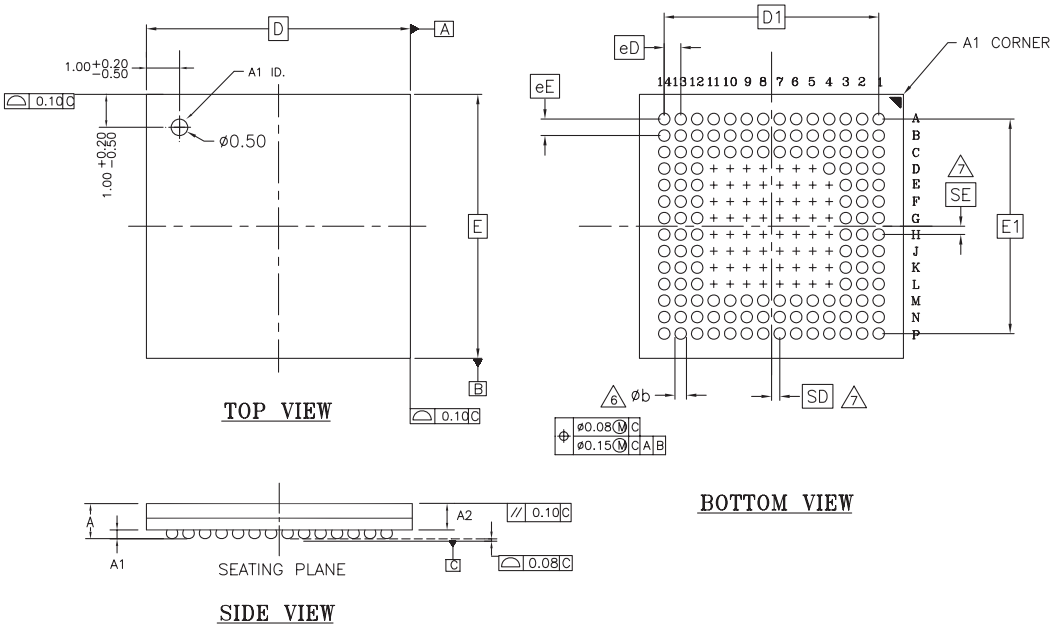
Valid Combinations							
Product Family	**Code Flash Density (Mb)**	**Process Technology**	**DDR Density (Mb)**	**Package Type/ Material**	**DDR Vendor**	**Flash & DDR Speed**	**Packing Type**
S72NS	128	R	D0	AHB, KHF	G, L, M	0	0, 3 (Note 1)
	256						
	512		E0	AHG, KHF	G, L		

Notes

1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*
3. *Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.*

6. Physical Dimensions

6.1 RLB133—133-ball Fine-Pitch Ball Grid Array (FBGA) 8.0 x 8.0 mm



PACKAGE	RLB 133			
JEDEC	N/A			
D x E	8.0 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	OVERALL THICKNESS
A1	0.18	0.23	0.28	BALL HEIGHT
A2	0.62	0.68	0.74	BODY THICKNESS
D	7.90	8.00	8.10	BODY SIZE
E	7.90	8.00	8.10	BODY SIZE
D1	6.50 BSC.			BALL FOOTPRINT
E1	6.50 BSC.			BALL FOOTPRINT
MD	14			ROW MATRIX SIZE D DIRECTION
ME	14			ROW MATRIX SIZE E DIRECTION
N	133			TOTAL BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
e	0.50 BSC.			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
	D5-D11, E4-E11, F4-F11 G4-G11, H4-H11, J4-J11 K4-K11, L4-L11			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

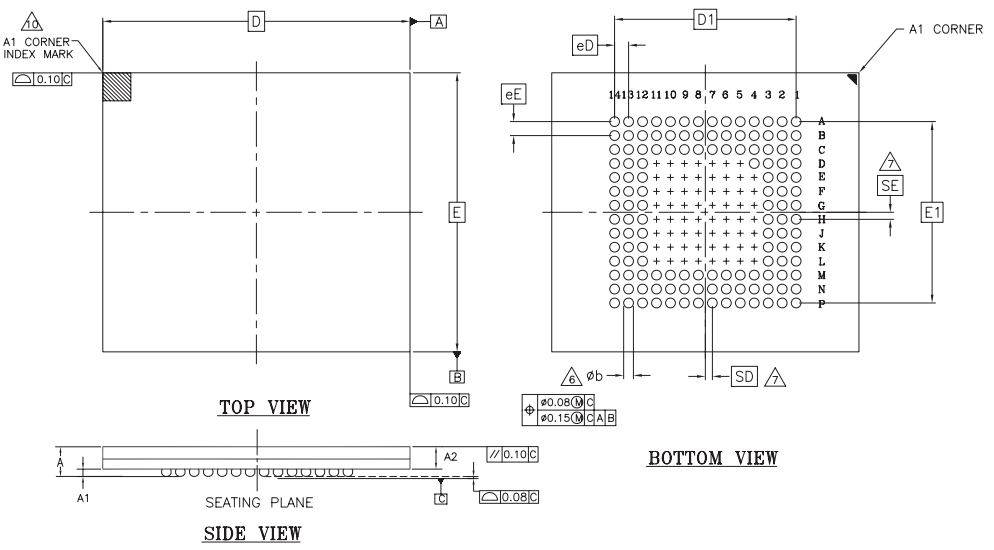
   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3627 \ 16-039.63 \ 8.21.7

6.2 RLD133—133-ball Fine-Pitch Ball Grid Array (FBGA) 11.0 x 10.0 mm



PACKAGE	RLD 133			
JEDEC	N/A			
D x E	11.0 mm x 10.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	---	1.00	OVERALL THICKNESS
A1	0.18	---	---	BALL HEIGHT
A2	0.62	---	0.74	BODY THICKNESS
D		11.00 BSC.		BODY SIZE
E		10.00 BSC.		BODY SIZE
D1		6.50 BSC.		BALL FOOTPRINT
E1		6.50 BSC.		BALL FOOTPRINT
MD		14		ROW MATRIX SIZE D DIRECTION
ME		14		ROW MATRIX SIZE E DIRECTION
N		133		TOTAL BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
e		0.50 BSC.		BALL PITCH
SD / SE		0.25 BSC.		SOLDER BALL PLACEMENT
		D5-D11, E4-E11, F4-F11 G4-G11, H4-H11, J4-J11 K4-K11, L4-L11		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

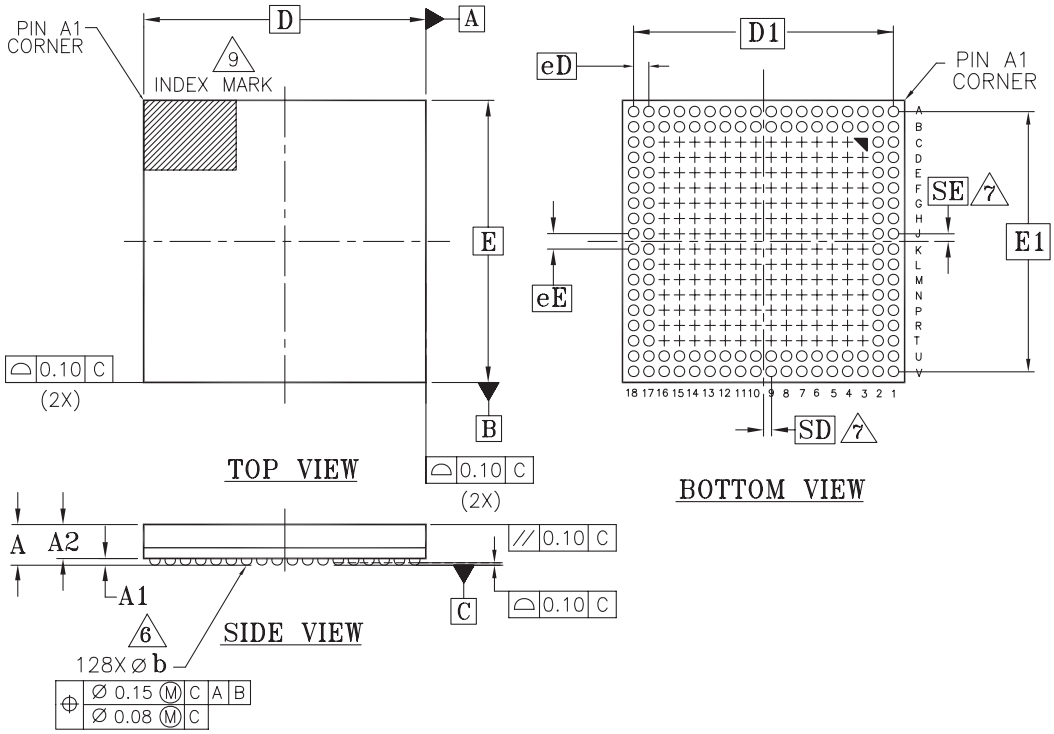
   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3674 \ 16-039.63 \ 2.11.8

6.3 ALF128—128-ball Fine-Pitch Ball Grid Array (FBGA) 12.0 x 12.0 mm



PACKAGE	ALF 128			
JEDEC	N/A			
D x E	12.00 mm x 12.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.85	0.95	1.05	PROFILE
A1	0.38	0.43	0.48	BALL HEIGHT
A2	0.49	0.54	0.59	BODY THICKNESS
D		12.00 BSC.		BODY SIZE
E		12.00 BSC.		BODY SIZE
D1		11.05 BSC.		MATRIX FOOTPRINT
E1		11.05 BSC.		MATRIX FOOTPRINT
MD		18		MATRIX SIZE D DIRECTION
ME		18		MATRIX SIZE E DIRECTION
n		128		BALL COUNT
N		128		MAXIMUM NUMBER OF BALLS
R		2		NUMBER OF LAND PERIMETERS
Ø b	0.43	0.48	0.53	BALL DIAMETER
eE		0.65 BSC.		BALL PITCH
eD		0.65 BSC.		BALL PITCH
SE / SD		0.325 BSC.		SOLDER BALL PLACEMENT
	C3-C16,D3-D16,E3-E16, F3-F16,G3-G16,H3-H16, J3-J16,K3-K16,L3-L16, M3-M16,N3-N16,P3-P16, R3-R16,T3-T16			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3.0, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

   N IS THE MAXIMUM NUMBER OF BALLS ON THE FBGA PACKAGE.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3658 \ 16-038.24 \ 10.12.7

7. Revision History

Section	Description
Revision 01 (August 7, 2007)	
	Initial release
Revision 02 (August 24, 2007)	
Global	Updated package names and drawings for S72NS-R MCPs
Revision 03 (January 15, 2008)	
Global	Updated speed grades for all S72NS-R product offerings
Revision 04 (February 13, 2008)	
Global	Changed RSA133 package to RLD133 and updated outline drawing
Ordering Information	Corrected typographical character errors in example OPN
Revision 05 (May 9, 2008)	
Global	Added ALF128 package and updated DRAM publication numbers
Ordering Information	Updated OPNs

Colophon

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