S72NS-P MCP/PoP Memory System Solutions

MirrorBit® Flash Memory and DRAM

128/256/512 Mb (8/16/32 M x 16 bit), 1.8 Volt-only, Multiplexed Simultaneous Read/Write, Burst Mode Flash Memory
128/256 Mb (8/16 M x 16 bit) DDR DRAM on Split Bus

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S72NS-P_00 **Revision** 05 **Issue Date** February 14, 2008

Notice On Data Sheet Designations

Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion Inc. is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion Inc. therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion Inc. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion Inc. reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications."

Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local sales office.

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Data Sheet *(Advance Information)*

Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **Burst Speeds**
  - Flash = 66 MHz, 83 MHz
  - DRAM = 133 MHz, 166 MHz
- **Packages**
  - 11.0 x 10.0 mm, 133-ball MCP
  - 8.0 x 8.0 mm, 133-ball MCP
  - 12.0 x 12.0 mm, 128-ball PoP
- **Operating Temperature of –25°C to +85°C**

General Description

This document contains information on the S72NS-P MCP stacked products. Refer to the S29NS-P data sheet (S29NS-P_00) for full electrical specifications of the Flash memory component.

The S72NS Series is a product line of stacked products (MCPs and PoPs), and consists of:

- NS family multiplexed Flash memory die
- DDR DRAM

The products covered by this document are listed in the tables below.

Flash Density	DRAM Density	
	128 Mb	256 Mb
128 Mb	S72NS128PD0	
256 Mb	S72NS256PD0	
512 Mb	S72NS512PD0	S72NS512PE0

For detailed specifications, please refer to the individual data sheets.

Density	Manufacturer	Publication Number
128	DRAM1	SDRAM_03
	DRAM5	SDRAM_07

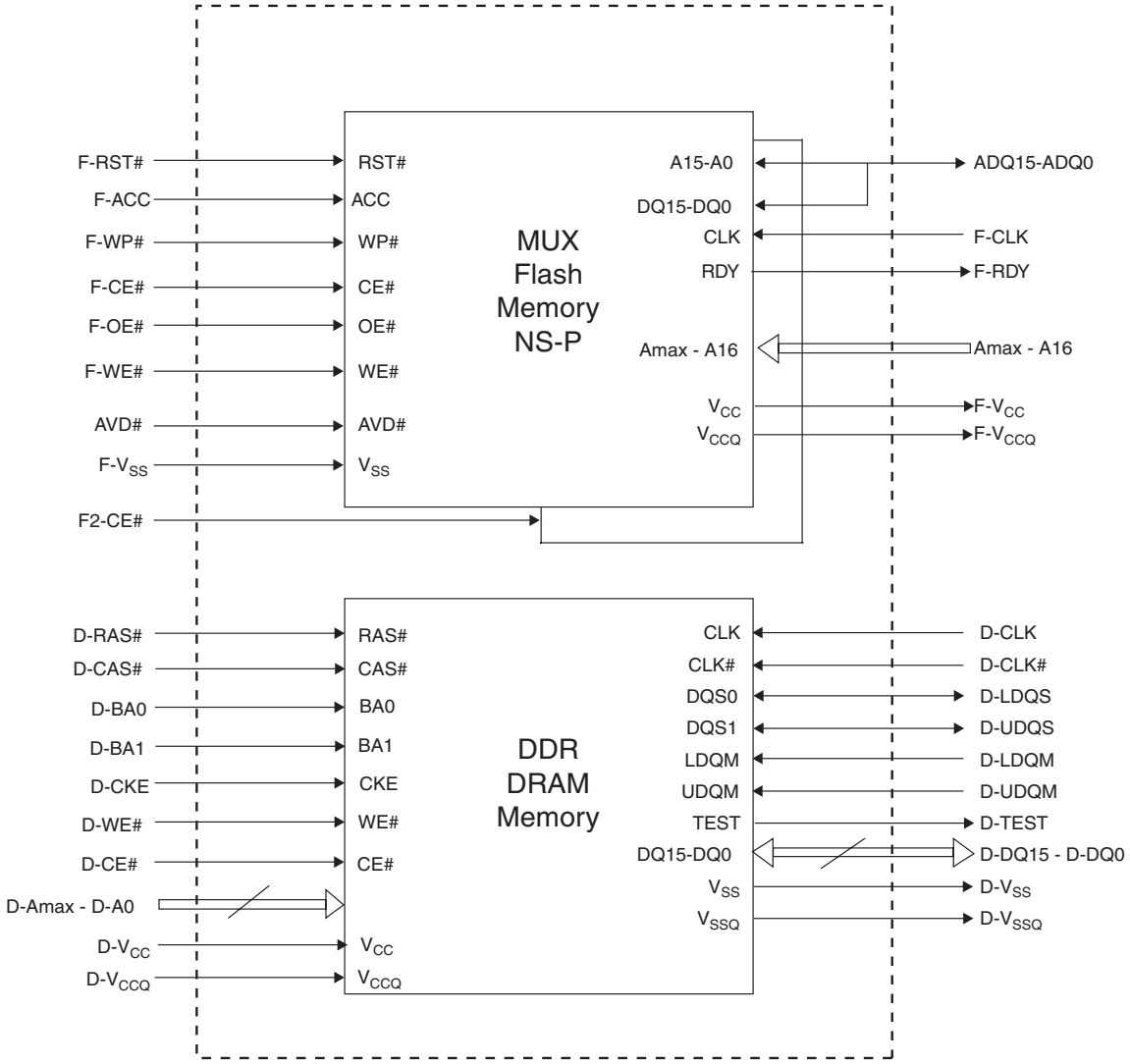
Density	Manufacturer	Publication Number
256	DRAM1	SDRAM_08
	DRAM5	SDRAM_11

Publication Number S72NS-P_00 **Revision** 05 **Issue Date** February 14, 2008

1. Product Selector Guide

Device OPN	Flash Density	DDR DRAM Density	Flash Speed (MHz)	DDR DRAM Speed (MHz)	Supplier	Package
S72NS128PD0AJBGG	128 Mb	128 Mb	66	133	DRAM1	8.0 x 8.0 mm 133-ball MCP (NSC133)
S72NS128PD0AJBGC			83			
S72NS128PD0AHBLG			66		DRAM5	
S72NS128PD0AHBLC			83			
S72NS256PD0AJBGG	256 Mb	128 Mb	66	133	DRAM1	8.0 x 8.0 mm 133-ball MCP (NSC133)
S72NS256PD0AJBGC			83			
S72NS256PD0AJBLG			66		DRAM5	
S72NS256PD0AJBLC			83			
S72NS512PD0AJGGG	512 Mb	128 Mb	66	133	DRAM1	11.0 x 10.0 mm 133-ball MCP (NLC133)
S72NS512PD0AJGGC			83			
S72NS512PD0AJGLG			66		DRAM5	
S72NS512PD0AHGLG			66			
S72NS512PD0AJGLC			83			
S72NS512PE0AJGLG	512 Mb	256 Mb	66	133	DRAM5	11.0 x 10.0 mm 133-ball MCP (NLC133)
S72NS512PE0AJGLC			83			
S72NS512PE0KFDGG	512 Mb	256 Mb	66	133	DRAM1	12.0 x 12.0 mm 128-ball PoP 0.45 mm ball (DLA128)
S72NS512PE0KFDG0			83	166		

2. Product Block Diagram

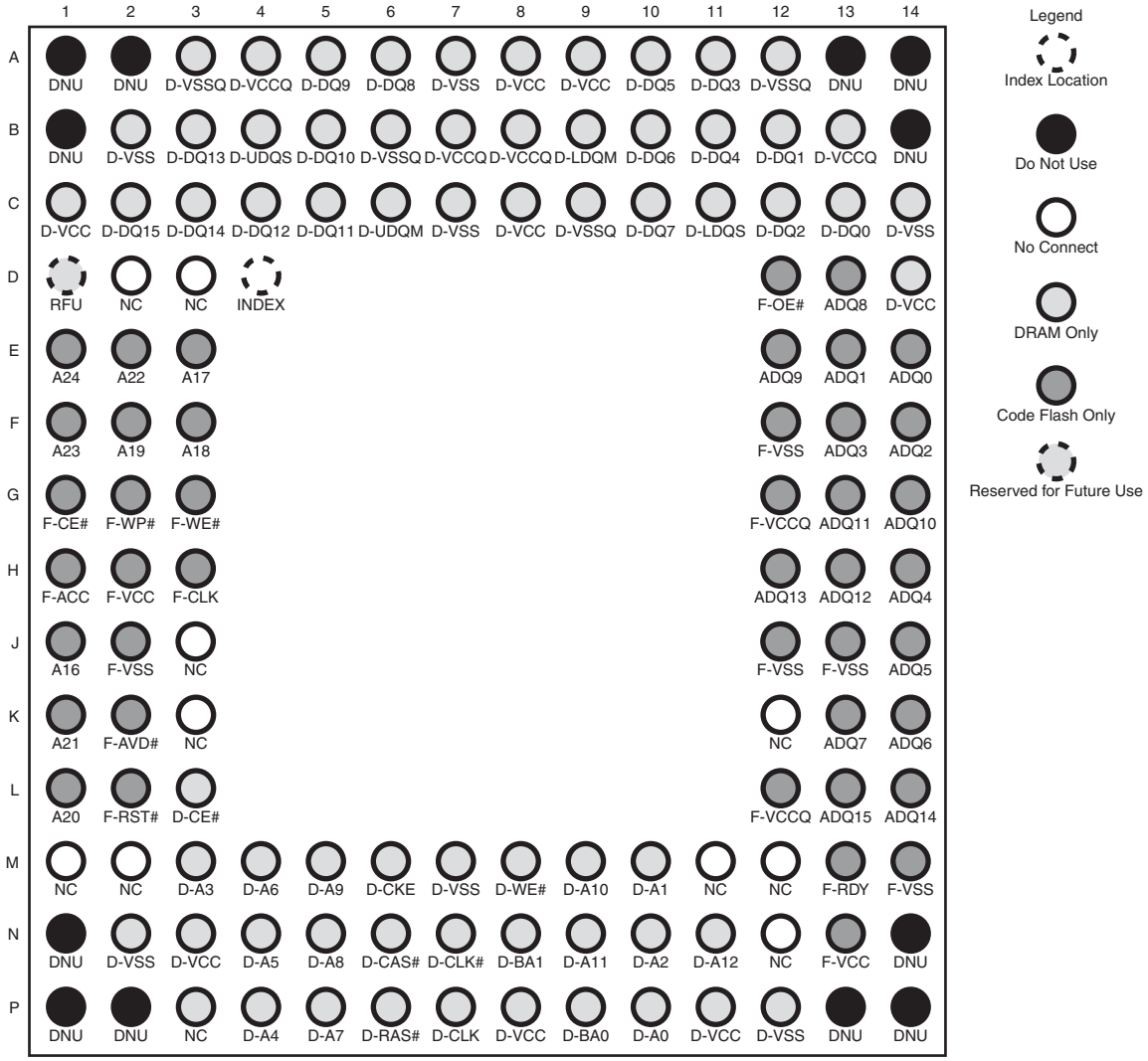


Notes:

1. *Amax indicates highest address bit for memory component:*
   a. *Amax = A24 for NS512P, A23 for NS256P, A22 for NS128P*
   b. *Amax = A11 for 128 Mb DDR DRAM*
   c. *Amax = A12 for 256 Mb DDR DRAM*
2. *For Flash, A15 - A0 is tied to DQ15 - DQ0.*
3. *F2-CE# applicable for second Flash die, if any.*

3. Connection Diagrams

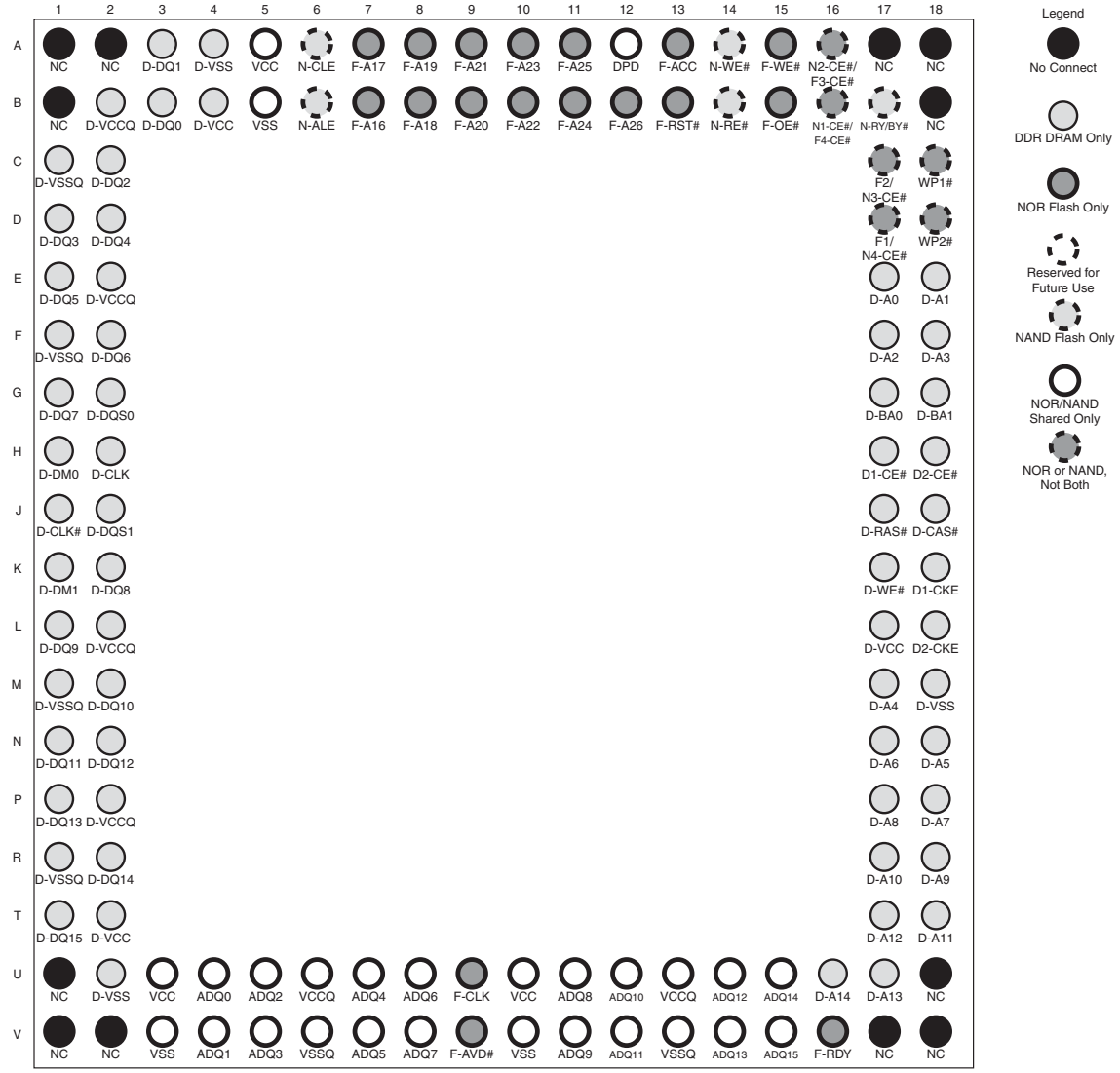
Figure 3.1 133-ball Fine-Pitch Ball Grid Array MCP



Note:
Additional NC locations are in reference to the superset connection diagram shown here

Device OPN	Flash Address Amax	DDR DRAM Address Amax	Additional NC Locations
S72NS128PD0	A22	A11	Ball F1, Ball E1, Ball N11
S72NS256PD0	A23	A11	Ball E1, Ball N11
S72NS512PD0	A24	A11	Ball N11
S72NS512PE0	A24	A12	N/A

Figure 3.2 128-ball Fine Pitch Ball Grid Array PoP



Note:
Additional NC locations are in reference to the superset connection diagram shown here

Device OPN	Flash Address Amax	DRAM Address Amax	Additional NC Locations
S72NS512PE0	A24	A12	Ball A6, A11, A12, A14, A16, B6, B12, B14, B16, B17, C17, D18, H18, L18, U16, U17

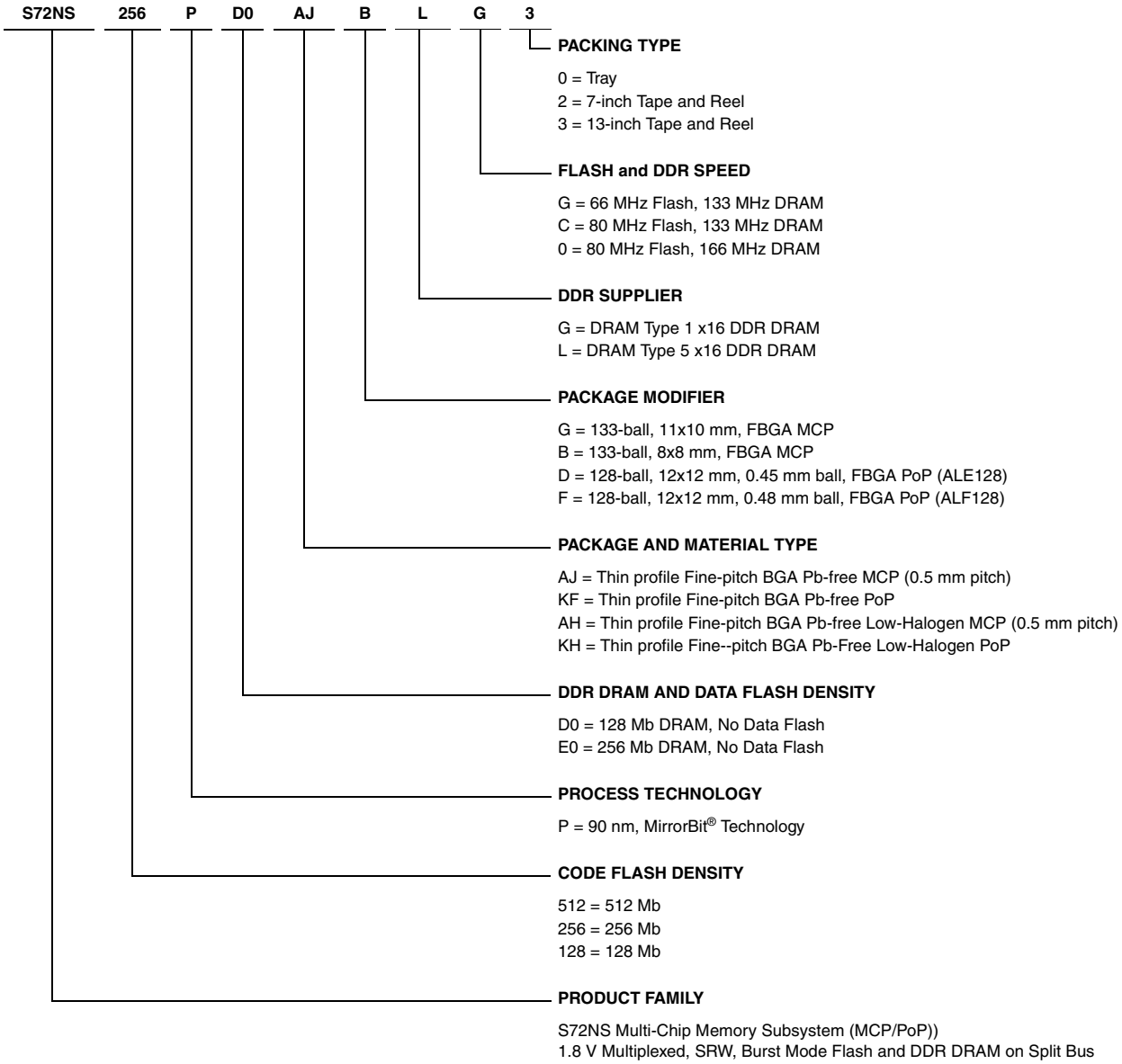
4. Input/Output Descriptions

Signal	Description	Flash	DRAM
Amax – A16	Flash Address inputs		
ADQ15 – ADQ0	Flash multiplexed Address and Data		
F-CE#	Flash Chip-enable input. Asynchronous relative to CLK for Burst Mode	X	
F-OE#	Flash Output Enable input. Asynchronous relative to CLK for Burst mode.	X	
F-WE#	Flash Write Enable input	X	
F-VCC	Flash device power supply (1.7 V to 1.95 V)	X	
F-VCCQ	Flash Input/Output Buffer power supply	X	
F-VSS	Flash Ground	X	
F-RDY	Flash ready output. Indicates the status of the Burst read. V_{OL} = data invalid. V_{OH} = data valid.	X	
F-CLK	Flash Clock. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.	X	
F-AVD#	Flash Address Valid input. Indicates to device that the valid address is present on the address inputs. V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs	X	
F-RST#	Flash hardware reset input. V_{IL}= device resets and returns to reading array data	X	
F-WP#	Flash hardware write protect input. V_{IL} = disables program and erase functions in the four outermost sectors	X	
F-ACC	Flash accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	X	
D-A12 – D-A0	DRAM Address inputs.		X
D-DQ15 – D-DQ0	DRAM Data input/output		X
D-CLK	DRAM System Clock		X
D-CE#	DRAM Chip Select		X
D-CKE	DRAM Clock Enable		X
D-BA1 – BA0	DRAM Bank Select		X
D-RAS#	DRAM Row Address Strobe		X
D-CAS#	DRAM Column Address Strobe		X
D-UDQM – D-LDQM	DRAM Data Input Mask		X
D-WE#	DRAM Write Enable input		X
D-VSS	DRAM Ground		X
D-VSSQ	DRAM Input/Output Buffer ground		X
D-VCCQ	DRAM Input/Output Buffer power supply		X
D-VCC	DRAM device power supply		X
D-UDQS	DRAM Upper Data Strobe, output with read data and input with write data		X
D-LDQS	DRAM Lower Data Strobe, output with read data and input with write data		X
D-CLK#	DDR Clock for negative edge of CLK		X
RFU	Reserved for Future Use		
NC	No Connect. Can be connected to ground or left floating.		
DNU	Do Not Use. This signal must be left floating		

Note
Signal descriptions apply only to valid products offered in the S72NS-P product family.

5. Ordering Information

The order number (Valid Combination) is formed by the following:



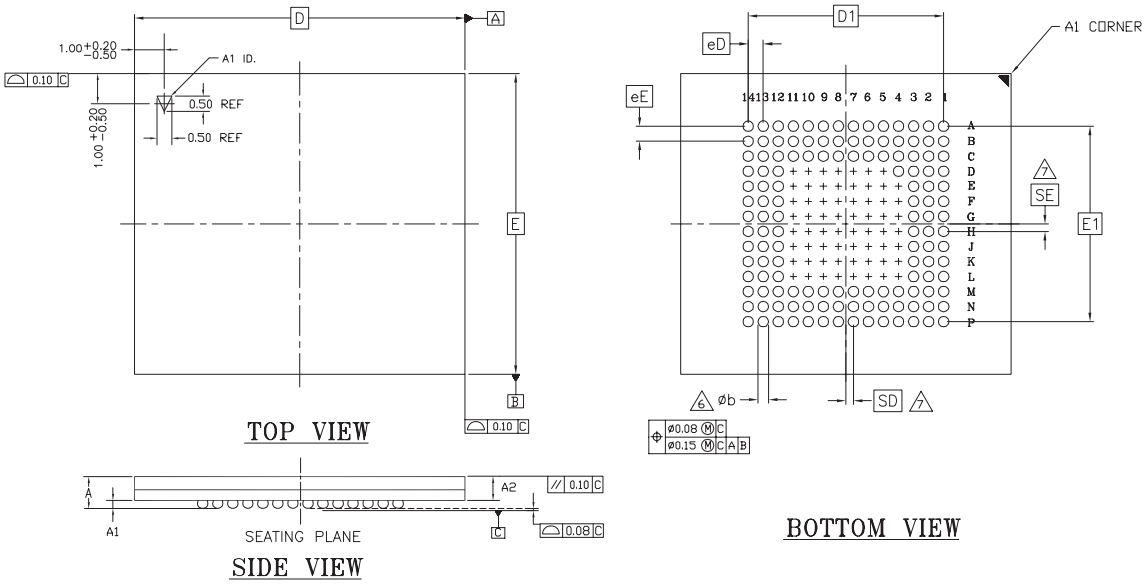
Valid Combinations							
Product Family	**Code Flash Density (Mb)**	**Process Technology**	**DRAM Density (Mb)**	**Package Type/ Material**	**DDR Vendor**	**Flash & DDR Speed**	**Packing Type**
S72NS	128	P	D0	AJB, AHB	G, L, J	G, C	0, 2, 3 (Note 1)
	256					G, C, 0	
	512		D0, E0	AHG, AJG, KFD			

Notes:

1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*
3. *Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.*

6. Physical Dimensions

6.1 NLC133—133-ball Fine-Pitch Ball Grid Array (FBGA) 11.0 x 10.0 mm



PACKAGE	NLC 133			
JEDEC	N/A			
D x E	11.0 mm x 10.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.90	1.00	1.10	PROFILE
A1	0.20	0.25	0.30	BALL HEIGHT
A2	0.70	0.76	0.82	BODY THICKNESS
D	10.9	11.0	11.1	BODY SIZE
E	9.9	10.0	10.1	BODY SIZE
D1	6.50 BSC.			MATRIX FOOTPRINT
E1	6.50 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	133			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
	D5-D11, E4-E11, F4-F11 G4-G11, H4-H11, J4-J11 K4-K11, L4-L11			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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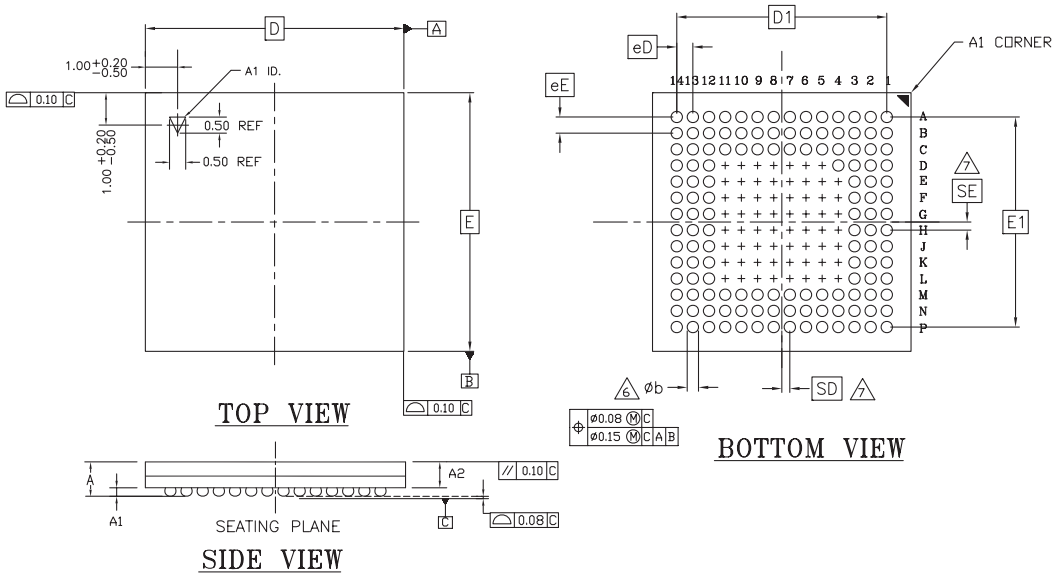
6.2 NSC133—133-ball Fine-Pitch Ball Grid Array (FBGA) 8.0 x 8.0 mm



PACKAGE	NSC 133			NOTE
JEDEC	N/A			
D x E	8.00 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	0.90	1.00	1.10	PROFILE
A1	0.20	0.25	0.30	BALL HEIGHT
A2	0.70	0.76	0.82	BODY THICKNESS
D		8.00 BSC		BODY SIZE
E		8.00 BSC		BODY SIZE
D1		6.50 BSC.		MATRIX FOOTPRINT
E1		6.50 BSC.		MATRIX FOOTPRINT
MD		14		MATRIX SIZE D DIRECTION
ME		14		MATRIX SIZE E DIRECTION
n		133		BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE		0.50 BSC.		BALL PITCH
eD		0.50 BSC		BALL PITCH
SD / SE		0.25 BSC.		SOLDER BALL PLACEMENT
	D5-D11,E4-E11,F4-F11,G4-G11 H4-H11,J4-J11,K4-K11,L4-L11			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1 SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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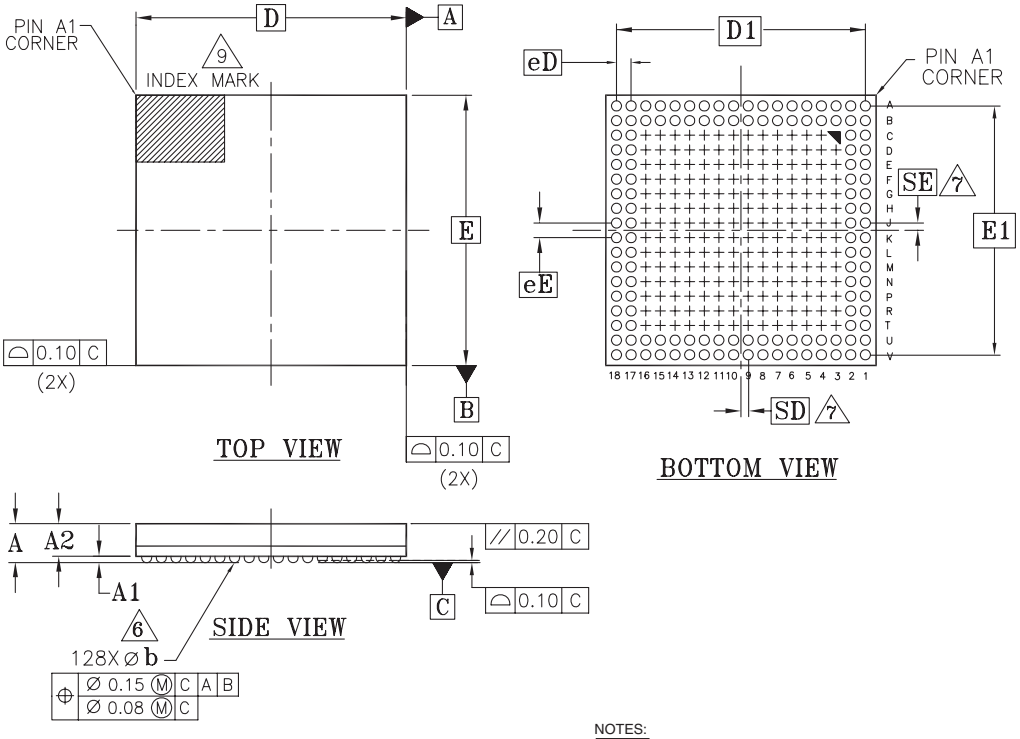
6.3 DLA128—128-ball Fine-Pitch Ball Grid Array (FBGA) 12.0 x 12.0 mm



PACKAGE	DLA 128			
JEDEC	N/A			
D X E	12.00 mm x 12.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.00	PROFILE
A1	0.35	---	---	BALL HEIGHT
A2	0.49	---	0.59	BODY THICKNESS
D		12.00 BSC.		BODY SIZE
E		12.00 BSC.		BODY SIZE
D1		11.05 BSC.		MATRIX FOOTPRINT
E1		11.05 BSC.		MATRIX FOOTPRINT
MD		18		MATRIX SIZE D DIRECTION
ME		18		MATRIX SIZE E DIRECTION
n		128		BALL COUNT
N		128		MAXIMUM NUMBER OF BALLS
R		2		NUMBER OF LAND PERIMETERS
Ø b	0.40	0.45	0.50	BALL DIAMETER
eE		0.65 BSC.		BALL PITCH
eD		0.65 BSC		BALL PITCH
SE SD		0.325 BSC.		SOLDER BALL PLACEMENT
	C3 ~ C16,D3 ~ D16,E3 ~ E16,F3 ~ F16 G3 ~ G16,H3 ~ H16,J3 ~ J16,K3 ~ K16 L3 ~ L16,M3 ~ M16,N3 ~ N16,P3 ~ P16 R3~R16,T3~T16			DEPOPULATED SOLDER BALL

NOTES:

1 DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2 ALL DIMENSIONS ARE IN MILLIMETERS.

3 BALL POSITION DESIGNATION PER JEP95, SECTION 3.0, SPP-010.

4 e REPRESENTS THE SOLDER BALL GRID PITCH.

5 SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

N IS THE MAXIMUM NUMBER OF BALLS ON THE FBGA PACKAGE.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

DATUM C IS THE SEATING PLANE AND IS DEFINED BY THE CROWNS OF THE SOLDER BALLS.

7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8 "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9 A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3675 / f16.038.69 / 2.11.8

7. Revision History

Section	Description
Revision 01 (September 6, 2006)	
	Initial release
Revision 02 (March 15, 2007)	
Global	Removed PoP option, including OPNs, valid combinations, connection diagrams and package drawings
General Description	Added DRAM Type 5 option for 256Mb DDR DRAM
Physical Dimensions	Added RLB133 Package drawing
Revision 03 (August 31, 2007)	
Global	Added S72NS512PE0 PoP product offering
General Description	Added DRAM Type 1 option for 256 Mb DDR DRAM
Product Selector Guide	Added OPNs for S72NS512PE0 PoP including speed and package options
Physical Dimensions	Removed RLB133 and added ALF128 and ALE128 packages
Revision 04 (October 15, 2007)	
Global	Added S72NS512PD0 Low-Halogen product offering Removed product offerings paired with DRAM Type 3 - modified Product Selector Guide and Ordering Information sections
Ordering Information	Added *AH* product descriptor for Pb-free Low-Halogen package
Revision 05 (February 14, 2008)	
Global	Added S72NS128PD0 Low-halogen product offering
Ordering Information	Revised product nomenclature to reflect accurate speed, material and package options
Physical Dimensions	Removed ALF128, ALE128 and added DLA128 packages

Colophon

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