S71NS-P Memory Subsystem Solutions

MirrorBit® 1.8 Volt-only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory and Burst Mode Multiplexed pSRAM

256 Mb (16 Mb x 16-bit) and 128 Mb (8 Mb x 16-bit) Flash 64 Mb (4 Mb x 16-bit), and 32 Mb (2 Mb x 16-bit) pSRAM

Data Sheet *(Preliminary)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71NS-P_00 **Revision** 05 **Issue Date** December 13, 2007

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Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion Inc. is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion Inc. therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion Inc. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion Inc. reserves the right to change or discontinue work on this proposed product without notice."

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local sales office.

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Data Sheet *(Preliminary)*

Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **Burst Speed (Flash and pSRAM): 66 MHz, 83 MHz**
- **MCP BGA Package**
  - 56 ball, 9.2 x 8.0 mm, 0.5 mm ball pitch
- **Operating Temperature**
  - Wireless, –25°C to +85°C

General Description

The S71NS-P Series is a product line of stacked Multi-Chip Package (MCP) memory solutions and consists of the following items:

- One or more S29NS-P flash memory die
- Multiplexed pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to their individual datasheet for further details.

	pSRAM		
	Density	**32 Mb**	**64 Mb**
Flash	128 Mb	S71NS128PB0	S71NS128PC0
	256 Mb	S71NS256PB0	S71NS256PC0

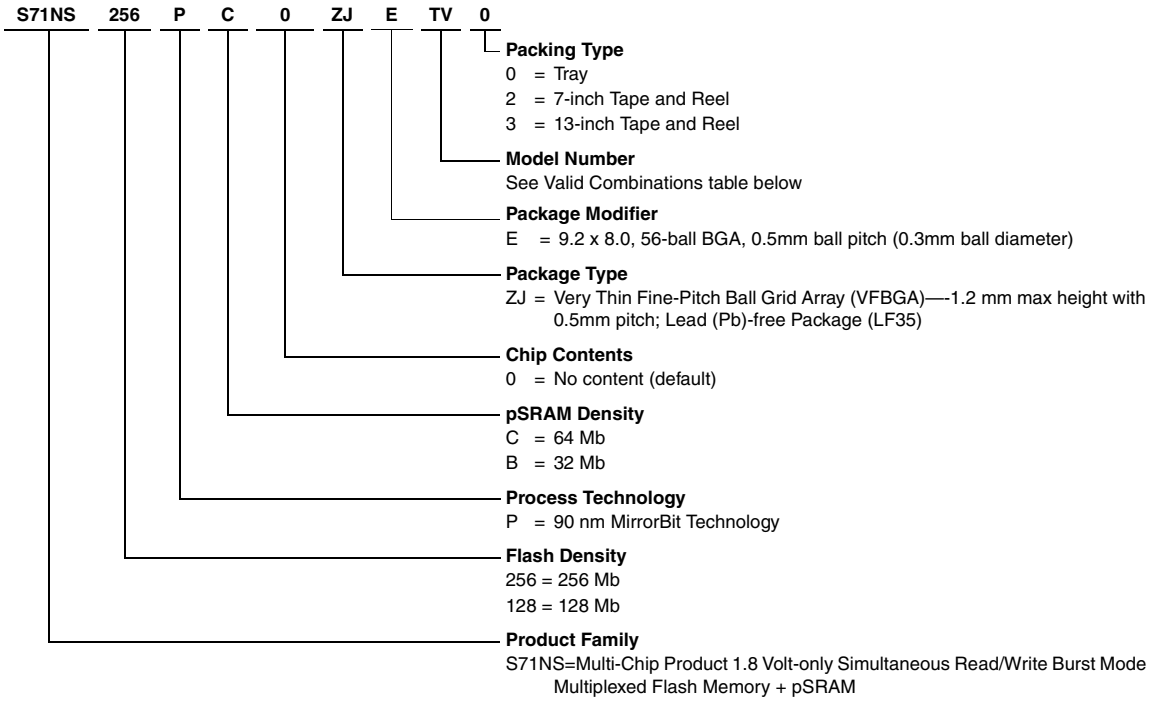
For detailed specifications, please refer to the individual data sheets:

Document	Publication Identification Number
S29NS-P	S29NS-P_00
32 M Multiplexed pSRAM Type 3	muxpsram_04
64 M Multiplexed pSRAM Type 3	muxpsram_01

Publication Number S71NS-P_00 **Revision** 05 **Issue Date** December 13, 2007

1. Ordering Information

The order number is formed by a valid combinations of the following:



Character Position Descriptions

Character 12	Character 14	Area	Ball Count	Ball Size
A or Z	A	6.2 x 7.7	44	0.30 mm
	B	8.0 x 8.0	133	
	C	8.0 x 9.2	44	
	D	8.0 x 9.2	48	
	E	8.0 x 9.2	56	
	F	10 x 11	60	
	G	10 x 11	133	
	H	10 x 11	133	
K	A	11 x 11	112	0.45 mm
	B			0.50 mm
	D	12 x 12	128	0.45 mm
	F			0.50 mm
	G	14 x 14	152	0.45 mm
	H			0.50 mm
	J	15 x 15	160	0.45 mm
	K			0.50 mm
	L	17 x 17	192	0.45 mm
	M			0.50 mm

1.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Base Ordering Part Number	Package	Model Number	Packing Type	pSRAM Type	MCP Speed
S71NS128PB0	ZJE	TV	0, 3	Type 3	66 MHz
S71NS128PC0					
S71NS256PB0					
S71NS256PC0					
S71NS128PB0		JR			83 MHz
S71NS128PC0					
S71NS256PB0					
S71NS256PC0					

2. Input/Output Descriptions

Table 2.1 identifies the input and output package connections provided on the device.

Table 2.1 Input/Output Descriptions (Sheet 1 of 2)

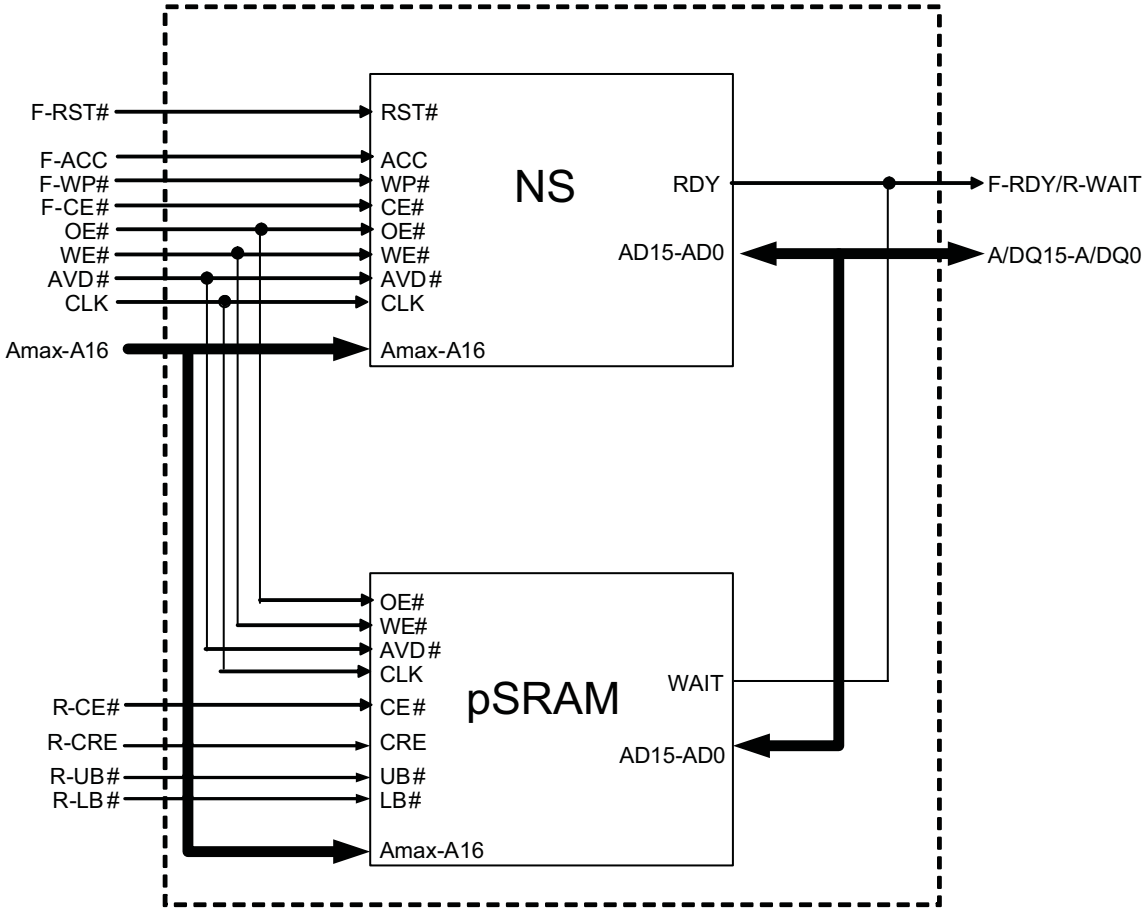
Symbol	Description	Flash	RAM
AMAX – A16	Address inputs	X	X
A/DQ15-A/DQ0	Multiplexed Address/Data	X	X
OE#	Output Enable input. Asynchronous relative to CLK for the Burst mode.	X	X
WE#	Write Enable input.	X	X
V_{SS}	Ground	X	X
NC	No Connect; not connected internally	X	X
F-RDY/R-WAIT	Ready output; indicates the status of the Burst read. Flash Memory RDY (using default "Active HIGH" configuration) V_{OL} = data invalid V_{OH} = data valid Note: The default polarity for the pSRAM WAIT signal is opposite the default polarity of the Flash RDY signal. pSRAM WAIT (using default “Active HIGH” configuration) V_{OL} = data valid V_{OH} = data invalid To match polarities, change bit 10 of the pSRAM Bus Configuration Register to 0 (Active LOW WAIT). Alternately, change bit 10 of the Flash Configuration Register to 0 (Active LOW RDY)	X	X
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{IL} or V_{IH} while in asynchronous mode	X	X
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs. Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched. High = device ignores address inputs	X	X
F-RST#	Hardware reset input. Low = device resets and returns to reading array data	X	
F-WP#	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.	X	
F-ACC	Accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	X	
R-CE#	Chip-enable input for pSRAM.		X
F-CE#	Chip-enable input for Flash. Asynchronous relative to CLK for Burst Mode.	X	
R-CRE	Control Register Enable (pSRAM).		X
F-VCC	Flash 1.8 Volt-only single power supply.	X	

Table 2.1 Input/Output Descriptions (Sheet 2 of 2)

Symbol	Description	Flash	RAM
R-VCC	pSRAM Power Supply.		X
R-UB#	Upper Byte Control (pSRAM).		X
R-LB#	Lower Byte Control (pSRAM)		X
DNU	Do Not Use		

3. MCP Block Diagram

Figure 3.1 MCP Block Diagram



4. Connection Diagrams/Physical Dimensions

This section contains the I/O designations and package specifications for the S71NS-P.

4.1 Special Handling Instructions for FBGA Packages

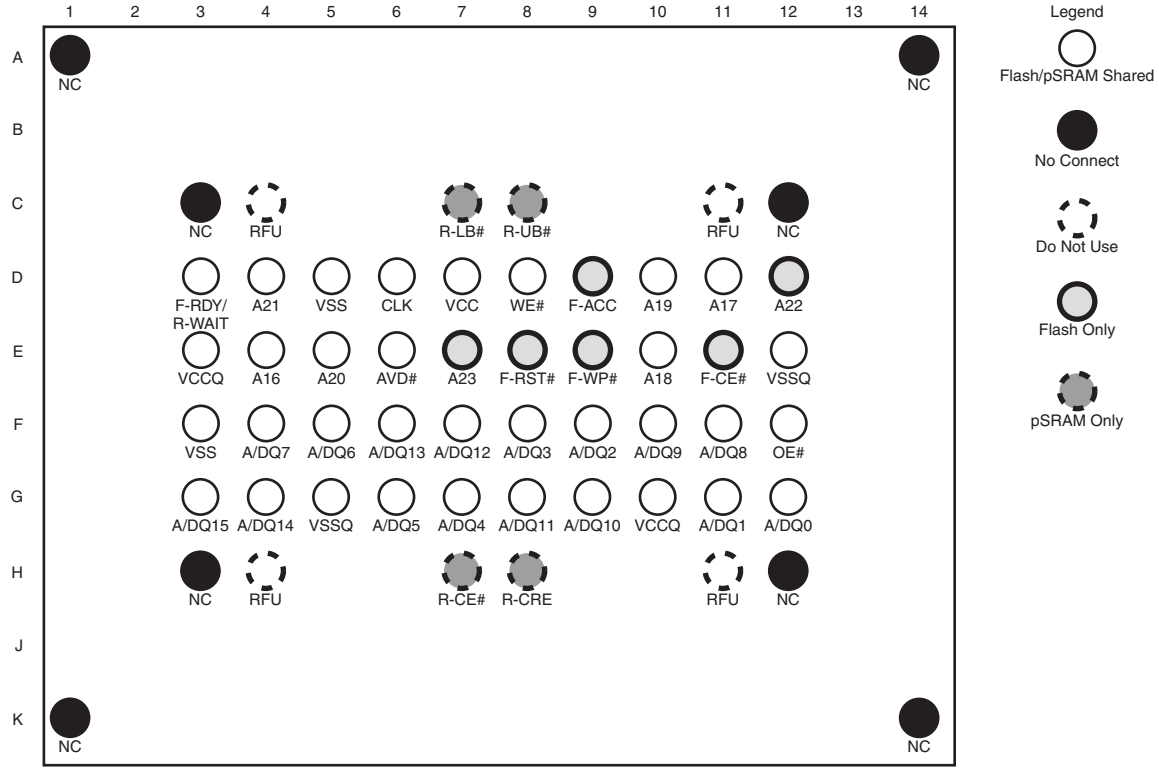
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4.2 Connection Diagrams

Figure 4.1 56-ball Fine-Pitch Ball Grid Array

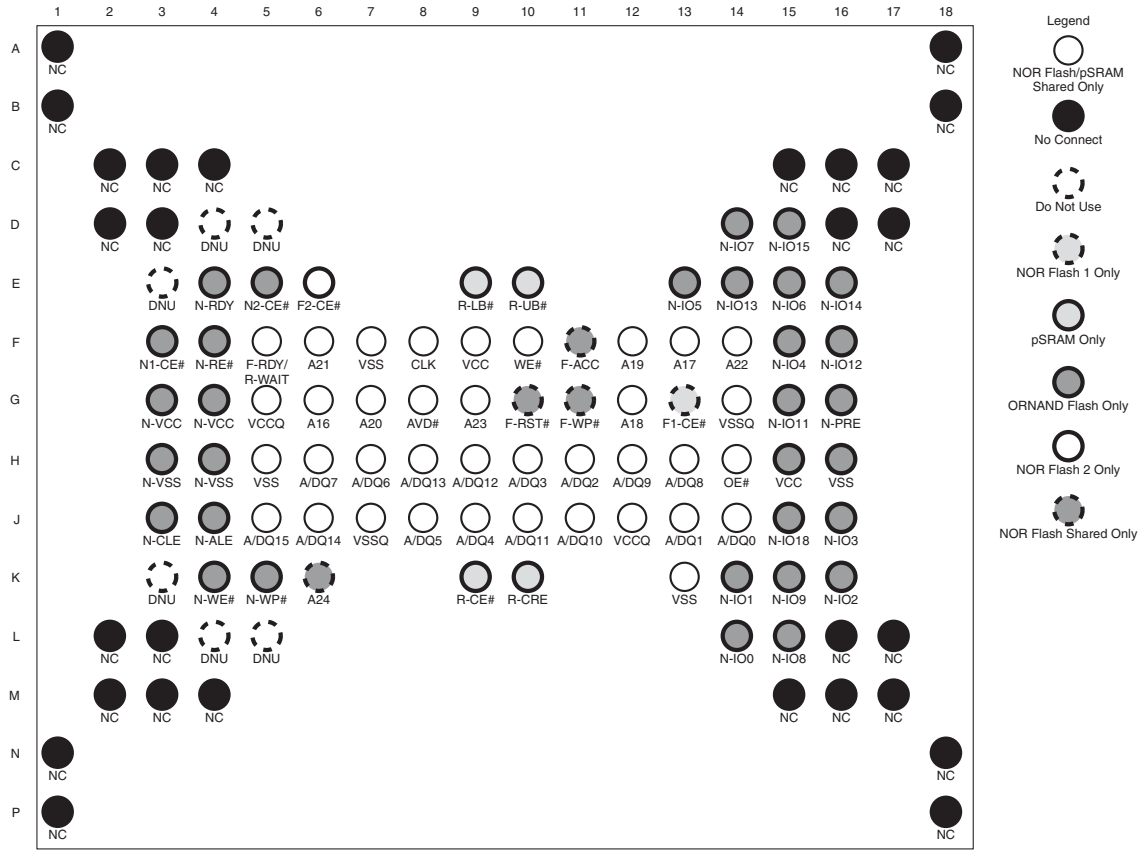
(Top View, Balls Facing Down)



Note:
Addresses are shared between Flash and RAM depending on the density of the pSRAM.

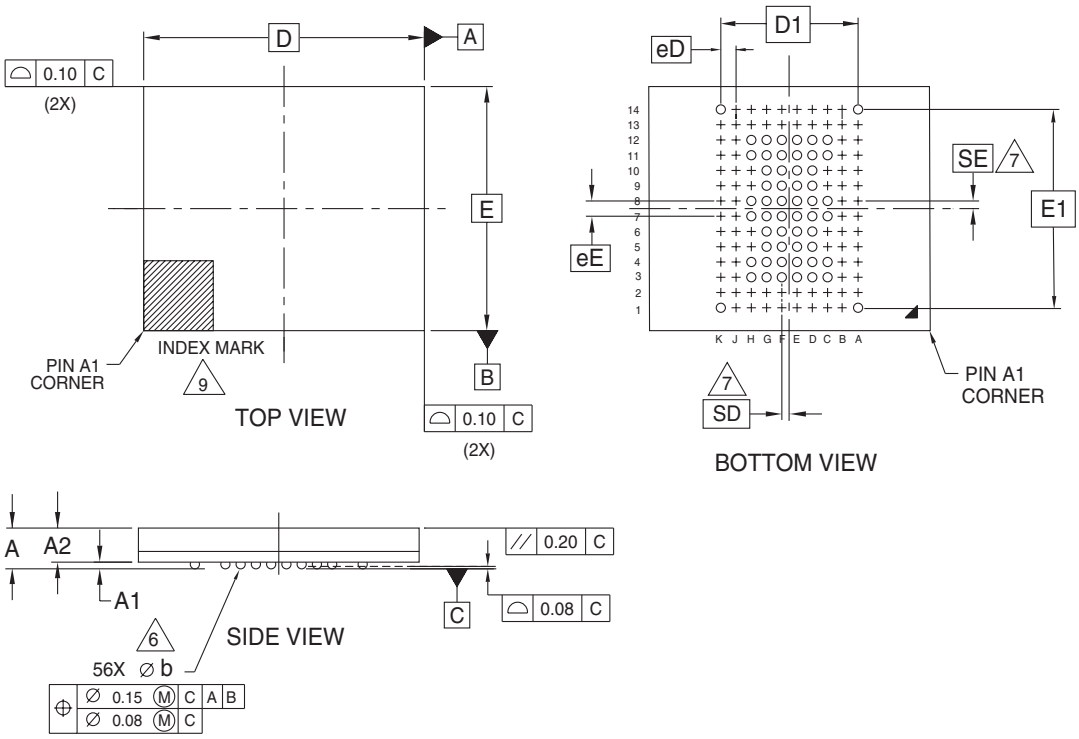
MCP	Flash-Only Addresses	Shared Addresses	Shared ADQ Pins
S71NS128PB0	A22-A21	A20-A16	A/DQ15-A/DQ0
S71NS128PC0	A22	A21-A16	
S71NS256PB0	A23-A21	A20-A16	
S71NS256PC0	A23-A22	A21-A16	

Figure 4.2 Look Ahead Diagram 112-ball x16 MUX NOR Flash + x16 MUX pSRAM on Shared Bus + x16 NAND-based ORNAND on separate bus



4.3 Physical Dimensions

Figure 4.3 NLB056—56-ball VFBGA 9.2 x 8.0 mm



PACKAGE	NLB 056			
JEDEC	N/A			
D x E	9.20 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.85	---	0.97	BODY THICKNESS
D		9.20 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		4.50 BSC.		MATRIX FOOTPRINT
E1		6.50 BSC.		MATRIX FOOTPRINT
MD		10		MATRIX SIZE D DIRECTION
ME		14		MATRIX SIZE E DIRECTION
n		56		BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE		0.50 BSC.		BALL PITCH
eD		0.50 BSC		BALL PITCH
SD / SE		0.25 BSC.		SOLDER BALL PLACEMENT
	A2 – A13,B1 – B14 C1,C2,C5,C6,C9,C10,C13,C14 D1,D2,D13,D14,E1,E2,E13,E14,F1,F2,F13,F14 G1,G2,G13,G14,H1,H2,H5,H6,H9,H10,H13,H14 J1 – J14, K2 – K13			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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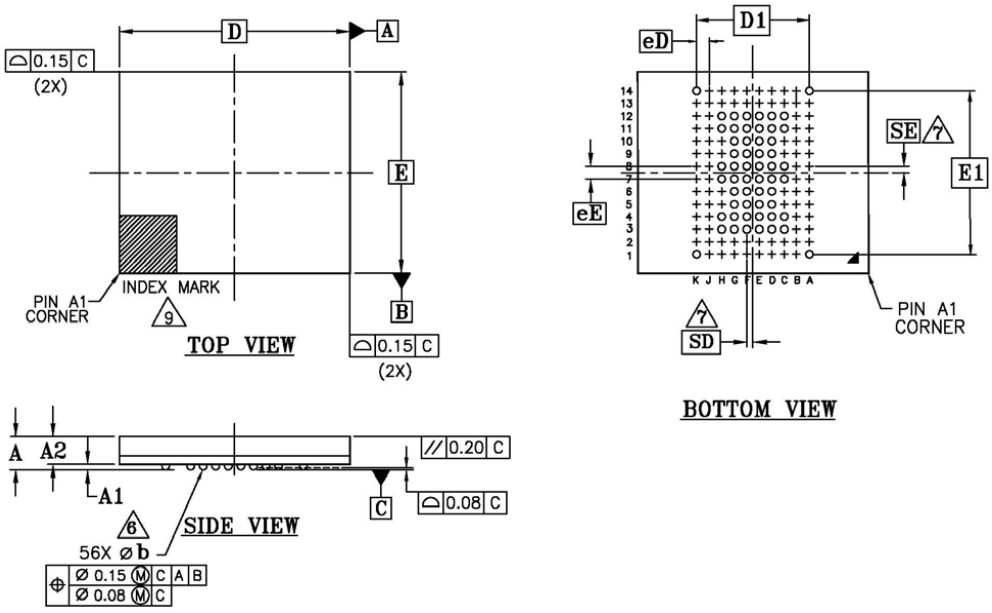
Figure 4.4 NSB056—56-ball VFBGA 9.2 x 8.0 mm



PACKAGE	NSB 056			NOTE
JEDEC	N/A			
D X E	9.20 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.85	---	0.97	BODY THICKNESS
D	9.20 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	4.50 BSC.			MATRIX FOOTPRINT
E1	6.50 BSC			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
Ø b	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC.			BALL PITCH
SE, SD	0.25 BSC.			SOLDER BALL PLACEMENT
	A2- A13,B1-B14,C1, C2,C5,C6,C9,C10,C13, C14, D1,D2,D13,D14,E1,E2, E13,E14,F1,F2,F13,F14,G1 ,G2,G13,G14,H1,H2, H5,H6,H9,H10,H13,H14, J1-J14, K2-K13			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

NSB056 \ 16.038.22 \ 9.25.7

5. Revision History

Section	Description
Revision 01 (October 12, 2006)	
	Initial release
Revision 02 (December 8, 2006)	
Global	Added S71NS128PC0
Revision 03 (September 10, 2007)	
Global	Added product details including ordering information for S71NS256PB0
Revision 04 (September 26, 2007)	
Physical Dimension	Added mechanical drawing for the NSB056 package
Revision 05 (December 13, 2007)	
Global	Added product information for 83 MHz MCPs, including ordering part numbers and valid combinations

Colophon

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